

FORM 1

609298

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

APPLICATION FOR A STANDARD PATENT

I\We,

SONY CORPORATION

of

7-35 KITASHINAGAWA 6-CHOME
SHINAGAWA-KU
TOKYO
JAPAN

hereby apply for the grant of a standard patent for an invention entitled:

DIGITAL SIGNAL PROCESSING APPARATUS.

which is described in the accompanying complete specification

Details of basic application(s):

Number of basic application	Name of Convention country in which basic application was filed	Date of basic application
126606/1988	JP	24 MAY 88

My/our address for service is care of GRIFFITH HACK & CO., Patent Attorneys, 601 St. Kilda Road, Melbourne 3004, Victoria, Australia.

DATED this 18th day of May 1989

SONY CORPORATION

GRIFFITH HACK & CO.

TO: The Commissioner of Patents.

M 009148 180589

APPLICATION ACCEPTED AND AMENDMENTS

ALLOWED 31.1.91

Forms 7 and 8

AUSTRALIA

Patents Act 1952

**DECLARATION IN SUPPORT OF A CONVENTION OR NON-CONVENTION
APPLICATION FOR A PATENT OR PATENT OF ADDITION**

Name(s) of
Applicant(s)

In support of the application made by SONY CORPORATION

Title

for a patent for an invention entitled DIGITAL SIGNAL PROCESSING APPARATUS

Name(s) and
address(es)
of person(s)
making
declaration

I/We, Shoji Wakayama, General Manager, Patents Div. of
c/o SONY CORPORATION, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, Japan

do solemnly and sincerely declare as follows:—

1. I am/we are the applicant(s) for the patent, or authorised by the abovementioned applicant to make this declaration on its behalf.
2. The basic application(s) as defined by Section 141 of the Act was/were made in the following country or countries on the following date(s) by the following applicant(s) namely:-

Country, filing
date and name
of Applicant
for the or
each basic
application

in JAPAN on May 24, 19 88
by SONY CORPORATION
in _____ on _____ 19 _____
by _____

3. The said basic application(s) was/were the first application(s) made in a Convention country in respect of the invention the subject of the application.

4. The actual inventor(s) of the said invention is/are

Name(s) and
address(es)
of the or each
actual inventor

Keiji Kanota and Michio Nagai
of all c/o SONY CORPORATION, 7-35, Kitashinagawa 6-chome,
Shinagawa-ku, Tokyo, Japan

5. The facts upon which the applicant(s) is/are entitled to make this application are as follows:-

The applicant is the assignee of the actual inventor(s).

See reverse
side of this
form for
guidance in
completing
this part

DECLARED at Tokyo, Japan this 12 day of May 19 89

SONY CORPORATION

(12) PATENT ABRIDGMENT (11) Document No. AU-B-34972/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 609298

(54) Title
DIGITAL SIGNAL PROCESSING APPARATUS

International Patent Classification(s)
(51)⁴ **G11B 020/10 H04N 005/92 H04N 005/93 H04N 007/167**

(21) Application No. : **34972/89** (22) Application Date : **18.05.89**

(30) Priority Data

(31) Number (32) Date (33) Country
63-126606 24.05.88 JP JAPAN

(43) Publication Date : **30.11.89**

(44) Publication Date of Accepted Application : **26.04.91**

(71) Applicant(s)
SONY CORPORATION

(72) Inventor(s)
KEIJI KANOTA; MICHIO NAGAI

(74) Attorney or Agent
GRIFFITH HACK & CO, GPO Box 1285K, MELBOURNE VIC 3001

(57) Claim

1. An apparatus for processing an input data signal comprising:

generator means for generating a plurality of pseudo-random signals;

scramble means for scrambling the input data signal by each of said plurality of pseudo-random signals and thereby providing a plurality of respective outputs;

detector means for detecting variation of a DC component for each of said outputs of said scramble means;

selector means for selecting one of said outputs of said scramble means under the control of said detector means;

means for adding to said one output selected by said selector means an identifying signal which identifies the pseudo-random signal used in scrambling said one selected output of the scramble means; and

(11) AU-B-34972/89
(10) 609298

-2-

means for transmitting a signal comprised of said one output selected by said selector means together with said identifying signal.

5. An apparatus according to claim 1; further comprising:

receiver means for receiving a signal transmitted by said means for transmitting;

detector means for detecting said identifying signal in the received, transmitted signal; and

de-scramble means for de-scrambling the received signal in accordance with a pseudo-random signal corresponding to the detected identifying signal.

609298

AUSTRALIA

PATENTS ACT 1952

Form 10

COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE

Short Title:

Int. Cl:

Application Number:
Lodged:

Complete Specification-Lodged:
Accepted:
Lapsed:
Published:

Priority:

Related Art:

TO BE COMPLETED BY APPLICANT

Name of Applicant:

SONY CORPORATION

Address of Applicant: 7-35 KITASHINAGAWA 6-CHOME
SHINAGAWA-KU
TOKYO
JAPAN

Actual Inventor:

Address for Service: GRIFFITH HACK & CO.,
401 St. Kilda Road,
Melbourne, Victoria 3004,
Australia.

Complete Specification for the invention entitled:
DIGITAL SIGNAL PROCESSING APPARATUS.

The following statement is a full description of this invention including the best method of performing it known to me:-

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the application of selective scrambling to a channel coding circuit, for example, in a digital video tape recorder.

Description of the Prior Art

A digital video tape recorder of a type to which the present invention is applicable will be described with reference to Fig. 1 in which a video signal, for example, according to the NTSC system, is supplied to an input terminal 1. The NTSC video signal applied to the input terminal 1 is supplied to an analog-to-digital (A/D) converting circuit 2, in which it is converted to a digital data signal. The digital data signal is supplied to a bit reduction circuit 3, in which it is reduced in bit number and is then fed to an error correction code (ECC) encoder 4. The ECC encoder 4 adds a parity code for error correction and the like to the data signal. The data signal having the parity code added thereto is supplied to a channel coder 5, in which it is converted to a data series whose characteristic conforms to the characteristic of a tape head system of the digital video tape recorder. The data series is supplied to an adding circuit 6, in which it is added to a predetermined synchronizing (SYNC) code from a synchronizing code generating circuit 7 to provide a recording data signal. The recording data signal which includes

the synchronizing code is supplied from the adding circuit 6 through a recording amplifier 8 to a recording head 9 and is thereby recorded on a magnetic tape 10.

Upon playback, a signal reproduced from the magnetic tape 10 by a reproducing head 11 is supplied through a playback amplifier 12 to an equalizer 13, in which it is waveform-shaped in a predetermined manner. The thus waveform-shaped signal is supplied to a data reproducing circuit 14 which reproduces a data series therefrom. The reproduced data series is supplied to a channel decoder 15 which operates in a manner exactly opposite the operation of the channel coder 5 provided at the recording side. The decoded signal from the channel decoder 5 is supplied to an error correction code (ECC) decoder 16, in which it is error-corrected by the above-mentioned parity code. The error-corrected signal is reduced in bit number by a bit reduction circuit 17 and is then converted from digital to analog form by a digital-to-analog (D/A) converting circuit 18. Finally, the reproduced analog video signal is provided at an output terminal 19.

In the use of the digital video tape recorder of Fig. 1 for recording on a previously recorded type, a video signal is generally rewritten by a so-called overwrite system. In such overwriting, if an already recorded signal contained a low frequency component, there is then the risk that a satisfactory

erasing characteristic will not be achieved in the next overwrite because the low frequency component is recorded in a relatively deep layer of the tape or other magnetic record medium. Further, there is a substantial possibility that a low frequency component in the signal recorded in adjacent tracks will result in a cross-talk component upon playback.

Furthermore, when a rotary transformer is provided for transmitting signals to and from the head or heads of the digital video tape recorder, the low frequency band that can be transmitted by the rotary transformer is limited so that a low frequency component in the recorded signal causes distortion in the waveform of the reproduced signal.

Therefore, the digital video tape recorder according to the prior art includes the channel coder 5 and the channel decoder 15 in order to reduce the low frequency component. Figs. 2A and 2B illustrate known circuit arrangements that can be used for the channel coder 5 and the channel decoder 15, respectively, in Fig. 1, and which utilize an M series signal as a pseudo-random signal.

In the channel coder 5 shown in Fig. 2A, the signal from the ECC encoder 4 (Fig. 1) is supplied through an input terminal 21 to a modulo (mod.) 2-adder 22 which may be constituted by an exclusive-OR gate. A reset signal associated with a predetermined synchronizing block, and which is applied to a

terminal 23, is supplied therefrom to an M series generator 24. The M series signal from the M series generator 24 is also supplied to the mod. 2-adder 22 which scrambles the M series signal for effecting the channel coding. The reset signal
5 applied to the terminal 23 is also supplied to the synchronizing code generator 7 which provides the above-mentioned synchronizing code. The synchronizing code is supplied to the adding circuit 6, in which it is added to the data series from the mod. 2-adder 22, and the resulting added output is applied from an output
10 terminal 25 to the recording amplifier 8 shown in Fig. 1.

In the channel decoder 15 shown in Fig. 2B, the data signal from the data reproducing circuit 14 (Fig. 1) is supplied through an input terminal 26 to a mod. 2-adder 27 which is also constituted by an exclusive-OR gate. The signal from the
15 terminal 26 is also supplied to a synchronizing code detecting circuit 28 which detects the above-mentioned synchronizing code. The detected signal is supplied from circuit 28 to an M series generator 29 which provides an M series signal to the mod. 2-adder 27 which effects channel decoding, that is, decodes the signal scrambled by the M series signal in the channel coder 5. The resulting decoded signal is supplied through an output
20 terminal 30 to the ECC decoder 16 (Fig. 1).

The low frequency component in the signal to be recorded is reduced by adding the M series signal to the pseudo-

random signal in the modulo 2 adder 22 in Fig. 2A, whereby a recording data signal having a reduced low frequency component is generated. Upon playback the M series signal is added in the mod.2-adder 27 to the same pseudo-random signal as in the recording mode resulting in the original data signal being decoded.

If the M series signal is added to the pseudo-random signal in a modulo 2 adder for effecting the channel coding and the channel decoding as described above, in the absence of any other data signal processing, when a certain relationship is established between the pattern of the recording signal and that of the M series signal, there is the possibility that such relationship will give rise to the occurrence of a low frequency component. The occurrence of the low frequency component is inevitable from a probability standpoint, and it is impossible to escape such inevitability. The occurrence of such low frequency component causes deterioration of the overwrite characteristic, the cross-talk characteristic, the waveform characteristic and the like, as described above.

Further, in a digital magnetic recording and reproducing apparatus, such as, the above described digital video tape recorder, if the digital data series (represented in the binary form of "1" or "0") is directly recorded, the following problems arise:

1. The maximal frequency of a recorded signal is increased to such extent that the recorded signal cannot be read.

2. Direct current and low frequency components frequently appear in the recorded signal so that, when a digital signal is recorded and reproduced by the head system utilizing a rotary transformer, distortion occurs in the reproduced signal. As a result, it is frequently observed that the reproduced information deviates considerably from the recorded information.

3. When digital data is recorded, a data series is generally recorded according to the so-called self-clock system together with a clock component. If many digital "1"s or "0"s appear in succession or contiguously, the error rate in extracting the clock component at the playback side is increased.

In order to solve the above-mentioned problems, it is known to arrange a digital magnetic recording and reproducing apparatus so that, upon recording, a digital input signal is converted to a recording signal having a predetermined frequency characteristic by a channel coding circuit, and this recording signal is recorded on a magnetic record medium by a recording head. Upon playback, a signal reproduced from the magnetic record medium by a playback head is supplied to, and is reproduced by, a decoder whose converting characteristic is opposite to that of the channel coding circuit. Three channel coding systems are known that are each based on a partial

response (PR) system which makes effective use of intersymbol interference in the digital recording. These three channel coding systems will be explained below:

A. Nonreturn to zero-inverted (NRZ-I) system

5 In the NRZ-I system, an NRZ signal (Fig. 3B), which represents an input signal shown in Fig. 3A in the form of a binary code, is converted to an NRZ-I recording signal shown in Fig. 3C. The NRZ-I system utilizes an encoder to convert the input signal to the recording signal just before the transmission
10 line, and this encoder is what might be called a precoder. The NRZ-I system precoder is called a PR (1, -1) encoder because it effects the coding, that is, the conversion, just opposite to the conversion of a PR (1, -1) transmission line based on the partial response system. Fig. 4A shows an example of a PR (1, -1) encoder that comprises a mod. 2 adder 31 and a one-bit delay
15 circuit 32.

The NRZ-I system has the disadvantage that, when the signal is not inverted, a direct current component frequently appears in the recording signal. Recently, the interleaved NRZ-I (I-NRZ-I) system has been employed in order to remove that
20 disadvantage of the NRZ-I system.

B. Interleaved NRZ-I (i-NRZ-I) system

According to the I-NRZ-I system, an NRZ signal shown in Fig. 3B is converted to an I-NRZ-I recording signal shown in Fig.

3D by means of an I-NRZ-I system precoder which performs a conversion reverse to that in a PR (1, 0, -1) transmission line based on the class IV partial response. Such I-NRZ-I system precoder is called a PR (1, 0, -1) encoder or a partial response class IV encoder. Fig. 4B shows an example of a PR (1, 0, -1) encoder that comprises a mod. 2 adder 31 and two one-bit delay circuits 32a and 32b.

An identifying signal, which results from recording and reproducing the I-NRZ-I recording signal, has frequency characteristics similar to those of the magnetic recording and reproducing systems so that it contains less high frequency components and does not contain a direct current component. In addition, the identifying signal cannot be affected by the cross-talk component caused by the increased wavelength of the recording signal and cannot be affected by the rotary transformer.

C. Scrambled I-NRZ-I (S-I-NRZ-I) system

Although the identifying signal reproduced according to the I-NRZ-I system does not contain a direct current component, the recording signal (see Fig. 3D) does contain a direct current component. In order to reduce the direct current component of the recording signal according to the I-NRZ-I system, the S-I-NRZ-I system has been proposed. In accordance with the

S-I-NRZ-I system, the M series signal (represented in the form of a binary random number) is added to the input signal in a mod. 2 adder, or the input signal is scrambled by the M series signal, so as to make possible reducing of the direct current component.

5 Referring now to Fig. 5, it will be seen that, in a prior-art digital video tape recorder utilizing the S-I-NRZ-I system channel coding circuit, a video signal is applied to an input terminal 43 and is supplied from the latter through a scramble circuit 44 to a PR (1, 0, -1) encoder or precoder 45. The scramble circuit 44 and the PR (1, 0, -1) encoder 45
10 constitute a channel coding circuit. A recording head 46A with an associated rotary transformer, a magnetic tape 46B and a reproducing head 46C with an associated rotary transformer constitute a PR (1, -1) transmission line 47. A PR (1, 1) decoder 48 is adapted to equalize input data [00100 ...] to provide data [001100 ...]. The PR (1, -1) transmission line 47 and the PR (1, 1) decoder 48 together constitute a PR (1, 0, -1) transmission line 49. A synchronizing pulse detecting circuit 50 is adapted to detect a synchronizing pulse SYP in the output of a discriminator 48A which is operatively interposed between the PR (1, 1) decoder 48 and the synchronizing pulse detecting circuit
15 50. The digital video tape recorder of Fig. 5 further has a descramble circuit 51 and an output terminal 52.

When a recording signal [00100 ...] is supplied from the PR (1, 0, -1) encoder 45 to the recording head 46A, such recording signal is converted, in the PR (1, -1) transmission line 47 including the recording head 46A, the tape 46B and the reproducing head 46C, to a reproduced signal [001-100 ...]. This reproduced signal [001-100 ...] is supplied to the PR (1, 1) decoder 48 and converted by the latter to an identifying signal [0010-100 ...]. The output from the PR (1, 1) decoder 48 is supplied to the discriminator 48A, in which it is processed so that [-1] is changed to [+1]. The resulting identifying signal is identical with the scramble signal [0010100 ...] that is used when the PR (1, 0, -1) encoder 45 generates the recording signal [00100 ...]. Therefore, it is to be understood that a conversion which is the reverse of that effected by the PR (1, 0, -1) encoder 45 is carried out in the PR (1, 0, -1) transmission line 49.

When a certain M series pseudo-random signal M_0 is added to the input signal in a mod. 2 adder in the scramble circuit 44, the same pseudo-random signal M_0 is added in a mod. 2 adder in the descramble circuit 51 to the identifying signal resulting when the output of the PR (1, 1) decoder 48 is processed in discriminator 48A such that [-1] is changed to [+1]. In such modulo 2 addition, the addition of the same number results in [000 ...] so that the pseudo-random signal M_0 is

removed to provide the same data at the terminal 52 as the input signal.

Therefore, with the channel coding circuit of the S-I-NRZ-I system, if the input signal has a particular pattern, the direct current component or the low frequency component of the recording signal derived from the PR (1, 0, -1) encoder cannot be reduced by the modulo 2 adding of the pseudo-random signal M_0 to the input signal.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved selective scramble circuit which can avoid the foregoing problems encountered with the prior art.

More specifically, it is an object of the present invention to provide a selective scramble circuit which can carry out the channel coding satisfactorily.

Another object of the present invention is to provide a selective scramble circuit, as aforesaid, which can efficiently suppress increasing of data redundancy.

Still another object of the present invention is to provide a selective scramble circuit, as aforesaid, which can reduce a direct current component in a recording signal regardless of variations in the input signal pattern.

Still another object of the present invention is to provide a selective scramble circuit, as aforesaid, which can

prevent conversion error from being mixed into a resultant recording signal.

A still further object of the present invention is to provide a selective scramble circuit which is suitable for application to a channel coding circuit of a digital video tape recorder.

According to an aspect of the present invention, an apparatus for processing a data signal comprises: generator means for generating a plurality of pseudo-random signals; scramble means for scrambling an input signal by a plurality of the pseudo-random signals and thereby providing a plurality of respective scrambled outputs; detector means for detecting variation of a DC component for each of the scrambled outputs of the scramble means; selector means for selecting one of the scrambled outputs under the control of the detector means, for example, the scrambled output having a digital sum value closest to zero; means for adding to the output of the selector means an information or identifying signal corresponding to the pseudo-random signal used in scrambling the input signal for providing such output of the selector means; and means for transmitting the output of the selector means with the information or identifying signal.

The above, and other objects, features and advantages of the present invention, will be apparent from the following

detailed description of preferred embodiments of the invention when read in conjunction with the accompanying drawings, wherein the same reference numerals are used to identify the same or similar elements in the several views.

5

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an arrangement of a prior-art digital video tape recorder;

10

Fig. 2A is a schematic block diagram showing an example of a known channel coder used in the digital video tape recorder of Fig. 1;

Fig. 2B is a schematic block diagram showing an example of a known channel decoder used in the digital video tape recorder of Fig. 1;

Figs. 3A to 3C are schematic diagrams to which reference is made in explaining channel coding of an input signal;

Fig. 4A is a schematic block diagram showing a known partial response IV (1, -1) encoder;

Fig. 4B is a schematic block diagram showing a known partial response class IV (1, 0, -1) encoder;

Fig. 5 is a schematic block diagram of a main portion of a digital video tape recorder according to the prior art;

Fig. 6 is a block diagram showing an M scramble circuit according to an embodiment of the present invention;

Fig. 7 is a diagrammatic view showing a data format and to which reference will be made in explaining the present invention;

Fig. 8 is a block diagram of a channel decoder according to an embodiment of the present invention;

Fig. 9 is a block diagram of a digital video tape recorder according to another embodiment of the present invention;

Fig. 10 (formed of Figs. 10A and 10B together) is a block diagram showing a selective scramble circuit included in the digital video tape recorder of Fig. 9;

Fig. 11 is a block diagram of a selective descramble circuit included in the digital video tape recorder shown in Fig. 9;

Fig. 12 is a diagram showing a data format of the digital data signal used in accordance with the present invention, and which shows the arrangement of one synchronizing block;

Fig. 13 is a diagram showing a data arrangement of an M series identifying code that is used in accordance with the present invention; and

Figs. 14A to 14F are timing charts to which reference will be made in explaining the operation of a digital video tape recorder according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings in detail, and initially to Fig. 6, it will be seen that, in a selective M scramble circuit according to an embodiment of this invention that may be advantageously employed in the digital video tape recorder of Fig. 1, an input data signal is supplied through an input terminal 61 to mod. 2 adders 62a, 62b, 62c and 62d. Each of the mod. 2 adders 62a-62d may be constituted by an exclusive-OR gate as shown. A reset signal associated with a predetermined synchronizing block of the input signal is supplied through a terminal 63 to an M series generator 64. The M series generator 64 is provided with four output terminals, from which there are derived four M series signals of different phases. The four kinds of M series signals are supplied to the adders 62a-62d, respectively.

The output signals from the adders 62a-62d, that is, the input data signal scrambled by the respective M series signals, are supplied to a circuit 65 which measures run lengths and digital sum values (DSV) corresponding to changes of the direct current components of the respective signals. The circuit 65 is reset in response to the reset signal of each synchronizing block and identifies the output signal from the adders 62a-62d which has the shortest maximum run length and/or the output signal which has the smallest maximum digital sum value in the

interval from one synchronizing block until the next synchronizing block. The run length is determined prior to the digital sum value.

5 The signals from the adders 62a-62d are supplied to respective buffer memories 66a-66d, each of which has a recording or storing capacity of one synchronizing block, and are then output therefrom in the first-in first-out (FIFO) fashion. The output signals from the buffer memories 66a-66d are fed to respective fixed contacts 67a-67d of a switch 67 which is
10 controlled by a switch control signal S_c from the circuit 65.

More particularly, the control signal S_c causes the switch 67 to select the output signal from the one of the buffer memories 66a-66d, and hence from the respective one of the adders 62a-62d, which has been determined by the circuit 65 to provide the M scramble signals with the shortest maximum run length and/or the smallest maximum digital sum value. The M scramble signal thus selected is supplied to a data adding circuit 68, in which it is added to a data code identifying or corresponding to the M series signal used for providing the selected M scramble signal.
20

The signal from the data adding circuit 68 is supplied to a synchronizing code adding circuit 69 and the reset signal from the terminal 63 is also applied to a synchronizing code generating circuit 70 which supplies a synchronizing code to the

adding circuit 69, whereupon, the output signal from the latter is fed to an output terminal 71.

With the above-described selective M scramble circuit, good channel coding is effected by selecting the best one from among a plurality of M scramble signals. further, by adding data identifying or corresponding to the M series signal used in the coding, it is possible to considerably reduce data redundancy.

The data format of the recording data signal developed at the output terminal 71 is represented in Fig. 7, where it will be seen that one synchronizing block is formed of a synchronizing code SYNC, a data code identifying or corresponding to the M series signal used in the coding and scrambled input data in this order. The data code can be expressed by, for example, two bits such as $a = (0, 0)$, $b = (0, 1)$, $c = (1, 0)$ and $d = (1, 1)$ in the illustrated case where four kinds of M series signals are provided. The increase of data redundancy is very small as a result.

When the circuit shown in Fig. 6 is applied to the digital video tape recorder described above with reference to Fig. 1, the output signal of the ECC encoder 4 is supplied to the input terminal 61, and the signal from the output terminal 71 is supplied to the recording amplifier 8, whereby recording can be effected similarly to the prior art.

Referring now to Fig. 8, it will be seen that, in a decoder according to an embodiment of this invention for use in the playback mode of the digital video tape recorder of Fig. 1, a signal applied to an input terminal 82 is supplied to a mod. 2 adder 83 again constituted by an exclusive-OR gate. The signal from the input terminal 82 is also supplied to a synchronizing code detecting circuit 84 which detects the above-mentioned synchronizing code. The detected signal is supplied from circuit 84 to an M series generator 85 that is the same as the M series generator 64 shown in Fig. 6. Four kinds of M series signals that differ in phase from each other are supplied from the generator 85 to respective fixed contacts 86a, 86b, 86c and 86d of a switch 86. The signal from the input terminal 82 is also supplied to a data code identifying circuit 87 which identifies the above-mentioned data code corresponding to the kind of M series signal used for the coding. By this identifying code, the switch 86 is controlled so as to select from the generator 85 the M series signal which is the same as that used in the recording mode.

The M series signal selectively derived from the switch 86 is supplied to the mod. 2 adder 83, and the signal from the adder 83 is fed to an output terminal 88. In this way, the data signal can be decoded. When the decoder described above with reference to Fig. 8 is applied to the digital video tape recorder

of Fig. 1, the output of the data reproducing circuit 14 in Fig. 1 is supplied to the input terminal 82, and the signal from the output terminal 88 is supplied to the ECC decoder 16 in Fig. 1.

In the circuits of Fig. 6 and 8, the M series generators 64 and 85 are not limited to those which provide the M series signal with different phases but they may be M series generators of the type providing M series signals having different recurrent cycles.

With the circuits of Figs. 6 and 8 included in the digital video tape recorder of Fig. 1, upon playback, it becomes possible to reproduce a clock signal with ease.

According to the present invention, as set forth above, good channel coding can be effected by selecting the best one from among the plurality of M scramble signals. Further, the increase of data redundancy is suppressed considerably by adding to the input or information signal data identifying to the M series signal used in the coding.

Another embodiment of the present invention to which the class IV partial response system can be applied will now be described with reference to Figs. 9-11 in which parts corresponding to those described with reference to Fig. 5 are identified by the same reference numerals and will not be again described in detail. In this embodiment, the present invention

is particularly applied to the channel coding circuit of the digital video tape recorder.

It will be seen in Fig. 9 that an input terminal 43 receives a digital input signal $x(t)$, in which t is the time, and this digital input signal $x(t)$ has been processed to have an error correction code, for example, a cyclic redundancy check (CRCC) code and a parity code.

A selective scramble circuit 93 according to the present invention receives the digital input signal $x(t)$ and includes a pseudo-random signal adding circuit and a plurality of PR (1, 0, -1) encoders or precoders used in the channel coding. By this selective scramble circuit 93, the digital input signal $x(t)$ is converted to a recording signal $y(t)$ having a reduced high frequency component and a reduced direct current component. The recording signal $y(t)$ is processed by a PR (1, -1) transmission line 47 formed of the recording head 46A with its associated rotary transformer, the magnetic tape 46B and the reproducing head 46C with its associated rotary transformer to provide a reproduced signal. The reproduced signal is fed to the PR (1, 1) decoder 48, and the output signal from the PR (1, 1) decoder 48 is processed by the discriminator 48A so that [-1] is converted to [+1]. The identifying signal $U_d(t)$ derived from the discriminator 48A is supplied to the synchronizing pulse detecting circuit 50 which separates the synchronizing pulse SYP

from the identifying signal $U_d(t)$. A selective descramble circuit 94 is connected to the synchronizing pulse detecting circuit 50 and receives therefrom the synchronizing pulse SYP and the identifying signal $U_d(t)$. The selective descramble circuit 94 is made to correspond to the selective scramble circuit 93 so as to remove the pseudo-random signal from the identifying signal $U_d(t)$, and to supply the resulting output signal $x_d(t)$ to the output terminal 52.

The selective scramble circuit 93 will now be described more fully with reference to Fig. 10 which is formed of Figs. 10A and 10B to permit the use of a suitably large scale, and in which a block synchronizing pulse BLSY of cycle H is supplied to an input terminal 115 from the external circuit. M series generating circuits 116A, 116B, 116C and 116D are provided to generate respective M series signals M_1 , M_2 , M_3 and M_4 which are different from one another so as to constitute pseudo-random signals. These M series signals M_1 - M_4 are supplied to mod. 2 adders 117A-117D, adapted to perform the mod. 2 addition thereto of the input data signal $x(t)$, and which are each constituted by, for example, an exclusive-OR gate. Three-input multiplexers 118A-118D receive the outputs of the mod. 2 adders 117-117d, respectively, and identifying codes from identifying code generating circuits 119A-119D, respectively, which correspond to the M_1 - M_4 series signals. The identifying codes generated by the

identifying code generating circuits 119A, 119B, 119C and 119D are referred to as code 1, code 2, code 3 and code 4, respectively. Further, a synchronizing pulse generating circuit 120 is provided to generate the synchronizing pulse SYP which is also supplied to each of the multiplexers 118A-118D.

The block synchronizing pulse BLSY is supplied to the M series generating circuits 116A-116D so that the latter are initialized at every cycle H. Then, signals $r_1(t)$ - $r_4(t)$ of the M_1 - M_4 series, respectively, generated by the M series generating circuits 116A-116D are added in mod. 2 to the input signal $x(t)$ by means of the mod. 2 adders 117A-117D. The output signals of the mod. 2 adders 117A-117D, the identifying codes from the identifying code generating circuits 119A-119D and the synchronizing pulse SYP generated by the synchronizing pulse generating circuit 120 are supplied to the multiplexers 118A-118D, respectively, in which they are combined in a time-division-manner to generate signals $u_1(t)$ - $u_4(t)$, respectively.

Each of the time series or multiplexed signals $u_1(t)$ - $u_4(t)$ is a cyclic signal of cycle H, and the signal format of one synchronizing block of cycle H is represented in Fig. 12. Such synchronizing block is shown to comprise synchronizing pulses SYNC0 and SYNC1 each of one byte, data identifying codes (program number, etc.) ID0 and ID1 each of one byte and an M series identifying code MSID1 of one byte. The identifying code MSID1

is followed by audio or video data DATA of k bytes, an error correction code, for example, a parity code, of m bytes, and an M series identifying code MSID2 of the same data format as the identifying code MSID1. The area S1 of the block formed of the data identifying codes ID0 and ID1 and the area S2 formed of the data and the error correction code are scrambled by the M series signals.

The M series identifying codes which were referred to above as the codes 1, 2, 3 and 4, and which selectively constitute the M series identifying codes MSID1 and MSID2, are represented as [00000000], [01010101], [10101010] and [11111111], respectively, as shown on Fig. 13.

With such arrangement, data of two bits ([00], [01], [10] or [11]) is shown to be repeatedly written four times for each of the codes 1, 2, 3 and 4, respectively, so that even when an error occurs in the transmission system, the identifying code of the M series being used can be positively read. Further, in the embodiment being here described, the M series identifying code MSID2 is of the same format as the code MSID1 and is located distant from each M series identifying code MSID1 by $(k + m)$ bytes. Thus, regardless of the occurrence of burst error, the identifying code can be accurately read on the basis of either one of the M series identifying codes MSID1 and MSID2.

Referring back to Fig. 10, it will be seen that the output signals $u_1(t)$ - $u_4(t)$ from the multiplexers 118A-118D are respectively supplied to partial response (PR) class IV (1, 0, -1) encoders 121A-121D acting as precoders, and in which the signals $u_1(t)$ - $u_4(t)$ are respectively converted to signals $y_1(t)$ - $y_4(t)$. The PR (1, 0, -1) encoders 121A-121D are all similarly constructed and, by way of example, the PR (1, 0, -1) encoder 121A will be described in detail.

The PR (1, 0, -1) encoder 121A is shown to be comprised of an exclusive-OR gate 122 that carries out the mod. 2 addition, a two-input switch circuit 123 and two one-bit delay circuits 124 and 125. The signal $y_1(t)$ is supplied from the output of the exclusive-OR gate 122 to a first input terminal of the switch circuit 123 and the switch circuit 123 responds to the level of a control signal J1 from a control circuit 129 to selectively supply one of its two input signals through the one-bit delay circuits 124 and 125, in succession, to an input of the exclusive-OR gate 122.

A four-input switch circuit 126 is shown to receive the signals $y_1(t)$ - $y_4(t)$ at its four input terminals, respectively. The switch circuit 126 responds to a code of a control signal J5 from the control circuit 129 to select one of the signals $y_1(t)$ - $y_4(t)$ and to supply such selected signal $y_{s0}(t)$ to the other or second input terminal of the switch circuit 123 in each of the

PR (1, 0, -1) encoders 121A-121D. The signals $y_1(t)$ - $y_4(t)$ from encoders 121A-121D are converted to signals $y_1(t-H)$ - $y_4(t-H)$, respectively, by delay circuits 127A-127D each having a delay time of one horizontal period (1H), and are then respectively fed to four input terminals of a switch circuit 128. The switch circuit 128 responds to a code of a control signal J6 also derived from the control circuit 129 to select one of the signals $y_1(t-H)$ - $y_4(t-H)$ as the recording signal $y(t)$. The recording signal $y(t)$ is recorded on the magnetic tape 46B by means of the recording head 46A.

The control circuit 129 is shown in Fig. 10 to include a sequence control circuit 130 which responds to the block synchronizing pulse BLSY from the terminal 115 to generate the control signals J1-J4 supplied to the switch circuits 123 of the encoders 121A-121D, respectively, and also to generate timing signals used to control the operation of additional hereinafter described circuits included in the control circuit 129. A control signal J7 is also generated by the sequence control circuit 130 and is employed to simultaneously switch the multiplexers 118A-118D.

The control circuit 129 is further shown to include digital sum value (DSV) measuring circuits 131A-131D. A digital sum value (DSV) of digital data series $y_i(t)$ from, for example, time t_1 to time t_2 , is defined by the following equation:

$$DSV = \sum_{t=t_1}^{t_2} a_i(t) \dots\dots\dots(1)$$

5 where $y_i(t) = 1$ results in $a_i(t) = 1$, and $y_i(t) = 0$ results in $a_i(t) = 0$, and further assuming that the digital data series $y_i(t)$ is generated bit by bit in synchronism with a clock pulse CK whose unit time is T. (Fig. 14A).

10 In the present embodiment, when the digital sum value is converged to zero, a direct current component of the digital data series $y_i(t)$ becomes zero. The signals $y_1(t)$ - $y_4(t)$ are supplied to the DSV measuring circuits 131A-131D, respectively, which measure the digital sum values DSV_1 - DSV_4 , respectively, during a predetermined period corresponding to a block K (Fig. 14C). The resultant digital sum values DSV_1 - DSV_4 are supplied to a determining circuit 132 within the control circuit 129. The determining circuit 132 determines which of the digital sum values DSV_1 - DSV_4 generated by the measuring circuits 131A-131D, respectively, is closest to zero and supplies a corresponding series number s_0 identifying the respective one of the M series signals $r_1(t)$ - $r_4(t)$ to a switch control circuit 133. If the digital sum values of the signals $y_1(t)$ - $y_4(t)$ are measured for one synchronizing block K in which time t ranges from $T_k (= 0)$ to $T_{k+1} (= T_k + H)$, in the next time t from T_{k+1} to T_{k+2} , the one of the signals $y_1(t)$ - $y_4(t)$ of the block K whose digital sum value is closest to zero is selected by the switch circuit

128 under the control of the switch control circuit 133 to provide the recording signal $y(t)$.

The operation of the embodiment of the invention illustrated in Fig. 10 will now be described with reference to Figs. 14A-14F.

The output signal $U_s(t)$ of each of the multiplexers 118A-118D is expressed, when the respective M series identifying code and the synchronizing pulse SYP are removed therefrom, by the following equation:

$$U_s(t) = x(t) + rs(t) \pmod{2}; = 1 - 4 \dots (2)$$

The output signal $y_s(t)$ of each of the PR (1, 0, -1) encoders 121A-121D is expressed as follows:

$$y_s(t) = y_s(t - 2) + U_s(t) \pmod{2} \dots (3)$$

If it is assumed that data becomes effective from time $t = 0$, that $y_s(-2) = y_s(-1) = 0$ is determined to initialize the PR (1, 0, -1) encoders 121A-121D, and that the time t is updated at every cycle T (= unit time 1) of the clock pulse CK (Fig. 14A and is expressed as $t = 2m$ or $t = 2m + 1$, equations (2) and (3) yield:

$$\begin{aligned} y_s(t=2m) &= y_s(2m-2) + (x(2m) + rs(2m)) \\ &= \sum_{i=0}^m x(2i) + \sum_{i=0}^m rs(2i) \pmod{2} \dots (4) \end{aligned}$$

$$y_s(t=2m+1) = \sum_{i=0}^m x(2i+1) + \sum_{i=0}^m rs(2i+1) \pmod{2} \dots (5)$$

The DSV measuring circuits 131A-131D measure the digital sum values during the measuring period K from time $t = T_k + \alpha$ to $t = T_{k+1} - 1$. In such case, the following equation (6) is established.

5
$$\alpha_{\min} \leq \alpha \leq \alpha_{\max} - 2 \quad \dots\dots(6)$$

in which α_{\min} is determined by the time required to compare the digital sum values and to determine the minimum value, and α_{\max} corresponds to the bit length of the synchronizing pulses SYNC0 and SYNC1. The portions of the synchronizing block constituted by the synchronizing pulses SYNC0 and SYNC1 are not scrambled so that the digital sum value in the period of $T_k \leq t < T_k + \alpha$ is not measured. The digital sum value, which is not measured, is too small to reduce the effects that the present invention achieves.

15 The DSV measuring circuits 131A-131D measure the digital sum values, DSV_1 - DSV_4 , of the respective series at time $t = T_{k+1}$. The determining circuit 132 in the control circuit 129 compares the digital sum values DSV_1 - DSV_4 during the time period of 3 clocks, and supplies to the switch control circuit 133 the series number s_0 (1-4) of the series signals $y_1(t)$ - $y_4(t)$ corresponding to the digital sum value which is closest to zero. The switch control circuit 133 responds to the series number s_0 to provide the signal J5 which controls the operation of the switch 126 as shown in Fig. 14D and to provide the signal J6

which controls the operation of the switch 128 as shown in Fig. 14E. The switch circuit 128 selectively passes the signal $y_s(t-H)$ ($s=s_0$) of the selected series number s_0 only during the period of $T_{k+1} + \alpha_{min} + 3 \leq t < T_{k+2} + \alpha_{min} + 3$. Hence, the following equation is established:

$$y(t) = y_s(t - H) \dots\dots\dots(7)$$

and the signal supplied to the recording head 46A as the recording signal $y(t)$ is $y_s(T_k + \alpha_{min} + 3)$ to $y_s(T_{k+1} + \alpha_{min} + 2)$.

10 This means that the switch circuit 128 selectively provides, during the measuring period K , the signal of the series selected during the preceding measuring period $K-1$ at a timing delayed by $1H$, or by the transmission time of one synchronizing block.

The switch circuit 126 is used to cause the PR (1, 0-, -1) encoders 121A-121D to feed-back their output signals $y_1(t)$ - $y_4(t)$. The switch 126 supplies the output signal $y_{s0}(t)$, selected as the recording signal during the period of $T_k + \alpha_{min} + 3 \leq t < T_{k+1} + \alpha_{min} + 3$, to the respective second input terminals of the switch circuits 123 of the PR (1, 0, -1) encoders 121A-121D during the period of two clocks, that is, during the time period $T_{k+1} + \alpha_{min} + 1 \leq t < T_{k+1} + \alpha_{min} + 3$ in which the PR (1, 0, -1) encoders 121A-121D are initialized. In the time period in which the PR (1, 0, -1) encoders 121A-121D are initialized, each switch circuit 123 selectively supplies to the

delay circuit 124 the signal $y_{s0}(t)$ supplied to the switch
circuit 123 from the switch circuit 126, whereby the switch
circuit 126 and the switch circuits 123 in the plurality of PR
(1, 0, -1) encoders 121A to 121D are operated in association with
5 one another. More specifically, within the precoder

initialization period, $T_{k+1} + \alpha_{\min} + 1 \leq t < T_{k+1}$
+ $\alpha_{\min} + 3$, the output signal $y_{s0}(t)$, which is selected as the
recording signal during the period of $T_k + \alpha_{\min} + 3 \leq t < T_{k+1} +$
 $\alpha_{\min} + 3$, is fed back to the input terminals of the PR (1, 0, -1)
10 encoders 121A-121D instead of the output signals $y_1(t)$ - $y_4(t)$.

Generally, the delay circuits 124 and 125 in the PR (1,
0, -1) encoders 121A-121D delay the output signals by 2 bits and
feed the delayed output signals back to the input terminals
thereof. Accordingly, in the absence of the described operation
15 of the switch circuit 126, the output signal $y_2(t)$, instead of
the recording signal $y_1(t)$ in the preceding period, would be fed
back to the input terminal of the PR (1, 0, -1) encoder 121B when
the recording signal, for example, is switched from the output
signal $y_1(t)$ of the PR (1, 0, -1) encoder 121A to the output
20 signal $y_2(t)$ of the PR (1, 0, -1) encoder 121B, with the result
that the succeeding recording signal is made different from the
original one. However, the switch circuit 126 is provided to
enable the PR (1, 0, 01) encoders to be initialized during a
predetermined period of time so that even when the recording

signal is switched, accurate signals are invariably fed back to the input terminals of the PR (1, 0, -1) encoders 121A-121D.

By reason of the switch circuit 126 and the plurality of switch circuits 123, the output signals $y_s(t)$ of the PR (1, 0, -1) encoders 121A-121D are precisely expressed as :

$$y_s(t) = y_s(t-2) + u_s(t) \pmod{2} \quad \dots\dots(8)$$

where $t \neq T_k + \alpha_{min} + 3$ and $t \neq T_k + \alpha_{min} + 4$, and are also expressed as

$$y_s(t) = y_{s0}(t-2) + u_s(t) \pmod{2} \quad \dots\dots(9)$$

where $t = T_k + \alpha_{min} + 3$ and $t = T_k + \alpha_{min} + 4$, and $y_{s0}(t)$ represents the signal selected as the recording signal in the time period of $t < T_k + \alpha_{min} + 3$. If it is assumed in equations (8) and (9) that $y_s(-2) = y_s(-1) = 0$, then equations (4) and (5) yield

$$y_s(t=2m) = \sum_{i=0}^m x(2i) + \sum_{i=0}^m s_x(2i) \pmod{2}; s = 1 \sim 4 \quad \dots\dots(10)$$

$$y_s(t=2m+1) = \sum_{i=0}^m x(2i+1) + \sum_{i=0}^m r_s x(2i+1) \pmod{2} \quad \dots\dots(11)$$

In equation (11), $r_s x(2i+1)$ represents, if the present time t lies in a range of $T_k + \alpha_{min} \leq t < T_{k+1} + \alpha_{min}$, a pseudo-random signal $rs_0(t)$ ($s_0 = 1 \sim 4$) of the series selected during the period of $(2i+1) \leq T_k + \alpha_{min}$. In the time period of $T_k + \alpha_{min} < (2i+1)$, $r_s x(2i+1)$ represents pseudo-random signals $r_1(t) \sim r_4(t)$

corresponding to the PR (1, 0, -1) encoders 121A-121D, which fact is expressed by the following equations.

$$rsx(t) = rs_0(t) ; t \leq T_k + \alpha_{min} \quad \dots\dots(12)$$

$$rsx(t) = rs(t) ; t > T_k + \alpha_{min} \quad \dots\dots(13)$$

5 The PR (1, 0, -1) encoders 121A-121D generate the output signals that had once contained the pseudo-random signals selected at every synchronizing block. The signal $y(t)$, selectively produced from the switch circuit 128 at time t , is a signal that is delayed by $1H$ (one horizontal period) after being scrambled by the selected pseudo-random pattern. The signal $y(t)$ is expressed
10 by the following equations

$$y(t) = ys_0(t-H)$$

$$= \sum_{i=0}^m x(2i-H) + \sum_{i=0}^m rs_0(2i-H) \pmod{2};$$

$$t = 2m \quad \dots\dots\dots(14)$$

$$y(t) = ys_0(t-H)$$

$$= \sum_{i=0}^m x(2i-H+1) + \sum_{i=0}^m rs_0(2i-H+1) \pmod{2};$$

$$t = 2m + 1 \quad \dots\dots\dots(15)$$

The arrangement of the reproducing side of the digital video tape recorder of Fig. 9, and particularly of the descramble circuit 94 included therein, will now be described with reference to Fig. 11 in which parts corresponding to those described with

reference to Fig. 9 are identified by the same reference numerals and are not again described in detail.

In Fig. 11, it will be seen that the PR (1, 1) decoder 48 is comprised of a one-bit delay circuit 134 and an exclusive-OR gate 135 forming a mod. 2 adder. The PR (1, 1) decoder 48, in association with the recording head 46A, the magnetic tape 46B and the playback head 46C constitutes the PR (1, 0, -1) transmission line 49 which is equivalent to the illustrated circuit comprised of two one-bit delay circuits 136, 137 and an exclusive-OR gate 138, namely, a mod. 2 adder. The PR (1, 0, -1) transmission line 49 effects the conversion just opposite to the conversion of the channel coding performed by the PR (1, 0, -1) encoders 121A-121D in the example shown in Fig. 10, thereby generating the identifying signal $U_d(t)$. The identifying signal $U_d(t)$ corresponds to the signals $U_1(t)$ to $U_4(t)$ shown in Fig. 10.

The synchronizing-signal-recorded-portions SYNC0, SYNC1 and the M series identifying code-recorded-portions MSID1, MSID2 in the identifying signal $U_d(t)$ are not scrambled by the use of pseudo-random signal, as shown in Fig. 12. Hence, the identifying signal $U_d(t)$ is supplied to the synchronizing pulse detecting circuit 50, in which the synchronizing pulse SYP of a predetermined pattern can be reliably separated from the identifying signal $U_d(t)$. The selective descramble circuit 94

receives the synchronizing pulse SYP and the identifying signal Ud(t) derived from the synchronizing pulse detecting circuit 50.

In the selective descramble circuit 94, the identifying signal Ud(t) is supplied to a 1H delay circuit 139 and to first and second registers 140 and 141. The M series identifying code MSID1 shown in Fig. 12 is supplied to the first register 140, whereas the M series identifying code MSID2 is supplied to the second register 141. These M series identifying codes MSID1 and MSID2 fed to the first and second registers 140 and 141 are fed therefrom to an error correction circuit 142. The error correction circuit 142 judges every byte of the identifying codes MSID1 and MSID2 in a majority-logic-fashion and supplies at least one byte of the judged result to a third register 143 as a correct identifying code ([00] to [11]).

A control circuit 144 is initialized by the synchronizing pulse SYP from the detecting circuit 50 and then drives the first, second and third registers 140, 141 and 143 in a predetermined timed relationship.

M series generating circuits 145A-145D are arranged in the same way as the M series generating circuits 116A-116D of Fig. 10. The M series generating circuits 145A-145D are initialized by the synchronizing pulse SYP to generate pseudo-random signals of M1-M4 series, which are fed to respective input terminals of a four-input switch circuit 146. The switch circuit

146 responds to an identifying code from the third register 143 to selectively produce one of the pseudo-random signals of the M1-M4 series. This selected pseudo-random signal $rs0d(t-H)$ is supplied to one input terminal of a mod. 2 adding circuit 147 (formed of, for example, an exclusive-OR gate). The output signal $Ud(t-H)$ from the 1H delay circuit 139 is supplied to the other input terminal of the adding circuit 147, and the output signal $xd(t)$ from the adding circuit 147 is fed to the output terminal 52.

The embodiment shown in Fig. 11 operates as follows:

The third register 143 stores the M series identifying code of the block K corresponding to the time period $T_k \leq t < T_{k+1}$ of the identifying signal $Ud(t)$ during the time period of $T_{k+1} \leq t < T_{k+2}$, and supplies the thus stored M series identifying code to the switch circuit 146. The switch circuit 146 supplies the signal $rs0d(t-H)$ corresponding to the M series identifying code to the adding circuit 147 during the time period of $T_{k+1} \leq t < T_{k+2}$. In the signals $Ud(t)$, $rs0d(t-H)$ and $xd(t)$, the legend [d] indicates in each case the possibility that the respective variable will contain an error.

In order to examine the influence exerted by the occurrence of error in the PR (1, 0, -1) transmission line 49, let it be assumed that the input signal $yd(t)$ applied to the recording head 46A, that is, the input to the PR (1, 0, -1)

transmission line 49, corresponds to that obtained when an error signal $e(t)$ is added to the recording signal $y(t)$ shown in Fig. 10. In other words,

$$y_d(t) = y(t) + e(t) \quad \dots\dots\dots(16)$$

and, if $t = 2m$, from equation (10), the identifying signal $U_d(t)$ which is the output signal from the PR (1, 0, -1) transmission line 49 is expressed by the following equation:

$$\begin{aligned} U_d(t=2m) &= U_d(2m) - y_d(2m-2) \pmod{2} \\ &= (y(2m) + e(2m)) - (y(2m-2) + e(2m-2)) \\ &= \sum_{i=0}^m (x(2i) + rs_0(2i)) + e(2m) \\ &= - \sum_{i=0}^{m-1} (x(2i) + rs_0(2i)) + e(2m-2) \\ &= x(2m) + rs_0(2m) + e(2m) + 2(2m-2) \quad \dots\dots\dots(17) \end{aligned}$$

From a mathematical standpoint, a feature that the addition of mod. 2 is equivalent to the subtraction is utilized to derive the equation (17). Similarly, from equation (11), if $t = 2m+1$, the identifying signal $U_d(t)$ is expressed by the following equation:

$$\begin{aligned} U_d(t=2m+1) &= x(2m+1) + rs_0(2m+1) + e(2m+1) \\ &\quad + 3(2m+3) \pmod{2} \quad \dots\dots\dots(18) \end{aligned}$$

Combining equations (17) and (18) yields

$$U_d(t) = x(t) + rs_0(t) + e(t) + e(t-2) \quad \dots\dots\dots(19)$$

Further, the output signal $x_d(t)$ of the adding circuit 147 can be calculated by the following equation:

$$\begin{aligned} x_d(t) &= U_d(t-H) + r_{s0}(t-H) \pmod{2} \\ &= x(t-H) + r_{s0}(t-H) + e(t-H) + (t-H-2) \\ &\quad + r_{s0d}(t-H) \dots\dots\dots(20) \end{aligned}$$

5 Since the equality, $r_{s0d}(t-H) = r_{s0}(t-H)$ is established when the correct M series signal is selected by the switch circuit 146, equation (20) can be modified to read:

$$x_d(t) = x(t-H) + e(t-H) + e(t-H-2) \dots\dots\dots(21)$$

10 Thus, the output signal $x_d(t)$ from the adding circuit 147 becomes equal to the output signal from the PR (1, 0, -1) transmission line. The fact that the addition of a number to the same number results in zero in the addition of mod. 2 is utilized to derive the equation (21) from equation (20). If $e(t-H) = e(t-H-2) = 0$ is established in equation (21), this yields:

$$x_d(t) = x(t-H) \dots\dots(22)$$

15 Thus, it is to be understood that the input to the circuit shown in Fig. 10, that is, the signal $x(t)$, delayed by $1H$, is equal to the signal $x_d(t)$ which is the output from the circuit shown in Fig. 11. When the selective descramble circuit 94 is used as described above, the pseudo-random signal of the same series as the scrambled M series signal is added in mod. 2 to the identifying signal $u_d(t)$ so that the scrambled M series signal is removed from the identifying signal $u_d(t)$, thus making it possible to correctly decode the input signal $x(t)$.

Although in the above-described embodiment shown in Fig. 10 the control circuit 129 in the selective scramble circuit 93 measures the digital sum values of the respective output signals $y_1(t)$ - $y_4(t)$ of the PR (1, 0, -1) encoders 121A-121D, the control circuit 129 may measure, instead of the digital sum values, the maximum run lengths RUN_1 - RUN_4 , that is, the maximum contiguous number of high level [1] bits or low level [0] bits, in the respective output signals $y_1(t)$ - $y_4(t)$ within predetermined time periods, and then generate, as the recording signal, the output signal $y_s(t)$ which has the shortest of these maximum run lengths RUN_1 - RUN_4 .

While the PR (1, 0, -1) encoders 121A-121D are employed as the precoders in the above described embodiment the present invention can be similarly applied to a channel coding circuit which, for example, utilizes PR (1, -1) encoders as the precoders.

Furthermore, the addition of the M series identifying code and of the synchronizing pulse may be effected, for example, between the switch circuit 128 and the recording head 46A, rather than at the multiplexers 119A-119D between the mod. 2 adders 117A-117D and the PR (1, 0, -1) encoders 121A-121D. In that case, although the M series identifying code and the synchronizing pulse are not processed by the channel coding

process, no problem is presented if a pattern is selected having reduced high frequency and direct current components.

5 Since, in accordance with the present invention, the precoders are used to reduce both the maximum frequency of the recording signal and the direct current component, and the pseudo-random signal, which scrambles the input signal, is selected so as to provide the best direct current component of the recording signal which is output from the precoders and to provide the best run length, regardless of the change of the
10 pattern of the input signal, it is possible to substantially suppress and thereby minimize the direct current component of the recording signal.

Further, in accordance with the present invention, when the signal constituting the recording signal is switched from the output of a first PR (1, 0, -1) encoder to the output of a second PR (1, 0, -1) encoder, the output signal of the first PR (1, 0, -1) encoder, that is, the present recording signal, can be fed back to the input terminal of the second PR (1, 0, -1) encoder by means of the switch circuit 126 so that the recording signal can be positively fed back to the input terminals of the respective PR (1, 0, -1) encoders. Hence, mixing of conversion error into the generated recording signal can be prevented.

Having described preferred embodiments of the invention with reference to the accompanying drawings, it is to be

understood that the invention is not limited to those precise
embodiments, and that various changes and modifications may be
effected therein by one skilled in the art without departing from
the scope or spirit of the invention as defined in the appended
5 claims.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. An apparatus for processing an input data signal comprising:

generator means for generating a plurality of pseudo-random signals;

scramble means for scrambling the input data signal by each of said plurality of pseudo-random signals and thereby providing a plurality of respective outputs;

detector means for detecting variation of a DC component for each of said outputs of said scramble means;

selector means for selecting one of said outputs of said scramble means under the control of said detector means;

means for adding to said one output selected by said selector means an identifying signal which identifies the pseudo-random signal used in scrambling said one selected output of the scramble means; and

means for transmitting a signal comprised of said one output selected by said selector means together with said identifying signal.

2. An apparatus according to claim 1; wherein said means for transmitting includes means for recording said one output selected by said selector means with said information signal on a magnetic tape.

3. An apparatus according to claim 2; wherein said detector means includes means for detecting run-lengths of said outputs of said scramble means.

4. An apparatus according to claim 2; wherein said detector means includes means for detecting digital sum values of said outputs of the scramble means, and said selector means selects the one of said outputs of the scramble means having a digital sum value closest to zero.

5. An apparatus according to claim 1; further comprising:

receiver means for receiving a signal transmitted by said means for transmitting;

detector means for detecting said identifying signal in the received, transmitted signal; and

de-scramble means for de-scrambling the received signal in accordance with a pseudo-random signal corresponding to the detected identifying signal.

6. An apparatus according to claim 1; further comprising precoder means for encoding each of said outputs of said scramble means to have a predetermined frequency characteristic.

7. An apparatus according to claim 6; wherein said precoder means is a partial response encoder means.

8. An apparatus according to claim 5; wherein said precoder means includes a plurality of partial response encoders each comprising feedback circuit means having a delay for encoding a respective output of said scramble means in accordance with a partial response method, and switching means for providing, as a feedback to one of said partial response encoders, an output signal of another of said partial response encoders.

DATED THIS 3RD DAY OF AUGUST 1989

SONY CORPORATION

By its Patent Attorneys:

GRIFFITH HACK & CO.

Fellows Institute of Patent
Attorneys of Australia

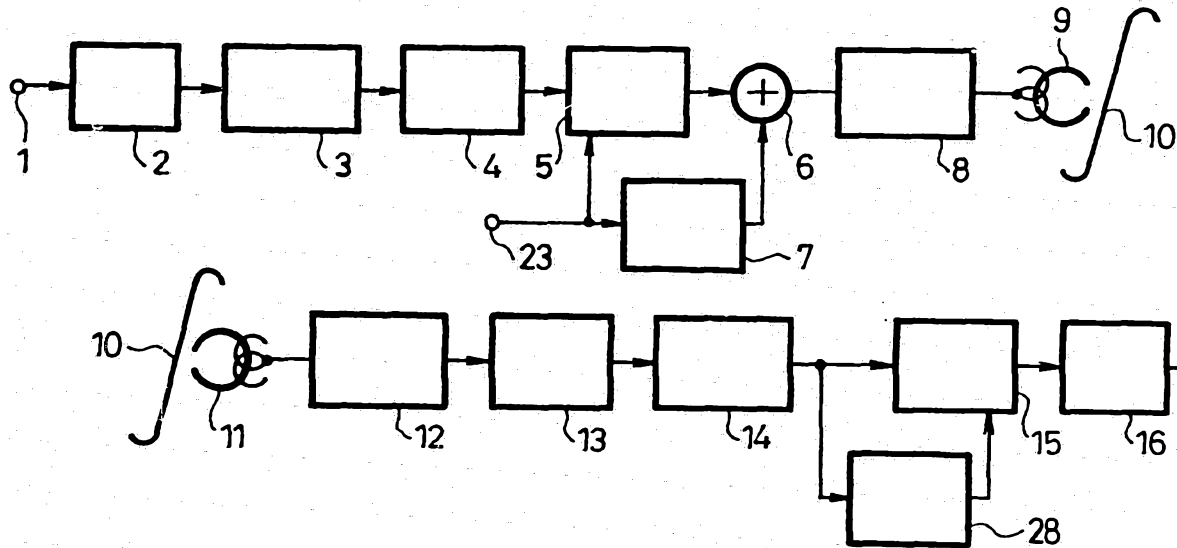


FIG. 1

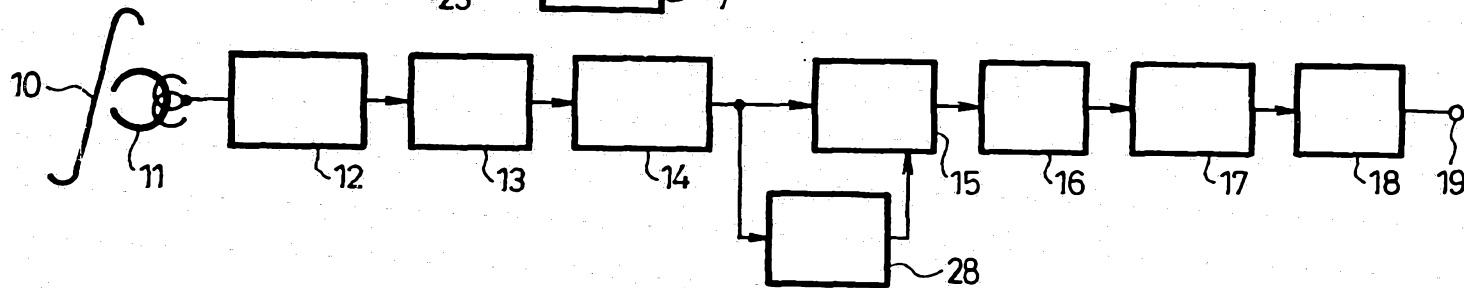


FIG. 2A

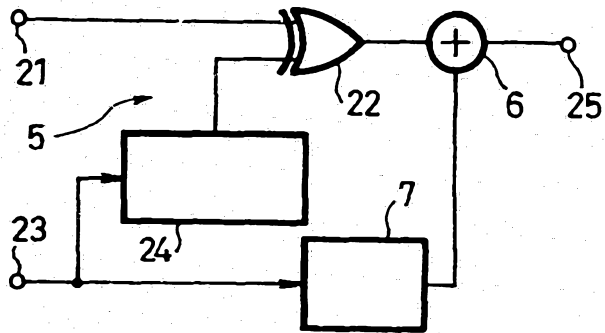
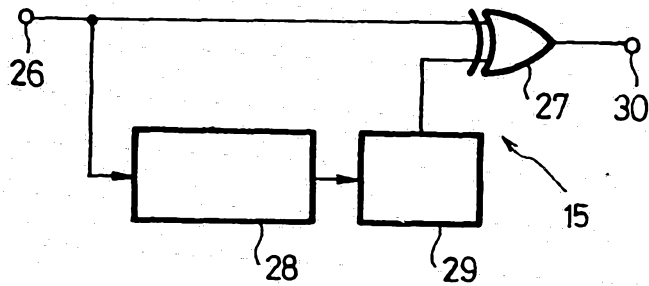


FIG. 2B



10 00 3472

FIG. 3A Input Signal | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

FIG. 3B NRZ



FIG. 3C NRZ-I



FIG. 3D I-NRZ-I



FIG. 4A

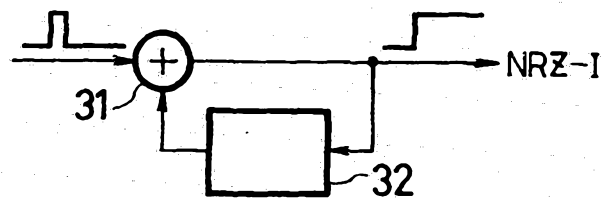


FIG. 4B

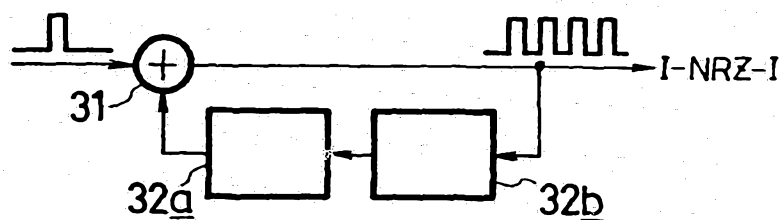
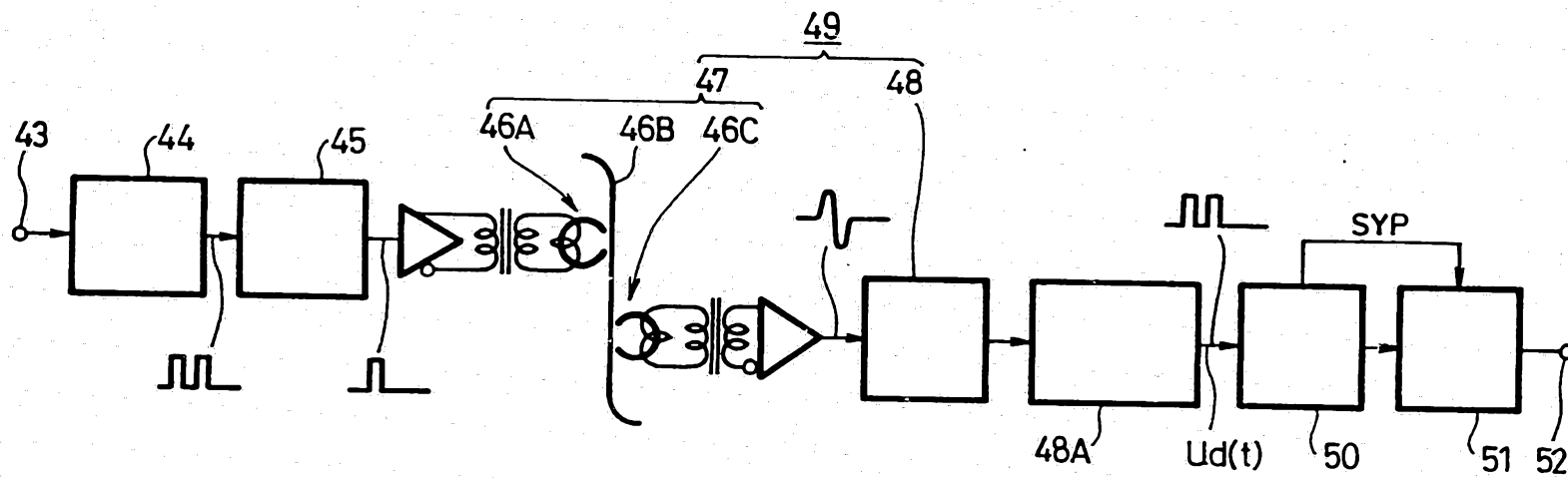


FIG. 5



34072/89

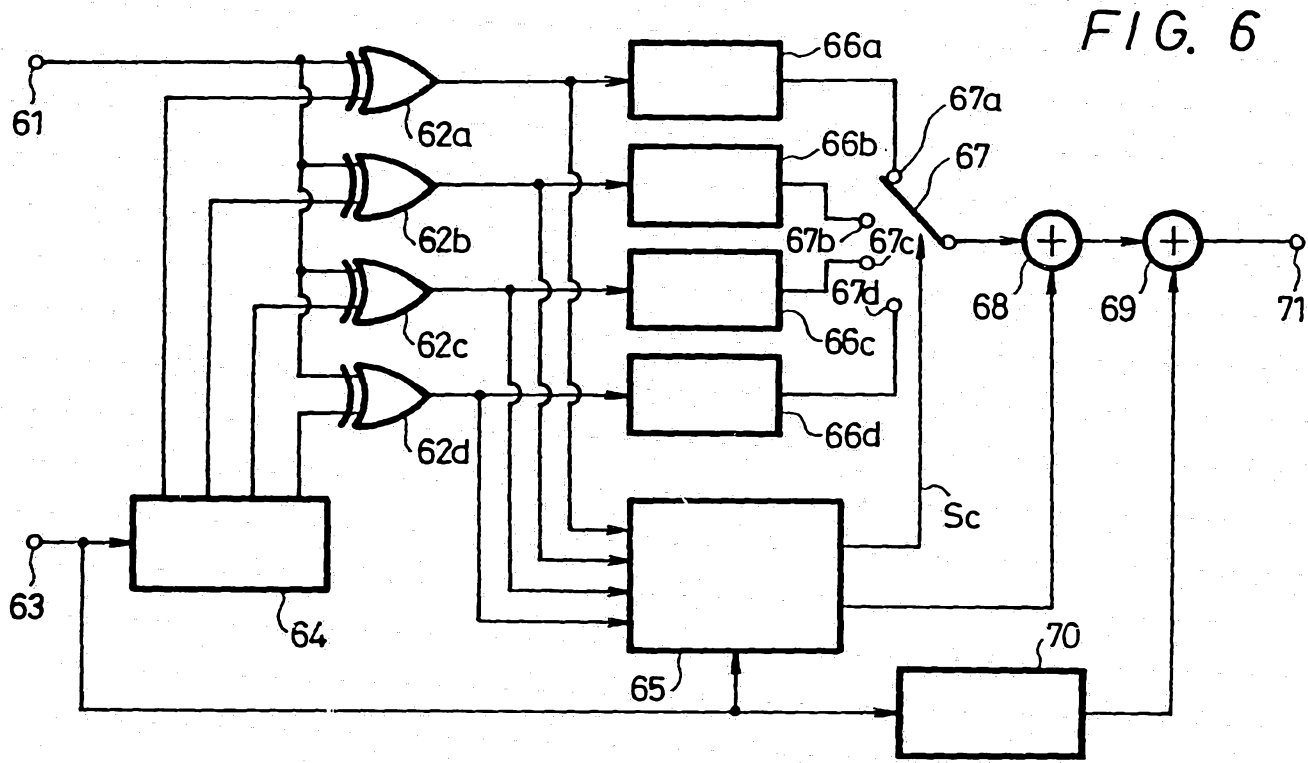
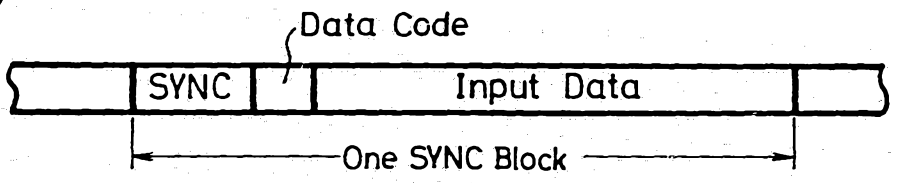


FIG. 6

FIG. 7



34072/89

FIG. 8

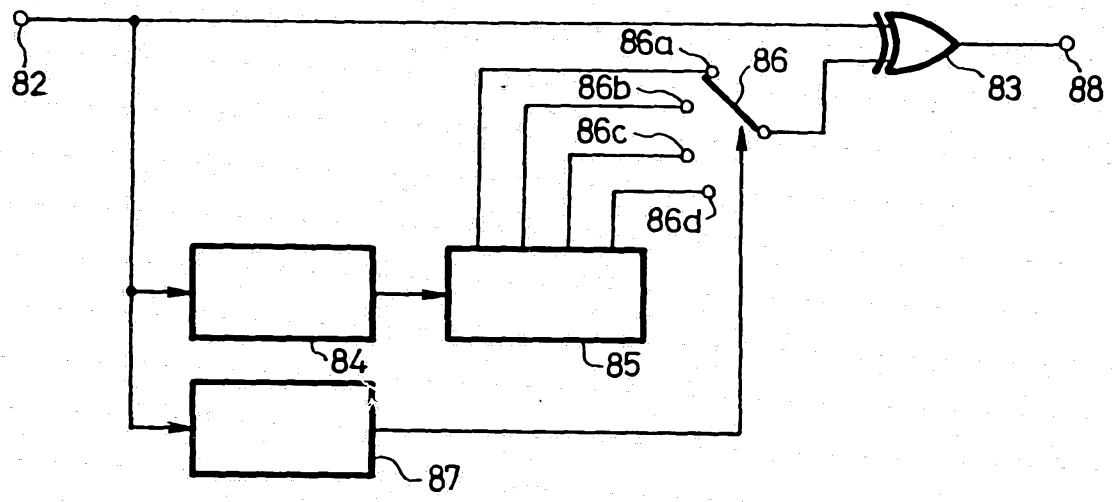


FIG. 9

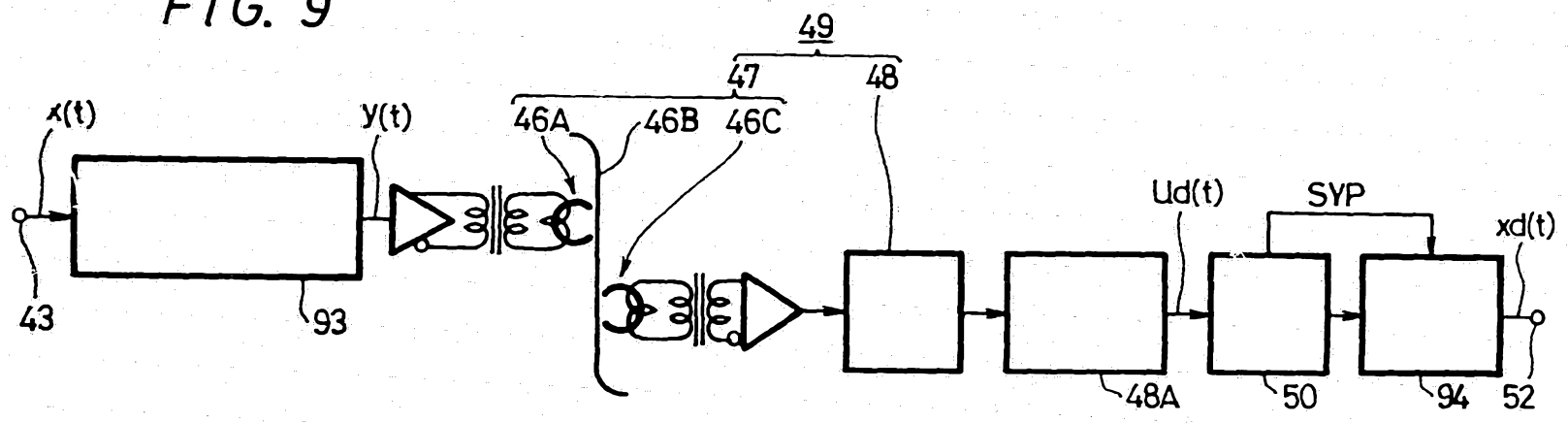


FIG. 10A

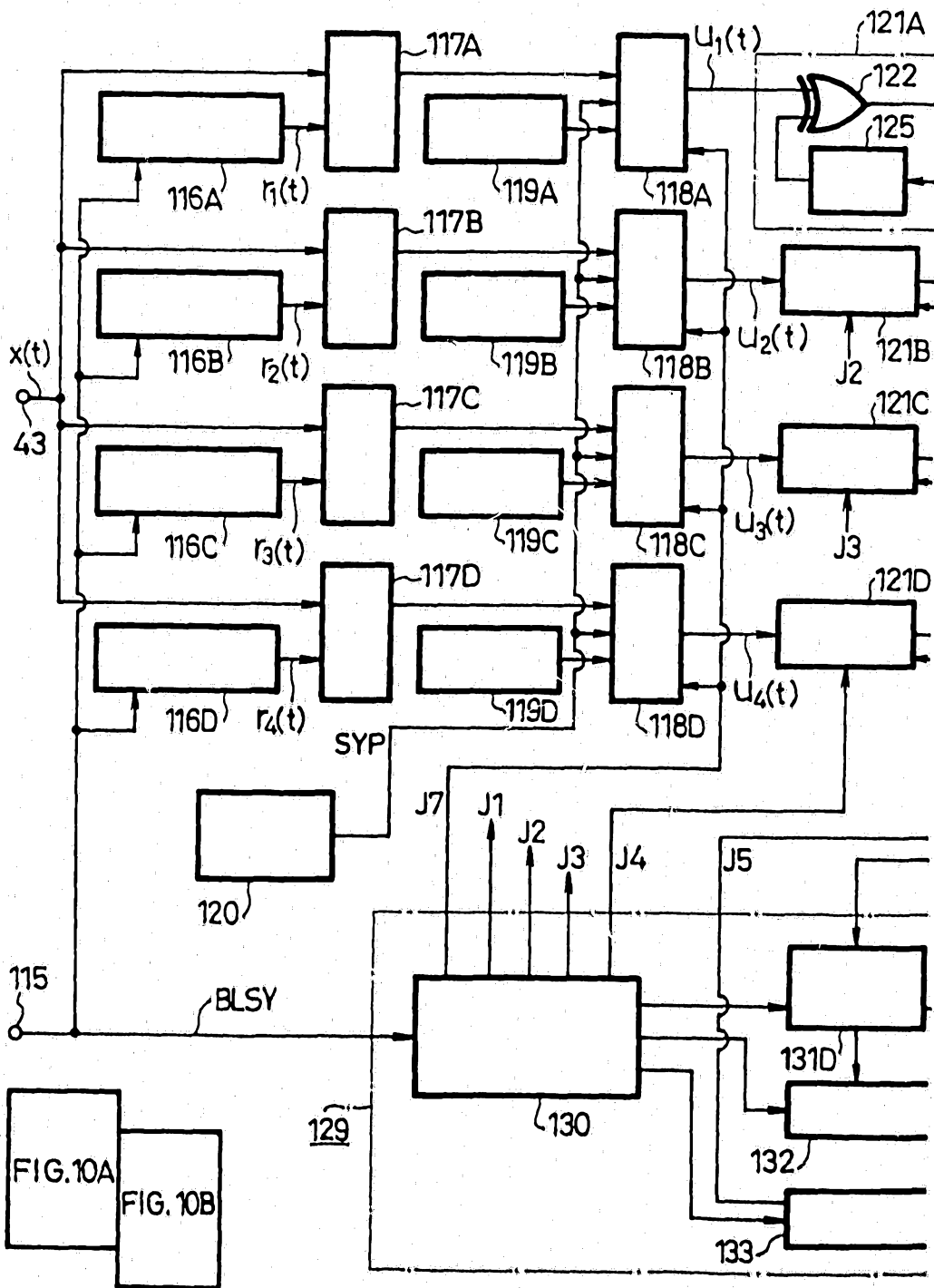


FIG. 10B

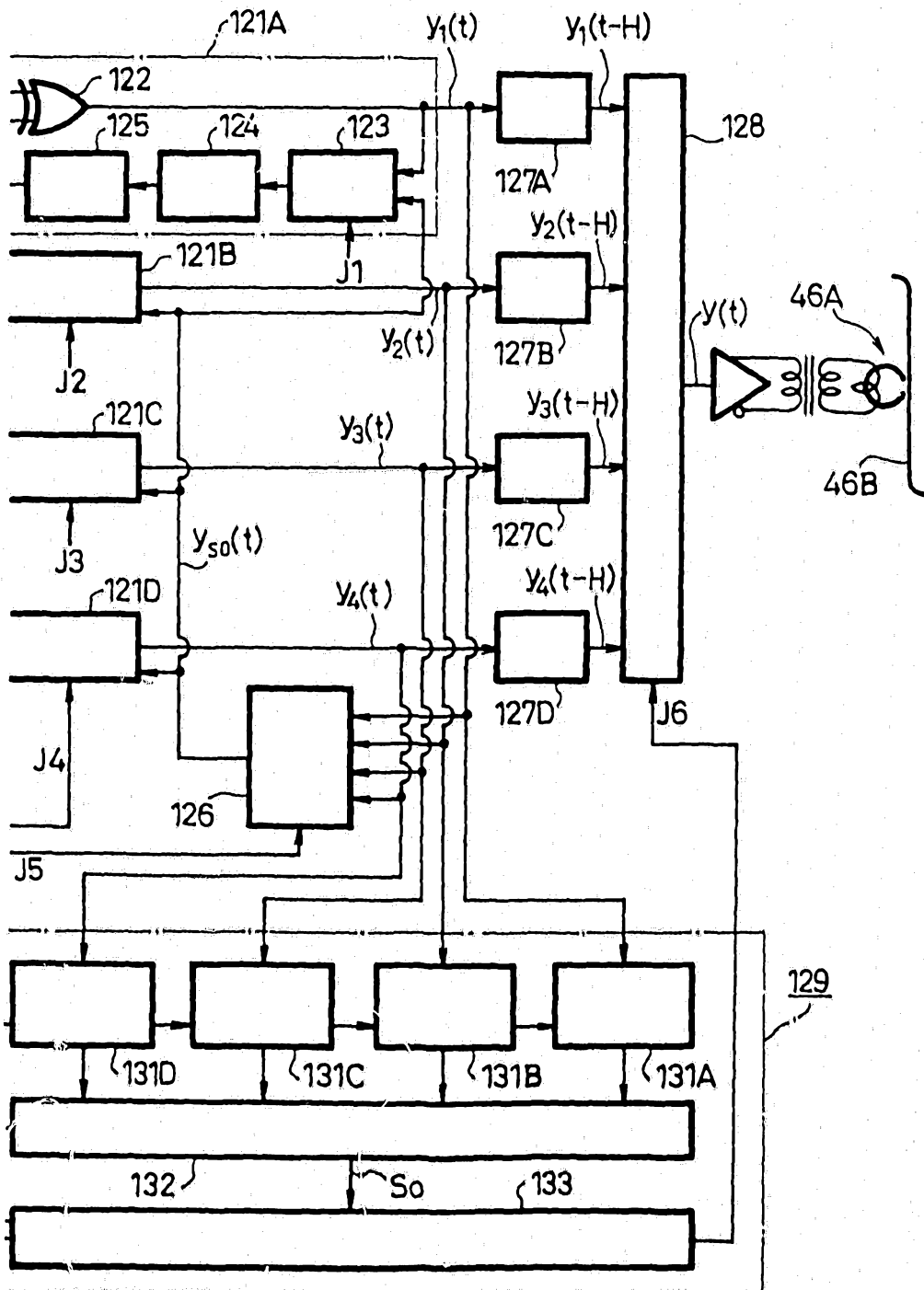


FIG. 11

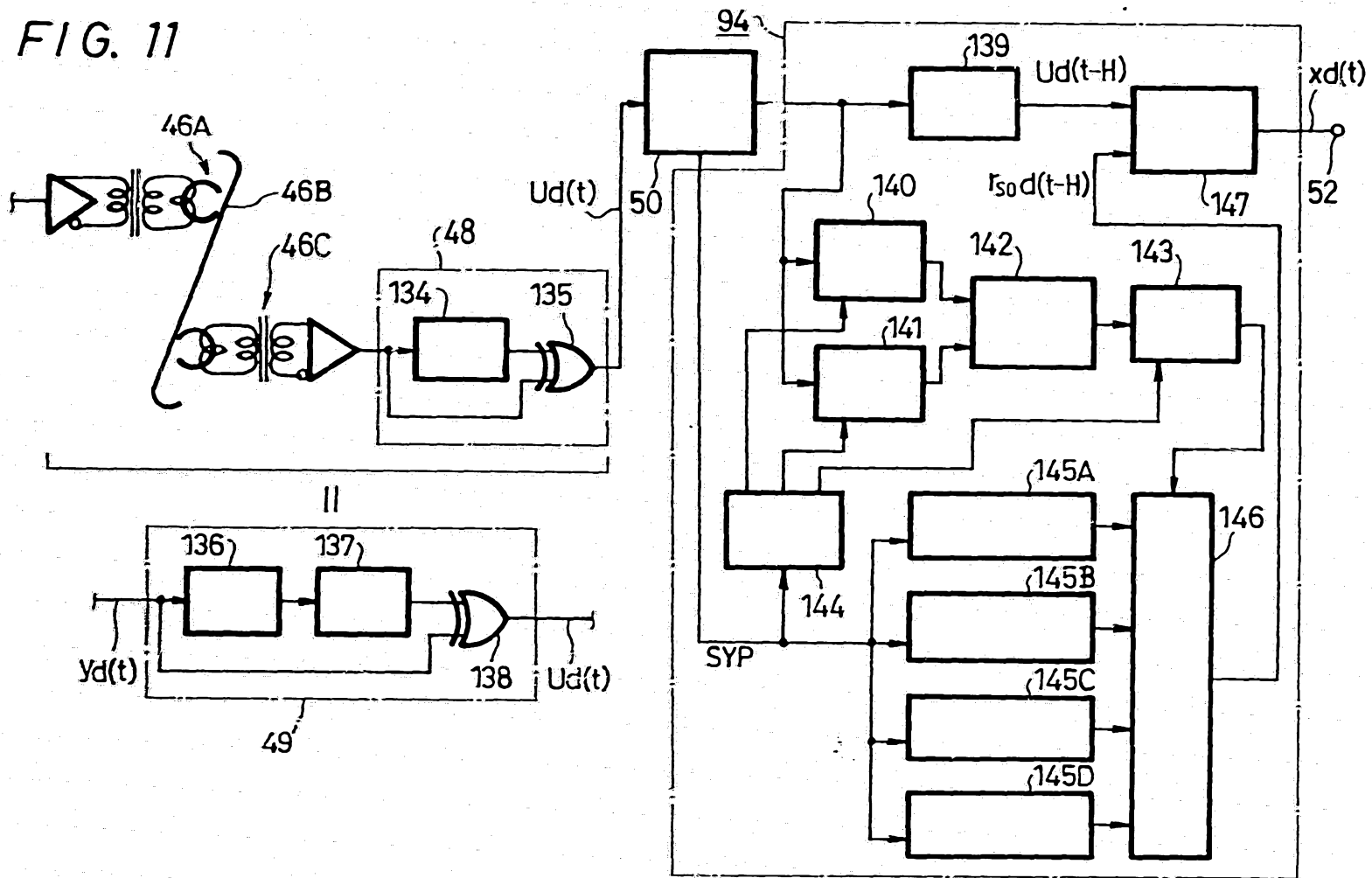


FIG. 12

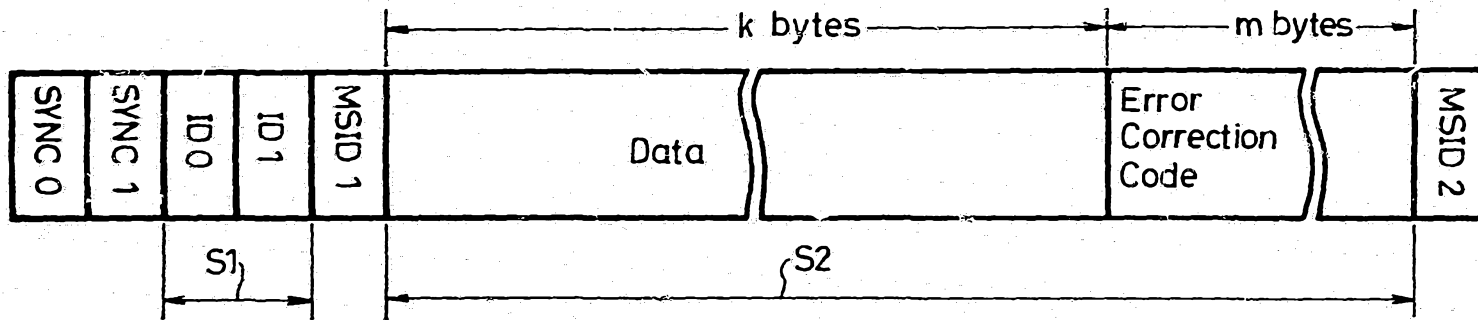


FIG. 13

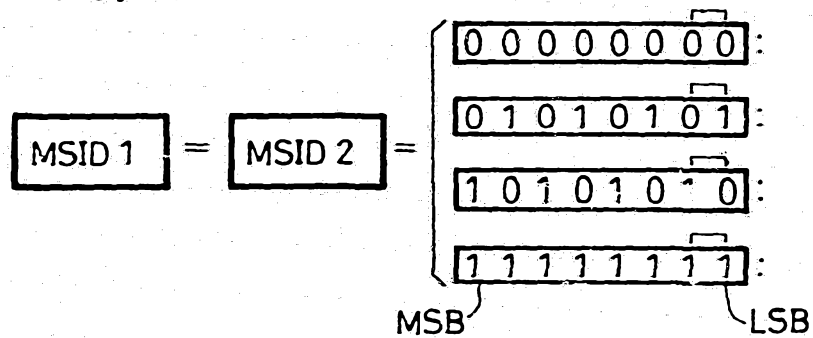


FIG. 14A

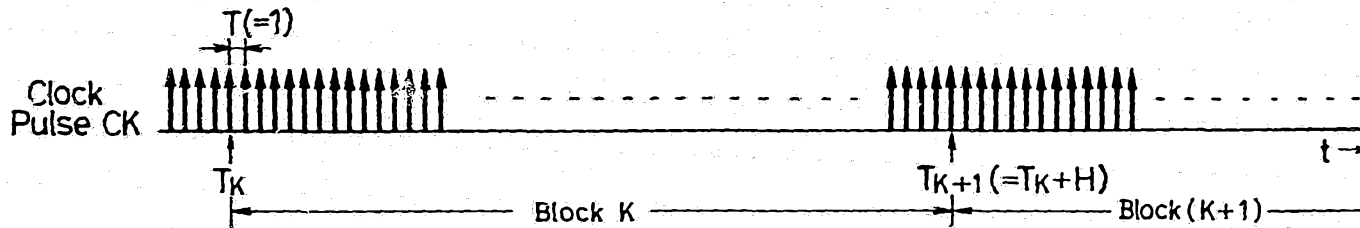


FIG. 14B

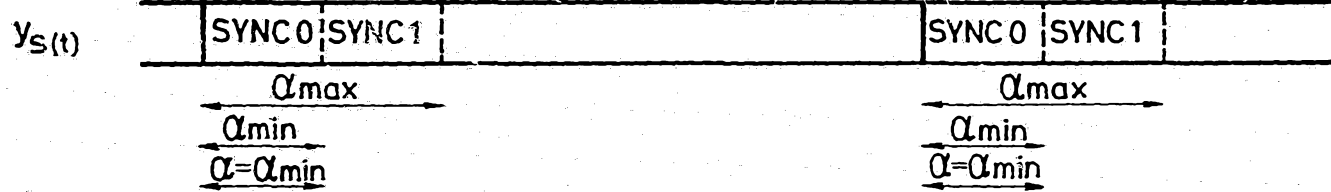


FIG. 14C

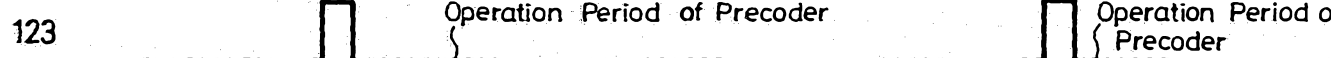


FIG. 14D

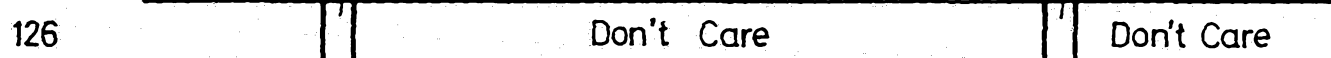


FIG. 14E



FIG. 14F

