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(54) **STRUCTURE AND FABRICATION METHOD OF ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT**

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(57) **ABSTRACT**

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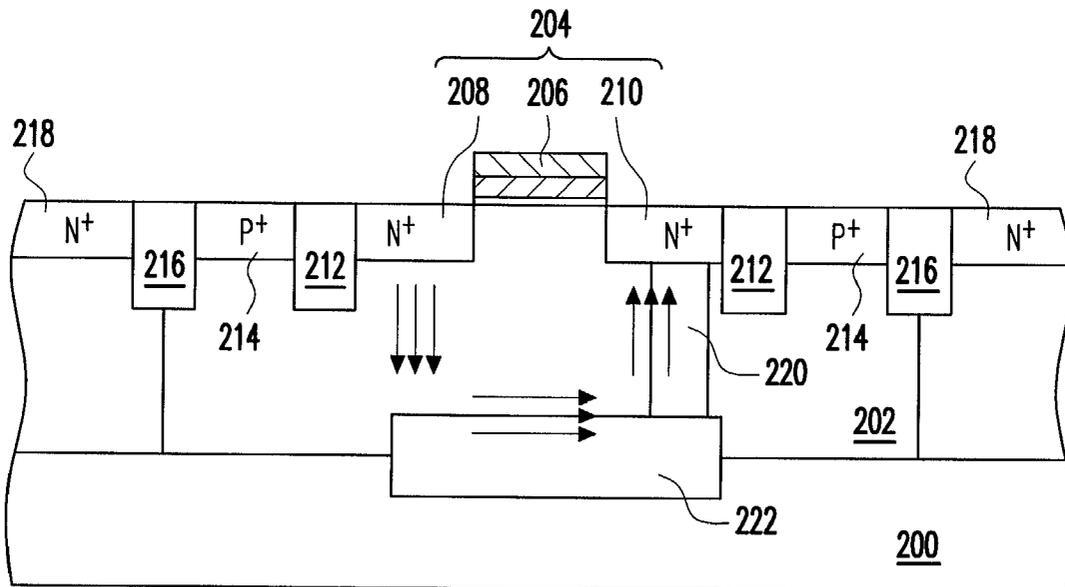
A structure of an electrostatic discharge protection circuit, in which a buried layer is formed in the substrate of the electrostatic discharge protection circuit, and a sinker layer electrically connected to the buried layer and a drain is also formed therein. Thereby, when the electrostatic discharge protection circuit is activated, the current flows from a source through the buried layer and the sinker layer to the drain. The current flow path is remote from the gate dielectric layer to avoid damaging the gate dielectric by a large current, so as to improve the dielectric strength of the electrostatic discharge protection circuit.

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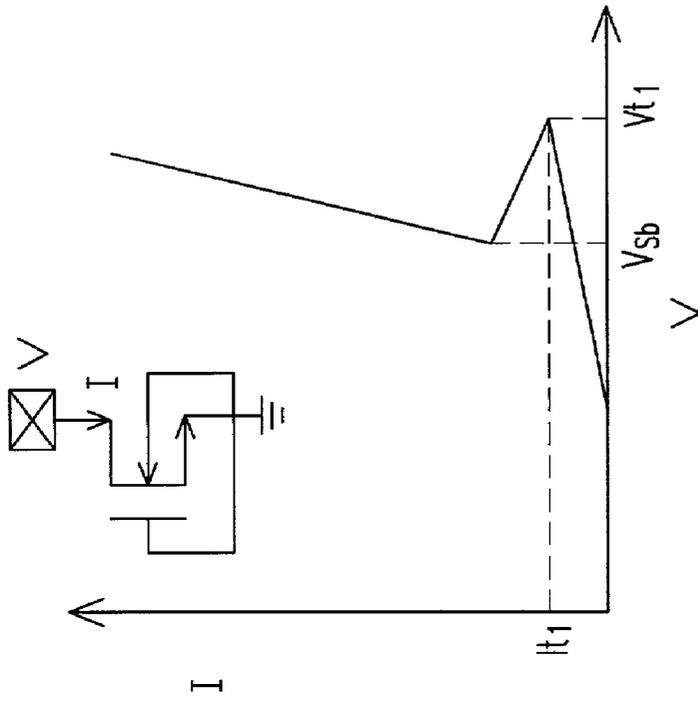


FIG. 2 (PRIOR ART)

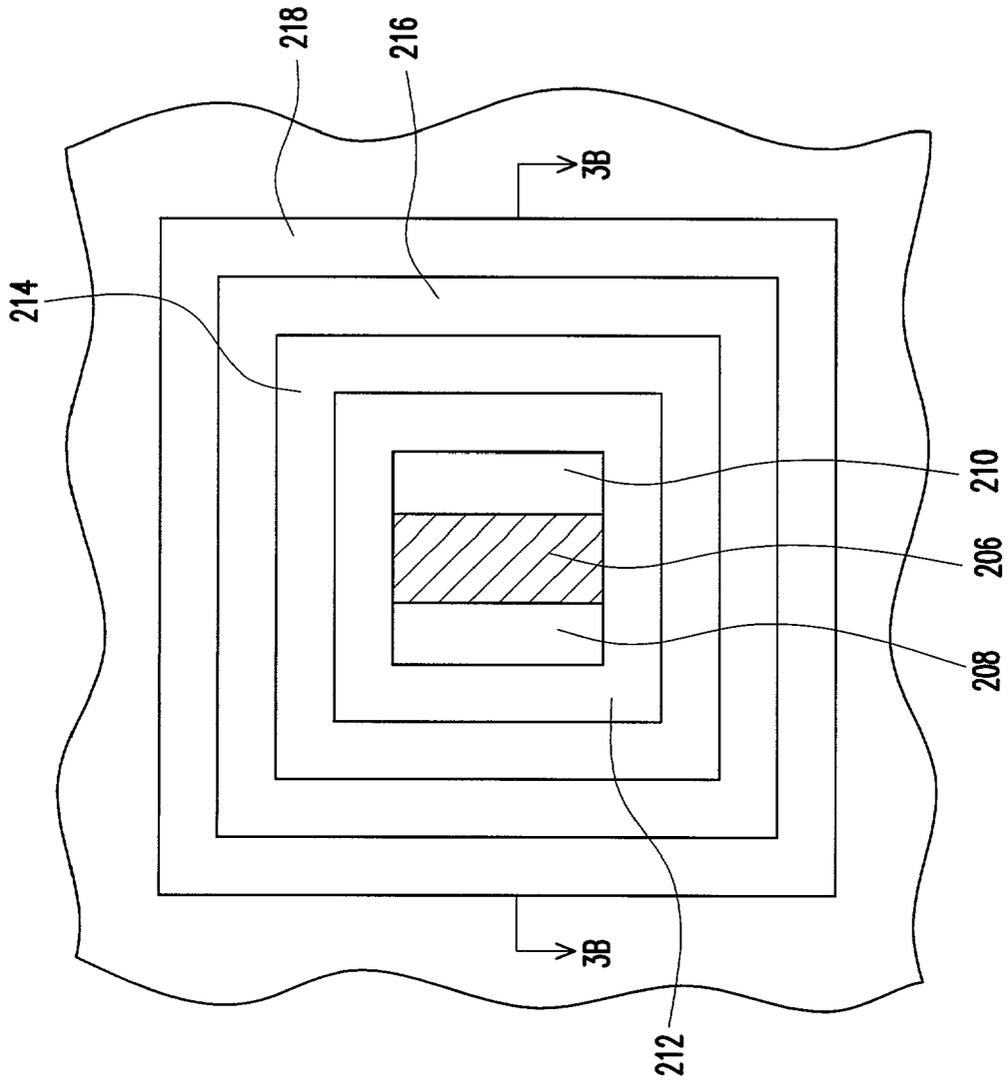


FIG. 3A

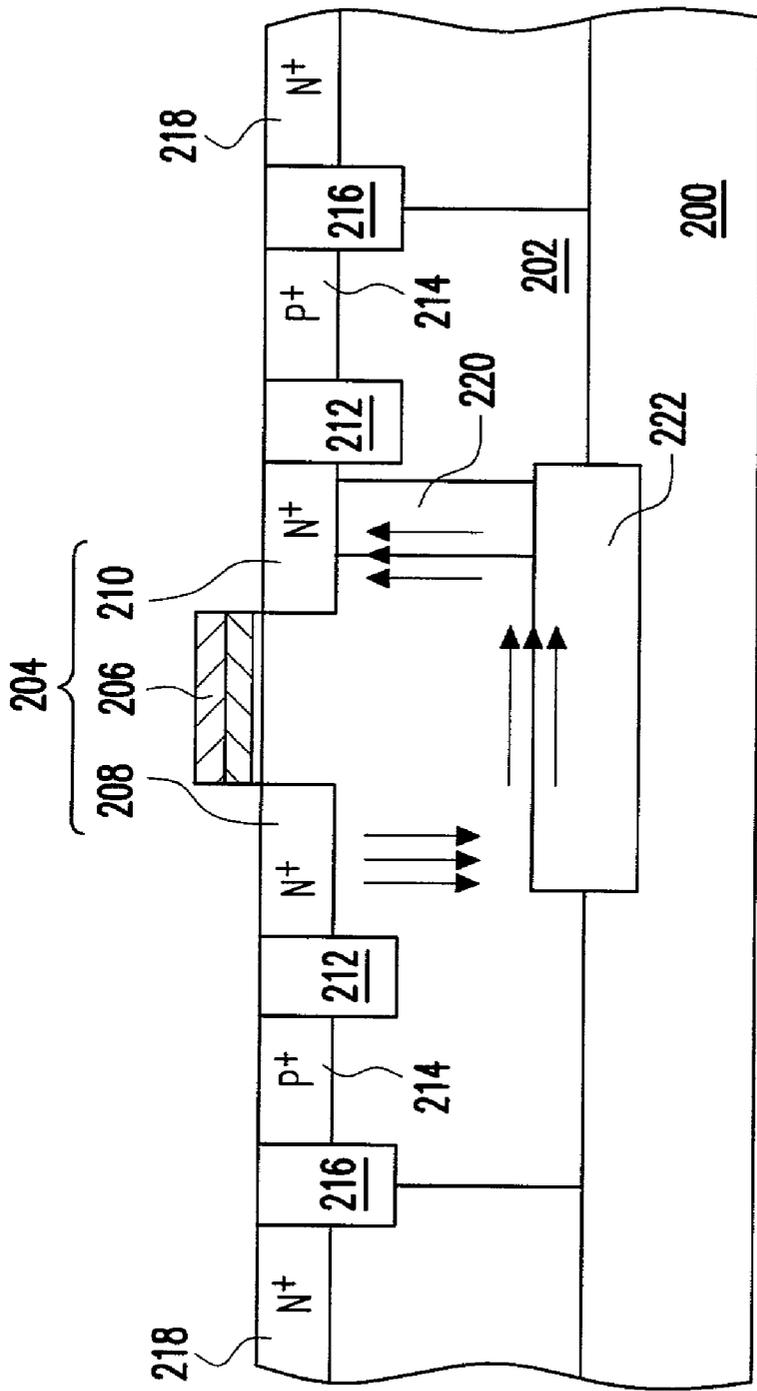


FIG. 3B

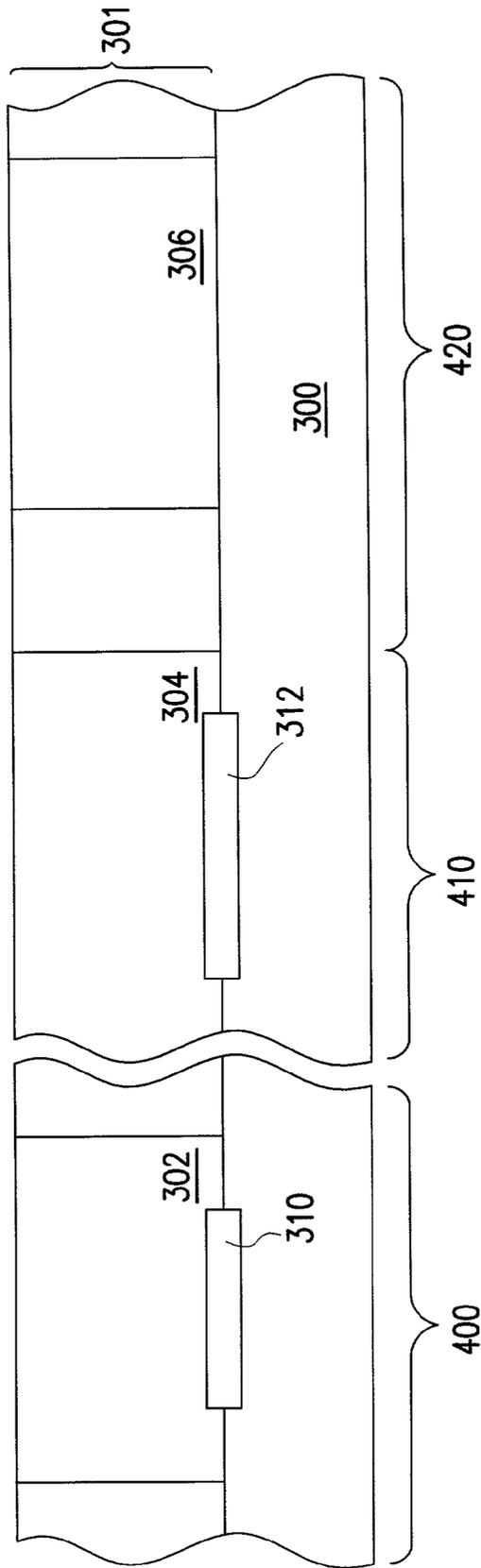


FIG. 4A

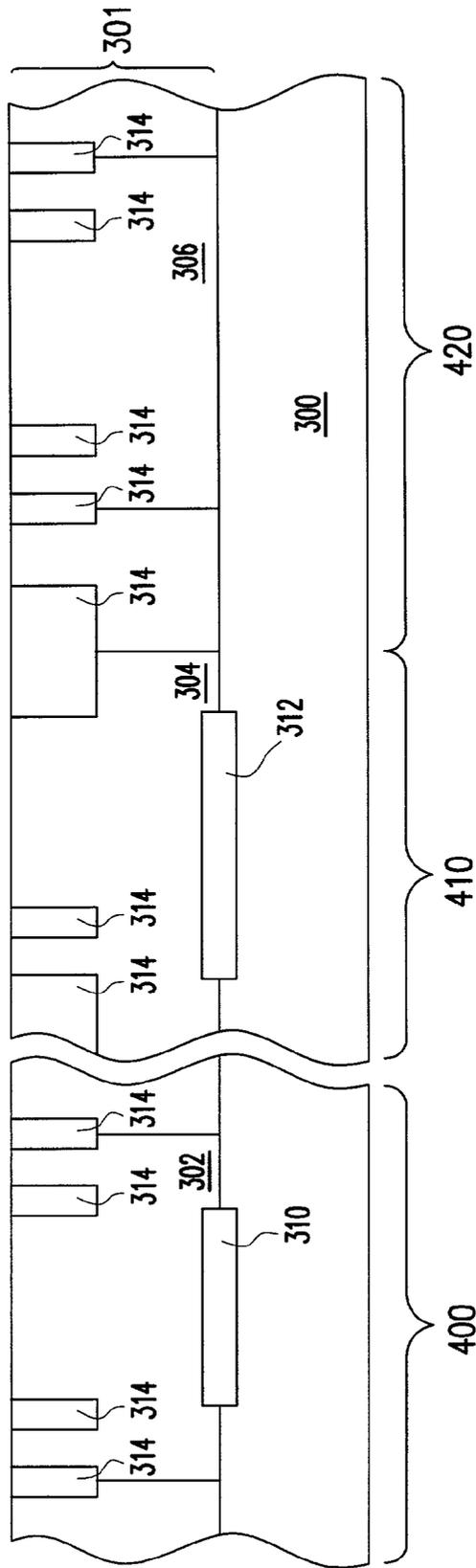


FIG. 4B

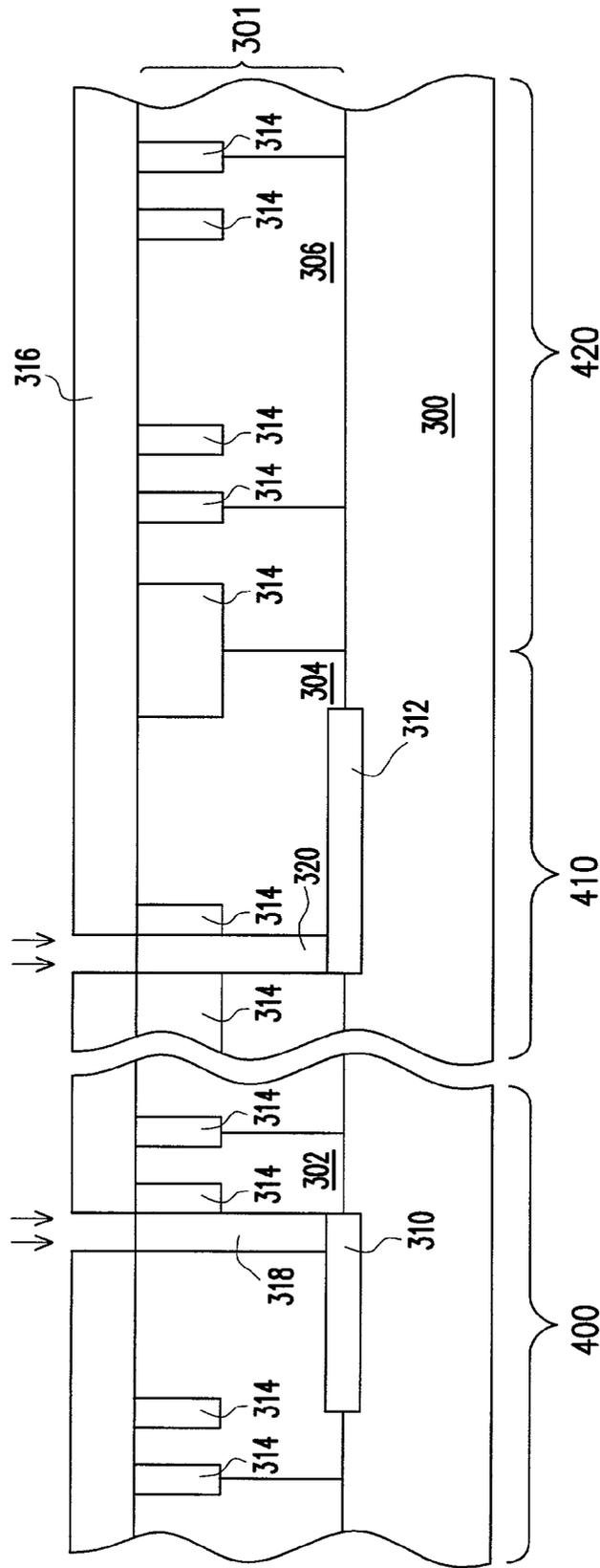


FIG. 4C

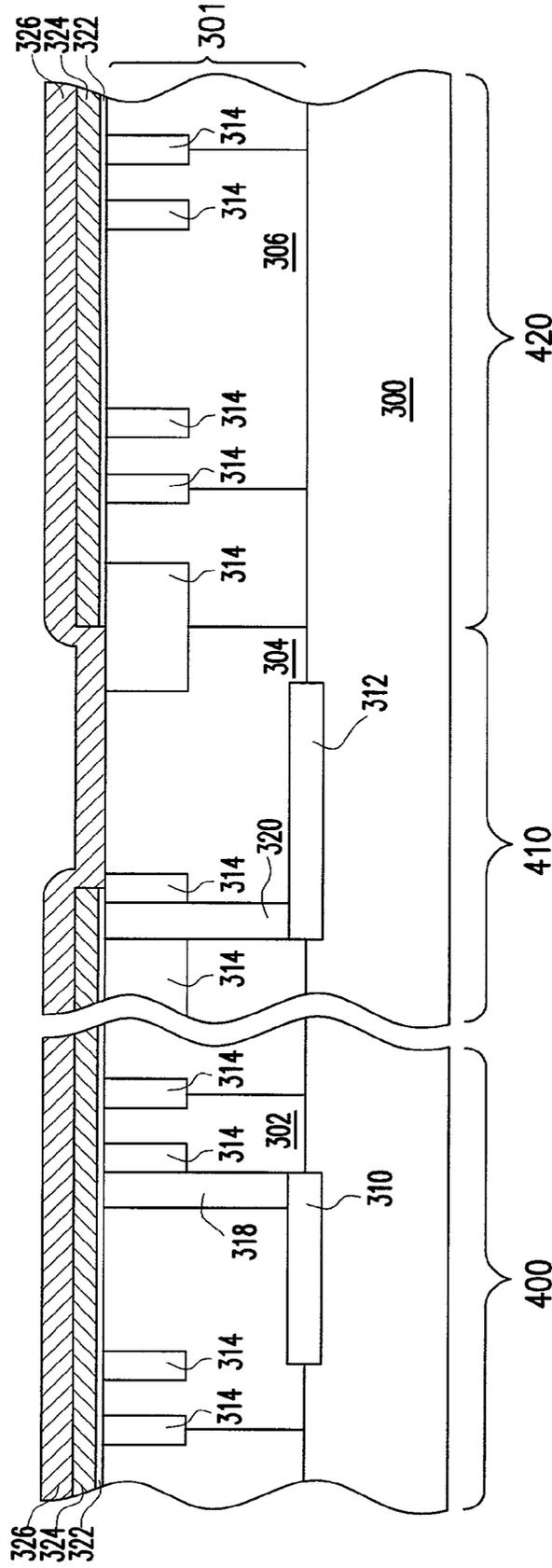


FIG. 4D

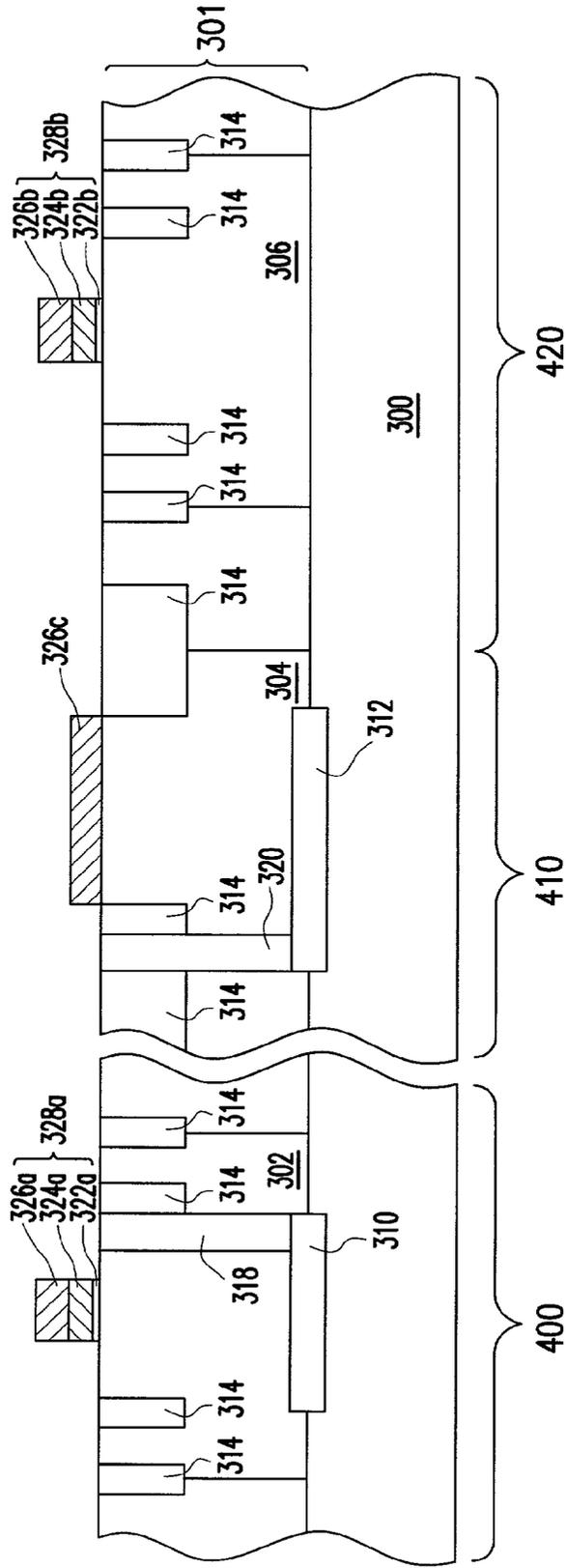


FIG. 4E

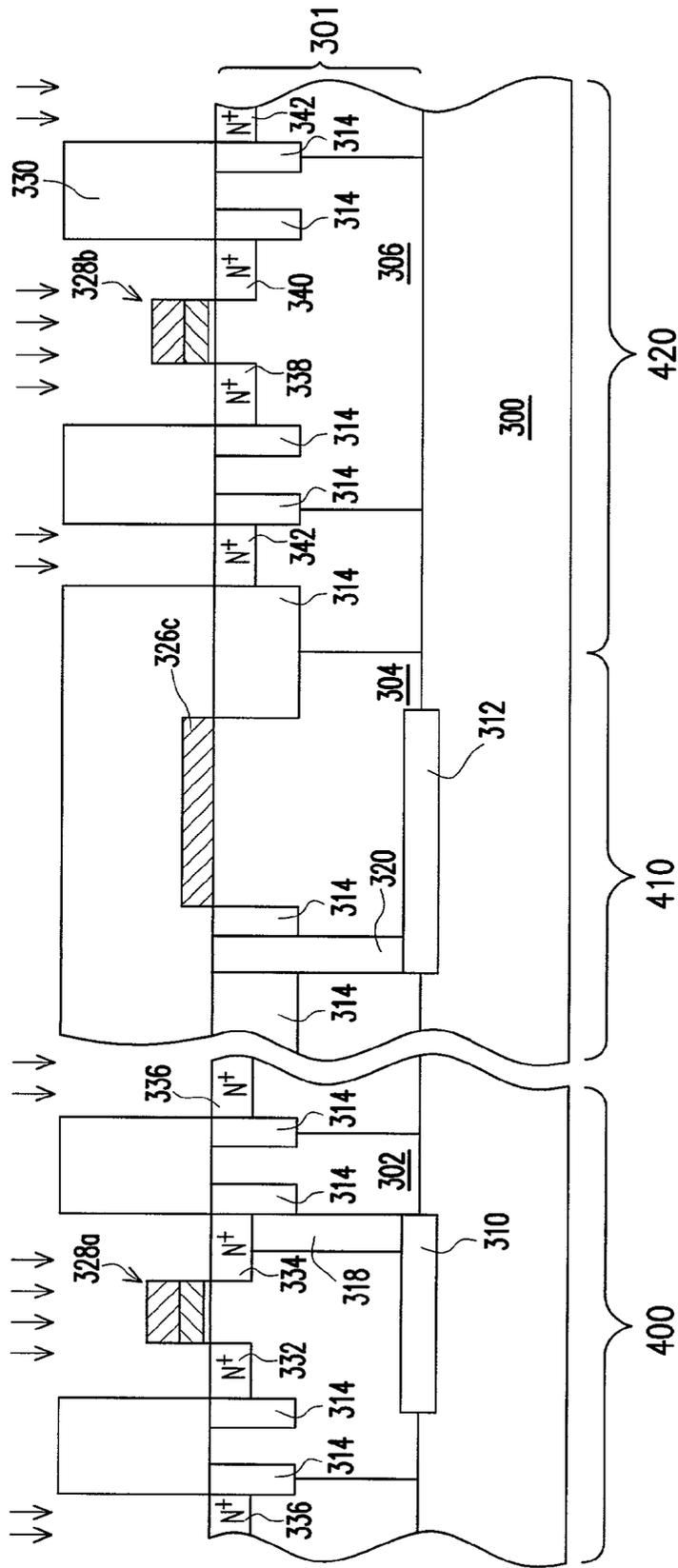


FIG. 4F



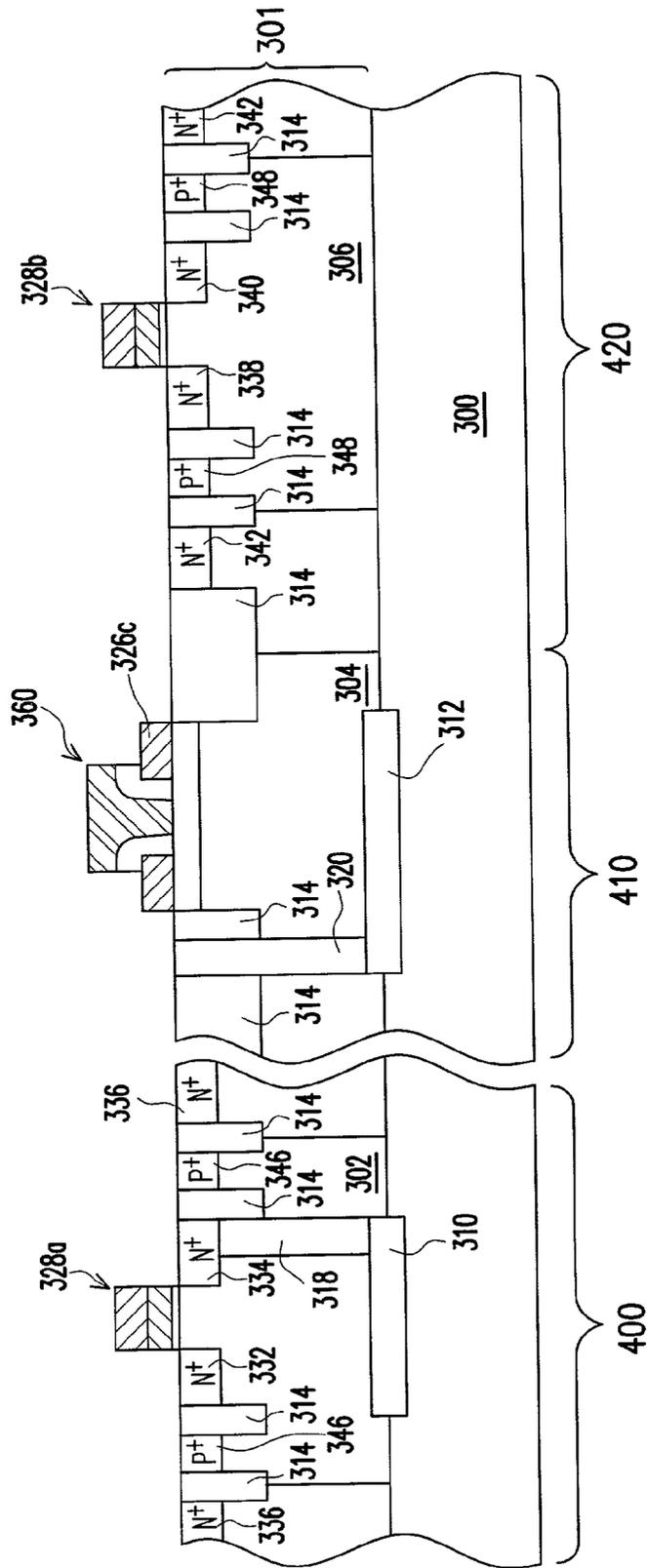


FIG. 4H

## STRUCTURE AND FABRICATION METHOD OF ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

### CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the priority benefit of Taiwan application serial no. 91108181, filed Apr. 22, 2002.

### BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates in general to a structure and a fabrication method of an electrostatic discharge protection circuit. More particularly, the invention relates to a structure and a fabrication method of an electrostatic discharge protection circuit, in which a sinker layer and a buried layer are formed to provide a low resistant current path.

[0004] 2. Description of the Related Art

[0005] The electrostatic discharge is an electrostatic drift phenomenon from a surface of a non-conductor that damages semiconductors or other circuit components in an integrated circuit. For example, hundreds to thousands of volts of static electricity carried by a human body walking on a blanket under a higher relative humidity can be detected. When the relative humidity is lower, more than ten thousand volts of electrostatic voltage can be detected. The equipment for packaging or testing integrated circuits also generates hundreds to thousands of volts of static electricity. When brought into contact with the above charge carriers (human body, equipment or instrument), the chips are discharged thereto. The surge caused by such electrostatic discharge may damage the integrated circuit of the chip or even cause failure of the integrated circuit.

[0006] To prevent damage to the integrated circuit of the chip, various mechanisms to suppress the electrostatic discharge have been proposed. Most commonly, hardware prevention is applied by forming an on-chip electrostatic discharge protection circuit between the internal circuit and each pad thereof.

[0007] FIG. 1 shows a schematic structure of a conventional NMOS electrostatic discharge protection circuit.

[0008] Referring to FIG. 1, a P well 102 is formed in a P-type substrate 100, and an NMOS transistor 104 and a P+ substrate-connecting region 114 are formed in the P well 102.

[0009] The above NMOS transistor 104 comprises a gate 106, a source 108, and a drain 110. The P+ substrate-connecting region 114 is isolated from the NMOS transistor 104 by a shallow trench isolation layer 112.

[0010] A guard ring 118 is formed on the substrate 100 surrounding the P+ substrate-connecting region 114. For the NMOS transistor 104, the guard ring 118 includes an N+ doped region with a conductive type opposite to that of the P well 102. The guard ring 118 and the P+ substrate-connecting region 114 are isolated from each other by a shallow trench isolation layer 116.

[0011] Referring to FIG. 2, the resistance of the substrate 100 is decreased as the voltage applied to the drain 110 is increased. When the voltage exceeds  $V_{t1}$ , the resistance of

the substrate 100 is reduced sufficiently to switch on the PN junction near the source 108. Meanwhile, the parasitic bipolar transistor is activated to generate a snapback voltage. Such snapback voltage rapidly drops to voltage  $V_{sb}$  and simultaneously conducts the electrostatic discharge current.

[0012] However, the flow path of the electrostatic discharge current is normally along a surface of the gate dielectric layer. When such current is large, the thermal energy generated thereby is concentrated near the flow path, that is, near the surface of the gate dielectric layer. A large thermal energy may blow the gate dielectric to cause failure of the electrostatic discharge protection circuit.

### SUMMARY OF THE INVENTION

[0013] The invention provides a structure and a fabrication method of an electrostatic discharge protection circuit, by which the protection performance of the electrostatic discharge protection circuit is enhanced.

[0014] The invention further provides a structure and a fabrication method of an electrostatic discharge protection circuit, by which the heat dissipation performance of the electrostatic discharge protection circuit is improved.

[0015] The structure of the electrostatic discharge protection circuit includes a substrate, a well, a transistor, a substrate-connecting region, a first isolation layer, a sinker layer, and a buried layer. The well is formed in the substrate, while the transistor is formed in the well. The transistor comprises a gate, a drain and a source. The substrate-connecting region is located in the well and isolated from the source and drain by the first isolation layer. The buried layer is formed at a junction between the well and the substrate under the transistor. The sinker layer is formed in the well and is electrically connected to the buried layer and the drain. The sinker layer and the buried layer have dopant with opposite conductive type to that of the well.

[0016] The above electrostatic discharge protection circuit further comprises a guard ring formed in the substrate. The guard ring is isolated from the substrate-connecting region by a second isolation layer. The guard ring is doped with a conductive type opposite to that of the well.

[0017] The invention further provides a method for fabricating an electrostatic discharge circuit. A substrate is provided. A well is formed in the substrate. At a lateral junction between the substrate and the well, a buried layer is formed. A sinker layer is further formed in the well to electrically connect the buried layer. A gate is formed in the well, and a source and a drain are formed in the well at two sides of the gate. The drain is electrically connected to the sinker layer. A substrate-connecting region is then formed in the well.

[0018] According to the above, in the electrostatic discharge protection circuit, a buried layer and a sinker layer electrically connected to the drain and the buried layer are formed. When the electrostatic discharge protection circuit is activated, the current flows in the substrate from the source through the buried layer and the sinker layer to the drain. Therefore, a large current flowing through a surface of the gate dielectric layer is prevented. Further, the gate dielectric layer is prevented from being blown. As a result, the dielectric strength of the electrostatic discharge protection circuit is increased, and the protection effect is enhanced.

[0019] Further, as the current flows in the substrate through the path from the source, the buried layer, the sinker layer to the drain, the thermal energy generated thereby is effectively dissipated. The heat dissipation performance of the electrostatic discharge protection circuit is significantly enhanced.

[0020] Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 shows a schematic drawing of a conventional electrostatic discharge protection circuit;

[0022] FIG. 2 shows a characteristics curve of a parasitic bipolar transistor;

[0023] FIG. 3A shows a top view of a structure of an electrostatic discharge protection circuit in one embodiment of the invention;

[0024] FIG. 3B shows a cross-sectional view of the electrostatic discharge protection circuit as shown in FIG. 3A; and

[0025] FIG. 4A to FIG. 4H show the process flow that incorporates both fabrication process of the electrostatic discharge protection circuit and the bipolar CMOS (Bi-CMOS) process.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] FIG. 3A shows a top view of an electrostatic discharge protection circuit in one embodiment of the invention, while FIG. 3B shows a cross-sectional view thereof.

[0027] Referring to FIG. 3A and FIG. 3B, the electrostatic discharge protection circuit provided by the invention includes a substrate 200, a well 202, an NMOS transistor 204, a P+ substrate-connecting region 214, a shallow trench isolation layer 212, a sinker layer 220 and a buried layer 222.

[0028] The P well 202 is formed in the substrate 200 and is doped with a first conductive type impurity.

[0029] The NMOS transistor 204 is formed in the P well 202. The NMOS transistor 204 has a gate 206, a source 208 and a drain 210. The source 208 and the drain 210 are formed in the P well 202 at two sides of the gate 206. The conductive type of the source 208 and the drain 210, which is the second conductive type, is opposite to the first conductive type of the P well 202.

[0030] The P+ substrate-connecting region 214 is formed in the P well at a periphery of the NMOS transistor 204. The P+ substrate-connecting region 214 is isolated from the NMOS transistor 204 by the shallow trench isolation layer 212.

[0031] The buried layer 222 is formed at a junction between the P well 202 and the substrate 200 under the transistor 204. The buried layer 222 is doped with the second conductive type of impurity, which is opposite to the first conductive type of the P well 202. The width of the buried layer 222 extends from the source 208 to the drain 210 of the NMOS transistor 204.

[0032] The sinker layer 220 is formed between the buried layer 222 and the drain 210 and is electrically connected to both the buried layer 222 and the drain 210. The doping type of the sinker layer 220 includes the second conductive type, and the width thereof is narrower than the width of the drain 210.

[0033] In addition, a guard ring 218 may be formed in the electrostatic discharge protection circuit. The guard ring 218 is formed in the substrate 200 and isolated from the P+ substrate-connecting region 214 of the NMOS transistor 204 by the shallow trench isolation layer 216. The guard ring 218 is doped with the second conductive type impurity, which is opposite to that of the P well 202.

[0034] The process for forming the sinker layer 220 includes performing a step of ion implantation after forming the buried layer 222. The sinker layer 220 electrically connected from a surface of the P well 202 to the buried layer 222 is thus formed in the P well 202.

[0035] The formation of the buried layer 222 and the sinker layer 220 provide a lower resistant path for electrostatic discharge current. The current thus flows from the source 208, through the buried layer 222 and the sinker layer 220 to the drain 210.

[0036] In the above embodiment, the structure of an NMOS electrostatic discharge protection circuit is used as an example for describing the invention. However, the application of the invention is not limited to the NMOS electrostatic discharge protection circuit. Instead, the invention can also be applied to the PMOS electrostatic discharge protection circuit. Under such circumstance, an N well is formed in a P substrate, and a PMOS transistor is formed in the N well. The buried layer is formed at a junction between the N well and the substrate under the PMOS transistor. The buried layer is doped with P type impurity, which is different from that of the N well. The sinker layer is electrically connected the drain and the buried layer. The sinker layer is doped with P type impurity, again, which is different from that of the N well.

[0037] In the above embodiment, the first conductive type includes P type, while the second conductive type includes N type. Or alternatively, the first and the second conductive types can be interchanged as N type and P type, respectively.

[0038] An embodiment for fabricating an electrostatic discharge protection circuit is shown in FIGS. 4A to 4H.

[0039] FIG. 4A to FIG. 4H illustrate an embodiment that incorporates processes for the electrostatic discharge protection circuit and a bipolar CMOS. For simplicity, the steps for forming the electrostatic discharge protection circuit and the PMOS device of the CMOS are omitted.

[0040] Referring to FIG. 4A, a substrate 300 is provided. The substrate 300 is divided into an electrostatic discharge protection circuit (ESD) region 400, a bipolar transistor (bipolar) region 410 and a CMOS transistor (CMOS) region 420. Buried layers 302, 304 are first formed on the substrate 300, and the a doped epitaxy layer 301 is formed over the substrate 300. P wells 302 and 306 are formed in the ESD region 400 and the CMOS region 420, respectively, while an N well 304 is formed in the bipolar region 410.

[0041] Referring to FIG. 4B, an isolation layer 314 is formed in the epitaxy layer 301. The isolation layer 314

includes a shallow trench isolation layer and is formed to isolate devices, or different regions in the same device.

[0042] Referring to FIG. 4C, a mask layer 316 is formed, and the surface of the substrate is doped to form sinker layers 318 and 320 in the ESD region 400 and the bipolar region 410. The sinker layers 318 and 320 are electrically connected to the buried layers 310 and 312, respectively. The doping type for the sinker layers 310 and 312 include N type, which is opposite to that of the P wells 302 and 306. The method for forming the sinker layers 318 and 320 includes ion implantation.

[0043] Referring to FIG. 4D, the mask layer 316 is removed. A gate dielectric layer 322 and a conductive layer 324 are formed on surfaces of the ESD region 400, the bipolar region 410 and the CMOS region 420. The gate dielectric layer 322 and the conductive layer 324 on the active region in the bipolar region 410 are removed to expose the surface thereof. A conductive layer 326 is formed to cover the exposed surface of the bipolar region 410.

[0044] Referring to FIG. 4E, the conductive layer 326, the conductive layer 324 and the gate dielectric layer 322 are patterned into the conductive layers 326a, 326b, the conductive layers 324a, 324b, and the gate dielectric layers 322a, 322b that construct the gates 328a and 328b in the ESD region 400, and the CMOS region 420, respectively, and the conductive layer 326c in the bipolar region 410.

[0045] Referring to FIG. 4F, a patterned mask 330 is formed in the ESD region 400, the bipolar region 410 and the CMOS region 420. A doping process is performed with the patterned mask as an implantation mask, so that a source 332 and a drain 334 of an NMOS transistor, and a guard ring 336 are formed in the ESD region 400. Meanwhile, a source 338 and a drain 340 of an NMOS transistor, and a guard ring 342 are formed in the CMOS region 420.

[0046] Referring to FIG. 4G, the mask layer 330 is removed. A patterned mask 330 is formed on the ESD region 400, the bipolar region 410 and the CMOS region 420 for performing a doping process. P+ substrate-connecting regions 346 and 348 for the NMOS transistors are formed in the ESD region 400 and the CMOS region 420, respectively.

[0047] The ESD protection circuit and the CMOS structure are completed by the processes shown up to FIG. 4G. FIG. 4H shows the subsequent process for forming the bipolar transistor. The bipolar transistor 360 is then formed in the bipolar region 410. As the process for forming the bipolar transistor is not essential to the subject matter of the invention, the description thereof is not further introduced.

[0048] In the above embodiment, the P type and N type doping regions or impurities can be interchanged with each other.

[0049] For the BiCMOS process, the sinker and buried layers of the structure of the electrostatic discharge protection circuit can be formed simultaneously with those of the bipolar transistor. That is, the pattern of the electrostatic discharge protection circuit is considered when designing the photomask. Therefore, in the BiCMOS process, the electrostatic discharge protection circuit with the sinker layer and the buried layer can be formed without introducing additional photomasks.

[0050] The above process for fabricating the electrostatic discharge protection circuit is integrated with the BiCMOS process. That is, the electrostatic discharge protection circuit with the sinker layer and the buried layer is formed together with formation of the BiCMOS process. However, the application of the invention is not limited to BiCMOS process only. In fact, the process for fabricating the electrostatic discharge protection circuit can be performed individually or integrated with other processes. Further, such process is not limited in forming the electrostatic discharge protection circuit for NMOS only. The process is also applicable for forming the PMOS electrostatic discharge protection circuit.

[0051] According to the above, by forming a buried layer and a sinker layer electrically connected to the buried layer and the sinker layer in the substrate for forming an electrostatic discharge protection circuit, the current flows from the source through the buried and sinker layers to the drain when the electrostatic discharge protection circuit is activated. As the current flows in the substrate, a large current flowing near the surface of the gate dielectric layer is avoided. The gate dielectric layer is thus prevented from being blown. The dielectric strength of the electrostatic discharge protection circuit is improved, and the protection performance thereof is enhanced.

[0052] The current path from the source through the sinker and buried layers to the drain allows the heat to dissipate through the substrate, so that dissipation of heat generated by the current is improved. That is, the heat dissipation performance of the electrostatic discharge protection circuit is improved.

[0053] In addition, the process for fabricating the electrostatic discharge protection circuit can be integrated with the BiCMOS process. Therefore, the sinker and buried layers of the electrostatic discharge protection circuit can be formed together with those of the bipolar transistor using the same photomask. That is, without increasing any additional photomasks, the buried and sinker layers of the electrostatic discharge protection circuit are formed.

[0054] Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is understood that the specification and examples are to be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. An electrostatic discharge protection circuit, comprising:

- a substrate;
- a well, formed in the substrate and doped with a first conductive type;
- a transistor, formed in the well and having a gate, a drain and a source;
- a substrate-connecting region, formed in the well at a periphery of the transistor, wherein the substrate-connecting region is doped with the first conductive type;
- a first isolation layer, formed in the well to isolate the substrate-connecting region from the transistor;

- a buried layer, formed at a junction between the well and the substrate under the transistor, wherein the buried layer is doped with a second conductive type; and
- a sinker layer, formed between the buried layer and the drain and electrically connected to the buried layer and the drain, wherein the sinker layer is doped with the second conductive type.
2. The electrostatic discharge protection circuit according to claim 1, further comprising a guard ring formed in the substrate, wherein the guard ring is isolated from the substrate-connecting region by a second isolation layer.
3. The electrostatic discharge protection circuit according to claim 1, wherein the guard ring is doped with the second conductive type.
4. The electrostatic discharge protection circuit according to claim 1, wherein the sinker layer has a width narrower than that of the drain.
5. The electrostatic discharge protection circuit according to claim 1, wherein the buried layer has a width extending from the source to the drain of the transistor.
6. The electrostatic discharge protection circuit according to claim 1, wherein the first conductive type includes P type, and the second conductive type includes N type.
7. The electrostatic discharge protection circuit according to claim 1, wherein the first conductive type includes N type, and the second conductive type includes P type.
8. A method for fabricating an electrostatic discharge protection circuit, comprising:
- providing a substrate;
  - forming a well in the substrate, wherein the well is doped with a first conductive type;
  - forming a buried layer at a lateral junction between the well and the substrate, wherein the buried layer is doped with a second conductive type;
  - forming a sinker layer doped with the second conductive type in the well, wherein the sinker layer is electrically connected to the buried layer;
  - forming a gate in the well;
  - forming a source and a drain in the well at two sides of the gate, wherein the drain is electrically connected to the sinker layer; and
  - forming a substrate-connecting region in the well.
9. The method according to claim 8, wherein the step for forming the buried layer includes ion implantation.
10. The method according to claim 8, wherein the step of forming the buried layer includes forming the buried layer with a width extending from the source to the drain under the transistor.
11. The method according to claim 8, wherein the step of forming the sinker layer includes ion implantation.
12. The method according to claim 8, wherein the steps for forming the sinker layer include forming the sinker layer with a width narrower than that of the drain.

13. The method according to claim 8, wherein the first conductive type includes P type and the second conductive type includes N type.

14. The method according to claim 8, wherein the first conductive type includes N type and the second conductive type includes P type.

15. A method of fabricating a semiconductor device, which comprises a bipolar transistor, a CMOS and an electrostatic discharge protection circuit, the method comprising

providing a substrate, which comprises an electrostatic discharge protection circuit region, a bipolar transistor region and a CMOS transistor region, wherein a first P well is formed in the electrostatic discharge protection circuit, a second P well is formed in the CMOS transistor region, and an N well is formed in the bipolar transistor region;

simultaneously forming a first buried layer at a lateral junction between the first P well and the substrate, and a second buried layer at a lateral junction between the N well and the substrate;

simultaneously forming a first sinker layer in the first P well and a second sinker layer in the N well, wherein the first sinker layer is electrically connected to the first buried layer, and the second sinker layer is electrically connected to the second buried layer;

forming a first NMOS gate on the first P well, a second NMOS gate on the second P well, and a conductive layer on the N well;

forming a first NMOS source and a first NMOS drain in the first P well at two sides of the first NMOS gate and a second NMOS source and a second NMOS drain in the second P well at two sides of the second NMOS gate simultaneously;

forming a first P+ substrate-connecting region in the first P well and a second P+ substrate-connecting region in the second P well simultaneously; and

forming a bipolar transistor on the conductive layer.

16. The method according to claim 15, wherein the step of forming the first and second buried layers includes forming the first and second buried layers with a width extending from the first NMOS and the second NMOS sources to the first NMOS and the second NMOS drains under the first and the second transistors, respectively.

17. The method according to claim 15, wherein the step of forming the first and the second sinker layers includes forming the first and the second sinker layers with a width narrower than those of the first and the second NMOS drains, respectively.

18. The method according to claim 15, wherein the first and the second buried layers are formed in the same process.

19. The method according to claim 15, wherein the first and the second sinker layers are formed in the same process.

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