

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
20 February 2003 (20.02.2003)

PCT

(10) International Publication Number
WO 03/015181 A1

(51) International Patent Classification⁷: **H01L 29/78**,
21/336

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(21) International Application Number: PCT/US02/25289

(22) International Filing Date: 9 August 2002 (09.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/928,124 10 August 2001 (10.08.2001) US
09/928,163 10 August 2001 (10.08.2001) US
60/381,320 16 May 2002 (16.05.2002) US

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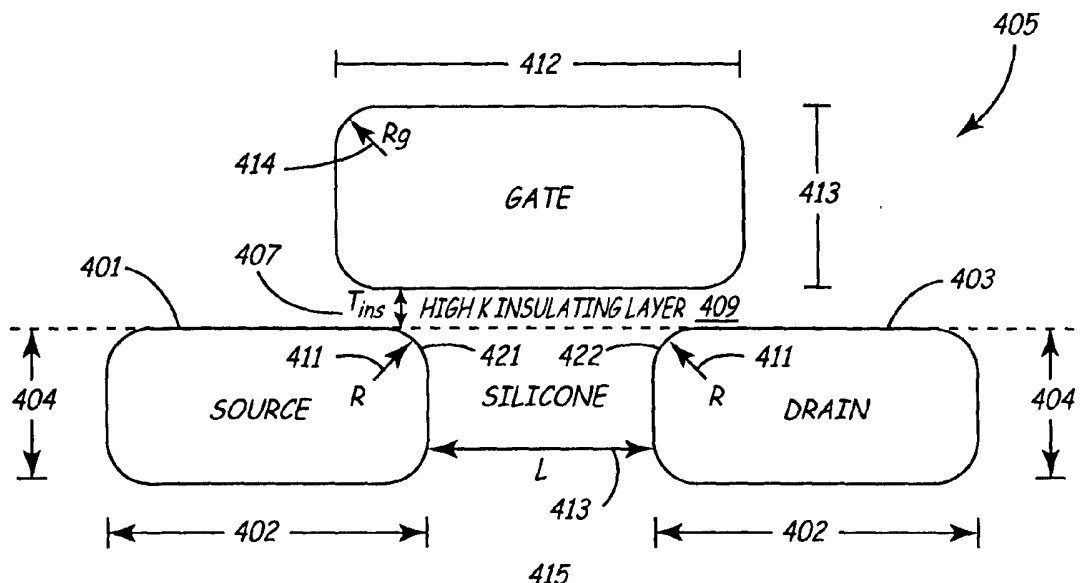
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG,
SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN,
YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK,
TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

[Continued on next page]

(54) Title: TRANSISTOR HAVING HIGH DIELECTRIC CONSTANT GATE INSULATING LAYER AND SOURCE AND DRAIN FORMING SCHOTTKY CONTACT WITH SUBSTRATE



(57) Abstract: The invention is directed to a device for regulating the flow of electric current with high dielectric constant gate insulating layer and a source and/or drain forming a Schottky contact or Schottky-like region with a substrate and its fabrication method. In one aspect, the gate insulating layer has a dielectric constant greater than the dielectric constant of silicon. In another aspect, the current regulating device may be a MOSFET device, optionally a planar P-type or N-type MOSFET, having any orientation. In another aspect, the source and/or drain may consist partially or fully of a silicide.

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— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

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**TRANSISTOR HAVING HIGH DIELECTRIC CONSTANT GATE
INSULATING LAYER AND SOURCE AND DRAIN FORMING
SCHOTTKY CONTACT WITH SUBSTRATE**

CROSS-REFERENCE TO RELATED APPLICATION(S)

5 This application is a continuation-in-part of U.S. patent application number 09/928,124, filed August 10, 2001 and of U.S. patent application number 09/928,163, filed August 10, 2001. This application claims further priority to U.S. provisional patent application number 60/381,320, filed on May 16, 2002, which is incorporated by reference in its entirety.

10 **BACKGROUND OF THE INVENTION**

 The present invention is directed to devices that regulate the flow of electric current and their fabrication methods. More specifically, the present invention is directed to Schottky-barrier source and/or drain transistors.

 An electric current flow regulating device such as semiconductor device
15 100 (for example a transistor), seen in prior art FIG. 1, may include a silicon substrate 110, with an impurity doped source 120 and impurity doped drain 130. Source 120 and drain 130 are separated by a channel region 140. Atop the channel region 140 is an insulating layer 150. Insulating layer 150 typically consists of silicon dioxide, which has a dielectric constant of 3.9. A gate
20 electrode 160, made from electrically conductive material, is located on top of the insulating layer 150.

 When a voltage V_G is applied to the gate electrode 160, current flows between the source 120 and drain 130 through the channel region 140. This current is referred to as the drive current, or I_D . For digital applications, a voltage

V_G can be applied to the gate electrode 160, to turn the semiconductor device 100 "on." In this state, the semiconductor device will have a relatively large drive current, ideally limited only by the resistance of the channel region 140. A different voltage V_G can be applied to the gate electrode 160 to turn the

5 semiconductor device 100 "off." In this state, the ideal leakage current is zero. However, in practical applications, the drive current in the "on" state is not ideal because of parasitic impedances associated with other parts of the semiconductor device 100. For example, the source and drain regions have a finite impedance, resulting in a parasitic impedance which adds to the resistance of the channel

10 region. Also, in practical applications, there is a certain finite amount of leakage current when the semiconductor device is "off."

In prior art current regulating devices, the drive current is linearly proportional to the dielectric constant K of the insulating layer 150, and linearly inversely proportional to the thickness T_{ins} of the insulating layer 150. The drive

15 current I_D is approximated by the relationship:

$$I_D \sim K/T_{ins}$$

where K is the dielectric constant of the insulating layer and T_{ins} is the thickness of the insulating layer.

One consideration in the design of current regulating devices is reducing

20 the amount of power required to achieve a desired drive current. One way to reduce power consumption is by using a metal source and drain and a simple, uniformly implanted channel dopant profile, as described in copending U.S. Patent Applications 09/465,357, filed on December 16, 1999, entitled "METHOD

OF MANUFACTURING A SHORT-CHANNEL FET WITH SCHOTTKY BARRIER SOURCE AND DRAIN CONTACTS,” and 09/777,536, filed on February 6, 2001, entitled “MOSFET DEVICE AND MANUFACTURING METHOD,” the contents of which are hereby incorporated by reference.

5 Another consideration in the design of current regulating devices is the manufacturability. One way to improve the manufacturability of current regulating devices having gate insulators with high dielectric constant materials is to form the source and drain electrodes using a low temperature process such as that used for formation of Schottky or Schottky-like source and drain electrodes,
10 as described in U.S. Provisional Patent Application 60/381,320, filed on May 16, 2002, entitled “LOW TEMPERATURE SOURCE AND DRAIN FORMATION PROCESS STEPS FOR THE MANUFACTURE OF MOSFET DEVICES,” the contents of which are hereby incorporated by reference.

 There is a need in the art for a device for regulating the flow of electric
15 current, which exhibits an improved drive current in the “on” state. There is a further need in the art for a method of manufacturing such a device at reduced temperatures.

BRIEF SUMMARY OF THE INVENTION

 By using the invention disclosed herein the drive current characteristics
20 can be improved, resulting in a non-linear relationship between the drive current I_D and both the dielectric constant (K) of the insulating layer and the thickness of the insulating layer T_{ins} . The resulting relationship results in current regulating devices that are more sensitive to variations in K and T_{ins} compared to the prior

art. Furthermore, by using the invention disclosed herein, the manufacturability of new gate insulator materials is improved substantially.

In one aspect, the invention provides a method for manufacturing a device for regulating the flow of electrical current. The method includes the steps of

5 providing for a semiconductor substrate; providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0; providing for a gate electrode in contact with at least a portion of the insulating layer; and providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the

10 gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate. In one aspect, the device for regulating the flow of electrical current may be a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. In another aspect, the dielectric constant may be greater than 7.6 or greater than

15 15.

In another aspect, the source and drain electrodes may be formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide. In another aspect, the source and drain electrodes may be formed from a member of the group consisting of the rare earth silicides. In

20 another aspect, the insulating layer may be formed from a member of the group consisting of the metal oxides. In another aspect, the Schottky contact or Schottky-like region may be at least in areas adjacent to the channel. In another aspect, an entire interface between at least one of the source and the drain

electrodes and the semiconductor substrate may form a Schottky contact or Schottky-like region with the semiconductor substrate. In another aspect, the channel region may be doped.

In another aspect, the invention provides a method for manufacturing a device for regulating the flow of electrical current. The method includes the steps of providing for a semiconductor substrate; providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0; providing for a gate electrode located in contact with at least a portion of the insulating layer; exposing the semiconductor substrate on one or more areas proximal to the gate electrode; providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and a drain electrode are formed on the semiconductor substrate. In one aspect, the device for regulating the flow of electrical current may be a MOSFET device. In another aspect, the dielectric constant may be greater than 7.6 or greater than 15.

In another aspect, the gate electrode may be provided by the steps of depositing a thin conducting film on the insulating layer; patterning and etching the conducting film to form a gate electrode; and forming one or more thin insulating layers on one or more sidewalls of the gate electrode. In another aspect, the method may include the step of removing metal not reacted during the reacting process. In another aspect, the reacting may include thermal annealing. In another aspect, the source and drain electrodes may be formed from a member

of the group consisting of: platinum silicide, palladium silicide and iridium silicide. In another aspect, the source and drain electrodes may be formed from a member of the group consisting of the rare earth silicides. In another aspect, the insulating layer may be formed from a member of the group consisting of metal
5 oxides. In another aspect, the Schottky contact or Schottky-like region may be formed at least in areas adjacent to the channel. In another aspect, an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate may form a Schottky contact or Schottky-like region with the semiconductor substrate. In another aspect, dopants may be introduced
10 into the channel region.

In another aspect, the invention provides a device for regulating the flow of electrical current. The device includes a semiconductor substrate, a gate electrode, an electrically insulating layer located between the gate electrode and the semiconductor substrate, the insulating layer having a dielectric constant
15 greater than 4.0, and a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contactor Schottky-like region with the semiconductor substrate. In one aspect, the device for regulating the flow of electrical current may be a Metal Oxide Semiconductor
20 Field Effect Transistor (MOSFET) device. In another aspect, the dielectric constant may be greater than 7.6 or greater than 15.

In another aspect, the source and drain electrodes may be formed from a member of the group consisting of: platinum silicide, palladium silicide and

iridium silicide. In another aspect, the source and drain electrodes may be formed from a member of the group consisting of the rare earth silicides. In another aspect, the insulating layer may be formed from a member of the metal oxides. In another aspect, the Schottky contact or Schottky-like region may be at least in areas adjacent to the channel. In another aspect, an entire interface between at least one of the source and the drain electrodes and the semiconductor substrate may form a Schottky contact or Schottky-like region with the semiconductor substrate. In another aspect, the channel region may be doped.

Aspects of the invention can include one or more of the following advantages. Conventional field effect transistors (FET) and other current regulating devices require a higher voltage than those fabricated in accordance with the invention to produce a similar drive current from source to drain. In an optimized conventional FET or current regulating device, the drive current varies generally linearly with the ratio of the insulating layer's dielectric constant to its thickness. One of the advantages of the invention is the unexpected result of the drive current being more sensitive to dielectric constant K than to T_{ins} , implying larger drive current I_D for larger K and constant K/T_{ins} ratio. These results are achieved by coupling a Schottky or Schottky-like source and/or drain with an insulating layer made of a high dielectric constant material. Lower voltage is required to produce high source to drain currents which results in lower power consumption for microelectronics utilizing this architecture.

Furthermore, the well-known benefit of achieving less gate leakage current (between gate and source/drain electrodes) by using larger K and constant

K/T_{ins} ratio, will still be observed in the present invention. For conventionally architected devices this particular benefit is the sole reason for using materials for the gate insulator having larger dielectric constants K than that of silicon dioxide, which has a dielectric constant of 3.9. These materials are denoted as “high K ”
5 materials. No other significant benefit is expected or observed. By using Schottky or Schottky-like source/drain devices in combination with a larger K , an unexpected and dramatic improvement in drive current I_d is achieved in addition to the reduction in gate leakage current.

Although there is a strong motivation for the industry to adopt new high K
10 gate insulator materials due to the problem of gate leakage current, there are technical obstacles that make production of high K gate insulators challenging. One of the most important problems is the degradation of the high K gate insulator materials during high temperature processing required for the formation of the impurity doped source and drain regions. This degradation is caused by
15 reactions with neighboring materials such as the silicon in the channel region or the gate electrode. The processing steps for the formation of the Schottky or Schottky-like source/drain regions occur at much lower temperatures such as 400 °C as compared to 1000 °C required for impurity doped source and drain formation. As a result of the significantly lower temperature processing steps for
20 the formation of the Schottky or Schottky-like source/drain regions, the high K materials do not react substantially with the neighboring materials. Therefore, another benefit of using Schottky or Schottky-like source/drain devices in

combination with high K gate insulator materials is the improved manufacturability of high K gate insulators.

While multiple embodiments are disclosed, still other embodiments of the present invention will become apparent to those skilled in the art from the following detailed description, which shows and describes illustrative
5 embodiments of the invention. As will be realized, the invention is capable of modifications in various obvious aspects, all without departing from the spirit and scope of the present invention. Accordingly, the drawings and detailed description are to be regarded as illustrative in nature and not restrictive.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a cross-section of a prior art semiconductor transistor.

FIG. 2 is a cross-section of a semiconductor substrate with Schottky contact source and drain combined with a non-silicon dioxide insulating layer between the gate and channel region.

15 FIG. 3a is a cross-section of a semiconductor device with Schottky contact source and drain combined with a non-silicon dioxide insulating layer between the gate and channel region. This is the device structure used for numerical simulations.

FIG. 3b is a logarithmic plot showing the simulated relationship between
20 the drive current I_D and gate voltage V_G for various K values, with the ratio K/T_{ins} held constant.

FIG. 3c is a linear plot with the same data as FIG. 3b.

FIG. 4a is a cross-section of a semiconductor device with Schottky contact source and drain combined with a non-silicon dioxide insulating layer between the gate and channel region. This is the device structure used for a second set of numerical simulations.

5 FIG. 4b is a logarithmic plot showing the simulated relationship between the drive current I_D and gate voltage V_G for various K values, with the ratio K/T_{ins} held constant.

FIG. 4c is a linear plot with the same data as FIG. 4b.

FIG. 5 is a cross-section of semiconductor substrate after ion
10 implantation.

FIG. 6 is a cross-section of semiconductor substrate after insulating layer growth and gate patterning.

FIG. 7 is a cross-section of semiconductor substrate after growth of an oxide layer on the sidewalls.

15 FIG. 8 is a cross-section of semiconductor substrate after creation of a metal silicide source and drain.

FIG. 9 is a cross-section of the semiconductor device resulting from the process steps outlined in FIG. 10.

FIG. 10 is a flow chart outlining the process flow for the fabrication of a
20 device for regulating flow of electric current in accordance with the invention.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring to FIG. 2, semiconductor device 200 includes a substrate 210 in which a source 220 and drain 230 are formed. Substrate 210 may be composed of silicon or may be a silicon-on-insulator (SOI) substrate. Source 220 and/or drain 230 may be composed partially or fully of a rare earth silicide. Source 220 and/or drain 230 may also be composed partially or fully of platinum silicide, palladium silicide or iridium silicide. Because the source and drain are composed in part of a metal, they form Schottky contacts or Schottky-like regions 270, 275 with the substrate 210, where a "Schottky contact" is defined by the contact between a metal and a semiconductor, and a "Schottky-like region" is a region formed by the close proximity of a semiconductor and a metal. The Schottky contacts or Schottky-like regions 270, 275 can be formed by forming the source and/or drain from a metal silicide. The Schottky contacts or Schottky-like regions 270, 275 are in an area adjacent to a channel region 240 formed between the source 220 and drain 230. The entire interface between either or both of the source 220 and the drain 230 may form a Schottky contact or Schottky-like region 270, 275 with the substrate 210. The channel region 240 may be impurity doped where the doping may be conventional non-uniform doping or may be uniform doping as described in copending U.S. Patent Application No. 09/465,357 and U.S. Patent Application No. 09/777,536.

An insulating layer 250 is formed on top of the channel region 240 and may be formed on part or all of the source 220 and drain 230. The insulating layer 250 is composed of a material with a dielectric constant greater than that of

silicon dioxide; e.g. a dielectric constant greater than 3.9. For example, insulating layer 250 may be composed of a metal oxide such as TaO₂ with a dielectric constant of approximately 25, TiO₂ with a dielectric constant of approximately 50-60, HfO₂ with a dielectric constant of approximately 15-20, or ZrO₂ with a dielectric constant of approximately 15-20. The insulating layer 250 may consist of a dielectric with a modest K value (e.g., 5-10), such as nitride/oxide or oxy-nitride stack; a medium K value (e.g., 10-20), such as unary oxides Ta₂O₃, TiO₂, ZrO₂, HfO₂, Y₂O₃, La₂O₃, Gd₂O₃, Sc₂O₃ or silicates ZrSiO₄, HfSiO₄, LaSiO₄, or TiSiO₄; or a high K value (e.g., greater than 20) such as amorphous LaAlO₃, ZrTiO₄, SnTiO₄, or SrZrO₄, or single crystals LaAl₃O₄, BaZrO₃, Y₂O₃, La₂O₃. Optionally, to improve manufacturability issues associated with transition metals, the insulating layer 250 may consist of more than one layer. The insulating layer 250 may be formed with a "bi-layer" approach and may consist of more than one type of dielectric, e.g., TiO₂ on top of Si₃N₄. A gate electrode 260 is positioned on top of the insulating layer 250. A thin insulating layer 225 surrounds the gate electrode 260.

By forming a semiconductor device with (1) a source 220 or drain 230 forming a Schottky contact or Schottky-like region 270, 275 with the substrate 110; and (2) an insulating layer 250 with a relatively high dielectric constant, one is able to achieve a larger drive current I_D for larger K, but constant K/T_{ins}.

Referring to FIGs. 3a-c, full two dimensional electrostatic simulations were performed on the MOSFET device 305 structure of FIG. 3a, for various

insulating layer 309 thicknesses T_{ins} 307 and insulator dielectric constants K . The simulation assumes the following:

- 1) P type MOS semiconductor device 305, metallic source 301/drain 303 at 300K.
- 5 2) Metallic source 301/drain 303 with radius of curvature R 311 of 10nm.
- 3) Channel length L 313 of 25nm, drain voltage V_D of 1.2V.
- 4) No significant charge, either fixed or mobile, in the silicon substrate 315.
- 10 5) The drain current, I_D , is limited solely by the emission process at the source 301 end of the semiconductor device 305.
- 6) The current density versus electric field (J vs. E) characteristic for the emission process at the source 301 is modeled after a platinum silicide-to-silicon Schottky contact. The Schottky barrier height is assumed to be 0.187eV,
- 15 hole effective mass in the silicon is 0.66 m_0 , fermi level is at 5.4eV, and temperature is 300K. For a given electric field strength at a particular point on the source 301, the current density is calculated via a complete, no approximations solution to the Schrödinger equation assuming a 1-D sharp triangular barrier. The effects of quantum tunneling and reflection have been
- 20 fully included. Because the total current density is integrated across the density of states, currents due to field emission, thermal emission, and thermally assisted field emission have been accounted for. The J vs. E relationship has been calibrated to experimental data for the pure thermal emission case ($E=0$).

These assumptions are valid in the real world case of short channel (<25nm) and undoped (or lightly doped) substrates. Although the absolute values of the calculated source 301 emission currents have not been calibrated for $E>0$, they are based on some experimental data and first-principles calculations. For the purposes of the proposed invention, the calculated J vs. E data is sufficient as the primary interest relates to the effect of the insulating layer 309 thickness (T_{ins}) 307 and dielectric constant (K) on source 301 emission current. Relative changes in source 301 emission current with T_{ins} and K are more relevant, in this case, than the absolute value of the current. Nevertheless, calculated values of both leakage and drive currents I_D are in good agreement with the measured data of actual transistors.

Simulations were run with a constant K/T_{ins} ratio of 0.156. The results are shown in FIGs. 3b-c. Starting with FIG. 3c, working upwards, curve 350 shows the relationship between the gate voltage V_G and the drive current I_D in a semiconductor device with an insulating layer dielectric constant of 3.9 ($T_{ins} = 25$ Å). Curves 360, 370 and 380 show the ratio of V_G and I_D in semiconductor devices with sources 220 and drains 230 that form a Schottky contact or Schottky-like region 270, 275 with the substrate and insulating dielectric constants of 10 ($T_{ins} = 64.1$ Å), 25 ($T_{ins} = 160.3$ Å), and 50 ($T_{ins} = 320.5$ Å), respectively. Referring to FIG. 3b, curve 355 shows the logarithmic relationship between the gate voltage V_G and the drive current I_D in a semiconductor device with an insulating layer dielectric constant of 3.9 ($T_{ins} = 25$ Å). Curves 365, 375 and 385 show the logarithmic ratio of V_G and I_D in semiconductor devices with

sources 220 and drains 230 that form a Schottky contact or Schottky-like region 270, 275 with the substrate and insulating dielectric constants of 10 ($T_{\text{ins}} = 64.1 \text{ \AA}$), 25 ($T_{\text{ins}} = 160.3 \text{ \AA}$), and 50 ($T_{\text{ins}} = 320.5 \text{ \AA}$), respectively. It is expected that similar results would be achieved regardless of the radius of curvature R 311, channel length 313 and drain voltage V_D . Drive current to leakage current ratios are 35, 38, 53 and 86 for the curves 350/355, 360/365, 370/375 and 380/385, respectively. Leakage currents can be lowered by at least a factor of 10, without sacrificing drive currents, by the addition of the appropriate dopants in the substrate (to control bulk-punchthrough currents) or by a reduction in operating temperature. Thus, by using a source 301 or drain 303 that forms a Schottky contact or Schottky-like region with the substrate, and by increasing K while maintaining a constant K/T_{ins} ratio, the drive current I_D increases significantly (from a little over $300 \mu\text{A}/\mu\text{m}$ for a V_G of 1.2V to approximately $1300 \mu\text{A}/\mu\text{m}$). Thus, for a desired drive current, a device would need a significantly lower voltage to operate than that required by the prior art. Because power consumption varies with the square of the voltage, the invention provides for significantly lower power usage.

To verify that changing the radius of curvature R 311 does not change the observed dramatic improvement in I_D , full 2-D electrostatic simulations were repeated on a slightly different device geometry. Referring to FIGs. 4a-c, the semiconductor device 405 structure of figure 4a was simulated for two insulating layer 409 thicknesses T_{ins} 407 and insulator dielectric constants K, such that the

ratio K/T_{ins} was constant. The simulation assumptions are the same as noted above, with the exception of the device geometry:

- 1) The channel length L_{413} is 27 nm
- 2) The width 402 and height 404 of the source and drain are 100 nm
5 and 30 nm respectively.
- 3) The width 412 and height 413 of the gate are 67 nm and 108 nm respectively.
- 4) The radius of curvature R_g_{414} of the gate was 10 nm for all simulations.
- 10 5) The radius of curvature R_{411} of the source and drain electrodes was either 1 nm or 10 nm.

Simulations were run with a constant K/T_{ins} ratio of 0.205. The results are shown in FIGs. 4b-c. Starting with FIG. 4c, curves 451 and 461 show the relationship between the gate voltage V_g and the drive current I_D in a
15 semiconductor device having a radius of curvature R_{411} of 10 nm with an insulating layer dielectric constant of 3.9 ($T_{\text{ins}} = 25 \text{ \AA}$) and 50 ($T_{\text{ins}} = 244 \text{ \AA}$), respectively. Continuing with FIG. 4c, curves 471 and 481 show the relationship between the gate voltage V_g and the drive current I_D in a semiconductor device having a radius of curvature R_{411} of 1 nm with an insulating layer dielectric
20 constant of 3.9 ($T_{\text{ins}} = 25 \text{ \AA}$) and 50 ($T_{\text{ins}} = 244 \text{ \AA}$), respectively. Referring to FIG. 4b, curves 455 and 465 show the logarithmic relationship between the gate voltage V_g and the drive current I_D in a semiconductor device having a radius of curvature R_{411} of 10 nm with an insulating layer dielectric constant of 3.9 (T_{ins}

= 25 Å) and 50 ($T_{\text{ins}} = 244$ Å), respectively. Continuing with FIG. 4b, curves 475 and 485 show the relationship between the gate voltage V_g and the drive current I_D in a semiconductor device having a radius of curvature R 411 of 1 nm with an insulating layer dielectric constant of 3.9 ($T_{\text{ins}} = 25$ Å) and 50 ($T_{\text{ins}} = 244$ Å), respectively. FIGs. 4b-c show that by using a source 401 or drain 403 that forms a Schottky contact or Schottky-like region with the substrate, and by increasing K while maintaining a constant K/T_{ins} ratio, the drive current I_D increases significantly (from approximately 650 mA/mm for a V_g of 1.2V to approximately 1700 mA/mm) for a device having a radius of curvature R 411 of 10 nm. The ratio of drive currents for the $K=50$ to the $K=3.9$ case is $1700/650 = 2.6$. Likewise, for the device having a radius of curvature R 411 of 1 nm, the drive current I_D increases significantly (from approximately 570 mA/mm for a V_g of 1.2V to approximately 2340 mA/mm). In this case, the ratio of drive current for the $K=50$ to the $K=3.9$ case is $2340/570 = 4.1$. These results indicate that the relative improvement in drive current I_D grows larger for smaller radii of curvature R 411. Further, these results indicate that increasing the ratio K/T_{ins} will lead to larger improvements in drive current I_D as compared to the case of constant K/T_{ins} . A conventional impurity doped source and drain device would have approximately the same drive current I_D for both $K=3.9$ and $K=50$ cases having constant K/T_{ins} .

Cross sectional scanning electron micrographs of the source and drain corner regions indicate that the radius of curvature R 411 for the top corner of the source 421 and top corner of the drain 422 electrode adjacent to the channel

region are closer to 1 nm, rather than 10 nm. The simulation predictions of FIGs. 4a-c indicate that for a desired drive current, by using a source 401 or drain 403 that forms a Schottky contact or Schottky-like region with the substrate, and by using high K dielectric gate insulator materials, the device would need a

5 significantly lower voltage to operate than that required by the prior art. Because power consumption varies with the square of the voltage, the invention provides for significantly lower power usage.

The device for regulating flow of electric current described above, for example a planar P-type or N-type MOSFET, may be formed using the process

10 shown in FIGs. 5-9 and described in FIG. 10. (Note that the planar P-type or N-type MOSFET need not be planar in the horizontal direction, but may assume any planar orientation.) Referring to FIGs. 5 and 10, a thin screen oxide 323 is grown on silicon substrate 310, the substrate 310 having a means for electrically isolating transistors from one another (905). The thin screen oxide, optionally a

15 thickness of 200 Å, acts as the implant mask for the channel region 340 doping. The appropriate channel dopant species (for example Arsenic and Indium for P-type and N-type devices respectively) is then ion-implanted through the screen oxide 323 to a pre-determined depth in the silicon (for example, 1000 Å) (910).

Referring to FIGs. 6 and 10, the screen oxide layer 323 of FIG. 5 is

20 removed with hydro-fluoric acid (915), and the thin insulating layer 450 is either grown or deposited at least on a portion of the channel region 340 (920). This insulating layer may consist of TiO_2 , TaO_2 , or any other appropriate compound with a high dielectric constant as discussed above. Immediately following the

insulating layer growth or deposition, an in-situ heavily doped silicon film is deposited (930). This silicon film will eventually make up the gate electrode. The silicon film may be doped with phosphorus for an N-type device or boron for a P-type device. The gate electrode is then patterned with a lithographic
5 technique and silicon etch that is highly selective to the insulating layer 450 (935).

Referring to FIGs. 7 and 10, a thin oxide, optionally approximately 100 Å in thickness, is formed on the top surface and sidewalls of the gate electrode (940). Some of the oxide layers then are removed by anisotropic etch to expose
10 the silicon on the horizontal surfaces 510, while preserving it on the vertical surfaces (945). This step serves both to create a gate sidewall oxide 525 and to electrically activate the dopants in the gate electrode and channel region 340 of the device.

Referring to FIGs. 8 and 10, a metal is deposited as a blanket film,
15 optionally approximately 400 Å thick, on all surfaces (950). The particular metal deposited will depend on whether the device is N-type or P-type. Platinum may be used for the P-type device while erbium may be used for an N-type device. The semiconductor device 600 is then annealed for a specified time at a specified temperature, for example, 45 minutes at 400 °C (955). This temperature is much
20 less the temperature typically required to form impurity doped source and drains, which is usually greater than 800 °C. Where the metal is in direct contact with the silicon, the annealing process causes a chemical reaction that converts the

metal to a metal silicide 606. The metal 616 not in contact with silicon does not react.

Referring to FIGs. 9 and 10, the unreacted metal 616 is removed with a wet chemical etch (960). For example, if the deposited metal was platinum or erbium, aqua regia or HNO₃, respectively, may be used to remove it. The silicide electrodes that remain are the source 620 and drain 630. The Schottky device for regulating flow of electric current with a high dielectric constant insulating layer is now complete and ready for electrical contacting to gate electrode 460, source 620, and drain 630 (965). Because the temperature required to form the Schottky or Schottky-like source and drain electrodes in this process is much lower than that required for impurity doped source 620 and drain 630 regions, the high K material used for the gate insulator 450 is much less likely to react with neighboring materials, making this process much more manufacturable than the prior art.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the semiconductor devices illustrated in the claims are by way of example only. It should be understood that the concepts of the invention apply to semiconductor devices with a variety of cross-sections. And, although the invention has been illustrated with respect to planar silicon MOS transistors, it can apply equally well to other devices for regulating the flow of electrical current. For example, devices built on other semiconductor substrates such as gallium arsenide GaAs,

indium phosphide InP, silicon carbide SiC, silicon germanium SiGe, etc. Further, the device is not required to have any particular radius of curvature for the source and drain electrode corners. And, the invention is not limited to any particular ratio(s) of K/T_{ins} . Accordingly, other embodiments are within the scope of the

5 following claims.

Although the present invention has been described with reference to preferred embodiments, persons skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention.

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CLAIMS

We claim:

1. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
 - 5 providing for a semiconductor substrate;
 - providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;
 - providing for a gate electrode in contact with at least a portion of the
 - 10 insulating layer; and
 - providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 15 2. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
3. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 20 4. The method of claim 1, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
5. The method of claim 1, wherein the insulating layer is formed from an oxy-nitride stack.

6. The method of claim 1, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
7. The method of claim 1, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
8. The method of claim 1, wherein dopants are introduced into the channel region.
9. The method of claim 1, wherein the insulating layer includes more than one layer.
10. The method of claim 2 or 3, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
11. The method of claim 2 or 3, wherein the insulating layer is formed from an oxy-nitride stack.
12. The method of claim 10, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel, and wherein dopants are introduced into the channel region.
13. The method of claim 11, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel, and wherein dopants are introduced into the channel region.
14. The method of claim 2 or 3, wherein providing a source electrode and a drain electrode in contact with the semiconductor substrate is performed at a processing temperature of less than about 800 °C.

15. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- providing for a semiconductor substrate;
 - providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;
 - providing for a gate electrode in contact with at least a portion of the insulating layer; and
 - providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.
16. The method of claim 15, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
17. The method of claim 15, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
18. The method of claim 15, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
19. The method of claim 15, wherein the insulating layer is formed from an oxy-nitride stack.
20. The method of claim 15, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

21. The method of claim 15, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 5 22. The method of claim 15, wherein the insulating layer includes more than one layer.
23. The method of claim 15, wherein dopants are introduced into the channel region.
24. A method for manufacture of a device for regulating the flow of
10 electrical current, the method comprising:
providing for a semiconductor substrate;
providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;
15 providing for a gate electrode in contact with at least a portion of the insulating layer; and
providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or
20 Schottky-like region with the semiconductor substrate.
25. The method of claim 24, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

26. The method of claim 24, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

27. The method of claim 24, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

5 28. The method of claim 24, wherein the insulating layer is formed from an oxy-nitride stack.

29. The method of claim 24, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

30. The method of claim 24, wherein an entire interface between at
10 least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

31. The method of claim 24, wherein dopants are introduced into the channel region.

15 32. The method of claim 24, wherein the insulating layer includes more than one layer.

33. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

20 providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

5 providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

10 34. The method of claim 33, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode; and

forming one or more thin insulating layers on one or more sidewalls of the

15 gate electrode.

35. The method of claim 33, further comprising removing metal not reacted during the reacting process.

36. The method of claim 33, wherein the reacting comprises thermal annealing.

20 37. The method of claim 33, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

38. The method of claim 33, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

39. The method of claim 33, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

5 40. The method of claim 33, wherein the insulating layer is formed from an oxy-nitride stack.

41. The method of claim 33, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

42. The method of claim 33, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

10

43. The method of claim 33, wherein dopants are introduced into the channel region.

15 44. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;

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providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

5 reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

45. The method of claim 44, wherein the gate electrode is provided by:

10 depositing a thin conducting film on the insulating layer;
 patterning and etching the conducting film to form a gate electrode; and
 forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

46. The method of claim 44, further comprising removing metal not
15 reacted during the reacting process.

47. The method of claim 44, wherein the reacting comprises thermal annealing.

48. The method of claim 44, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide,
20 palladium silicide and iridium silicide.

49. The method of claim 44, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

50. The method of claim 44, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

51. The method of claim 44, wherein the insulating layer is formed from an oxy-nitride stack.

5 52. The method of claim 44, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

53. The method of claim 44, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the
10 semiconductor substrate.

54. The method of claim 44, wherein dopants are introduced into the channel region.

55. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:

15 providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;

providing for a gate electrode located in contact with at least a portion of
20 the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

56. The method of claim 55, wherein the gate electrode is provided by:

depositing a thin conducting film on the insulating layer;
patterning and etching the conducting film to form a gate electrode; and
10 forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

57. The method of claim 55, further comprising removing metal not reacted during the reacting process.

58. The method of claim 55, wherein the reacting comprises thermal
15 annealing.

59. The method of claim 55, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

60. The method of claim 55, wherein the source and drain electrodes
20 are formed from a member of the group consisting of the rare earth silicides.

61. The method of claim 55, wherein the insulating layer is formed from a member of the group consisting of metal oxides.

62. The method of claim 55, wherein the insulating layer is formed from an oxy-nitride stack.

63. The method of claim 55, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.

5 64. The method of claim 55, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

65. The method of claim 55, wherein dopants are introduced into the
10 channel region.

66. A device for regulating the flow of electrical current, the device comprising:

a semiconductor substrate;

a gate electrode;

15 an electrically insulating layer located between the gate electrode and the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0; and

a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source
20 electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

67. The device of claim 66, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

68. The device of claim 66, wherein the source and drain electrodes
5 are formed from a member of the group consisting of the rare earth silicides.

69. The device of claim 66, wherein the insulating layer is formed from a member of the group consisting of the metal oxides.

70. The device of claim 66, wherein the insulating layer is formed from an oxy-nitride stack.

10 71. The device of claim 66, wherein the Schottky contact or Schottky-like region is at least in areas adjacent to the channel.

72. The device of claim 66, wherein an entire interface between at least one of the source and the drain electrodes and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor
15 substrate.

73. The device of claim 66, wherein the channel region is doped.

74. The device of claim 66, wherein the insulating layer includes more than one layer.

75. The device of claim 67 or 68, wherein the insulating layer is
20 formed from a member of the group consisting of metal oxides.

76. The device of claim 67 or 68, wherein the insulating layer is formed from an oxy-nitride stack.

77. The device of claim 75, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel, and wherein the channel region is doped.

78. The device of claim 76, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel, and wherein the channel region is doped.

79. A device for regulating the flow of electrical current, the device comprising:

a semiconductor substrate;

10 a gate electrode;

an electrically insulating layer located between the gate electrode and the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6; and

a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

80. The device of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.

81. The device of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

82. The device of claim 79, wherein the insulating layer is formed from a member of the group consisting of the metal oxides.

83. The device of claim 79, wherein the insulating layer is formed from an oxy-nitride stack.

5 84. The device of claim 79, wherein the Schottky contact or Schottky-like region is at least in areas adjacent to the channel.

85. The device of claim 79, wherein an entire interface between at least one of the source and the drain electrodes and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor
10 substrate.

86. The device of claim 79, wherein the channel region is doped.

87. The device of claim 79, wherein the insulating layer includes more than one layer.

88. A device for regulating the flow of electrical current, the device
15 comprising:

 a semiconductor substrate;

 a gate electrode;

 an electrically insulating layer located between the gate electrode and the semiconductor substrate, the insulating layer having a dielectric constant greater
20 than 15; and

 a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source

electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

89. The device of claim 88, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide,
5 palladium silicide and iridium silicide.

90. The device of claim 88, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.

91. The device of claim 88, wherein the insulating layer is formed from a member of the group consisting of the metal oxides.

10 92. The device of claim 88, wherein the insulating layer is formed from an oxy-nitride stack.

93. The device of claim 88, wherein the Schottky contact or Schottky-like region is at least in areas adjacent to the channel.

94. The device of claim 88, wherein an entire interface between at
15 least one of the source and the drain electrodes and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.

95. The device of claim 88, wherein the channel region is doped.

96. The device of claim 88, wherein the insulating layer includes more
20 than one layer.

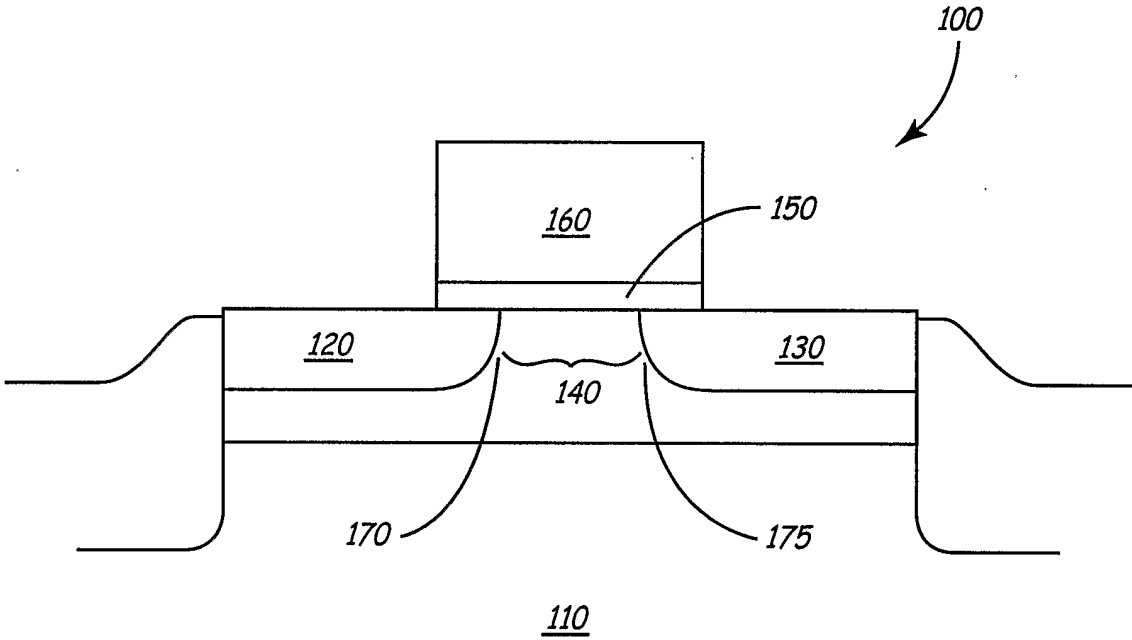


FIG. 1
(PRIOR ART)

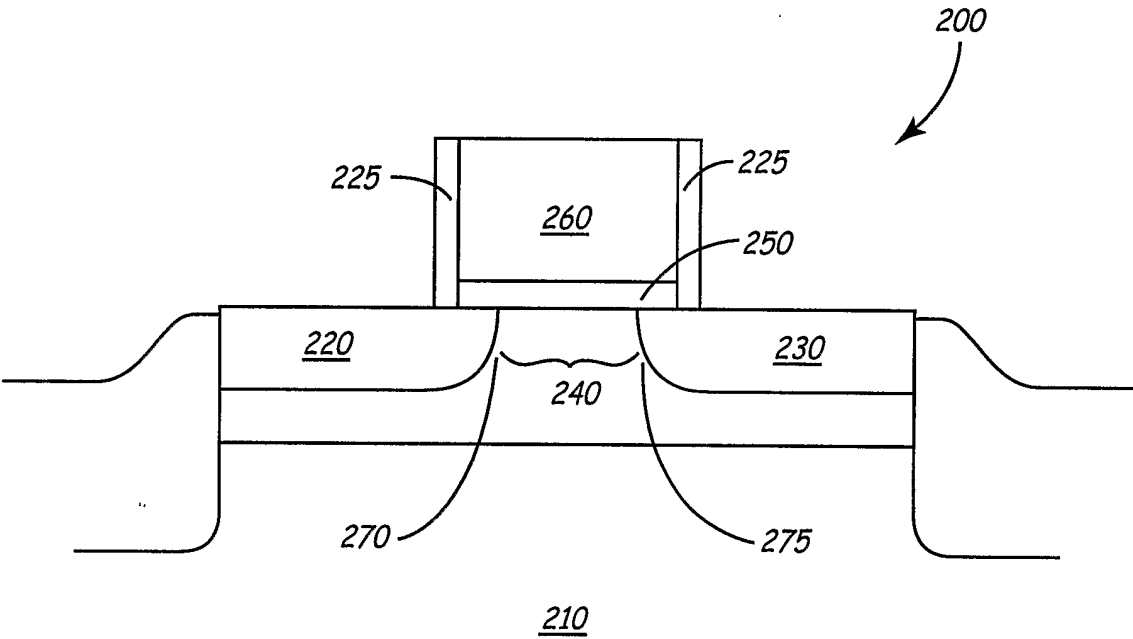


FIG. 2

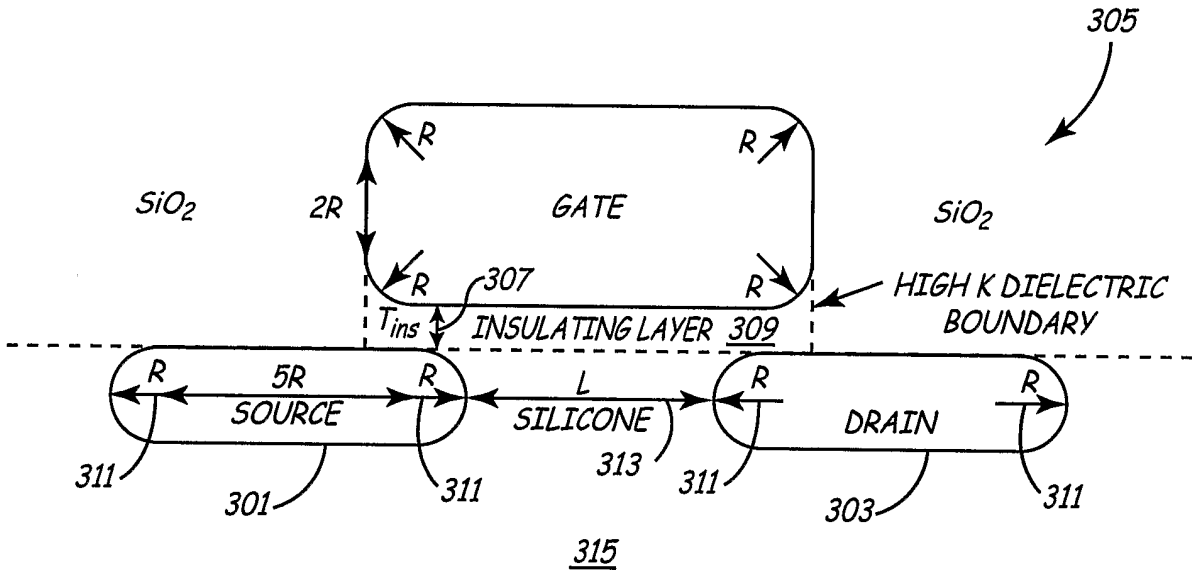


FIG. 3a

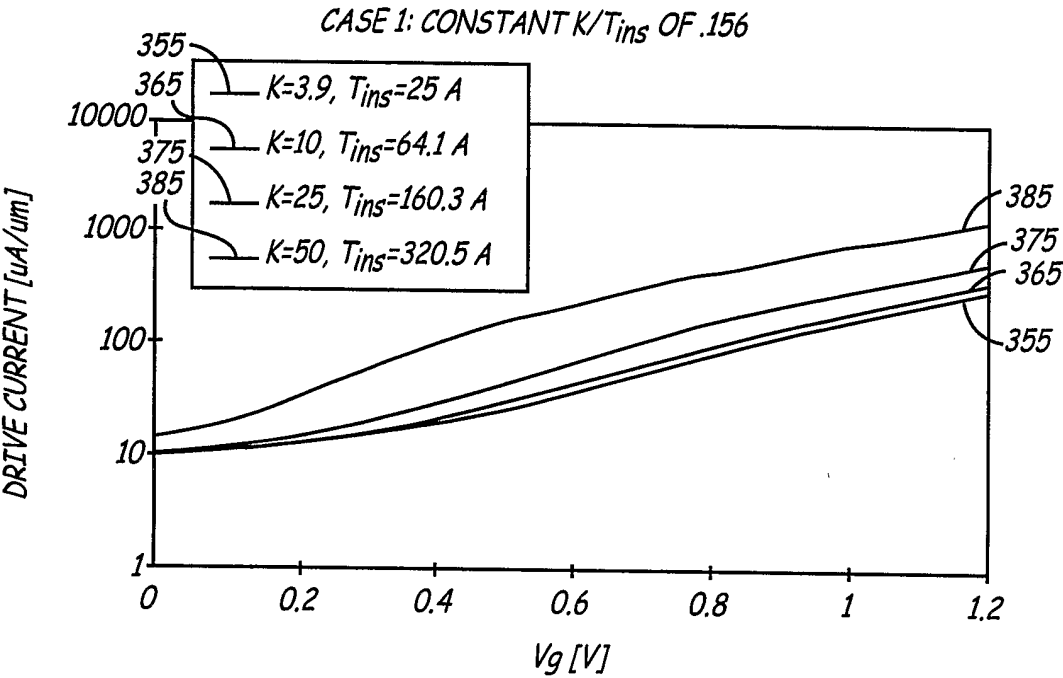


FIG. 3b

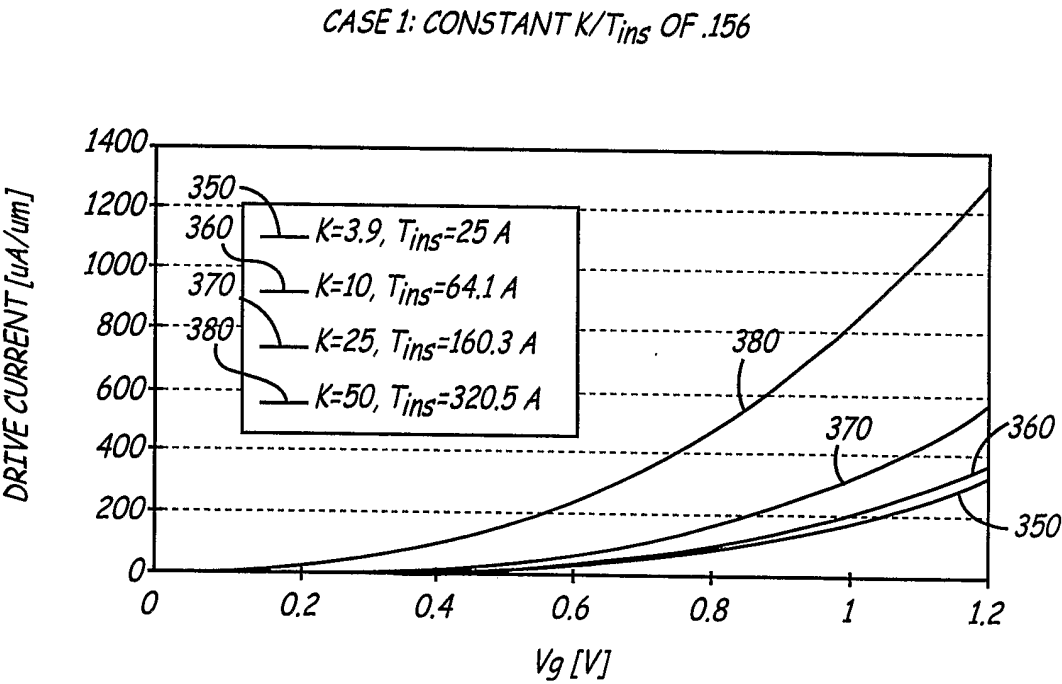


FIG. 3c

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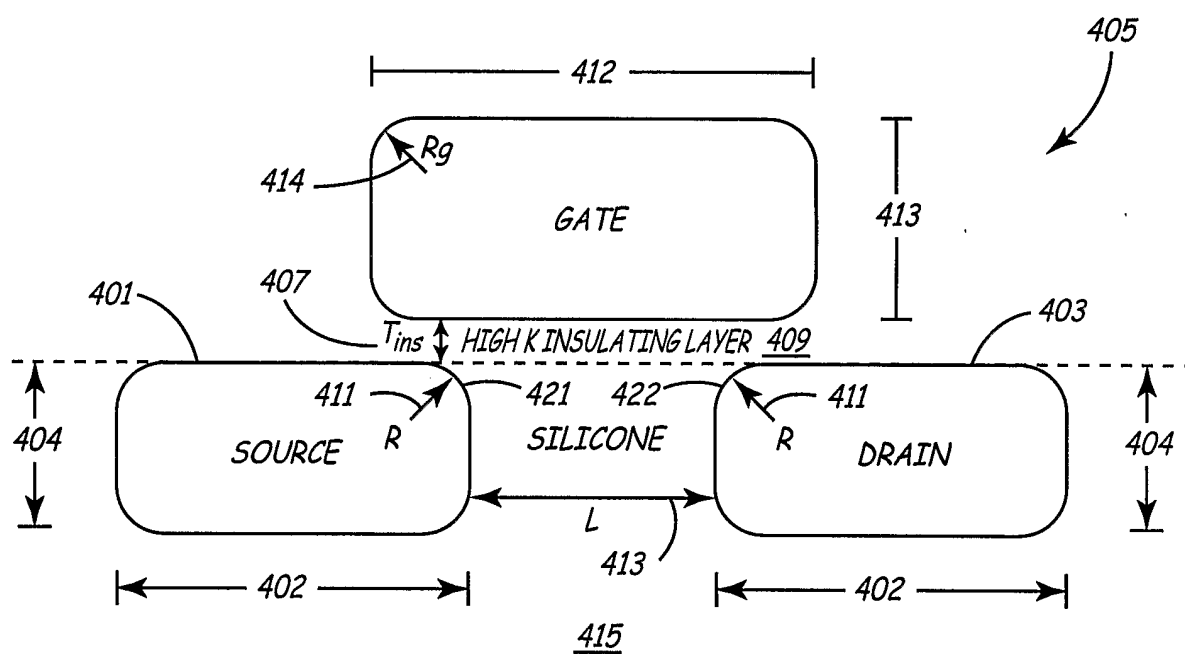


FIG. 4a

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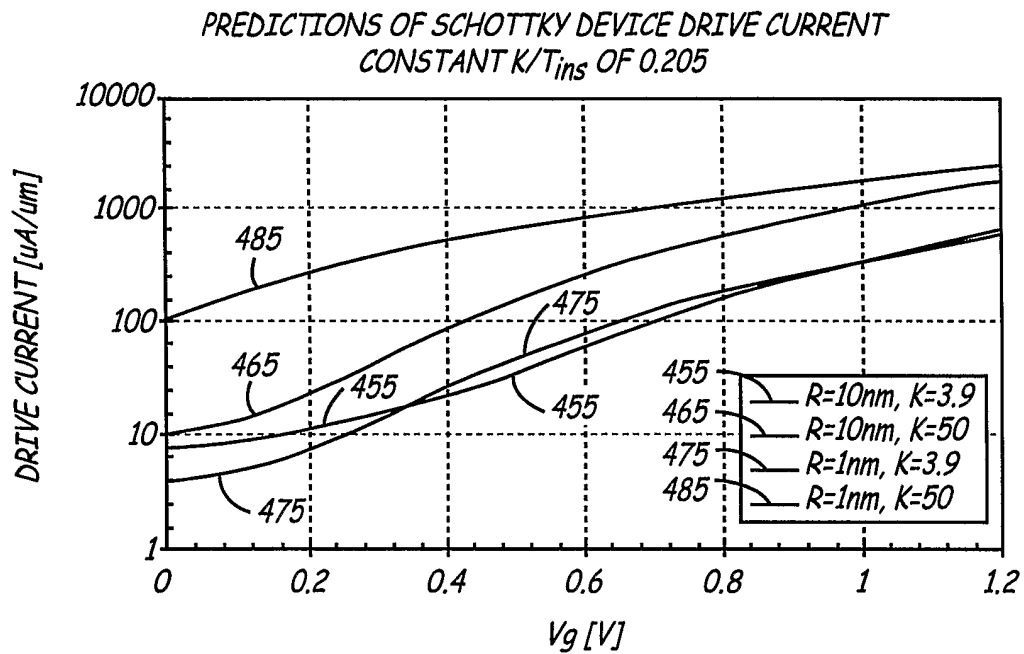


FIG. 4b

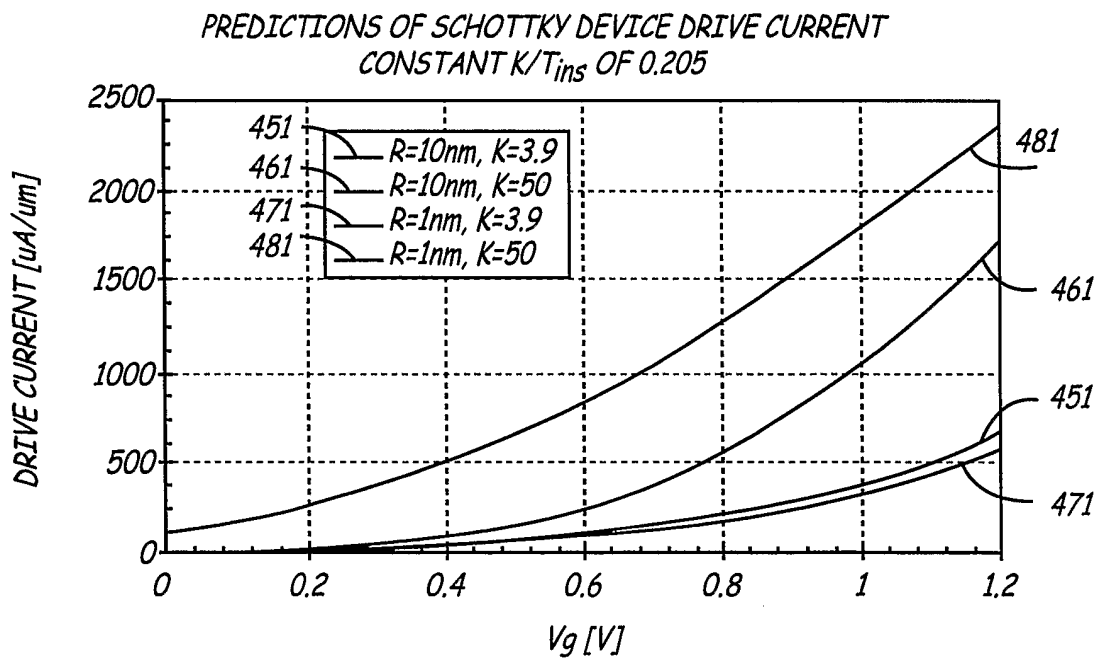


FIG. 4c

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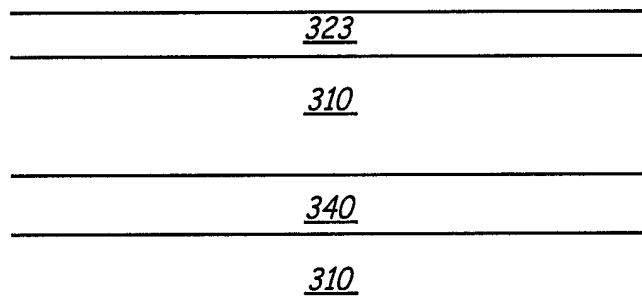


FIG. 5

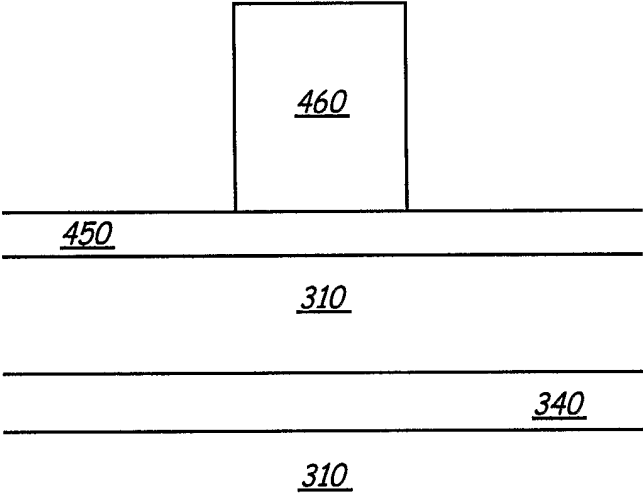


FIG. 6

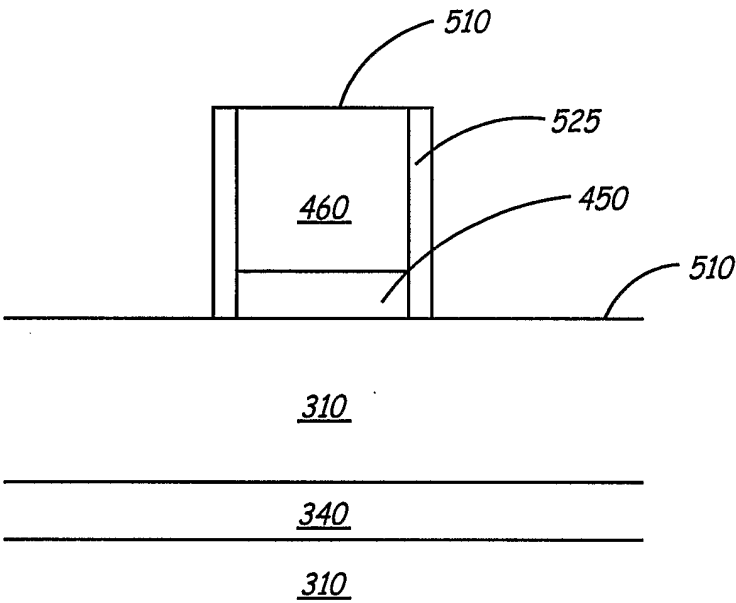


FIG. 7

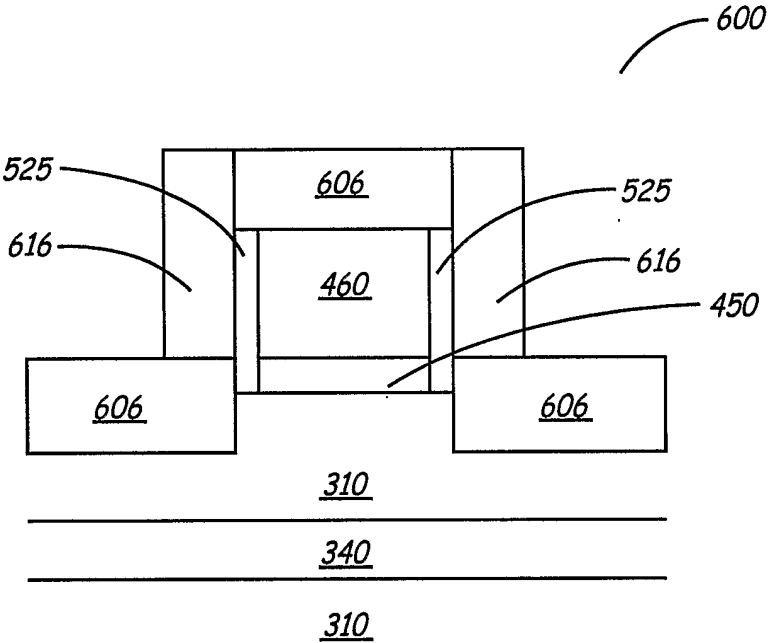


FIG. 8

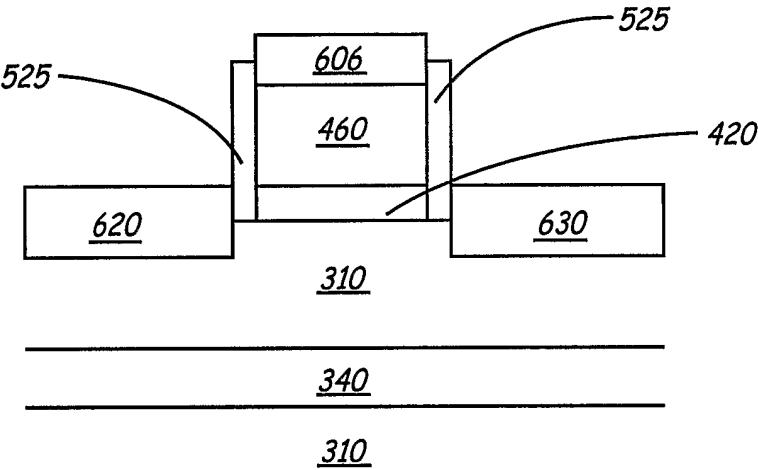
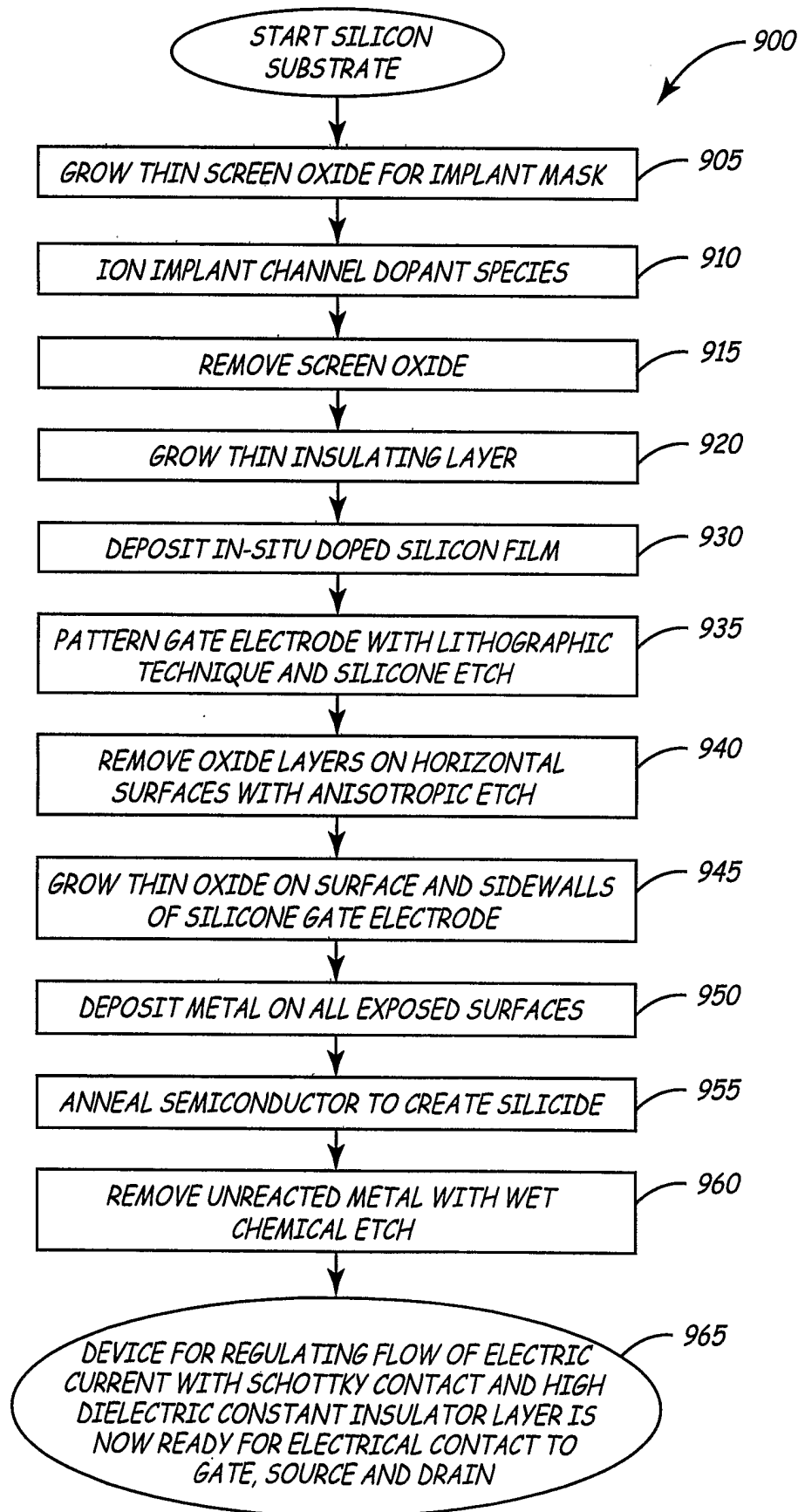


FIG. 9

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**FIG. 10**

INTERNATIONAL SEARCH REPORT

Inter | Application No
PCT/US 02/25289

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 361 225 A (OZAWA TAKANORI) 1 November 1994 (1994-11-01) column 9, line 5 - line 53; figure 3G ---	1-96
A	WO 01 45157 A (SPINNAKER SEMICONDUCTOR INC) 21 June 2001 (2001-06-21) page 19, line 5-8; claims 10-12,28 ---	2,3
A	US 5 040 034 A (MURAKAMI YOSHINORI ET AL) 13 August 1991 (1991-08-13) figure 21C -----	1-96



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *Z* document member of the same patent family

Date of the actual completion of the international search

10 January 2003

Date of mailing of the international search report

21/01/2003

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Juh1, A

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter Application No

PCT/US 02/25289

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