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(54) **Title**: THIN FILM TRANSISTOR

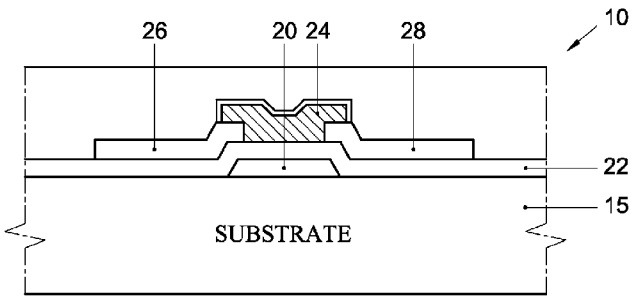

Fig. 1 (e)

(57) **Abstract**: In one aspect, the present invention relates to a method of manufacturing of a thin film transistor, comprising: forming an oxide semiconductor channel layer of thickness less than 20nm on a substrate; forming source and drain electrodes at opposing sides of the channel layer; and applying an oxidizing agent to the channel layer. In another aspect, the present invention relates to a method of manufacturing a thin film transistor, comprising: forming an oxide semiconductor channel layer on a substrate; forming source and drain electrodes at opposing sides of the channel layer; applying an oxidizing agent to the channel layer; and forming a self-assembled monolayer (SAM) on the channel layer, wherein the SAM comprises an unreactive chain having an end group that is non-oxidizing with respect to the oxidizing semiconductor.

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Thin Film Transistor

The present invention relates to the manufacture of a thin film transistor having an oxide semiconductor channel layer.

For (metal) oxide thin film transistors, an important parameter is the threshold voltage i.e. the gate voltage at which the device switches on. The threshold voltage is sensitive to defects in the oxide semiconductor channel layer caused by under oxidation during manufacture. Such under oxidation (deficiency of oxygen) in the oxide semiconductor channel layer leaves an excess of free positive charge carriers in the channel layer which results in a current leakage in the off-state and a high negative threshold voltage.

One conventional approach for suppressing this effect is to perform, during manufacture, an annealing step at high temperature (typically 400°C) under an oxygen atmosphere (in air) to allow oxygen to diffuse and neutralize the excess positive charge carriers in the channel layer. However, this approach suffers from the drawback that it requires a minimum temperature of approximately to 250°C to function which is not compatible with low cost

substrates, for example, foils made from PEN (polyethylene naphthalate) or PET (polyethylene terephthalate).

US7767505 discloses the manufacture of a thin film transistor having an oxide semiconductor channel layer in which, during manufacture, a nitrous oxide plasma process is used to supply oxygen ions to the surface of the channel layer, and then an annealing step activates the supplied oxygen ions so as to form oxygen bonds within the channel layer, thereby reducing the excess of free positive charge carriers. This approach is disadvantageous as it requires using expensive plasma equipment and hazardous nitrous oxide gas.

US2009/0140243 discloses the manufacture of a thin film transistor having an oxide semiconductor channel layer in which, during manufacture, the carrier density of a surface of the channel layer is controlled by an oxidization treatment using an oxidizing agent. Three methods are disclosed. According to a first method, a liquid oxidizing agent is placed in contact with the surface of the channel layer. The liquid oxidizing agent may include permanganate, perchlorate and peroxide compounds. According to a second method, the oxidization treatment includes forming a SAM (self-assembled monolayer), that includes an oxidizing agent, on the surface of the channel layer. The SAM may be a phosphonic acid group containing SAM. According to a third method, as an alternative the first or second methods, a passivation layer formed of an organic insulating material and including a functional group that is capable of

oxidizing the channel layer is used. It may be necessary to anneal the passivation layer.

According to a first aspect, the present invention may provide a method of manufacturing of a thin film transistor, comprising:

forming an oxide semiconductor channel layer of thickness less than 20nm on a substrate;

forming source and drain electrodes at opposing sides of the channel layer; and

applying an oxidizing agent to the channel layer.

A typical prior art thin film transistor has a channel layer with a thickness of 50-60nm (nanometers). The applicant has found that by limiting the thickness of the channel layer, a thin film transistor manufactured according to the first aspect of the present invention may have a much reduced negative or even positive threshold voltage. Although the mechanism is not presently understood, the effect becomes appreciable when the channel layer has a thickness of less than around 20nm and progressively more pronounced as the channel layer becomes thinner as is illustrated in Figures 3(a-c). Preferably, the thickness of the channel layer is less than around 15nm, more preferably less than around 12nm, and most preferably less than around 10nm.

The channel layer may be originally deposited at the required thickness. Alternatively, the channel layer may be deposited at a thickness greater than required and etched down to the required thickness.

In a preferred embodiment, the oxidizing agent is liquid. A preferred oxidizing agent is hydrogen peroxide. The hydrogen peroxide is preferably in neutral form i.e. not in combination with an acid or a catalyst. The applying step may comprise submerging the channel layer in a preferably 25-35%, less preferably 15-45%, hydrogen peroxide solution in water. The applying step results in a semiconductor layer having a predetermined threshold voltage.

Preferably, the method further comprises forming a self-assembled monolayer (SAM) on the channel layer, wherein the SAM comprises an unreactive chain having an end group that is non-oxidizing with respect to the oxide semiconductor. The end group may be an acid group which undergoes an acid-oxide reaction with the surface of the channel layer. By applying the SAM, the transistor is stabilized, whereby the threshold voltage may be maintained at the predetermined level.

In a preferred embodiment, the SAM comprises an unreactive alkane octadecyl chain having a phosphonic acid end group. Alternatively, carboxylic, sulphonic, or silane may be used as the end group. Linear or branched alkane molecules

or aromatic compounds may be used as part of the unreactive chain. None of these molecules have oxidizing properties with respect to the oxide semiconductor.

According to a second aspect, the present invention may provide a thin film transistor, comprising:

an oxide semiconductor channel layer on a substrate;

source and drain electrodes at opposing sides of the channel layer;

wherein the channel layer has a thickness of less than 20nm.

According to a third aspect, the present invention may provide a method of manufacturing a thin film transistor, comprising:

forming an oxide semiconductor channel layer on a substrate;

forming source and drain electrodes at opposing sides of the channel layer;

applying an oxidizing agent to the channel layer; and

forming a self-assembled monolayer (SAM) on the channel layer, wherein the SAM comprises an unreactive chain having an end group that is non-oxidizing with respect to the oxide semiconductor.

Using a SAM comprising an unreactive chain having an end group that is non-oxidizing with respect to the oxide semiconductor to stabilize the already-oxidized channel layer is not taught by the prior art. In particular, the above-mentioned US2009/0140243 discloses using a SAM that specifically includes a functional group to perform the oxidization of the channel layer.

The end group may be an acid group which undergoes an acid-oxide reaction with the surface of the channel layer. In a preferred embodiment, the SAM comprises an unreactive aliphatic chain, such as an alkane octadecyl chain, having a phosphonic acid end group. Alternatively, carboxylic, sulphonic, or silane may be used as the end group. Linear or branched alkane molecules or aromatic compounds may be used as the unreactive chain. None of these molecules have oxidizing properties with respect to the oxide semiconductor. Phosphoric acid and monochlorosilanes based SAMs create significant defects during formation and therefore benefit most from an initial oxidation step to create an over-oxidation/buffer of oxygen at the surface.

Preferably, the SAM does not react with itself, whereby a polymerization reaction at the surface does not occur. For this reason, phosphoric acid is a

preferred choice as it is unlikely to polymerize at normal atmospheric conditions. And for this same reason, trifunctional silanes are unsuitable.

The third aspect of the present invention may be used independently of the first aspect of the present invention.

According to a fourth aspect, the present invention may provide a thin film transistor, comprising:

an oxide semiconductor channel layer on a substrate;

source and drain electrodes at opposing sides of the channel layer; and

a self-assembled monolayer (SAM) on the channel layer, wherein the SAM comprises an unreactive chain having an end group that is non-oxidizing with respect to the oxide semiconductor. .

Throughout the specification, "or" is used in a non mutually exclusive sense.

Exemplary embodiments of the present invention are hereinafter described with reference to the accompanying drawings, in which:

Figures 1(a-e) illustrate the manufacture of a thin film transistor (TFT) of the bottom contact type;

Figure 2 shows a SAM in accordance with a preferred embodiment of the invention; and

Figures 3(a-c) illustrate how in a TFT the threshold voltage is shifted through oxidization treatment by hydrogen peroxide for various thicknesses of channel layer.

Throughout this description the same or corresponding parts have been given the same or corresponding reference numerals.

Figures 1(a-e) illustrate the manufacture of a thin film transistor (TFT) of the bottom contact type, which is generally designated 10.

Referring to Figure 1(a), a gate 20 is formed on a substrate 15. The substrate 15 preferably comprises a PEN or PET foil. A gate insulating layer 22 that covers the gate 20 is formed on the substrate 15. The gate insulating layer 22 may be a SiOx (e.g., SiO2) or SiNx layer. After forming the gate insulating layer 22, a wet washing process is optionally performed to eliminate (or remove) impurities on a top surface of the gate insulating layer 22. During the wet washing process, at least one of isopropyl (IPA), deionized water, acetone

or the like may be used as a washing solution.

Referring to Figure 1(b), a conductive material layer (not shown) is formed on the gate insulating layer 22. The conductive material layer may be patterned to form a source electrode 26 and a drain electrode 28. A general dry, or wet method may be used for patterning the source electrode 26 and the drain electrode 28. In the case of a wet method, an etchant having phosphoric acid, nitric acid, acetic acid or the like as a main (or primary) component may be used. The patterned conductive material layer, or the electrodes 26, 28, obtained may be made of one of a molybdenum (Mo) single metal layer, a multi-metal layer including a molybdenum (Mo) layer, a metal layer including titanium (Ti), and a metal layer including chromium (Cr). The conductive material layer, or the electrodes 26,28, may be formed of a conductive material including at least one of Mo, Ti, Pt, Cu, Al, W, MoW, AlNd, Ni, Ag, Au, IZO, ITO and combinations thereof. The conductive material layer or the electrodes 26,28 may be formed of a silicide including at least one of Mo, Ti, Pt, Cu, Al, W, MoW, AlNd, Ni, Ag, Au, IZO, ITO and combinations thereof. The conductive material, or the silicide, used to form the conductive material layer, or the electrodes 26,28 may include at least one of Cu, Mo, Al and combinations thereof. The conductive material layer may be formed using a physical vapour deposition (PVD) method.

Referring to Figure 1(c), a channel layer 24 corresponding to the gate 20 is

formed on the gate insulating layer 22 between the source electrode 26 and the drain electrode 28. The channel layer 24 may be formed using a PVD method including general sputtering and evaporation methods.

In a preferred embodiment, the channel layers 24 is made of a ZnO based material, for example, amorphous Ga-In-Zn-O (GIZO). GIZO may be formed of a(In2O3).b(Ga2O3).c(ZnO) where a, b and c are actual numbers respectively satisfying the following expression: a>=0, b>=0 and c>0. GIZO may be formed of a(In2O3).b(Ga2O3).c(ZnO) where a, b and c are numbers respectively satisfying the following expressions: a>=1, b>=1, and 0<c<=1. In other embodiments, other semiconductor material systems may be used.

The channel layer 24 is formed with a thickness of 10nm or less. In less preferred embodiments, the channel layer 24 is formed with a thickness of from 10nm to 20nm.

Since the channel layer 24 is particularly sensitive to defects caused by under oxidation during its manufacture, an oxidation treatment using an oxidizing agent is performed as illustrated in Figure 1(d). In a preferred embodiment, that treatment comprises submersing the wafer in 30% hydrogen peroxide solution for 10-15 minutes at 70°C. The hydrogen peroxide solution is in normal form i.e. an acid or a catalyst is not present. This treatment results in

a (slightly) p-doped surface/semiconductor having a predetermined threshold voltage.

In other embodiments, other oxidizing agents may be used. But hydrogen peroxide is preferred due to its availability and low toxicity.

Referring to Figure 1(e), in order to stabilize the oxidized surface, whereby the predetermined threshold voltage is maintained, a self-assembled monolayer (SAM) 30 is formed on the channel layer. In a preferred embodiment, an octadecyl phosphonic acid SAM is used. As shown in Figure 2, the SAM 30 more generally comprises an unreactive chain 30a having an end group 30b that is non-oxidizing with respect to the oxide semiconductor material (but could be oxidizing with respect to other materials); for example, the end group 30b may be an acid group which undergoes an acid-oxide reaction with the oxidized surface of the channel layer 24 and in so doing becomes grafted thereto. Other SAMs may be used.

Referring still to Figure 1(e), a passivation layer 32 is optionally formed on the SAM 30, the source and drain electrodes 26,28 and the insulating layer 22 by using a known deposition method. The passivation layer 24 may be formed of SiN_x or SiO_x.

Figure 3(a-c) show how the threshold voltage of transistors manufactured according to the above-described preferred embodiment varies according to the thickness of the channel layer. As can be seen from Figure 3(a), a transistor having a channel layer with a 10nm thickness shifts from a switch-on of -2V to +7V. As can be seen from Figure 3(b), a transistor having a channel layer with a 15nm thickness shifts from a switch-on of -5 V to approximately 0V. For transistors having a channel layer with a thickness greater than 20nm, the shift in switch-on voltage is much less pronounced. For example, as can be seen in Figure 3(c), at 25nm only a slight shift from -12V to -10V can be achieved.

In other embodiments, the transistor may have a different architecture, for example, it may be a top contact type transistor.

The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole in the light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that aspects of the present invention may consist of any such individual feature or combination of features. In view of the foregoing description it will be evident to a person

skilled in the art that various modifications may be made within the scope of the invention.

List of parts

Transistor	10
Substrate	15
Gate	20
Insulating layer	22
Channel layer	24
Source electrode	26
Drain electrode	28
SAM	30
Unreactive chain	30a
Non-oxidizing end group	30b
Passivation layer	32

Claims

1. A method of manufacturing a thin film transistor, comprising:

forming an oxide semiconductor channel layer on a substrate;

forming source and drain electrodes at opposing sides of the channel layer;

applying an oxidizing agent to the channel layer; and

forming a self-assembled monolayer (SAM) on a surface of the channel layer to which the oxidizing agent has been applied, wherein the SAM comprises a chain that is unreactive with respect to the oxide semiconductor having an end group that is non-oxidizing with respect to the oxide semiconductor.

2. A method as in claim 1, wherein the end group is an acid group which undergoes an acid-oxide reaction with the surface of the channel layer.

3. A method as in any preceding claim, wherein an aliphatic chain is the unreactive chain.

4. A method as in any preceding claim, wherein the SAM comprises one of an alkane octadecyl chain, linear alkane molecules, branched alkane molecules, or aromatic compounds as the unreactive chain.

5. A method as in claim 4, wherein the SAM comprises one of a phosphonic, carboxylic, sulphonic or silane acid as the end group.

6. A method of manufacturing of a thin film transistor, comprising:

forming an oxide semiconductor channel layer of thickness less than 20nm on a substrate;

forming source and drain electrodes at opposing sides of the channel layer; and

applying an oxidizing agent to the channel layer.

7. A method as in claim 6, wherein the thickness of the channel layer is less than 15nm, preferably less than 12nm, and most preferably less than 10nm.

8. A method as in claims 6 or 7, wherein the oxidizing agent is liquid hydrogen peroxide in normal form.

9. A method as in any preceding claim, further comprising forming a self-assembled monolayer (SAM) on the channel layer, wherein the SAM comprises an unreactive chain having an end group that is non-oxidizing with respect to the oxide semiconductor.

10. A thin film transistor, comprising:

an oxide semiconductor channel layer on a substrate;

source and drain electrodes at opposing sides of the channel layer;

wherein the channel layer has a thickness of less than 20nm.

11. A thin film transistor, comprising:

an oxide semiconductor channel layer on a substrate;

source and drain electrodes at opposing sides of the channel layer; and

a self-assembled monolayer (SAM) on the channel layer, wherein the SAM comprises a chain that is unreactive with respect to the oxide semiconductor having an end group that is non-oxidizing with respect to the oxide semiconductor.

12. A thin film transistor as in claim 11, wherein the SAM is a phosphoric acid or monochlorosilanes based SAM.

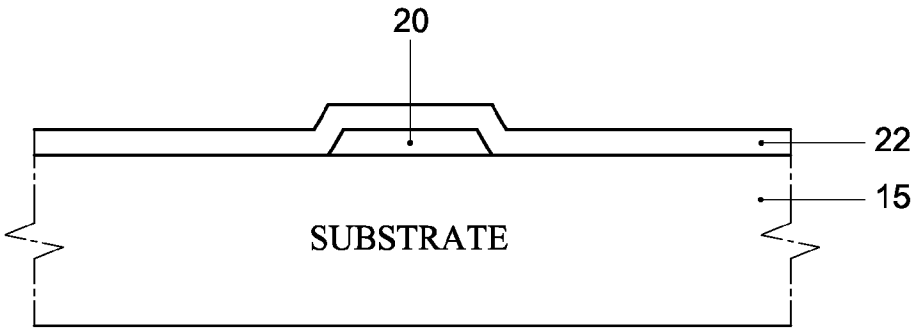

Fig. 1 (a)

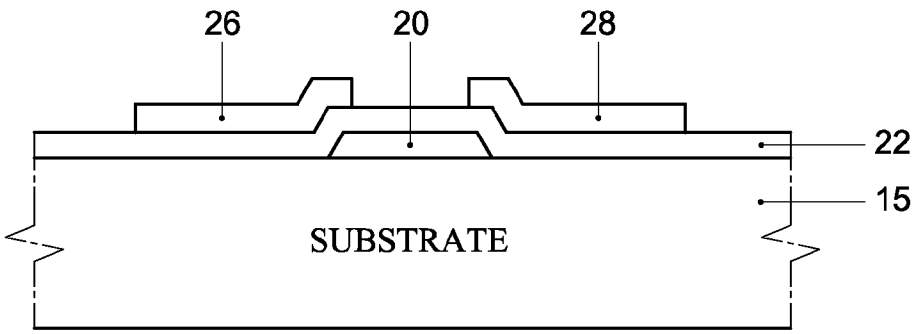

Fig. 1 (b)

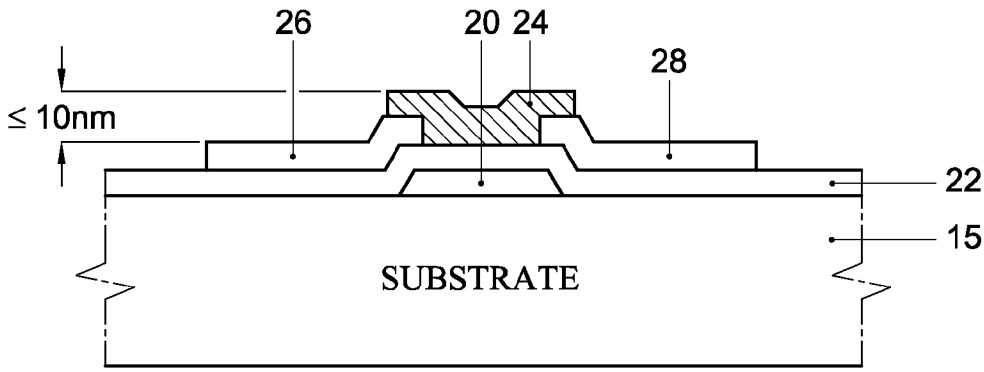

Fig. 1 (c)

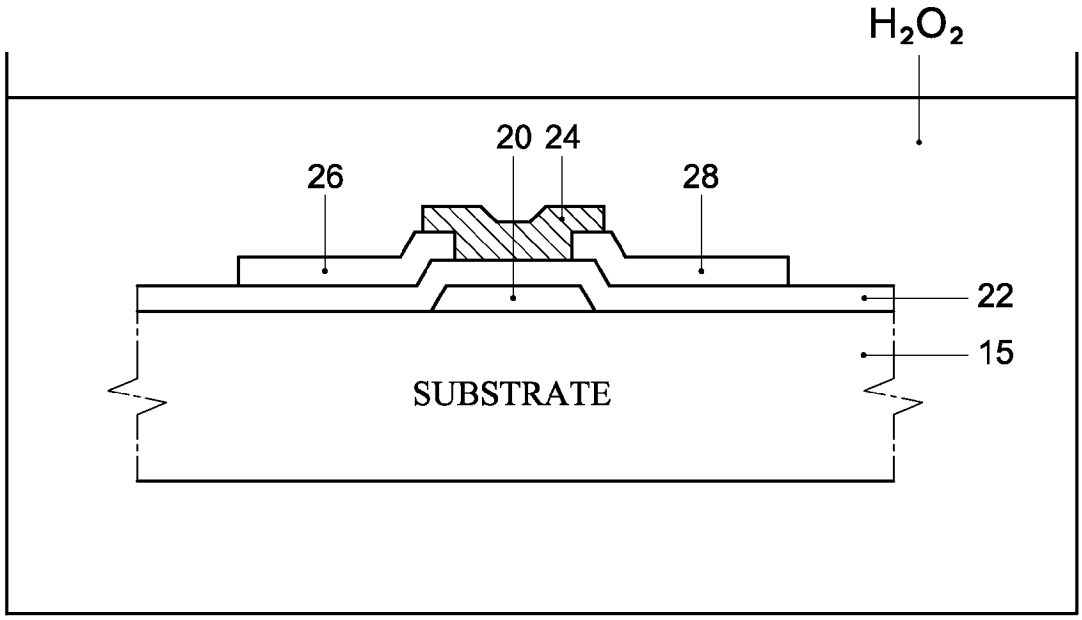

Fig. 1 (d)

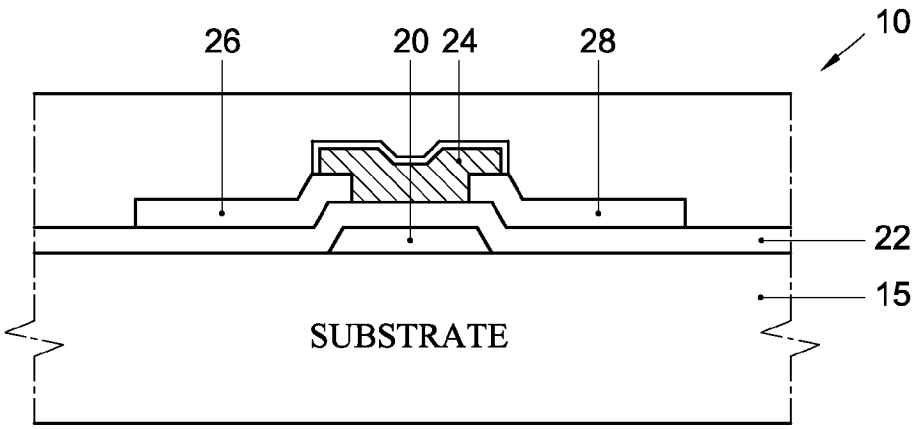

Fig. 1 (e)

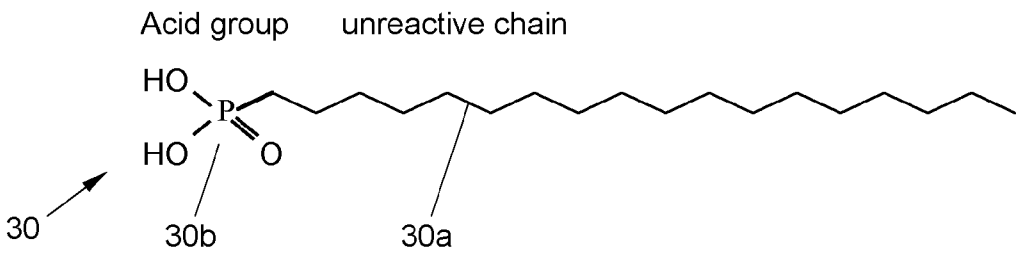
Acid group
unreactive chain
HO
P
HO
O
30
30b
30a

Fig. 2

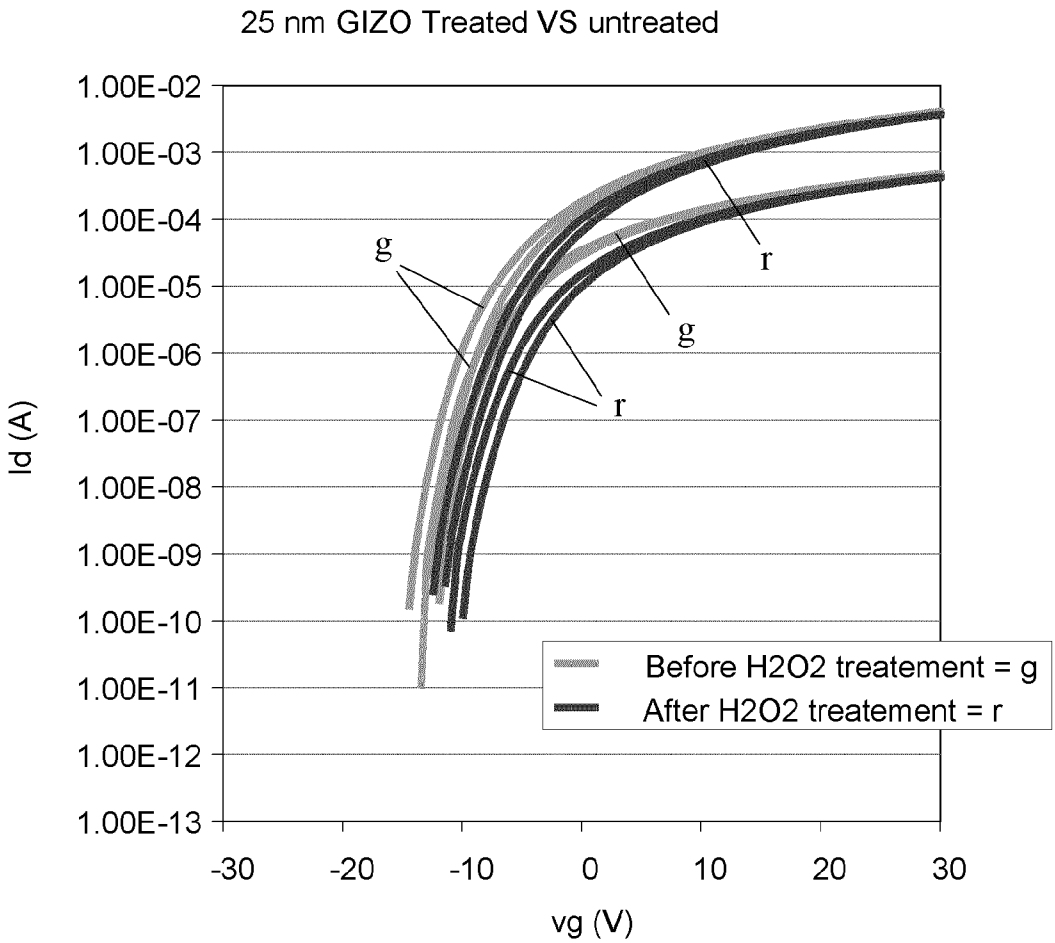
25 nm GIZO Treated VS untreated
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
Id (A)
-30
-20
-10
0
10
20
30
vg (V)
g
r
g
r
Before H2O2 treatement = g
After H2O2 treatement = r

Fig. 3 (a)

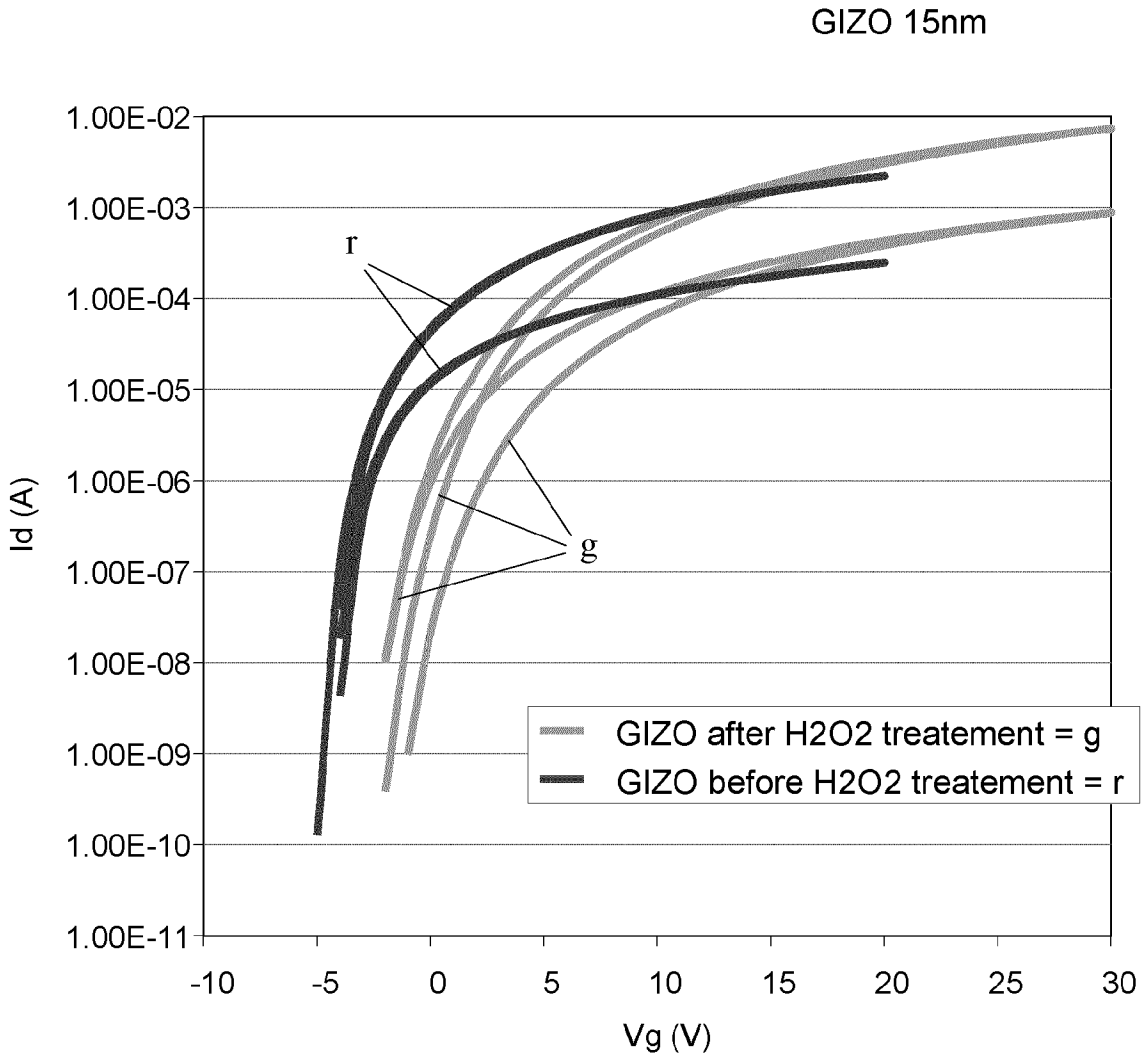
GIZO 15nm
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
Id (A)
r
g
GIZO after H2O2 treatement = g
GIZO before H2O2 treatement = r
-10
-5
0
5
10
15
20
25
30
Vg (V)

Fig. 3 (b)

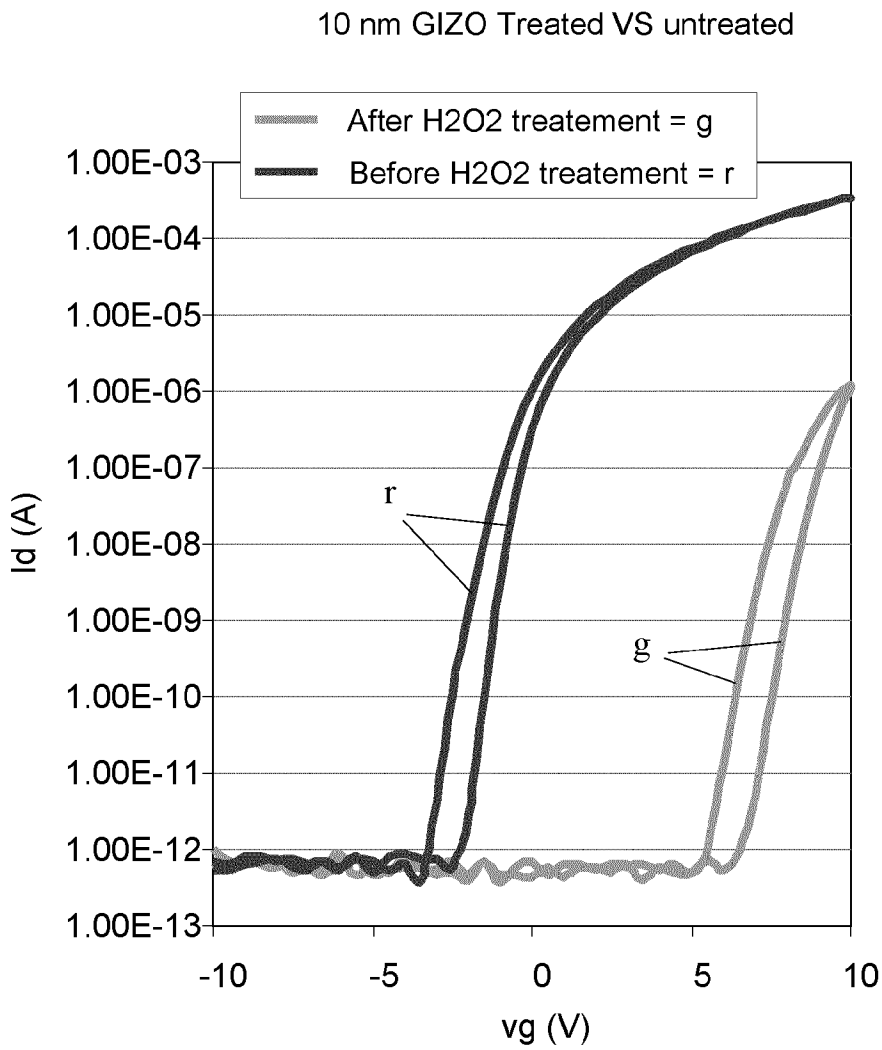
10 nm GIZO Treated VS untreated
After H2O2 treatement = g
Before H2O2 treatement = r
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
Id (A)
r
g
-10
-5
0
5
10
vg (V)

Fig. 3 (c)

INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2012/050411

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/786
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MOUREY D A ET AL: "Passivation of ZnO TFTs", JOURNAL OF THE SOCIETY FOR INFORMATION DISPLAY, SOCIETY FOR INFORMATION DISPLAY, PLAYA DEL REY, CALIF., USA, vol. 18, no. 10, 1 October 2010 (2010-10-01), pages 753-761, XP009151865, ISSN: 0734-1768, DOI: 10.1889/JSID18.10.753	6-8,10
Y	the whole document	1-5,9

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 July 2012	25/07/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann, Niels

INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2012/050411

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	D. H. Cho ET AL: "The effect of self assembled monolayer(SAM) on the back interface of a-IGZO TFT", , 3 May 2011 (2011-05-03), XP055006572, Retrieved from the Internet: URL:http://www.ecsdl.org/getpdf/servlet/GetPDFServlet?filetype=pdf&id=MAECES00110100001600115000000 1&idtype=cvips [retrieved on 2011-09-08]	11,12
Y	the whole document	1-5,9
X	-& DATABASE COMPENDEX [Online] ENGINEERING INFORMATION, INC., NEW YORK, NY, US; 2011, CHO S-H ET AL: "The effect of self assembled monolayer(SAM) on the back interface of a-IGZO TFT", XP002658587, Database accession no. E20113114194062	11,12
Y	abstract	1-5,9

X	US 2009/140243 A1 (KIM TAE-SANG [KR] ET AL) 4 June 2009 (2009-06-04) paragraph [0041] - paragraph [0042] paragraph [0044] paragraph [0056] paragraph [0063]	1-12

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INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2012/050411

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	D. H. CHO ET AL: "Passivation of Bottom-Gate IGZO Thin Film Transistors", JOURNAL OF THE KOREAN PHYSICAL SOCIETY, vol. 54, no. 925, 15 January 2009 (2009-01-15), page 531, XP055006585, ISSN: 0374-4884, DOI: 10.3938/jkps.54.531 the whole document	1-5,9,11
A	KYOUNG-SEOK SON ET AL: "Threshold Voltage Control of Amorphous Gallium Indium Zinc Oxide TFTs by Suppressing Back-Channel Current", ELECTROCHEMICAL AND SOLID-STATE LETTERS, vol. 12, no. 1, 1 January 2009 (2009-01-01), page H26, XP055006586, ISSN: 1099-0062, DOI: 10.1149/1.3020766 the whole document	1-12
A	TSAI CHIA-HUNG ET AL: "Surface modification of ZnO film by hydrogen peroxide solution", JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 104, no. 5, 11 September 2008 (2008-09-11), pages 53521-53521, XP012117391, ISSN: 0021-8979, DOI: 10.1063/1.2976321 the whole document	1,6,8
A	CHEN Y ET AL: "Influence of hydrogen peroxide solution on the properties of ZnO thin films", JOURNAL OF CRYSTAL GROWTH, ELSEVIER, AMSTERDAM, NL, vol. 268, no. 1-2, 15 July 2004 (2004-07-15), pages 71-75, XP004517262, ISSN: 0022-0248, DOI: 10.1016/J.JCRYSGRO.2004.03.069 the whole document	1,6,8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NL2012/050411

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 11, 12

Method of fabricating oxide semiconductor TFT having a SAM comprising an unreactive chain having an end group that is non-oxidizing with respect to the oxide semiconductor

1.1. claims: 6-10

Method of manufacturing oxide semiconductor TFT having a thickness of less than 20 nm

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/NL2012/050411

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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