US 20020003266A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0003266 A1

MANNING (43) Pub. Date: Jan. 10, 2002

(54) APPARATUS IMPROVING LATCHUP IMMUNITY IN A DUAL-POLYSILICON GATE

(76) Inventor: MONTE MANNING, KUNA, ID (US)

Correspondence Address:
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402 (US)

(*) Notice: This is a publication of a continued prosecution application (CPA) filed under 37 CFR 1.53(d).

(21) Appl. No.: 09/126,182

(22) Filed: Jul. 30, 1998

Related U.S. Application Data

(63) Continuation of application No. 08/762,741, filed on Dec. 10, 1996, now Pat. No. 5,801,423.

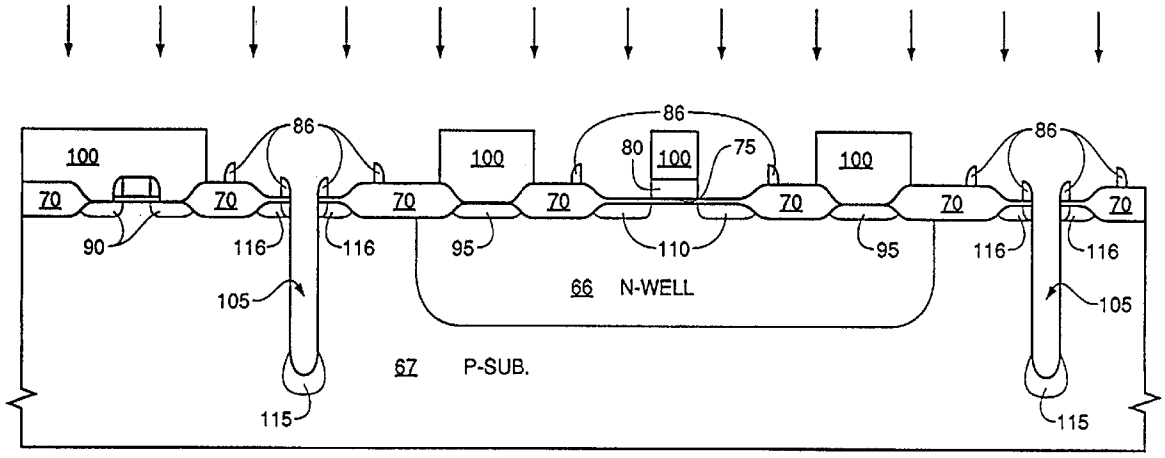
Publication Classification

(51) Int. Cl.[7] H01L 29/00

(52) U.S. Cl. 257/372; 257/374; 257/376; 257/510

(57) ABSTRACT

The invention is a method for creating a portion of an integrated circuit on a semiconductor wafer. The invention comprises doping a substrate to form a doped well region having an opposite conductivity type than the substrate. Separate photomasking steps are used to define N-channel and P-channel metal oxide semiconductor (MOS) transistor gates. A trench is formed near the well without using additional masking steps. The trench improves the latch up immunity of the device. The invention is also the apparatus created by the method and comprises a trench positioned in the substrate to interrupt the conduction of minority carriers between two regions of the substrate. Thus, the invention improves latch up immunity without additional process complexity.



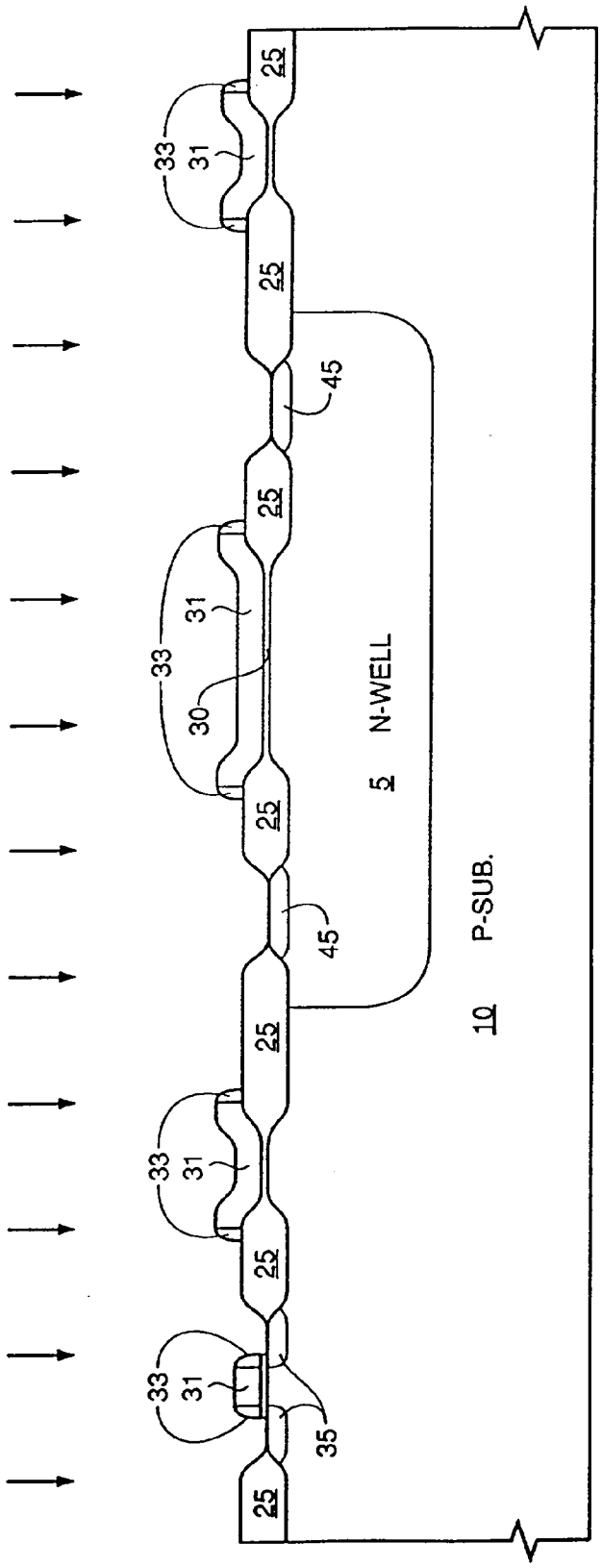


FIG. 1
(RELATED ART)

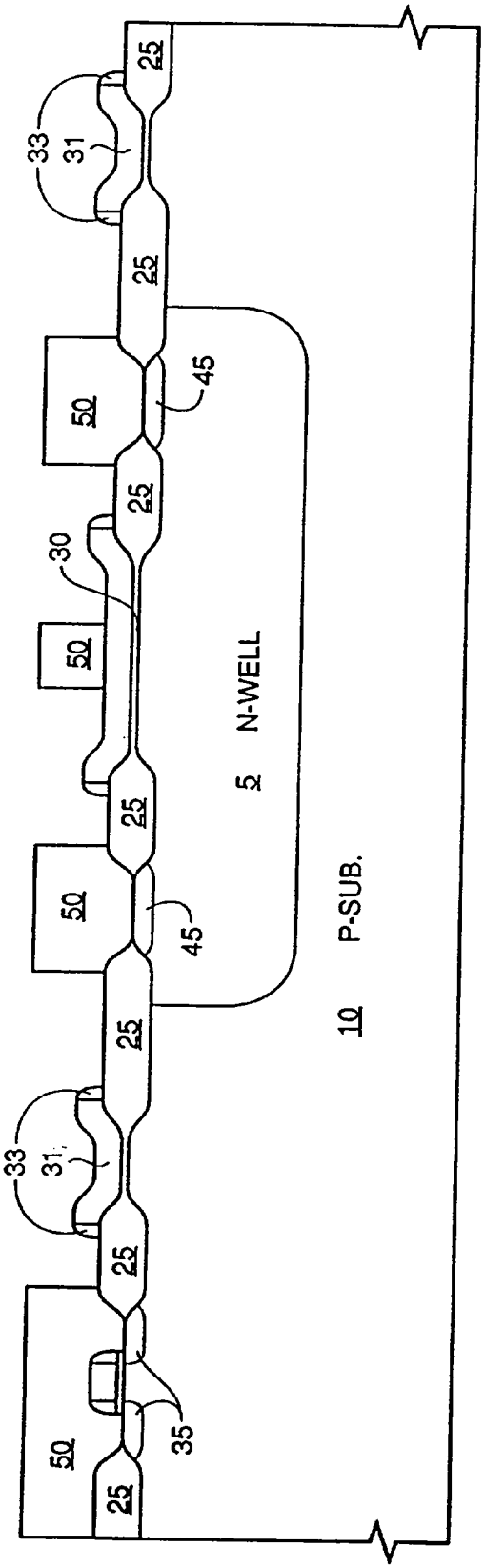


FIG. 2
(RELATED ART)

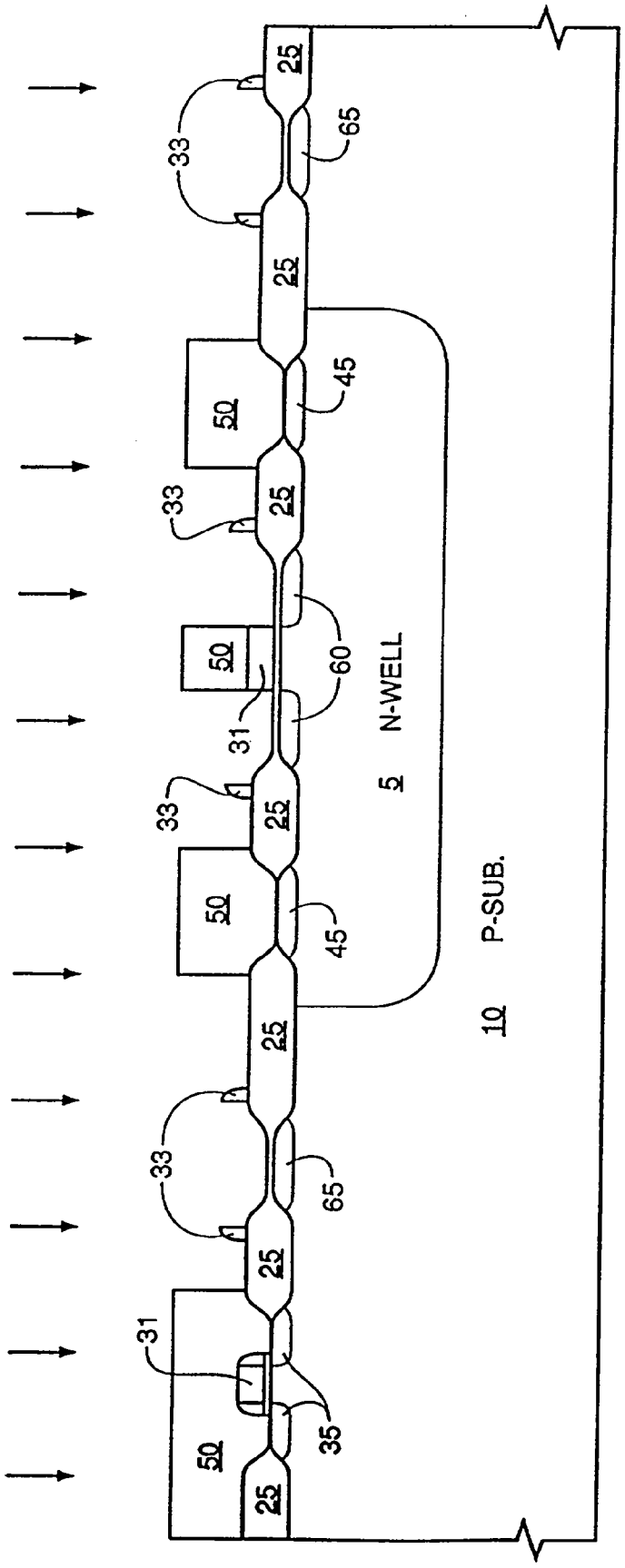


FIG. 3
(RELATED ART)

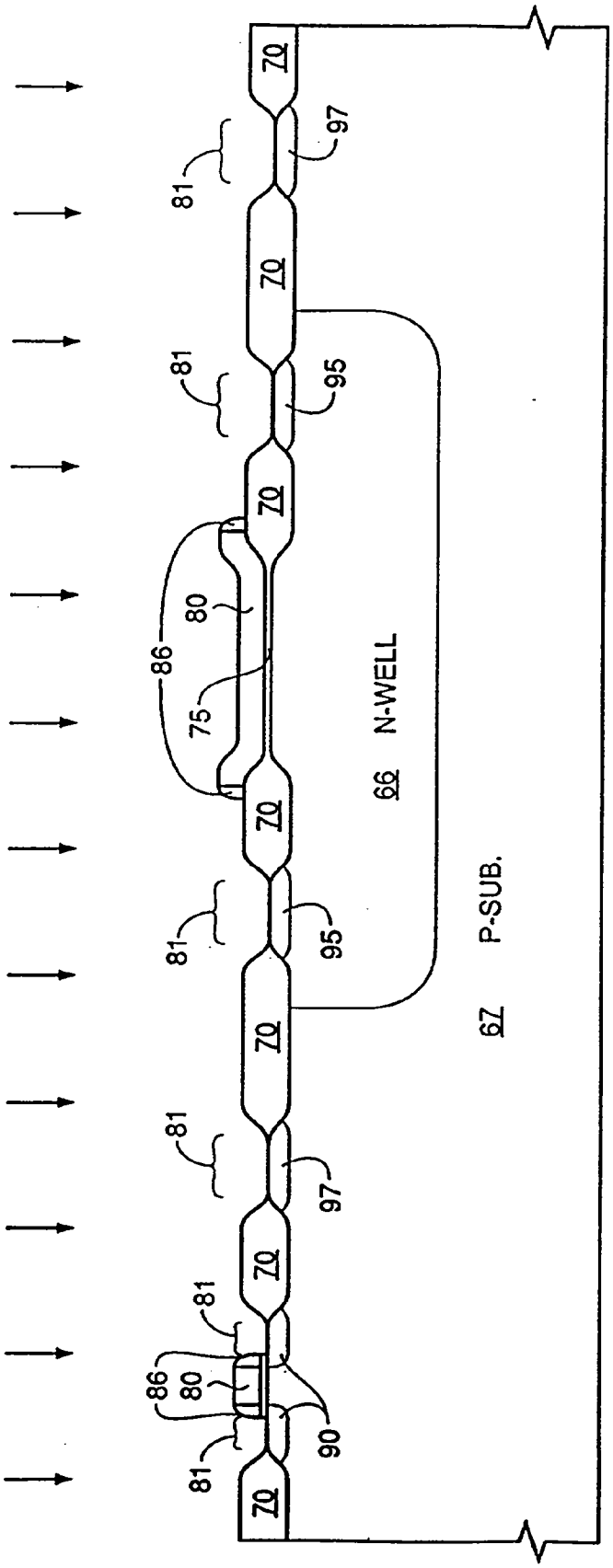


FIG. 4A

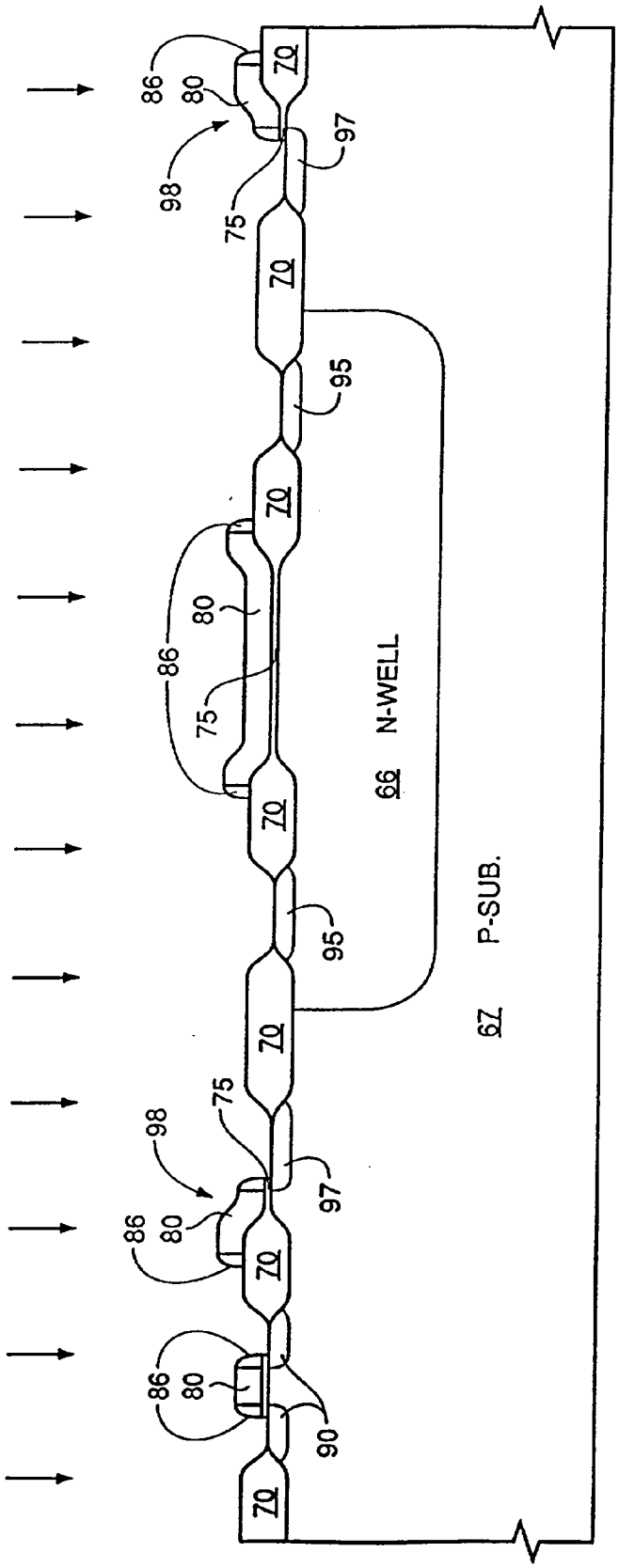


FIG. 4B

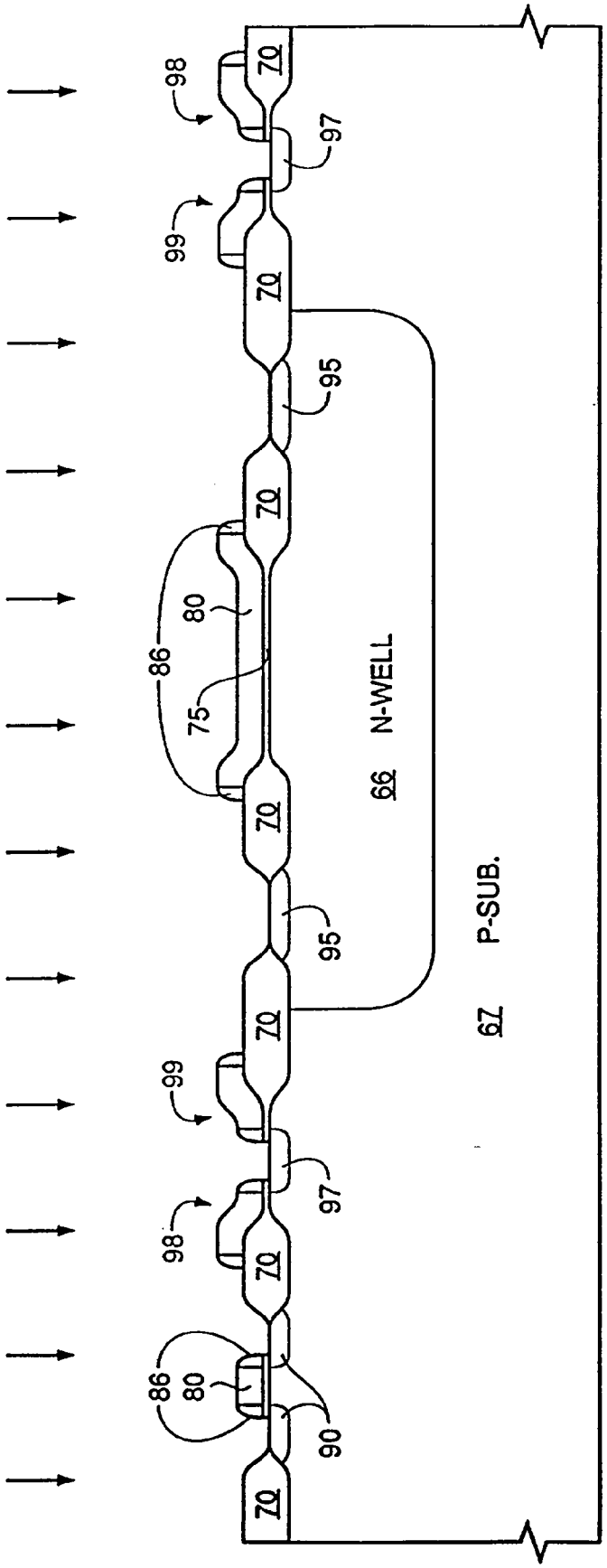
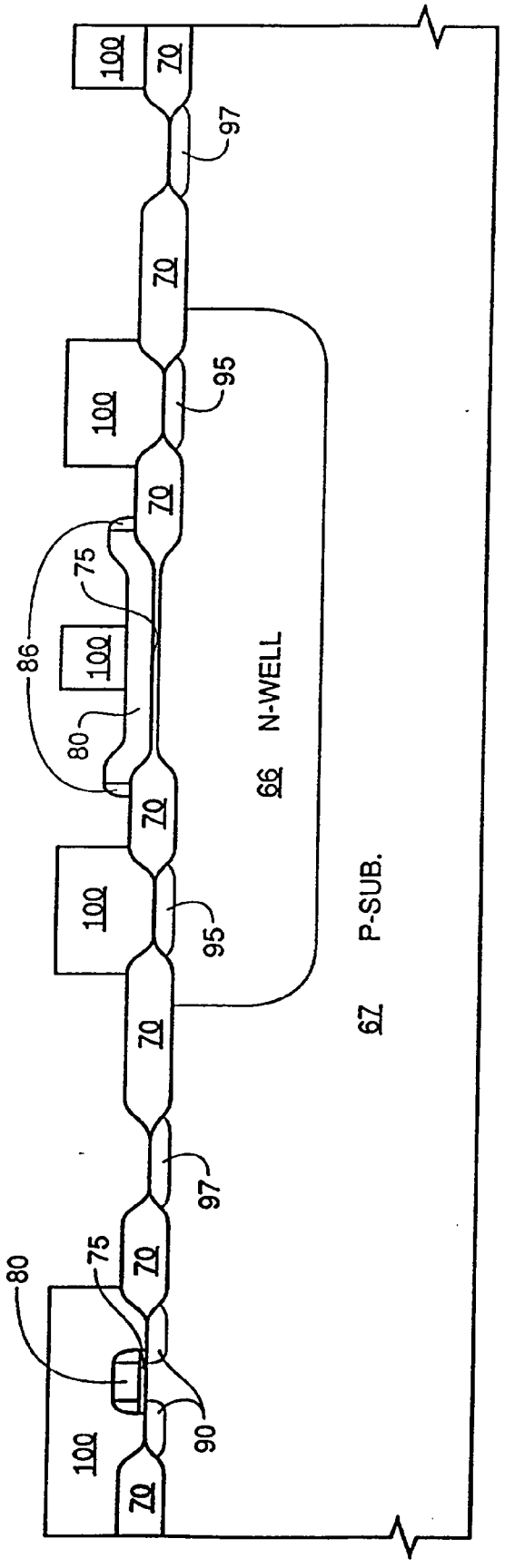


FIG. 4C


100
70
97
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86
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66 N-WELL
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100
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67 P-SUB.
97
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100
90
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FIG. 5A

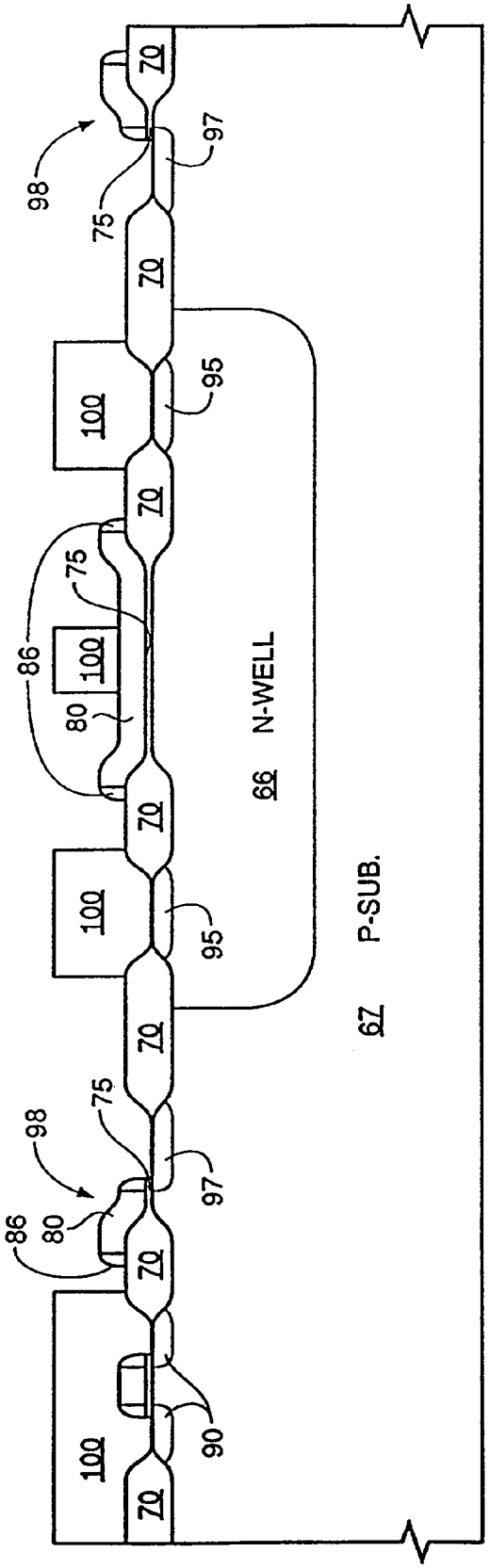
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FIG. 5B

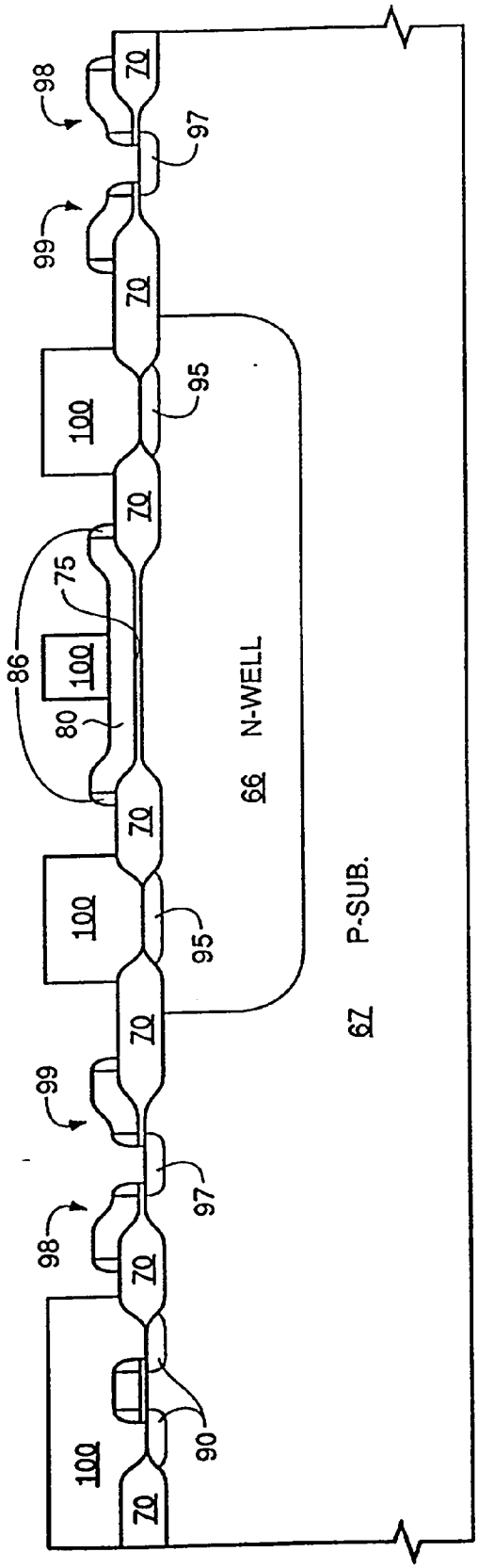

FIG. 5C

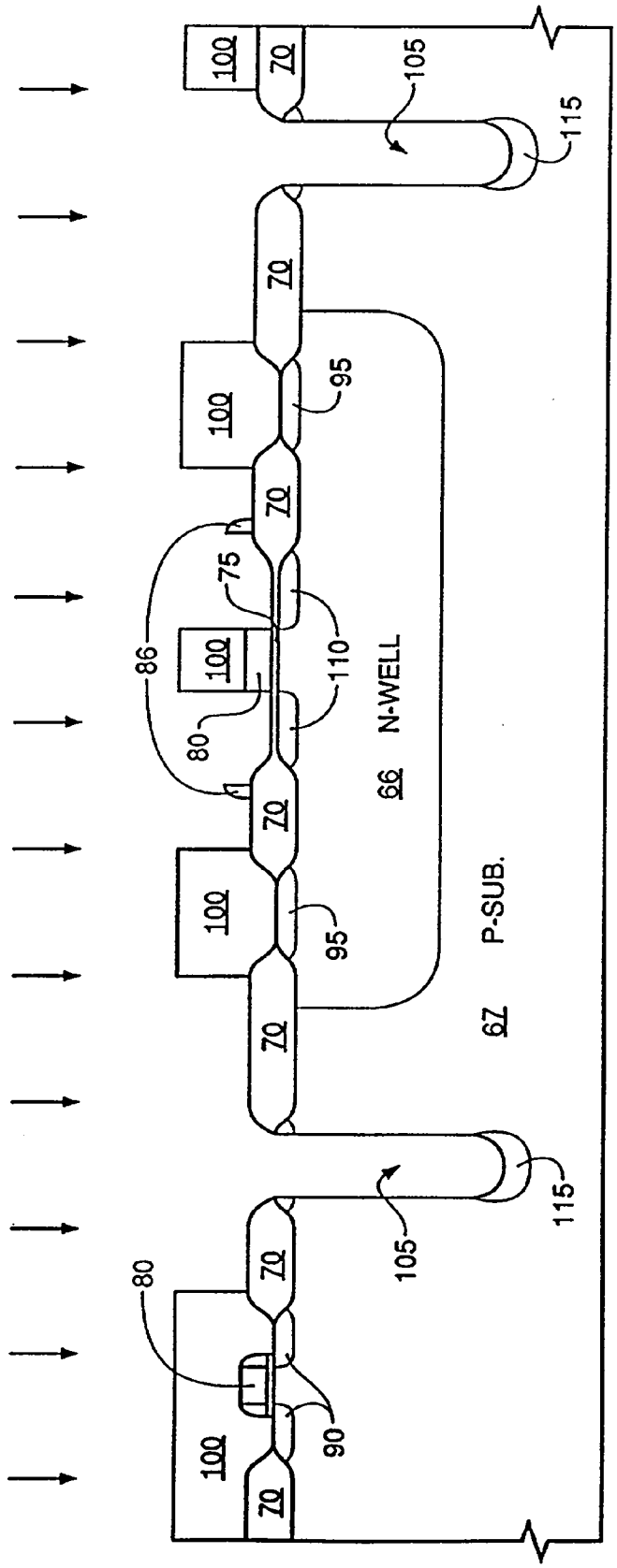

FIG. 6A

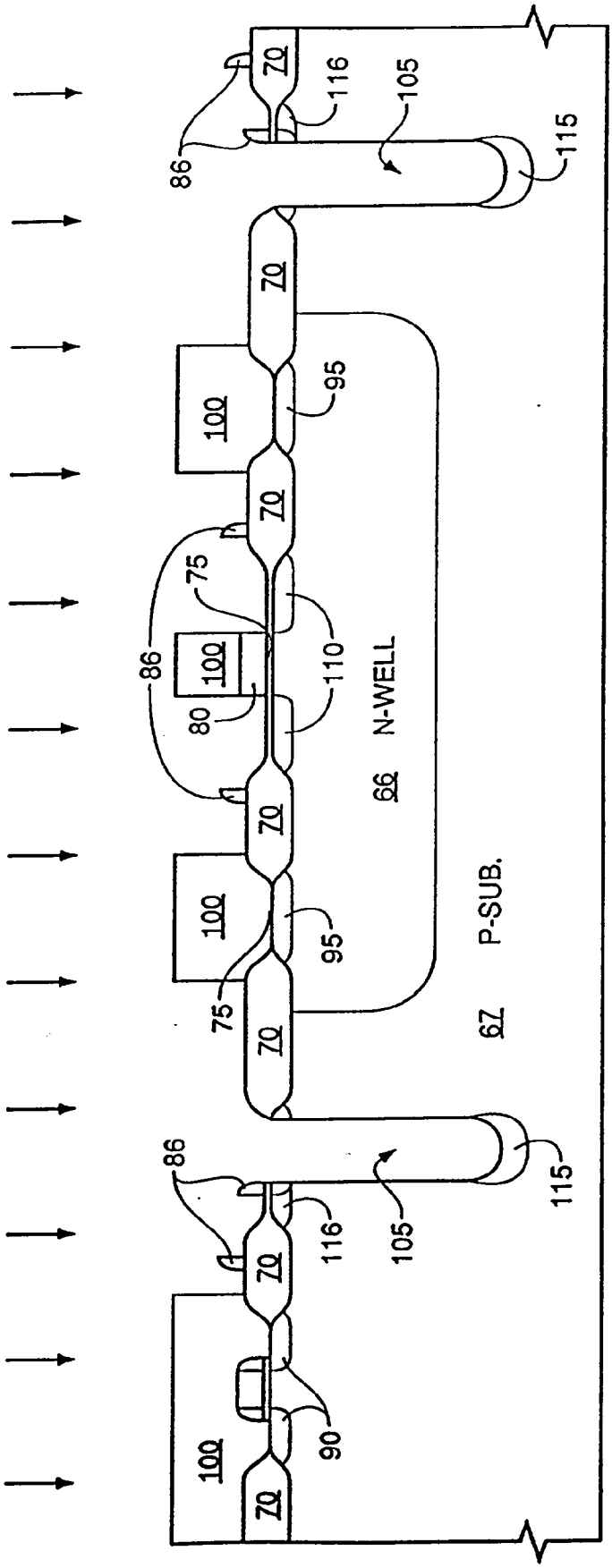

FIG. 6B

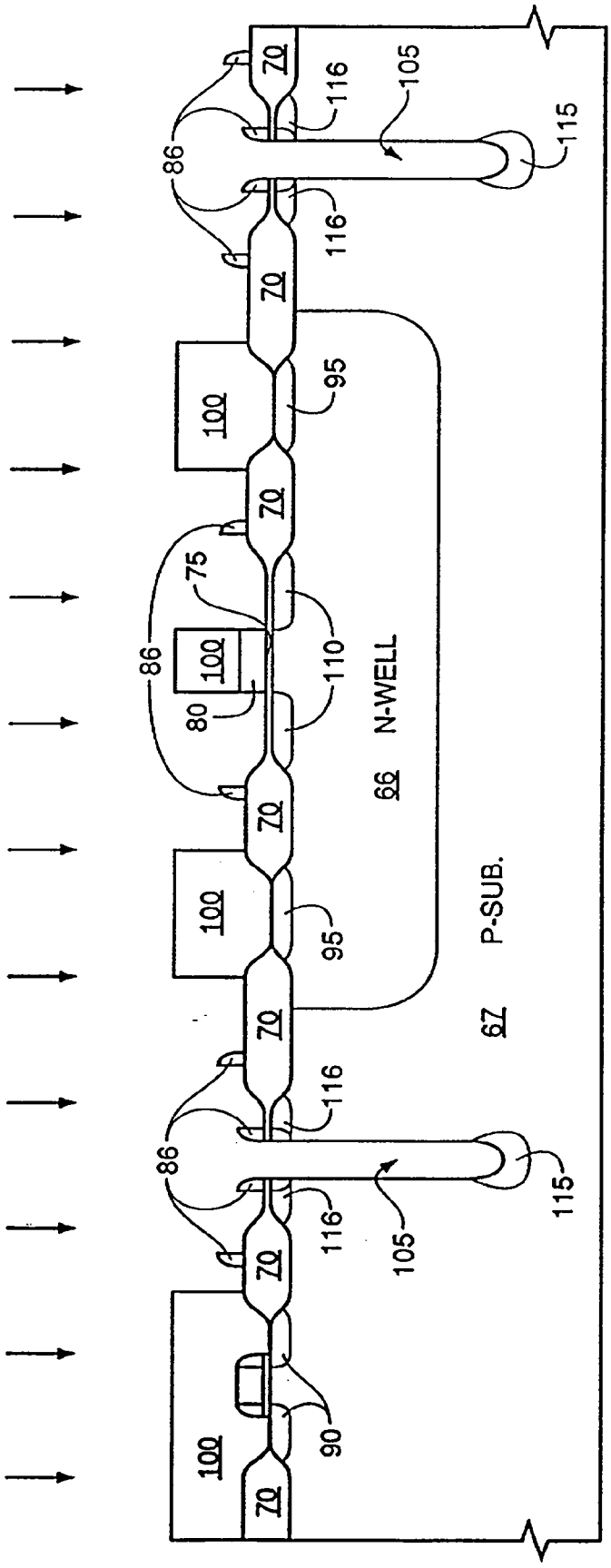

FIG. 6C

APPARATUS IMPROVING LATCHUP IMMUNITY IN A DUAL-POLYSILICON GATE

FIELD OF THE INVENTION

[0001] The invention relates to semiconductor devices and the fabrication thereof and, more particularly, to isolation and well regions formed in a substrate and the fabrication thereof.

BACKGROUND OF THE INVENTION

[0002] In one method of the related art P and N-channel MOS transistors are fabricated in a semiconductor substrate in a dual polysilicon gate process. In a dual polysilicon gate process, N-channel and P-channel gates are defined with separate individual masks, in contrast to a single polysilicon gate process wherein both the N-channel and the P-channel gates are formed using a single photolithographic process. The semiconductor substrate is doped with negative impurity atoms and positive impurity atoms to create negative and positive active regions respectively. These active regions can be thought of as having opposite polarities or opposite conductivities. One of the regions is created in the substrate while the other region is created in a well. The well is formed by doping a portion of the substrate to have a conductivity opposite to that of the original substrate.

[0003] FIGS. **1-3** show a cross sectional portion of a semiconductor wafer following process fabrication steps used in a method of the related art to form P- and N-channel MOS transistors. In FIGS. **1-3** an N-well **5** has been created in a P-substrate **10** by conventional fabrication means.

[0004] The N-well is a counterpart to the P-substrate in that it functions as a region in which to form P-channel MOS transistors, while the P-substrate functions as a region in which to form N-channel MOS transistors. A P-type region and an N-type region are opposite of each other with respect to energy bands. An N-type region has many electrons in its conduction band, while a P-type region has relatively few electrons in its conduction band; and a P-type region has many holes in its valence band while an N-type region has relatively few holes in its valence band. Micro Chip, A Practical Guide to Semiconductor Processing, by Peter Van Zant and Electronic Principles, third edition, by Albert Paul Malvino are herein incorporated by reference in order to determine a minimal knowledge of someone skilled in the art.

[0005] Thick oxide **25** is grown to form field oxide regions to electrically isolate active regions from each other, and a thin gate oxide **30** is grown overlying the active regions. The formation of the thick oxide layer **25** and the gate oxide layer **30** are well known to those skilled in the art.

[0006] Referring to **FIG. 1**, the conventional fabrication means is continued, and a polysilicon layer **31** is masked with photoresist to define an N-channel gate polysilicon and interconnect and an N-well tie. The polysilicon is etched and spacers **33** are formed on opposing sides of the polysilicon remaining after the etch.

[0007] The in-process wafer is bombarded with negative ions to form N-type regions in the active regions not covered with polysilicon **31**. N-type active regions **35** function as source/drain regions of an N-channel MOS transistor, and polysilicon layer **31** interposed between the regions **35** functions as the gate of the N-channel MOS transistor thus formed. N-type active region **45** is an N-well tie. An N-well tie is a region formed in the surface of the substrate in the N-well region that provides ohmic contact of the N-well to an external supply potential.

[0008] In **FIG. 2 a** second photoresist mask **50** defines P-channel gate polysilicon and interconnect and protects the N-channel gate polysilicon and N-type active regions **35** and **45** previously defined.

[0009] In **FIG. 3** the polysilicon layer **31** remaining exposed at this juncture are etched. The substrate is now bombarded with positive ions and P-type active regions **60** and **65** are formed in the surface of the substrate. It is important to note that the thick oxide regions **25** also function as masks during both the positive and negative ion bombardments that form the N-channel and P-channel source/drain regions and well/substrate ties.

[0010] P-type active regions **60** function as the sources/drain regions of a P-channel MOS transistor. Polysilicon layer **31** interposed between source/drain regions **60** functions as the gate of the P-channel MOS transistor thus formed. P-type active region **65** is a P-substrate tie and provides ohmic contact to the substrate from an external supply potential.

[0011] Although it would seem that the N-well tie **45** shown in the cross section comprises two portions, the N-well tie **45** may actually be a continuous ring surrounding the P-channel transistors, and the P-substrate tie **65** may actually be a continuous ring surrounding the N-well **5**. In further fabrication steps, contacts (not shown) are formed with the P-substrate tie **65** and the N-well tie **45** as well as the source/drain and gate terminals of the MOS devices. The P-substrate tie **65** is connected to a potential having a low voltage, typically ground, and the N-well tie **45** is connected to a potential having a high voltage, typically V_{CC}. The P-substrate tie and N-well tie help prevent latch up of the device when interposed between the N-MOS and P-MOS device.

[0012] Latchup occurs when two parasitic cross coupled bipolar transistors are actuated and essentially short a first external supply potential, V_{CC}, to a ground potential, V_{SS}. When the fabrication of the transistors is completed the N-channel source/drain regions **35** form the emitter, P-substrate **10** forms the base, and the N-well **5** forms the collector of a horizontal parasitic NPN transistor; and the P-channel source/drain regions **60** form the emitter, the N-well **5** forms the base, and the p-substrate **10** forms the collector of a vertical parasitic PNP transistor. The parasitic PNP and NPN bipolar transistors thus formed are actuated by the injection of minority carriers in the bulk of the substrate or the N-well. To prevent latch up, the lifetime of these carriers must be reduced, or the resistance of the substrate must be decreased. The latter method may force compromise in device performance by increasing junction capacitance and body effect.

[0013] The N and P substrate ties formed in the related art are gaurdbands which reduce the lifetime of the minority carriers. The gaurdbands act as a sink for the minority carriers that are injected into the substrate or N-well when the emitter/base junction of either parasitic bipolar device is forward biased. The gaurdbands also increase the distance these minority carriers must travel thereby increasing the

probability that they will recombine with majority carriers. The gaurdbands are typically formed between the N-channel MOS transistor and the P-channel MOS transistor. The gaurdbands are strips of P+ active regions in the P-substrate and N+ active regions in the N-well. The gaurdbands tie down the substrate and well potentials and prevent latchup by collecting any injected minority carriers from forward biasing the MOS device source or drain regions.

OBJECTS OF THE INVENTION

[0014] It is an object of the invention to achieve improved latchup immunity without increasing the complexity of the process steps in a dual-polysilicon process. It is a further object of the invention to reduce the lifetime of the minority carriers, and increase the distance minority carriers must travel to reach a parasitic bipolar collector.

SUMMARY OF THE INVENTION

[0015] The invention features a method for forming a trench in an active region of a substrate, and features the trench thus formed. The substrate surface reserved for trench formation is doped to have a first type conductivity. Portions of the substrate are protected, and the substrate is etched in the unprotected areas to form the trench. At the same time the trench is etched a layer overlying the substrate is also etched to form a gate region. Thus, the trench is formed without increasing processing steps. A substrate region at the bottom of the trench is doped to create a substrate region having a second type conductivity. The trench is positioned between a first and second active device and directly in a desired path of the minority carriers. The trench reduces minority current, thereby reducing the possibility of latchup.

[0016] In one embodiment of the invention, unannealed damage caused by the trench etch functions as a recombination medium for minority carriers.

[0017] In a further embodiment of the invention the trench is filled with polysilicon. The polysilicon functions as a recombination medium.

[0018] In addition the polysilicon may function as an electrical interconnect between the doped substrate and an external potential. In this embodiment the polysilicon filled trench is also a substrate tie.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] **FIG. 1** is a cross section of a portion of a related art semiconductor wafer following the formation of an N-well and N+ active regions.

[0020] **FIG. 2** is a cross section of the related art semiconductor wafer of **FIG. 1** following the masking of the N+ regions.

[0021] **FIG. 3** is a cross section of the related art semiconductor wafer of **FIG. 2** following the formation of a P+ active regions.

[0022] FIGS. **4**A-C are cross sections of a portion of a semiconductor wafer of the invention following the formation of N+ regions in the substrate.

[0023] FIGS. **5**A-C are cross sections of a portion of the semiconductor wafer of **FIGS. 4A and 4B**, respectively, following the masking of the substrate to protect selected N+ regions.

[0024] FIGS. **6**A-C are cross sections of a portion of the semiconductor wafer of **FIGS. 5A and 5B**, respectively, following the formation of a trench and P+ regions in the substrate.

DETAILED DESCRIPTION OF THE INVENTION

[0025] The invention is a method for creating a portion of an integrated circuit on a semiconductor wafer. In the method of the invention an isolation trench and an isolation region are formed in order to electrically isolate two regions of the integrated circuit from each other. The isolation trench and the isolation region minimize undesired effects, such as latch up caused by the actuation of parasitic bipolar transistors.

[0026] Although the method of the invention pertains to the fabrication of the isolation trench and the isolation region of the integrated circuit, the method will be described in conjunction with the formation of transistors in order to provide a clearer picture of the function of the invention.

[0027] Referring to FIGS. **4**A-C, an N-well **66** is formed in a P-substrate **67**. Creating an N-well within a P-type substrate is well known to those skilled in the art and involves doping the substrate with impurity atoms to create a negatively doped region in which to fabricate a P-channel metal oxide semiconductor (MOS) transistor. Since a P-type substrate is positively doped the P-type substrate and the N-well can be thought of as having opposite polarities or opposite conductivities.

[0028] Still referring to FIGS. **4**A-C, the substrate has been patterned and a thick oxide **70** has been formed in isolation regions using a conventional local oxidation of silicon (LOCOS) process. Optionally other isolation schemes, such as trench isolation and poly buffered LOCOS, may be used. These alternate isolation schemes are also well known to those skilled in the art.

[0029] Following the removal of the mask used to grow the field oxide, thin gate oxide **75** is formed in future active regions. The creation of thin gate oxide is also well known to those skilled in the art.

[0030] Following the formation of the gate oxide **75** a polysilicon layer **80** is deposited. A photoresist mask, not shown, is used to pattern the polysilicon layer **80** thereby exposing a selected first portion of the future active regions. The unprotected portion of the polysilicon is etched exposing gate oxide **75** in the selected first portion of the future active regions. The polysilicon etch also exposes portions of the thick oxide **70**. Spacers **86** are created on the opposed exposed ends of the etched polysilicon layer **80**. The spacers **86** may be electrically insulative and are created with methods well known to those skilled in the art. The spacers **86** are typically oxide.

[0031] Next the substrate is bombarded with ions having a sufficient dose to form highly doped N+ regions in each of the selected first portion of exposed active regions. Typical ions used to fabricate N+ regions are arsenic, antimony, or phosphorous. N+ active regions **90** function as source/drain regions of an N-channel MOS transistor. The gate of the N-channel MOS transistor is the polysilicon layer **80** interposed between the N+ active regions **90**. N+ active region **95** is an isolation region which functions as an N-well tie when

connected to an external supply potential, such as V_{CC}. N+ active region **95** may be a contiguous annular ring. It should be noted that an annular ring is not necessarily circular. N+ active region **97** fabricated during this step will be removed during the formation of a substrate trench. N+ active region **97** may form a contiguous annular ring surrounding the N-well **66** and basically concentric to the annular ring formed by N+ active region **95**. The distance between the two regions **95** and **97** may vary due to variations in the width of the thick oxide layer **70** interposed between the two active regions **95** and **97**.

[**0032**] In addition to the polysilicon layer **80** with spacers **86**, the thick oxide **70** functions as a mask during the ion bombardment.

[**0033**] In **FIG. 4B** a segment **98** of polysilicon layer **80** with spacers **86** functions as a mask to define active region **97**. It can be seen by studying **FIG. 4B** that segment **98** extends beyond the thick oxide **70** and actually overlies a portion of the gate oxide layer **75**. In addition it is possible to use a second segment **99** of polysilicon layer **80** with spacers **86** to mask the other side of active area **97** as shown in **FIG. 4C**.

[**0034**] During spacer formation, all oxide overlying exposed active regions is typically removed (FIGS. **4**A-C), although this is not a requirement of this invention.

[**0035**] Referring now to FIGS. **5**A-C, a photoresist mask **100** is formed to protect the N+ active regions **90** and **95** during the formation of a second portion of active regions. If remaining oxide **75** has not yet been removed from active region **92** it is now removed in exposed areas during a short oxide etch. This oxide etch is selective over the exposed polysilicon **80**.

[**0036**] Referring now to FIGS. **6**A-C, an etch selective to silicon over oxide is performed to create a trench **105** in the silicon substrate **67**. The etch substantially removes the active area **97** to create a recess and then removes the substrate underlying the recess to complete the trench formation. In **FIG. 6A** the trench **105** is self-aligned to the thick oxide **70**. In **FIG. 6B** the trench **105** is self aligned on one side to the thick oxide **70** and is aligned on the other side to the edge of the spacer **86**. In **FIG. 6C** the trench is aligned on both sides to the edge of the spacers **86**. During the etch unmasked portions of polysilicon layer **80**, including segments **98** and **99**, are also etched. However, the substrate **67** underlying the etched polysilicon layer **80** is protected during the etch by the gate oxide layer **75**. In addition, the spacers **86** protect the substrate **67** during the etch. In a preferred embodiment the trench **105** is created to have a depth greater than the depth of the N-well **66**.

[**0037**] Following the trench formation the wafer is bombarded with positive ions having a sufficient energy to form highly doped to P+ regions in the unmasked portions of the substrate. Typical ions used during the ion bombardment are aluminum, boron, or gallium. P+ active regions **110** are source/drain regions of a P-channel MOS transistor. The gate of the P-channel MOS transistor is the polysilicon layer **80** interposed between the P+ active regions **110**. P+ region **115** is formed in the silicon substrate **67** at the base of the trench **105**. The trench **105** with its P+ region **115** and the N+ active region **95** functioning as an N-well tie separate the P-channel MOS transistor from the N-channel MOS transistor thus formed. In **FIGS. 6B and 6C** an additional P+ active region **116** is formed adjacent to a top portion of the trench. Standard metalization contacts can readily be formed overlying the P+ active region **116**.

[**0038**] A P+ region and an N+ region are opposite of each other with respect to energy bands. An N+ region has many electrons in its conduction band, while a P+ region has relatively few electrons in its conduction band; and a P+ region has many holes in its valence band while an N+ region has relatively few holes in its valence band.

[**0039**] Once the trench **105** has been fabricated according to the steps of the invention alternate embodiments may be employed at the discretion of the designer. In one option a high temperature anneal is performed subsequent to the trench formation in order to create regions at the bottom of the trench **105** which have recombination centers even when high temperature anneals are performed later in the fabrication process. These regions function as recombination centers for the minority carriers and further reduce the concentration of the minority carriers in the device.

[**0040**] An additional option comprises filling the trench **105** with polysilicon. The polysilicon provides additional recombination centers. In the present embodiment the polysilicon is either P+ type or undoped.

[**0041**] In a further embodiment the substrate adjacent to the sidewalls of the trench are positively doped. In this embodiment the trench may be filled with polysilicon or a dielectric following the trench etch and sidewall doping. Alternately the substrate adjacent to the sidewalls may be doped automatically during the doping of a previously deposited filler material such as the polysilicon.

[**0042**] In a further embodiment the P+ region **115** may be connected to an external potential having a low voltage, typically ground via polysilicon deposited in the trench. In this case the P+ region **115** is a substrate tie.

[**0043**] In addition the shape of the trench is not important, although one skilled in the art would be aware of the importance of using suitable design rules to prevent shorting the trench to the boundary of the N-well or an adjacent N-channel region.

[**0044**] Although the detailed description has described the formation of one trench **105**, the invention is applicable when forming a plurality of trenches.

[**0045**] Although the invention has been described in terms of forming the trench in a P-type substrate with an N-well formed therein, the invention is equally applicable to forming a trench in an N-type substrate with a P-well formed therein and to creating an N-type region at the base of the trench thus formed.

[**0046**] There are many methods that may be employed to dope a substrate in addition to bombarding the substrate with dopant ions. These alternate methods are well known to those skilled in the art. One alternate method is diffusion.

[**0047**] Although the method is more effective when the trench is formed in the substrate rather than the well, the invention can be performed for either case, and in either case the trench is positioned to reduce minority current caused by parasitic bipolar transistors.

[0048] No additional mask steps are required in this invention over those typically used in a dual poly gate patterning process. However, the invention is not limited to MOS devices. Other options include using the method and or apparatus of the invention to improve the isolation of bipolar devices one from another.

[0049] Although the invention has been described as a dual polysilicon process the method could also be applied to MOS or bipolar process that etch layers of polysilicon doped and patterned at different steps. Such a process could use polysilicon **1** and polysilicon **2** etch steps to form the trench.

[0050] While this invention has been described with reference to an illustrative embodiment, this description is not intended to be construed in a limiting sense. Various modifications as well as other embodiments for fabricating a trench in a previously doped active region or for the trench formed therein will be apparent to persons skilled in the art upon reference to this description. It is, therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

What is claimed is:

1. A method for increasing latch-up immunity in a semiconductor circuit, comprising the following steps:

a) creating a well region having a first type conductivity in a substrate having a second type conductivity;

b) creating a first active device having said second type conductivity in said well region;

c) creating a second active device having said first type conductivity in said substrate outside of said well region; and

d) creating a trench in said substrate between said first active device and said second active device thereby increasing a distance minority carriers must travel between said first and said second active devices, thereby increasing the latch-up immunity.

2. The method as specified in claim 1, wherein said step of increasing said distance decreases a current between said first and said second active devices.

3. The method as specified in claim 1, further comprising the steps of:

a) increasing a quantity of recombination centers in response to said step of creating said trench; thereby

b) reducing a lifetime of said minority carriers in said substrate, as a result of said minority carriers combining with majority carriers at said recombination centers.

4. The method as specified in claim 1, further comprising the steps of:

a) damaging said substrate during said step of creating said trench;

b) performing a high temperature first anneal prior to a high temperature second anneal and subsequent to said step of creating said trench; and

c) retaining some damage to said substrate as a result of said step of performing said first anneal, said retained damage having recombination centers.

5. The method as specified in claim 1, further comprising the step of filling said trench with a filler material to provide recombination centers.

6. The method as specified in claim 5, further comprising the step of doping said filler material.

7. The method as specified in claim 6, further comprising the step of automatically doping said substrate adjacent to said filler material during said step of doping said filler material.

8. The method as specified in claim 5, further comprising the step of fabricating an electrical interconnect overlying said filler material.

9. The method as specified in claim 1, further comprising the step of doping said substrate adjacent to at least one sidewall of said trench.

10. The method as specified in claim 1, further comprising the step of creating a doped region of said substrate at a base of said trench during one of said steps of creating said first and said second active devices, said doped region having a same type conductivity as said active device being created.

11. The method as specified in claim 10, further comprising the step of creating a doped contact area in a surface of said substrate adjacent to said trench, said doped contact area created during said step of creating said doped region, said doped contact area having a same type conductivity as said doped region.

12. The method as specified in claim 11, further comprising the step of fabricating an electrical interconnect overlying said doped contact area.

13. A method for fabricating a circuit, comprising the following steps:

a) defining active regions of a substrate;

b) adding ions having a first type conductivity to at least two of said active regions to form first type active areas having said first type conductivity;

c) masking at least one of said first type active areas thereby creating a primary exposed region, said primary exposed region having at least one of said first type active areas; and

d) removing said first type active area in said primary exposed region to form a recess.

14. The method as specified in claim 13, further comprising the step of removing a further portion of said substrate underlying said recess thereby creating a trench.

15. The method as specified in claim 14, further comprising the step of removing at least a portion of a mask overlying said substrate at least during said step of removing said first type active area and optionally during said step of removing said further portion of said substrate, thereby creating a secondary exposed region.

16. The method as specified in claim 15, further comprising the step of adding ions having a second type conductivity to said substrate in said primary and said secondary exposed regions, thereby forming a second type active area having said second type conductivity in said surface of said substrate in said secondary exposed region and a doped region having said second type conductivity in said substrate at a base of said trench.

17. The method as specified in claim 16, further comprising the step of forming said second type active area in said substrate adjacent to an upper portion of said trench.

18. A method for creating first conductive areas and second conductive areas in a substrate, comprising the following steps:

a) protecting active regions of said substrate with a first mask;

b) forming thick electrically insulative isolation regions in exposed regions of a surface of said substrate;

c) removing said first mask;

d) creating a thin electrically insulative layer overlying said substrate in said active regions;

e) protecting a first portion of said active regions with a second mask, thereby leaving a second portion of said active regions unprotected;

f) adding impurity ions having a first type conductivity to said active regions in said second portion, thereby forming a plurality of the first conductive areas in said second portion;

g) protecting at least one of said first conductive areas and at least a portion of said second mask with a third mask, at least one of said first conductive areas and at least a portion of said second mask remaining exposed;

h) removing said thin electrically insulative layer overlying said exposed first conductive area, thereby exposing said substrate;

i) removing said exposed first conductive area to form a recess;

j) removing a portion of said substrate underlying a base of said recess to form a trench;

k) removing exposed portions of said second mask during at least one of said steps of removing said exposed first conductive area and said removing a portion of said substrate, thereby exposing portions of said thin electrically insulative layer; and

l) adding impurity ions having a second type conductivity to exposed portions of said substrate thereby forming the second conductive areas.

19. The method as specified in claim 18, further comprising the step of forming a doped region in said substrate at a base of said trench during said step l.

20. The method as specified in claim 18, further comprising the step of forming one of the second conductive areas in a surface of said substrate adjacent to a top portion of said trench.

21. The method as specified in claim 18, further comprising the step of adding impurity ions to said substrate to form a well region in a portion of said substrate, said well region and said substrate having opposite conductivities.

22. The method as specified in claim 21, further comprising the step of performing said steps i and j until said trench has a depth at least equal to a depth of said well region.

23. The method as specified in claim 21, further comprising the step of forming said trench in said well region.

24. The method as specified in claim 21, further comprising the step of forming said trench in said substrate outside said well region.

25. The method as specified in claim 18, further comprising decreasing a lifetime of minority carriers.

26. The method as specified in claim 18, further comprising the step of interposing said trench between at least one of said first conductive areas and at least one of said second conductive areas.

27. A method for fabricating a circuit structure, comprising the following steps:

a) doping a portion of a substrate having a first type conductivity to create a well region having a second type conductivity;

b) creating isolation regions overlying said substrate and said well region, said isolation regions interposed between active regions of said substrate and said well region;

c) forming a thin gate dielectric layer overlying said active regions;

d) forming a conductive layer overlying said gate dielectric layer and said isolation regions;

e) masking said conductive layer with a first mask;

f) removing exposed portions of said conductive layer thereby exposing at least two of said active regions;

g) doping said exposed active regions to form first type active areas;

h) masking portions of said conductive layer and at least one of said first -type active areas with a second mask, at least one of said first type active areas remaining exposed;

i) removing said gate dielectric over said exposed first type active area; and

j) creating a trench by

removing said exposed first type active area and by

removing said substrate underlying exposed said trench to further increase a depth of said trench.

28. The method as specified in claim 27, further comprising the step of creating said trench in said well region.

29. The method as specified in claim 27, wherein said step of removing said substrate is performed sufficiently to create a trench having at least a depth equal to a depth of said well region.

30. The method as specified in claim 27, further comprising the step of creating said trench in said substrate outside of said well region.

31. The method as specified in claim 27, further comprising the step of removing an exposed portion of said conductive layer to expose said gate dielectric layer during said step of creating said trench.

32. The method as specified in claim 31, further comprising the step of doping exposed active regions with ions having a second type conductivity to create second type active areas in said exposed active regions.

33. The method as specified in claim 32, further comprising creating a doped region in said substrate at a base of said trench during said step of doping said exposed active regions.

34. The method as specified in claim 32, further comprising creating a doped region in said substrate adjacent to an upper portion of said trench during said step of doping said exposed active regions.

35. The method as specified in claim 32, further comprising the step of positioning said trench between at least one of said first type active areas and at least one of said second type active areas.

36. The method as specified in claim 27, further comprising creating recombination centers disposed about said trench.

37. A method for fabricating a semiconductor circuit, comprising the following steps:

a) forming a well region having a first type conductivity in a portion of a substrate having a second type conductivity;

b) forming a plurality of isolation regions, active regions interposed between said isolation regions;

c) forming a gate dielectric layer to overly said active regions;

d) forming a conductive layer overlying said gate dielectric and said isolation regions;

e) removing portions of said conductive layer to expose a first portion of said active regions, while

retaining portions of said conductive layer, said retained portions masking a second portion of said active regions;

f) doping said substrate in said first portions of said active regions with impurity ions having either one of said first and said second type conductivities thereby forming first type active regions;

g) masking at least one of said first type active areas and portions of said conductive layer, at least another one of said first type active areas and at least a portion of said conductive layer remaining exposed;

h) removing said gate dielectric layer in said exposed first type active area;

i) forming a trench in said exposed first type active area

j) removing said exposed portion of said conductive layer; and

k) doping exposed substrate with impurity ions having one of said first and said second type conductivities to create a second type active area and to create a doped region at a base of said trench interposed between at least one of said first type and at least one of said second type active areas, said first type and said second type active areas having opposite type conductivities.

38. The method as specified in claim 37, wherein said step of forming said trench comprises removing said exposed first type active area and said substrate underlying said exposed first type active area.

39. The method as specified in claim 37, further comprising the step of creating at least one said second type active areas in a surface of said substrate adjacent to said trench.

40. The method as specified in claim 37, further comprising increasing a number of recombination centers at which minority carriers may combine with majority carriers, said recombination centers disposed about said trench.

41. The method as specified in claim 40, wherein said step of increasing said number of recombination centers comprises the step of creating damage to said substrate during said step of forming said trench.

42. The method as specified in claim 41, further comprising the step of performing a first anneal to retain at least a portion of said damage during a subsequent second anneal.

43. The method as specified in claim 40, wherein said step of increasing said number of recombination centers comprises the step of filling said trench with a filler material.

44. The method as specified in claim 43, further comprising the step of doping said filler material.

45. The method as specified in claim 44, further comprising the step of automatically doping said substrate adjacent to said filler material during said step of doping said filler material.

46. The method as specified in claim 37, further comprising the following steps:

a) forming at least two of said first type active areas in said well to form a first type active device; and

b) forming at least two of said second type active areas in said substrate outside of said well to form a second type active device.

47. The method as specified in claim 46, further comprising the step of positioning said trench between said first type and said second type active devices.

48. The method as specified in claim 37, further comprising the step of positioning said trench in said well.

49. The method as specified in claim 37, further comprising the step of positioning said trench in said substrate outside of said well.

50. The method as specified in claim 37, wherein said step of forming said trench comprises removing said substrate in sufficient quantities such that a depth of said trench is at least equal to a depth of said well.

51. The method as specified in claim 37, wherein said second type active area is p-type wherein said first type active area is n-type.

52. The method as specified in claim 37, wherein said first type active area is p-type and wherein said second type active area is n-type.

53. A semiconductor circuit, comprising:

a) a first region of a substrate having a first type conductivity;

b) a second region of said substrate doped to a second type conductivity; and

c) a trench interposed between portions of said first and said second regions, said trench increasing a distance minority carriers must travel between said first and said second regions, the increased distance providing opportunities for said minority carriers to recombine with majority carriers.

54. The semiconductor circuit as specified in claim 53, further comprising a doped region in said substrate at a base of said trench.

55. The semiconductor circuit as specified in claim 53, further comprising:

a) a first active device within said first region; and

b) a second active device within said second region, said trench interposed between said first and said second active devices.

56. The semiconductor circuit as specified in claim 53, further comprising recombination centers disposed about said trench.

57. A semiconductor circuit, comprising:

a) a substrate of a first type conductivity;

b) a well region of said substrate having a second type conductivity;

c) a first active device having said second type conductivity and fabricated to lie within said substrate having said first type conductivity;

d) a second active device having said first type conductivity and fabricated to lie within said well region; and

e) a trench disposed from a surface of said substrate and interposed between said first and said second active devices, said trench increasing a distance minority carriers must travel between said first active device and said second active device.

58. The circuit as specified in claim 57, wherein said trench lies within said well region.

59. The circuit as specified in claim 58, further comprising a doped region of said second type conductivity fabricated to lie at a base of said trench.

60. The circuit as specified in claim 58, further comprising a doped region of said second type conductivity fabricated to lie in said surface of said substrate adjacent to an upper portion of said trench.

61. The circuit as specified in claim 57, wherein said trench lies in said substrate of said first type conductivity.

62. The circuit as specified in claim 61, further comprising a doped region of said first type conductivity fabricated to lie at a base of said trench.

63. The circuit as specified in claim 61, further comprising a doped region of said second type conductivity fabricated to lie in said surface of said substrate adjacent to an upper portion of said trench.

64. The circuit as specified in claim 57, wherein said trench has a depth at least equal to a depth of said well region.

65. The circuit as specified in claim 57, further comprising a plurality of recombination centers disposed about said trench.

66. The circuit as specified in claim 65, further comprising a trench filler within said trench, said trench filler having at least a portion of said plurality of recombination centers.

67. The circuit as specified in claim 66, wherein said trench filler is doped.

68. The circuit as specified in claim 65, further comprising a region of damage formed as a result of forming said trench and formed adjacent to said trench, said region of damage having at least a portion of said plurality of recombination centers.

69. The circuit as specified in claim 65, further comprising a doped region lying at a base of said trench.

70. The circuit as specified in claim 69, further comprising an electrical interconnect overlying and in electrical communication with said doped region.

71. The circuit as specified in claim 57, further comprising a doped region formed adjacent to at least one sidewall of said trench.

72. The circuit as specified in claim 57, further comprising isolation regions overlying said substrate, one of said isolation regions interposed between said first active device and said trench and one of said isolation regions interposed between said second active device and said trench.

73. The circuit as specified in claim 57, wherein said first type conductivity is p-type, and wherein said second type conductivity is n-type.

74. The circuit as specified in claim 57, wherein said first type conductivity is n-type, and wherein said second type conductivity is p-type.

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