United States Patent

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[32] Priorities **Sept. 9, 1968**
[33] **Japan**
[31] **43/64261;**
Jan. 30, 1969, Japan, No. 44/7110; Jan.
30, 1969, Japan, No. 44/8499

[54] **DISPLAY APPARATUS**
5 Claims, 21 Drawing Figs.

[52] **U.S. Cl.** ..... **340/324 A,** 340/172.5
[51] **Int. Cl.** **G06f 3/14**
[50] **Field of Search** ..... 340/324 A, 220

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ABSTRACT: A display apparatus having a keyboard for encoding elements for the display of various characters, symbols or graphs by the combination of dots on a cathode ray tube operated in accordance with the standard television system, and MOS (Metal Oxide Semiconductor) dynamic shift registers for storing the codes representing the characters, symbols on graphs to be displayed. A video signal according to the codes applies intensity modulation to the scanning lines or rasters thereby to effect the desired display on the cathode ray tube. Renewal of displayed character can be effected by displaying a cursor at a renewed position on the cathode ray tube and manipulating the keyboard.

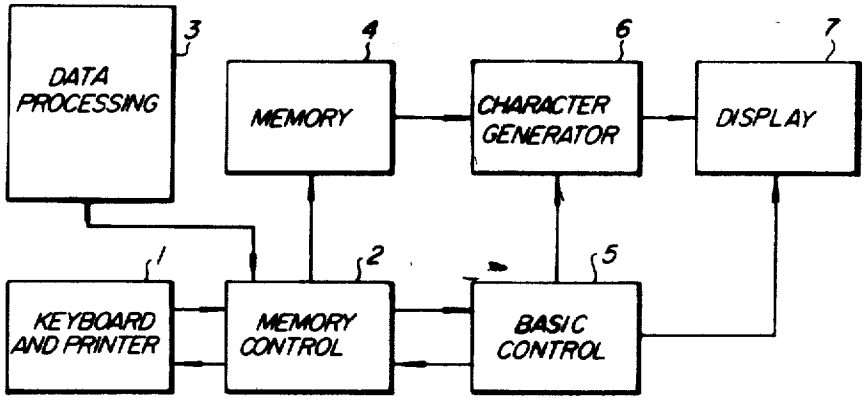

FIG. 1

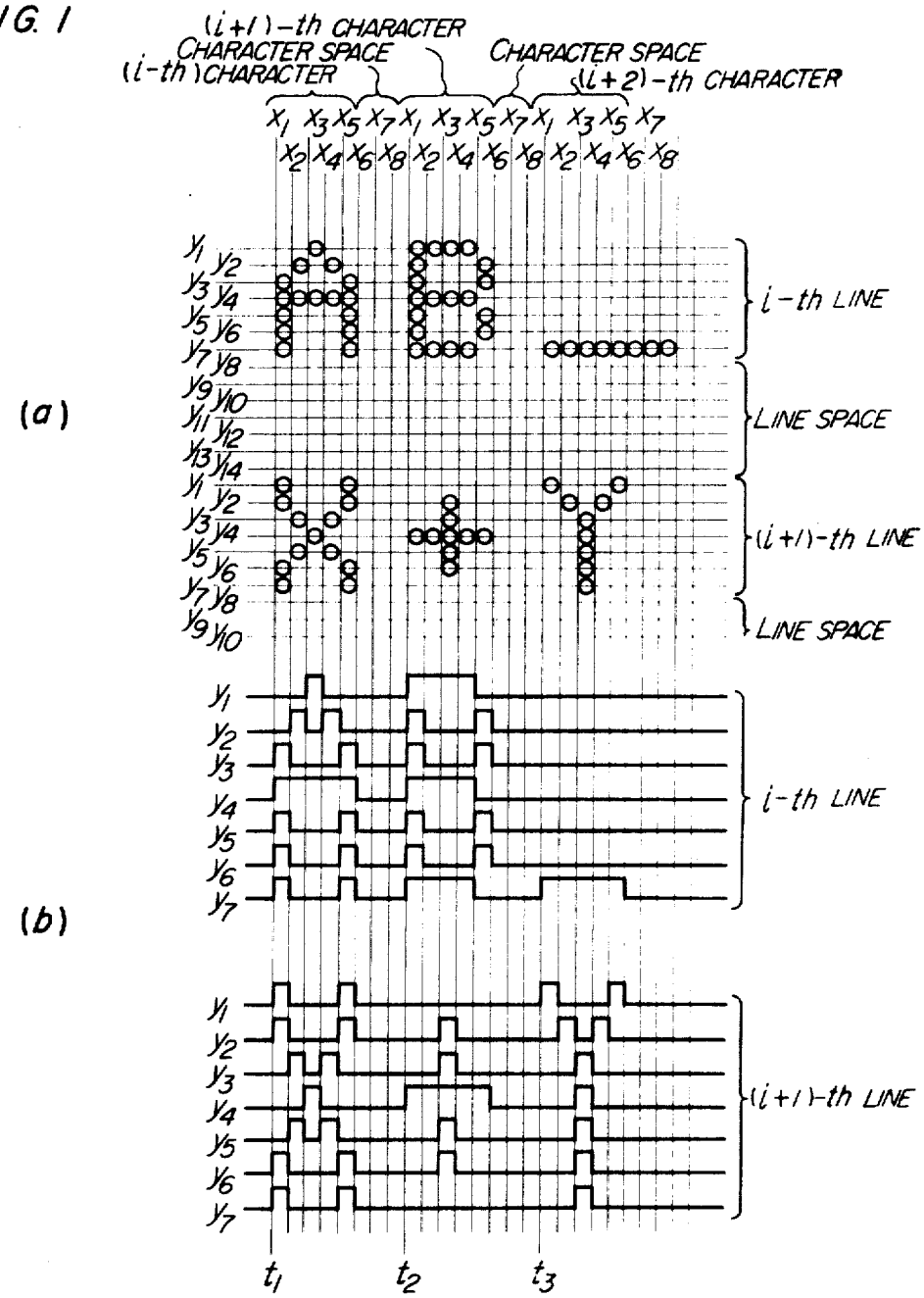

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FIG. 2

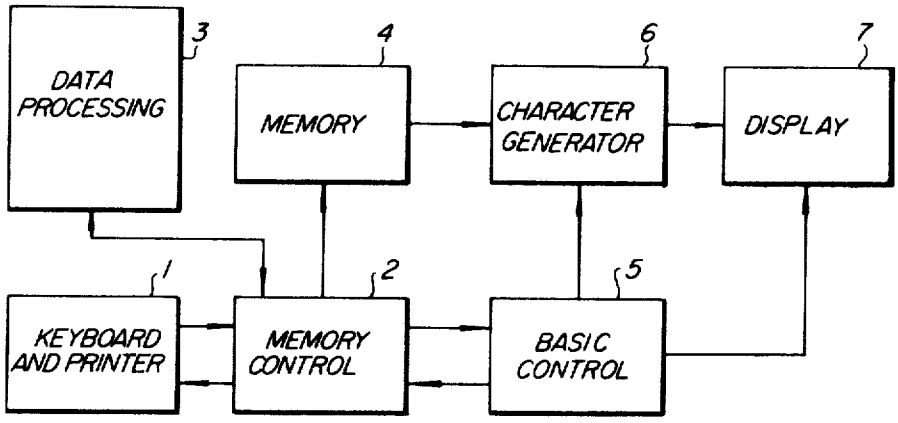
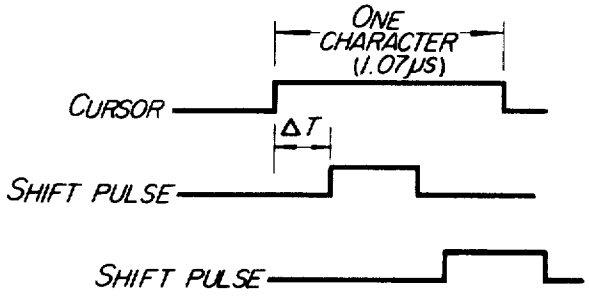


FIG. 15



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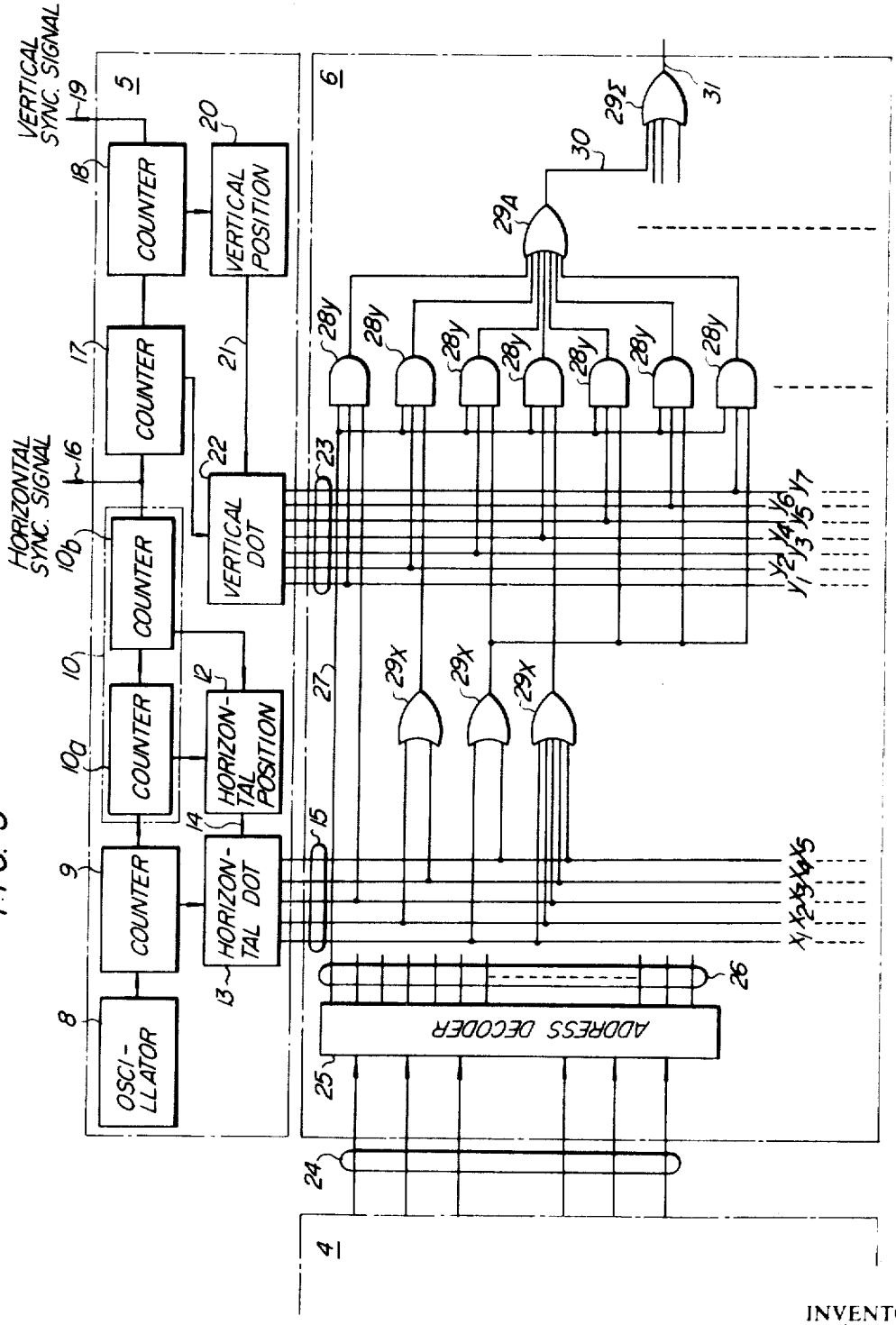

FIG. 3

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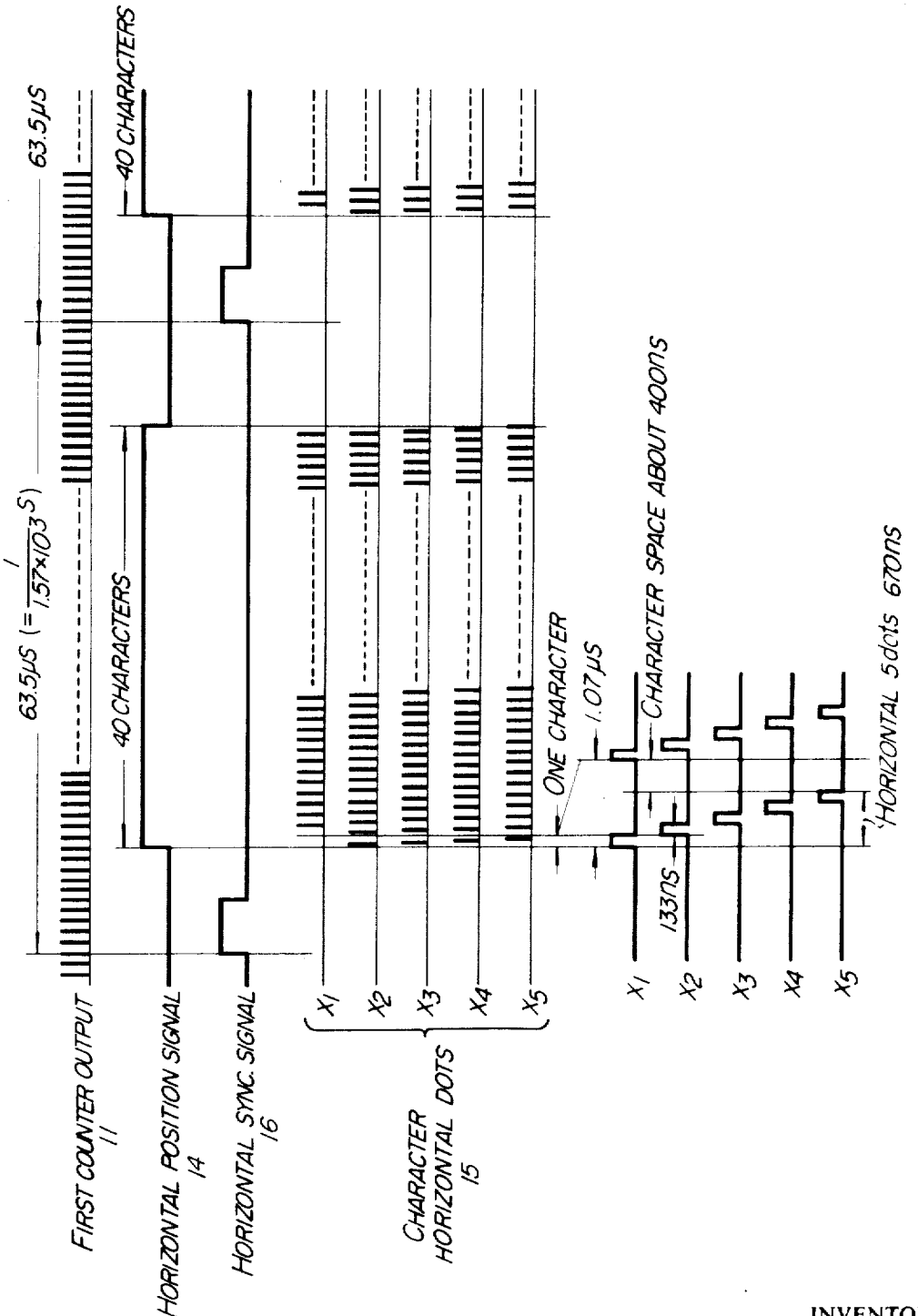

FIG. 4

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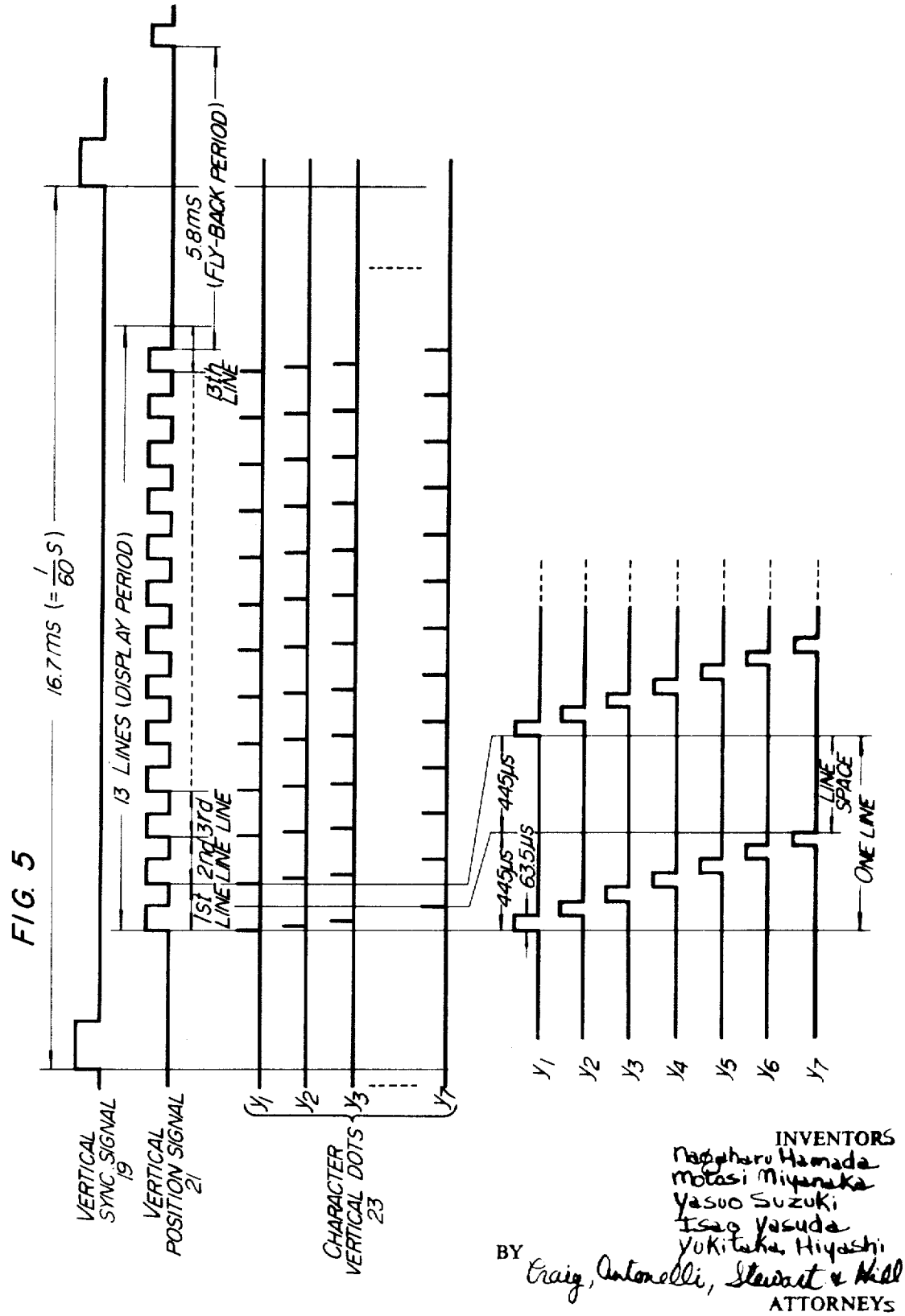

FIG. 5

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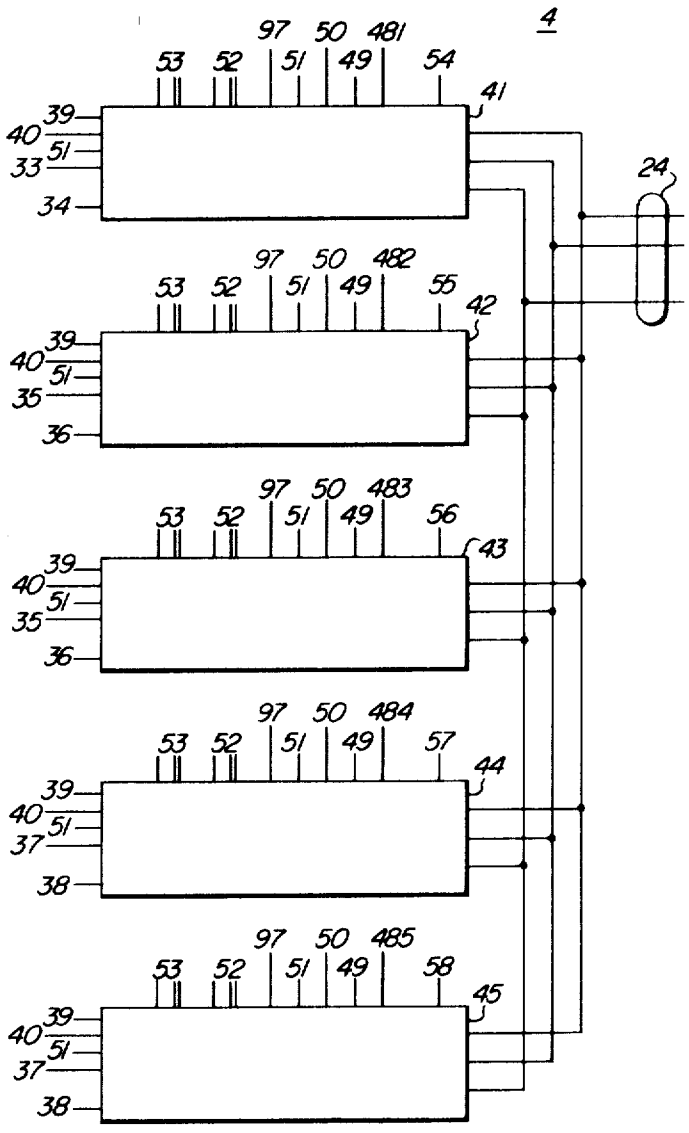
FIG. 6a



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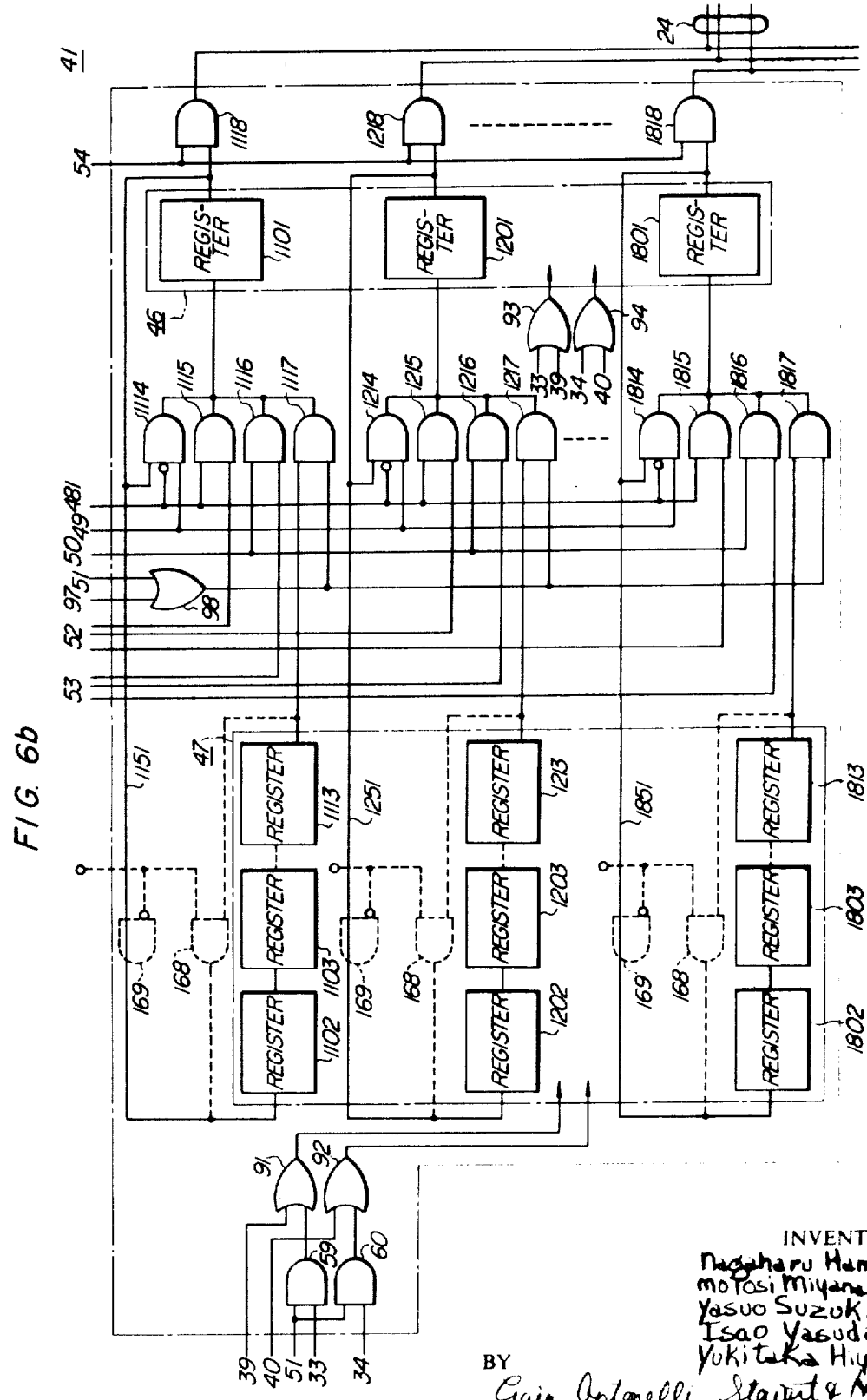

FIG. 6b

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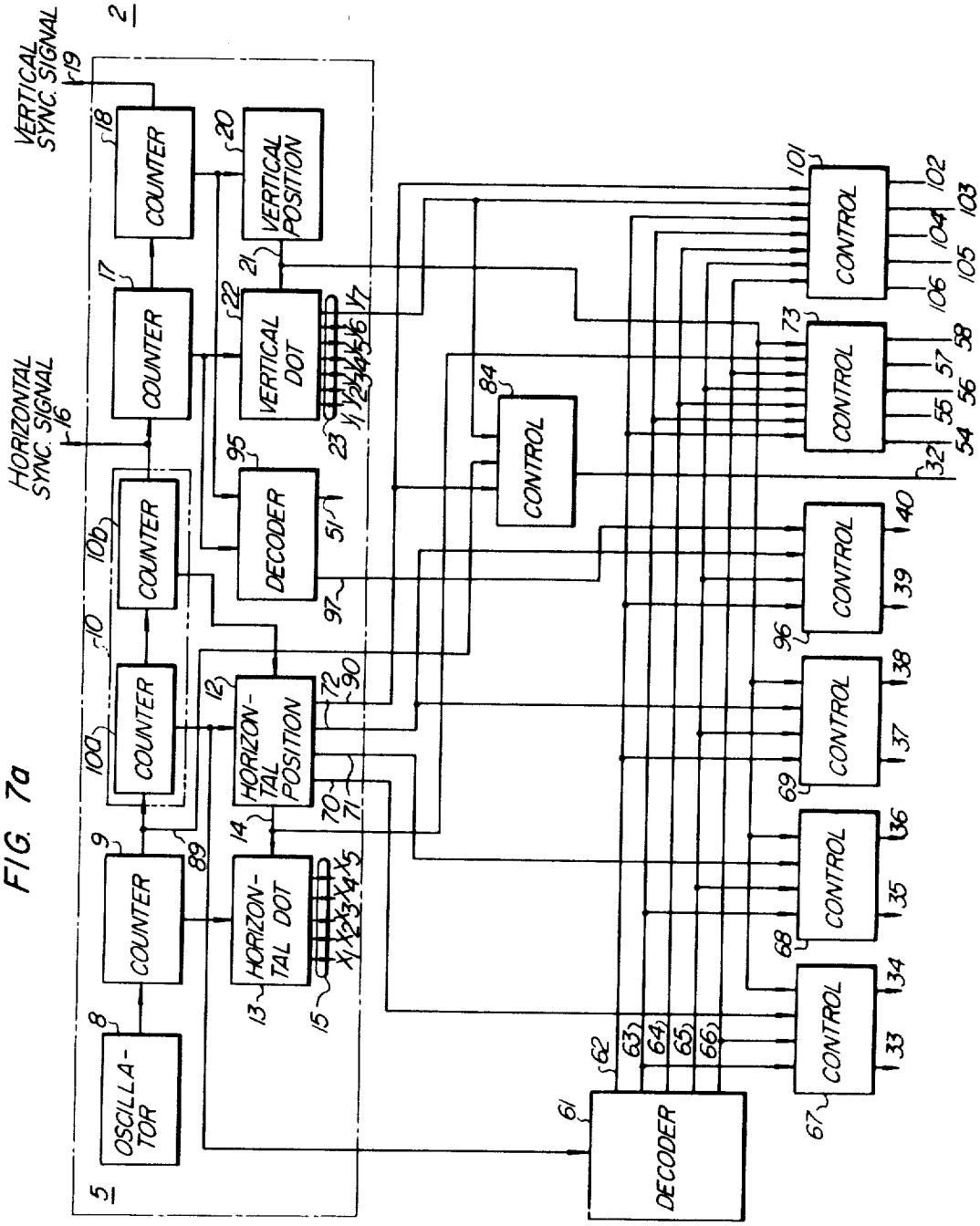

FIG. 7a

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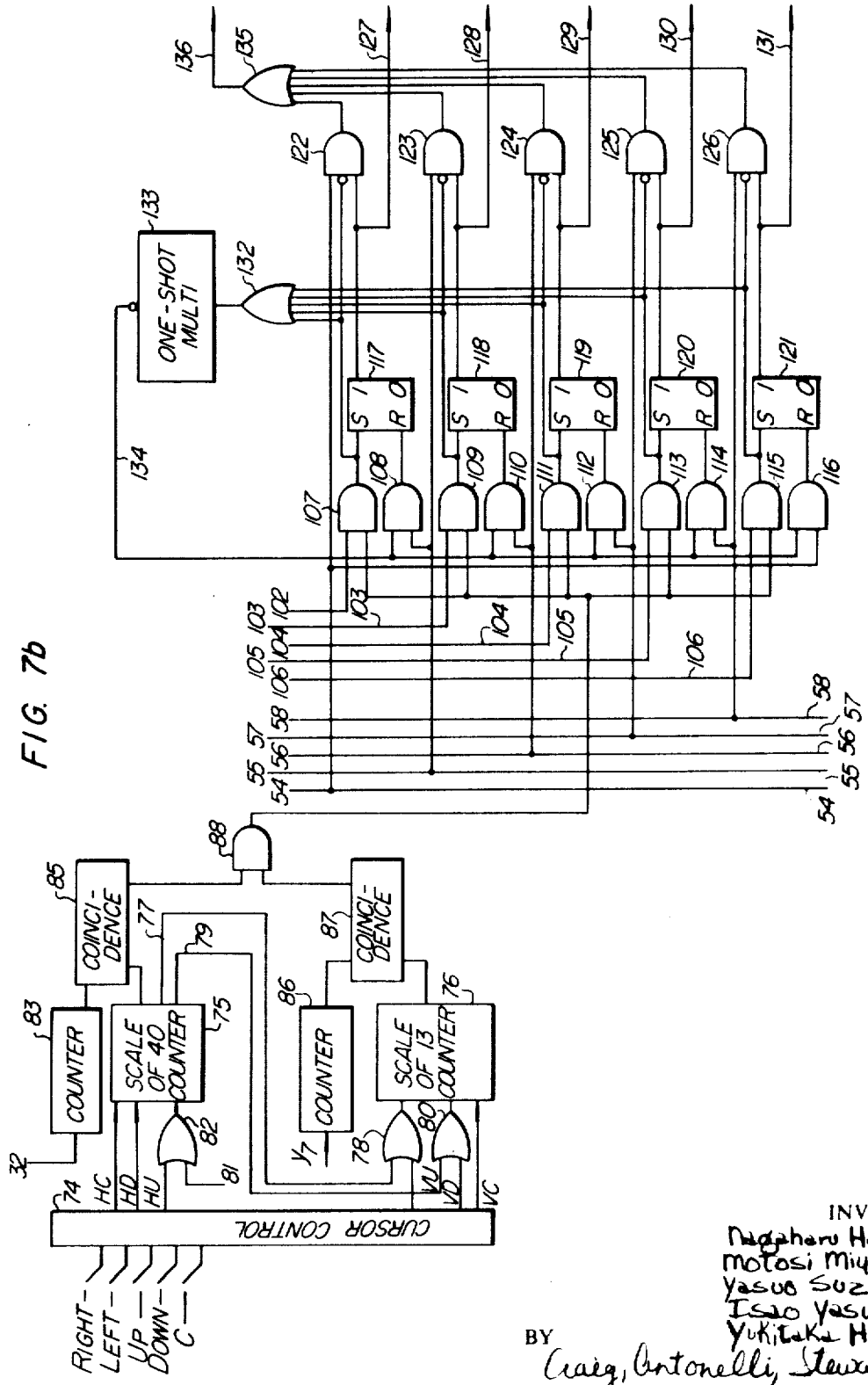

FIG. 7b

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FIG. 8a

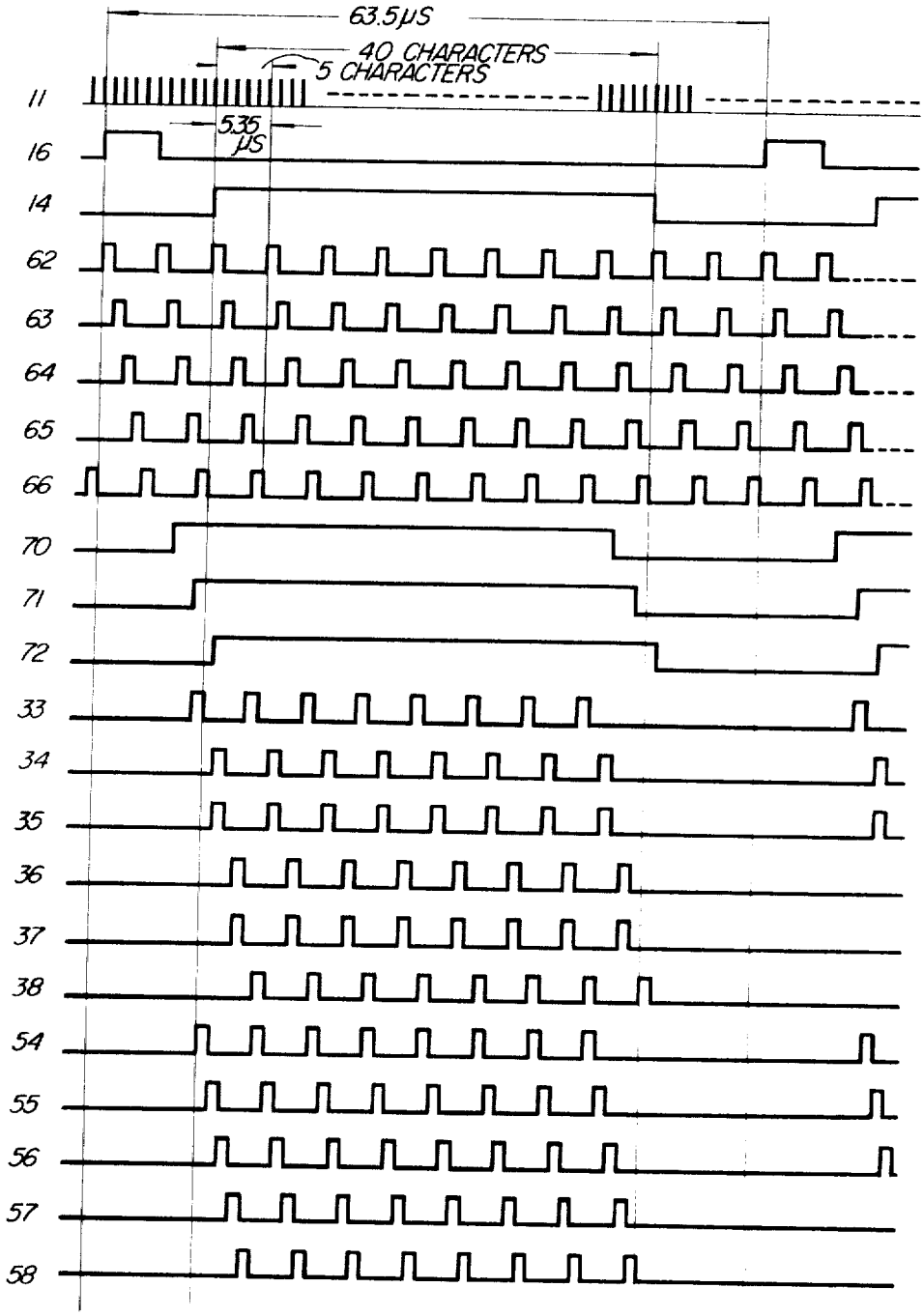

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FIG. 8b

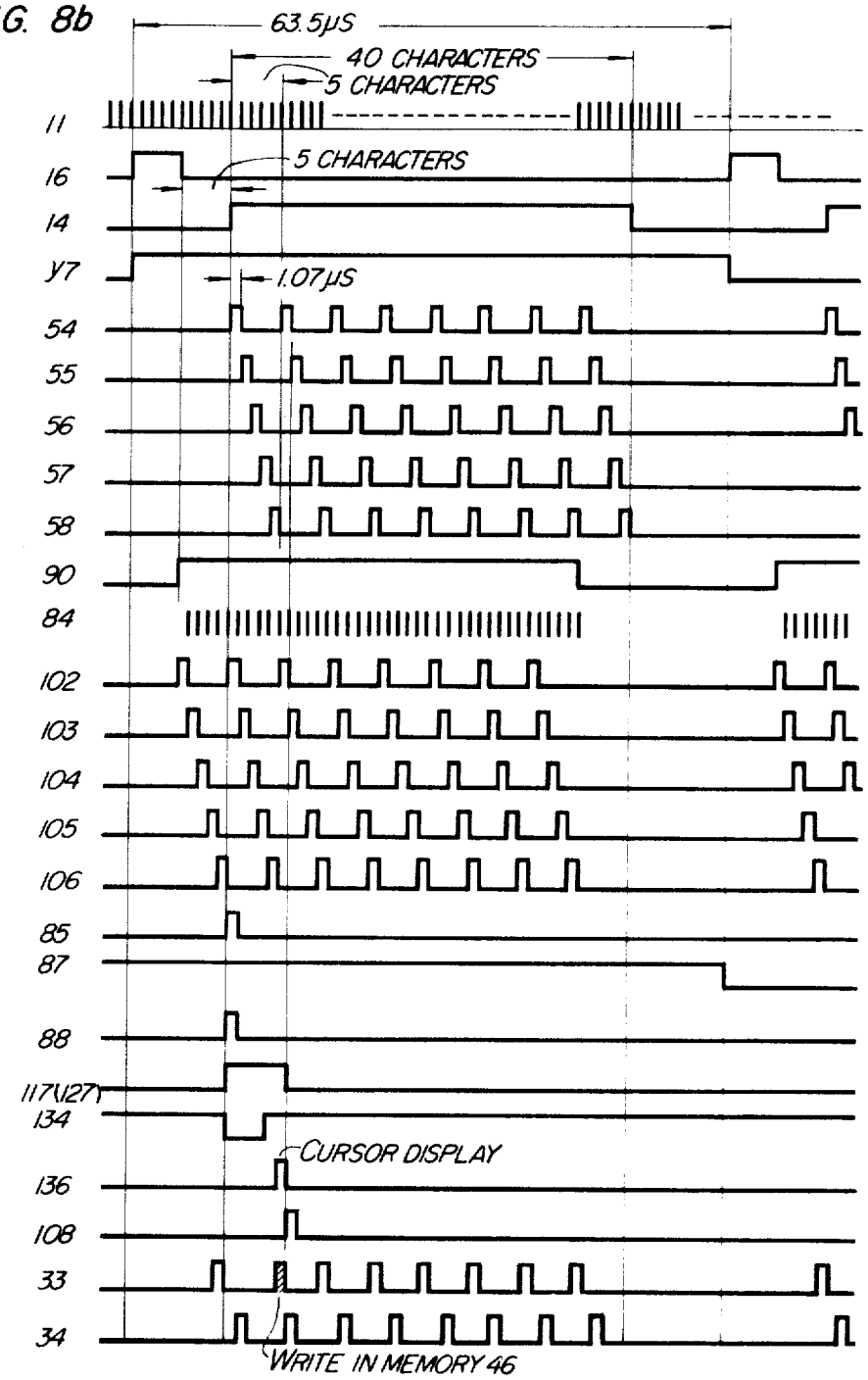

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FIG. 9

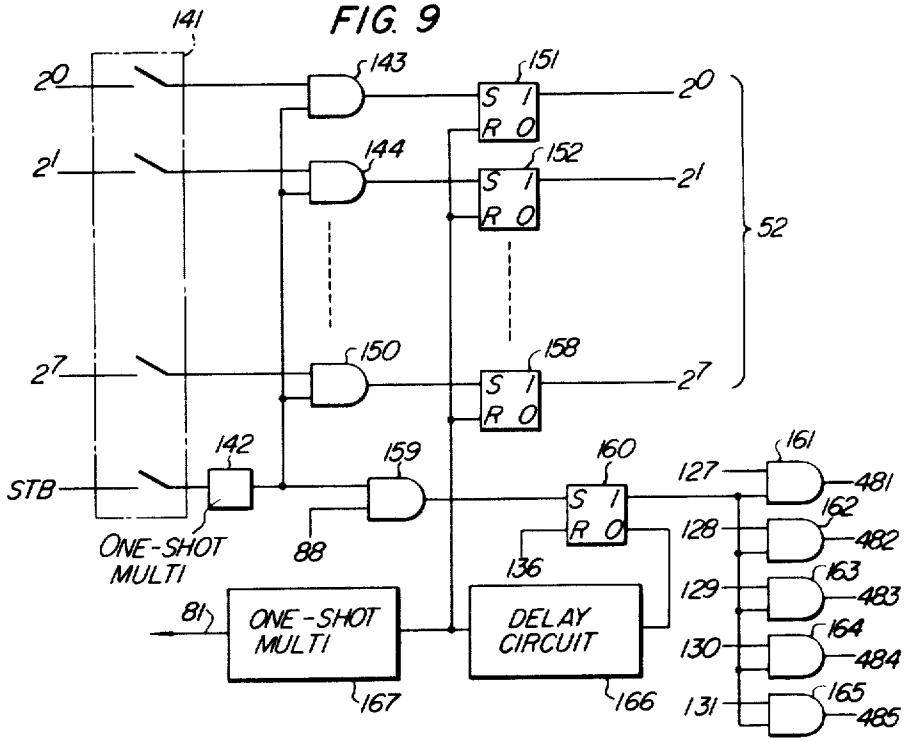

FIG. 10

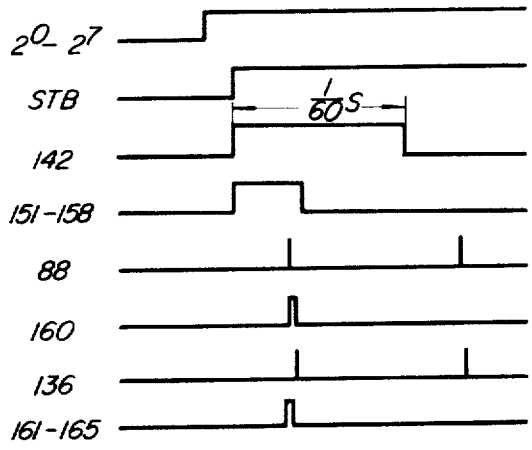

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FIG. 11

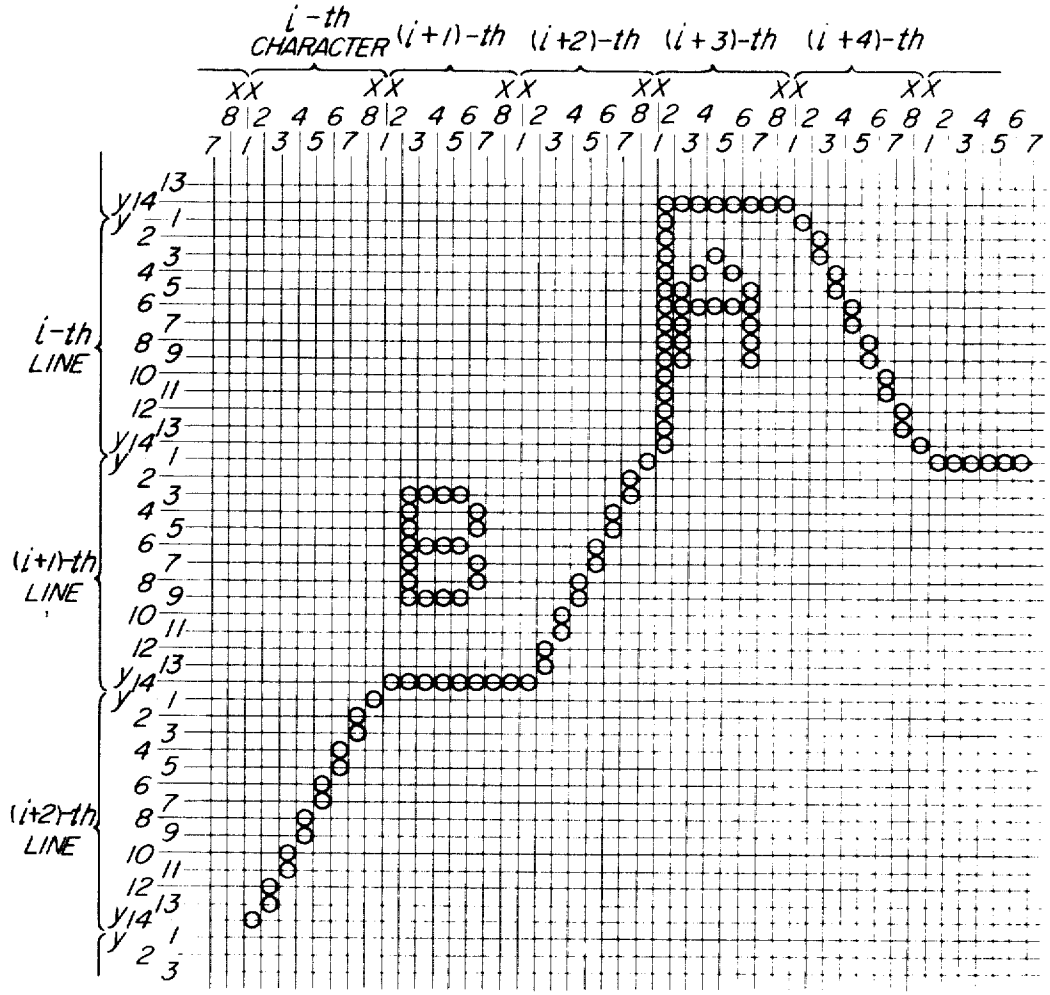

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FIG. 12a

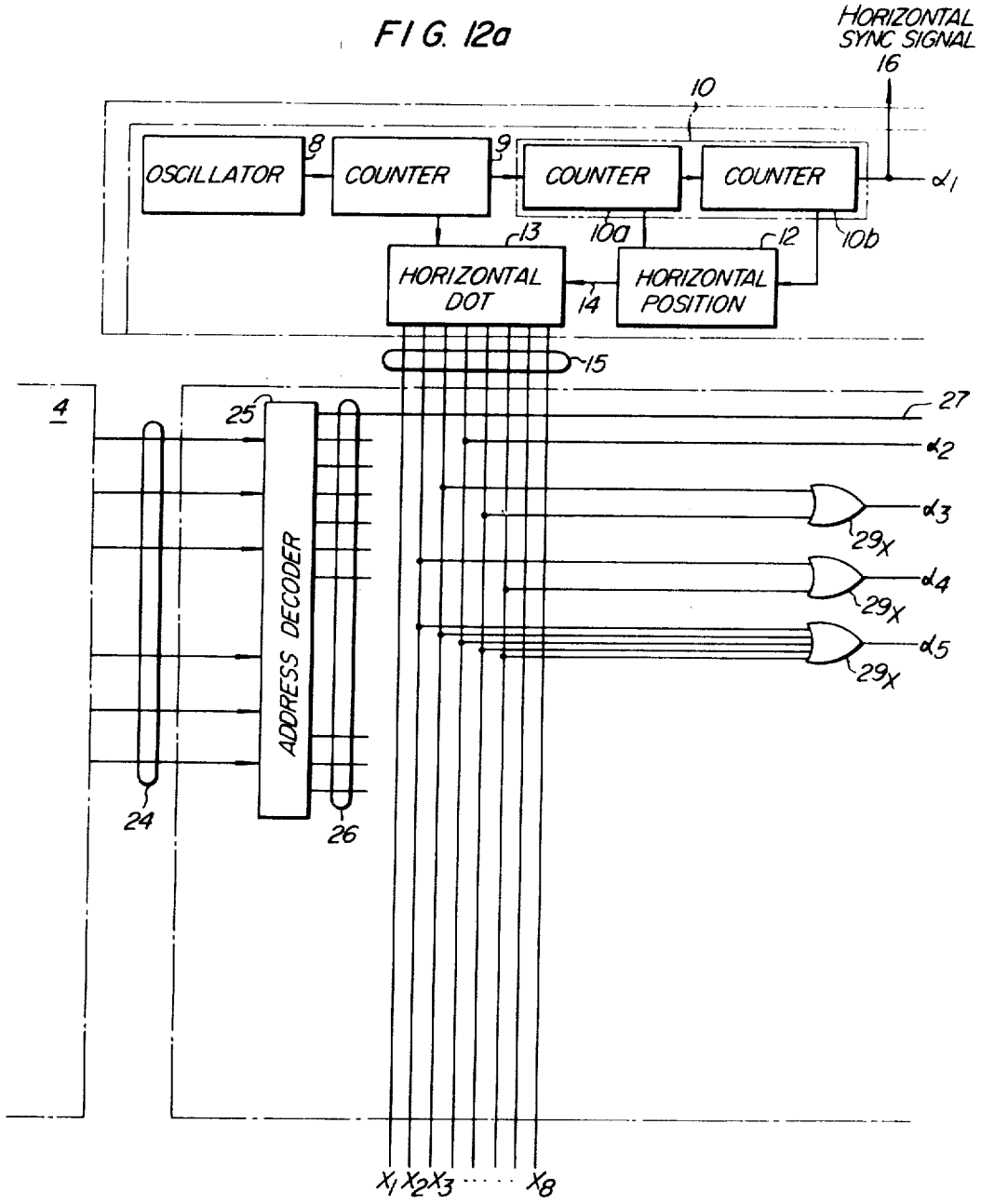

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FIG. 12b

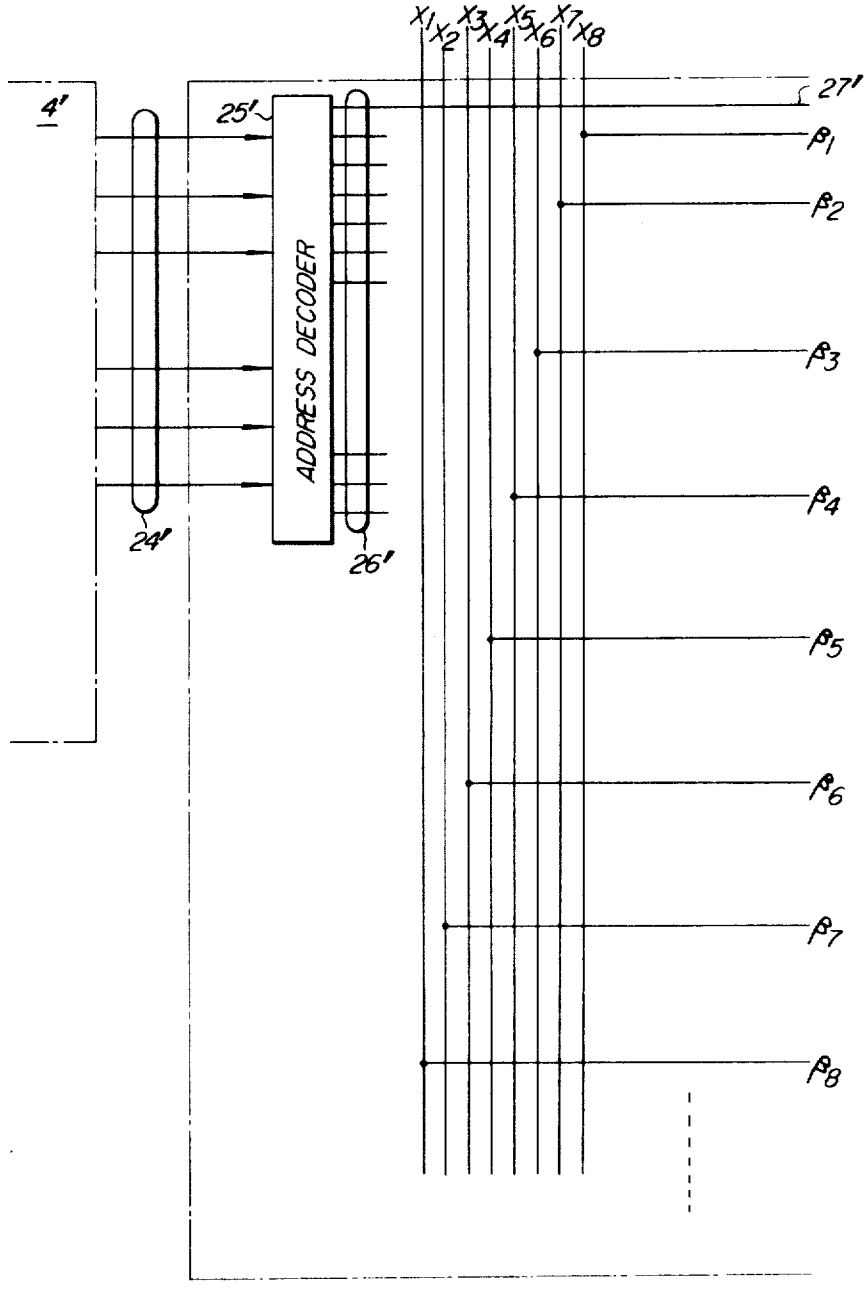

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FIG. 12c

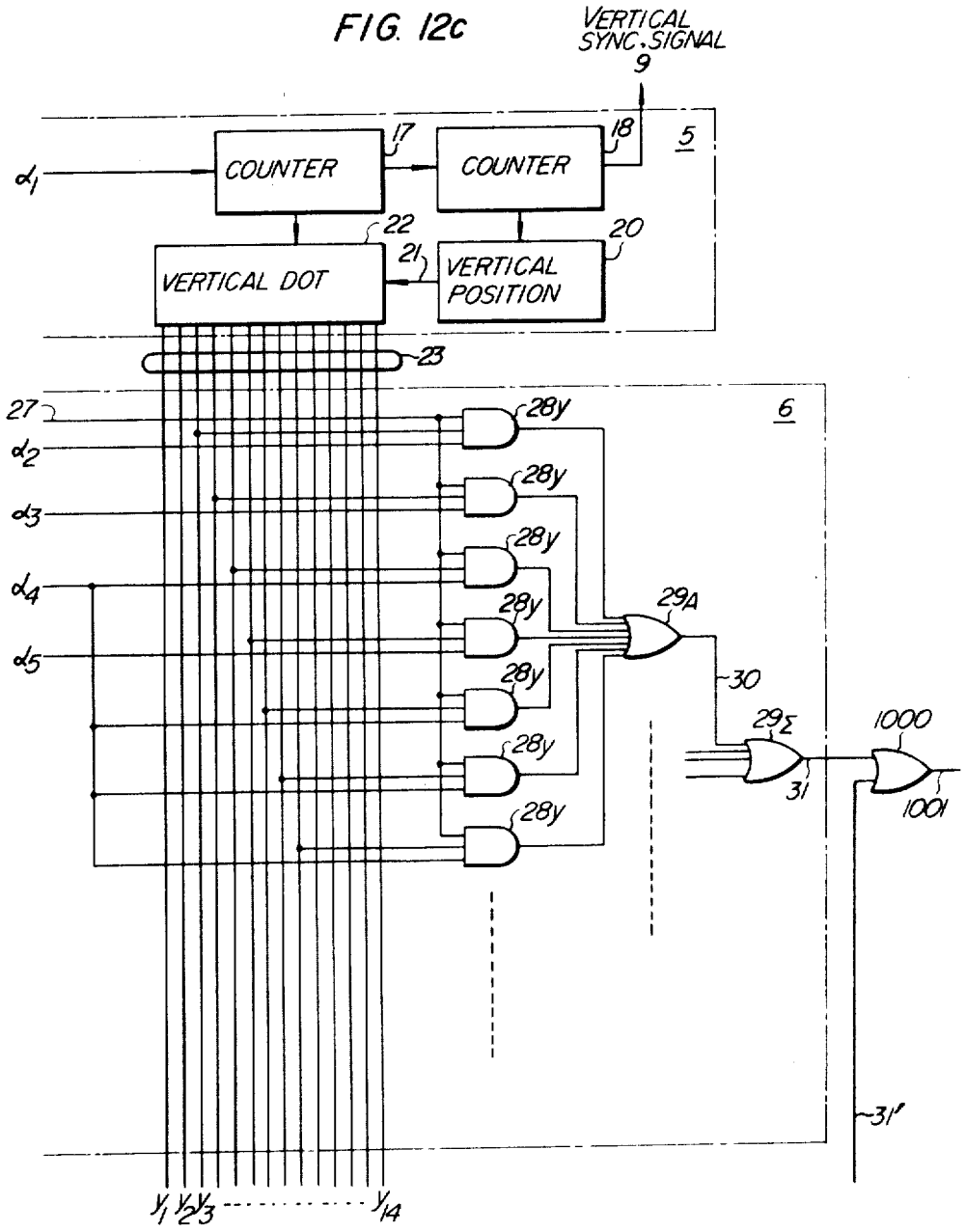

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FIG. 12d

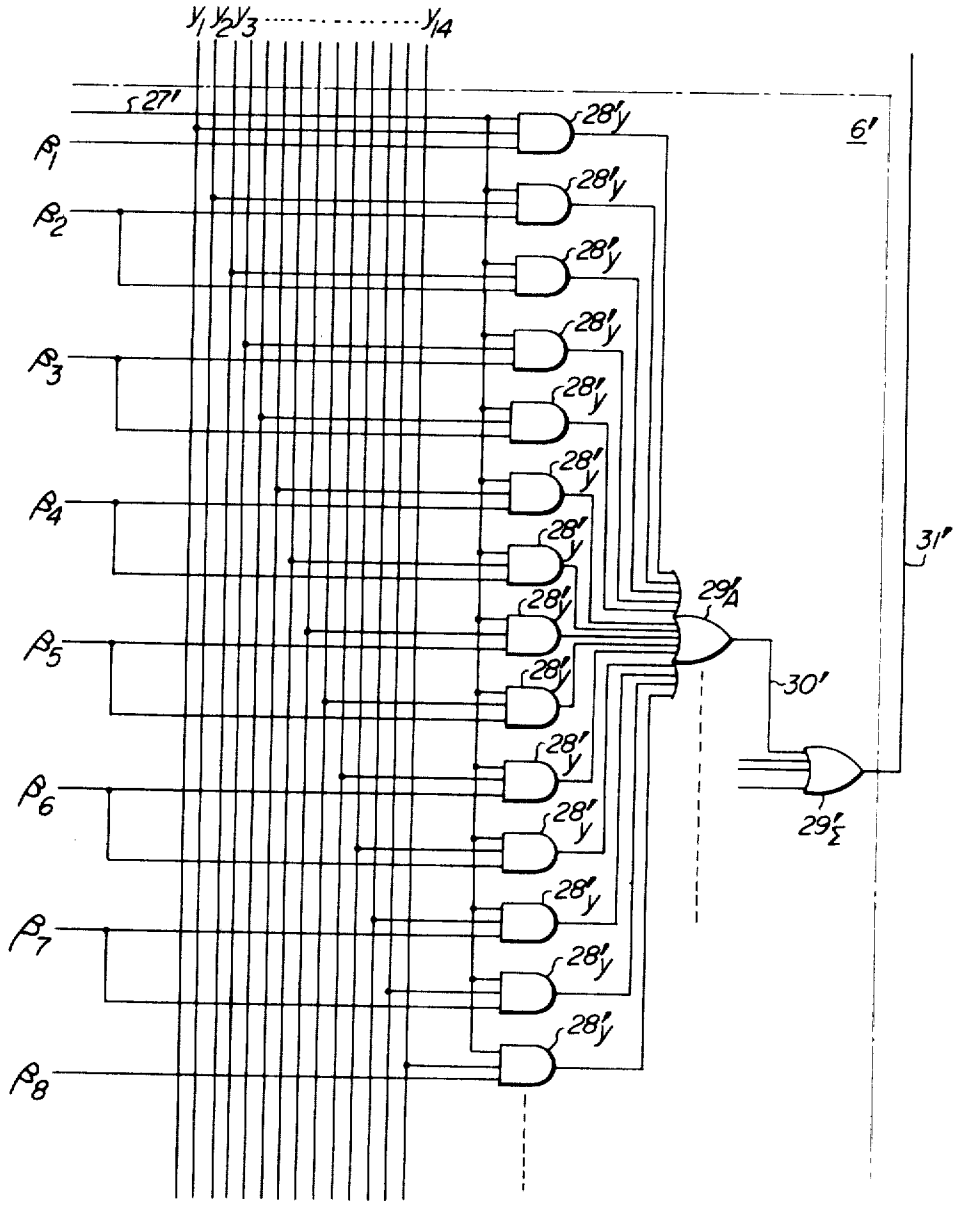

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FIG. 14

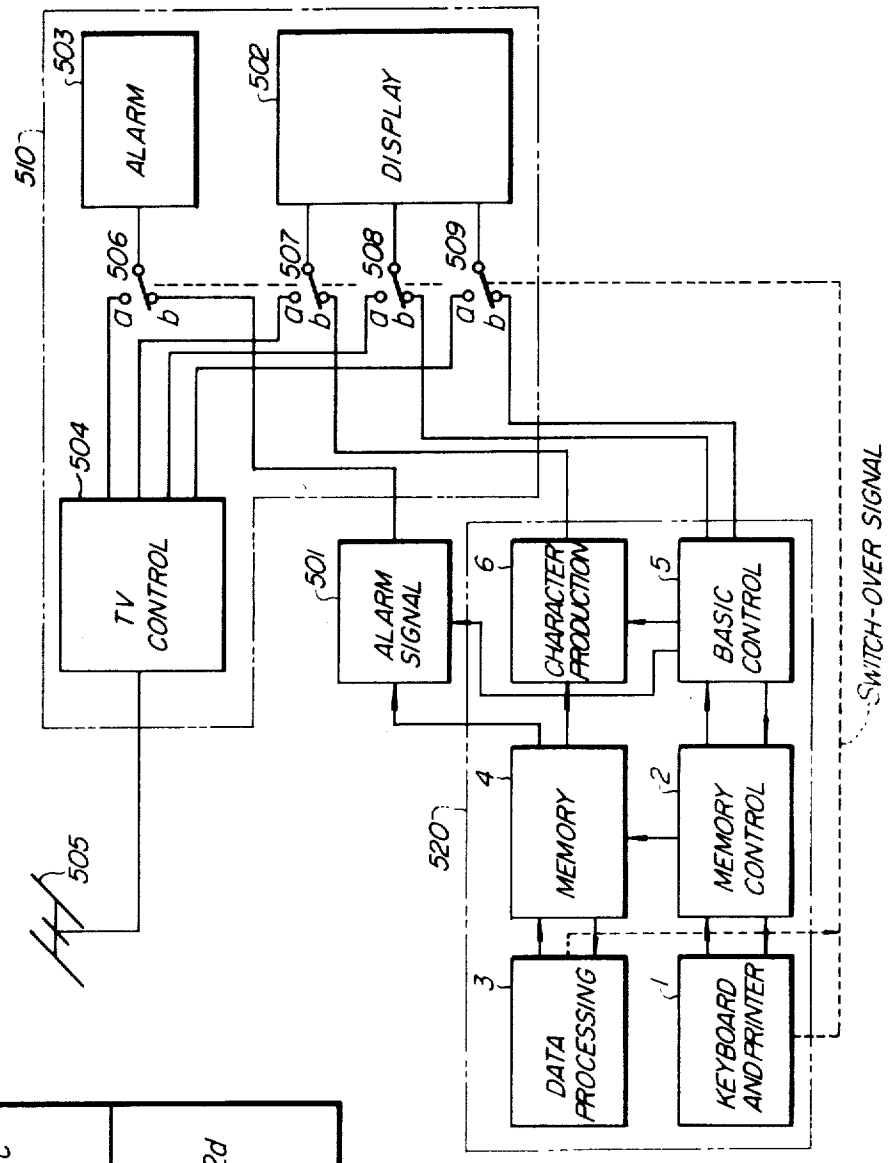
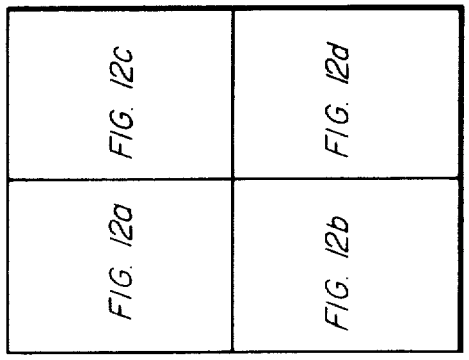


FIG. 13



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DISPLAY APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a display apparatus.

2. Description of the Prior Art

A remarkable increase in the amount of information handled by electronic computers is seen as the size of electronic computers becomes larger, and therefore it is desired to simplify the means available for man-machine communication.

Various types of character display apparatus, pattern display apparatus and the like have been developed and some of them have been disclosed, for example, in the Japanese magazine "Fuji" Vol. 12, No. 4 and the Japanese magazine "OHM" Feb. 1968.

However, the known apparatus of this kind are relatively costly and involve economical problems. Thus, it is the present practice that the apparatus of this kind is not so popularly used as to match the increase in the amount of information in spite of the emphasis placed on the necessity for such apparatus. These problems mainly arise from the fact that the apparatus employ a special cathode-ray tube in the display section which includes a complex control circuit. Therefore, the appearance of an economical display apparatus employing a cathode-ray tube commonly used in commercial television sets and an inexpensive control circuit are strongly required.

SUMMARY OF THE INVENTION

The present invention proposes a display apparatus in which intensity modulation is applied to scanning lines of a cathode-ray tube with suitable timing so as to display a character, symbol or pattern by an assembly of bright spots or dots, that is, by a suitable combination of horizontal and vertical dots. According to the present invention, the display section may merely consist of a television receiver of the standard television system, and circulating memories, such as delay line memories or dynamic shift registers, are employed in the control circuit to obtain an inexpensive display apparatus.

It is a primary object of the present invention to provide an inexpensive and highly reliable display apparatus.

Another object of the present invention is to provide a display apparatus which can display patterns including a graph in spite of a very small memory capacity.

Other objects, features and advantages of the present invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating the basic principle of the present invention.

FIG. 2 is a block diagram showing the basic structure of the present invention.

FIG. 3 is a block diagram for the explanation of a basic control circuit and a character-generating circuit in an embodiment of the present invention.

FIGS. 4 and 5 show a time chart for the explanation operation of the circuits shown in FIG. 3.

FIG. 6*a* is a block diagram showing the structure of a memory 4 in the embodiment of the present invention.

FIG. 6*b* is a circuit diagram of one of the blocks shown in FIG. 6*a*.

FIGS. 7*a* and 7*b* are block diagrams respectively showing the structure of a memory control circuit and a cursor control circuit in the embodiment of the present invention.

FIGS. 8*a* and 8*b* show a time chart for the explanation of the operation of the memory control and cursor control.

FIG. 9 is a block diagram showing the structure of a circuit for writing data from a keyboard in the memory in the embodiment of the present invention.

FIG. 10 shows a time chart for the explanation of operation of the circuit shown in FIG. 9.

FIG. 11 is a diagram illustrating how a pattern and a character are simultaneously displayed by the present invention.

FIGS. 12*a* through 12*d* illustrate a circuit diagram of another embodiment of the present invention for effecting a display as shown in FIG. 11.

FIG. 13 is a view showing the relation between FIGS. 12*a*, 12*b*, 12*c* and 12*d*.

FIG. 14 is a block diagram showing a practical example comprising a combination of a display apparatus and a television receiver.

FIG. 15 shows a time chart for the explanation of write-in operation with a high-speed shift register.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described with regard to an example in which a television receiver of the standard television system (horizontal synchronizing frequency of 15.75 kHz. and vertical synchronizing frequency of 60 Hz. commonly used in Japan and the United States is utilized in the display section of the display apparatus according to the present invention.

FIG. 1 is a diagram illustrating the basic principle of the present invention. FIG. 1*a* shows diagrammatically a part of the display on the screen of a cathode-ray tube. In FIG. 1*a*, y_1, y_2,–,ay_{14}, y_1, y_2,–represent the scanning lines running across the face of a cathode-ray tube in the horizontal direction (flyback lines are not shown herein), while x_1, x_2,–, x_8, x_1, x_2,– represent the timing for applying intensity modulation to the scanning lines. It will be seen from FIG. 1*a* that, in accordance with the present invention, intensity modulation is applied to the rasters with suitable timing so as to display a character, symbol or pattern by an assembly of bright spots or dots. Thus, special deflection circuits are not required for the display and a television receiver of the standard television system can be utilized. In accordance with the present invention, the video signal corresponding to the respective raster may be controlled in a manner as seen in FIG. 1*b* so that they can display a specific character or symbol. In the case of FIG. 1, 14 rasters are allotted to one line of a character or symbol to be displayed, with 7 rasters being used for display and the remaining rasters are used to provide a space between lines, while in the horizontal direction, eight dots are allotted, with five dots used for display and the remaining dots used to provide a space between characters or symbols. According to this example, therefore, any desired character or symbol can be displayed by the combination of 35 dots consisting of five horizontal dots and seven vertical dots.

Referring to FIG. 2 which is a block diagram showing the basic structure of the present invention, the display apparatus comprises a keyboard and printer unit 1, a memory control circuit 2, a data processing unit 3 such as a computer or data logger, a memory 4, a basic control circuit 5, a character-generating circuit 6 and a display unit 7. The keyboard and printer unit 1 writes in desired characters or symbols and prints displayed characters or symbols for preservation. The memory control circuit 2 controls the acceptance and delivery of data between the keyboard and printer unit 1, the computer 3 and the memory 4 and readout of data from the memory 4 for delivery to the character-generating circuit 6 for the sake of display. The memory 4 stores the code of the characters to be displayed on the screen and effects readout and write-in of data under the control of the memory control circuit 2. The basic control circuit 5 produces the horizontal and vertical synchronizing signals to be applied to the display unit 7, and at the same time, applies signals designating the position of the characters, space between characters and space between lines to the character-generating circuit 6 and memory control circuit 2. The character-generating circuit 6 generates a video signal according to the timing designated by the basic control circuit 5 on the basis of the code supplied from the memory 4 and delivers the video signal to the display unit 7. The display unit 7 displays a character or symbol on the face of a cathode-ray tube when it receives the video signal described above and the synchronizing signals supplied from the basic control circuit 5. A display apparatus having a plurality of input units

(keyboards 1) and output units (display units 7) capable of making a plurality of displays may be provided in which a memory control circuit 2, a data processing unit 3 and a basic control circuit 5 may be provided in common to all the input and output units and a plurality of keyboards 1, memories 4, character-generating circuits 6 and display units 7 may be simultaneously controlled.

In an embodiment of the present invention which will be described hereunder, MOS dynamic shift registers having a relatively slow operating speed, for example, having a shift pulse frequency of the order of 200 kHz. at the maximum and 1 kHz. at the minimum are employed to form the memory. In the case of characters or symbols, one line includes 40 characters and one frame includes 13 lines making a total of 520 characters or symbols per frame at the maximum, and each character or symbol consists of a combination of five horizontal dots and seven vertical dots or seven rasters. In the case of graphs, vector display is given by a combination of eight horizontal dots and 14 vertical dots in each unit area.

In order than an MOS dynamic shift register can be employed as the memory, special attention must be given to the following points:

I. In order to display 40 characters on one line, the character code supplied to the character-generating circuit must be renewed about every 1 μs. (Refer to FIG. 4.)

II. In order to complete one character or symbol, the same character or symbol code must be repeatedly supplied to the same place for seven vertical dots, that is, seven rasters y_1, y_2,–, y_7. (Refer to FIG. 1.)

III. The memory must not vanish during the flyback period which is 5.8 ms. in the illustrated embodiment, that is, until the first raster in the first line of the next frame is displayed after the last raster in the last line of the preceding frame has been displayed.

Such a problem would still arise whatever circulating memory may be employed. For example, the use of a dynamic shift register of higher speed will facilitate the countermeasure against the point (I), but the countermeasure against the point (III) will become much more troublesome than in the present embodiment. The countermeasures employed in the embodiment of the present invention will be described with reference to the drawings. At first, fundamental means for displaying characters or symbols will be described.

FIG. 3 is a block diagram of the basic control circuit 5 and character-generating circuit 6. FIGS. 4 and 5 show a time chart for the explanation of the timing for the respective circuits shown in FIG. 3.

The basic control circuit 5 comprises a master oscillator 8, a first counter 9, a second counter 10, a third counter 17, a fourth counter 18, a character horizontal position-designating circuit 12, a character horizontal dot-producting circuit 13, a character vertical position-designating circuit 20 and a character vertical dot-producing circuit 22. In the present invention, it is convenient that the outputs from the second counter 10 and fourth counter 18 may readily be utilized as the horizontal synchronizing signal and vertical synchronizing signal, respectively. At the same time, the size and shape of a character to be displayed are determined by the oscillating frequency of the master oscillator 8 as well as by the first and third counter 9 and 17. Thus, the constants of these elements are suitably selected taking the above into consideration. The master oscillator 8 has an oscillation frequency of 7.5 MHz. The first counter 9, second counter 10, third counter 17 and fourth counter 18 are herein an octonal counter, a divide-by-60 counter, a divide-by-14 counter and a divide-by-19 counter, respectively. For the convenience of control which will be described later, the second counter 10 consists of a quinary counter 10_a and a divide-by-12 counter 10_b connected in cascade. Therefore, outputs 16 and 19 from the second counter 10 and fourth counter 18 have respective frequencies of the order of 15.7 kHz. and 60 Hz. so that they can be utilized as the horizontal and vertical synchronizing signals.

The character horizontal dot-producing circuit 13 decodes the output from the first counter 9 to deliver a pulse output with respective timings x_1, x_2,–, x_5 as shown in FIG. 4. The circuit 13 delivers its output to a lead group 15 only when the horizontal character position-designating circuit 12 which designated the horizontal display position on the face of the cathode-ray tube delivers its output as a result of decoding of the output from the second counter 10. Of course, it is so selected that the circuit 12 delivers its output in the period in which the rasters scan a central portion (horizontal direction) of the cathode-ray tube as shown in FIG. 4. The vertical character dot-producing circuit 22 decodes the output from the third counter 17 and delivers a pulse output with respective timings y_1, y_2,–, y_7 as shown in FIG. 5. The circuit 22 delivers its output to a lead group 23 only when the vertical character position-designating circuit 20 which designates the vertical display position on the face of the cathode-ray tube delivers its output as a result of the decoding of the output from the fourth counter 18. Of course, it is so selected that the circuit 20 delivers its output in the period in which the rasters scan a central portion (vertical direction) of the cathode-ray tube as shown in FIG. 5. Thus, a desired character or symbol can be displayed when the screen is disposed at a desired position on the face of the cathode-ray tube and the horizontal dots and vertical dots are suitably combined depending on the character or symbol to be displayed.

In the character-generating circuit 6, the horizontal dots x and vertical dots y supplied to the respective lead groups 15 and 23 are suitably combined to constitute a desired character. Generation of a character A will be described with reference to FIG. 3. As apparent from reference to FIG. 1, the character A can be formed by applying intensity modulation to the rasters y_1, y_2, y_3,–, y_7 with predetermined timings x_3, x_2 and x_4, x_1 and x_5,–, x_1 and x_5, respectively. AND-gates 28_y and OR-gates 29_x are provided to combine the x-dots and y-dots in the above relationship. Further, a timing signal is applied to the AND-gates 28_y by way of a lead 27 so as to regulate the time at which the above combination is to be delivered as an output. In other words, since the combination of the x-dots and y-dots holds independently of the existing position of the raster, it is necessary to open the AND-gates 28_y with suitable timing depending on the position of the raster. Suppose, for example, that the rasters appear on the first line in FIG. 1. In such a case, the timing signal may be applied to the AND-gates 28_y by way of the lead 27 only from time t_1 to t_2 for the raster y_1, from time t_1 to time t_2 for the raster y_2,–, and from time t_1 to time t_2 for the raster y_7 so as to display the character A on a predetermined position of the first line. An OR-gate 29_A receives outputs from the AND-gates $28y$ and delivers an output corresponding to the character A to its output lead 30. An OR-gate 29_Σ receives outputs from OR gates (including those not shown) corresponding to individual characters or symbols, and thus a composite video signal for each raster as shown in FIG. 1b appears on an output lead 31. A character address decoder 25 decodes data supplied from the memory 4 by way of a lead group 24, selects a character, and delivers an output to a corresponding lead of a lead group 26. When, for example, a character A is selected, the character address decoder 25 delivers an output to the lead 27.

FIG. 6a is a block diagram showing the structure of the memory 4. FIG. 6b is a schematic circuit diagram of one of the above blocks (41). FIGS. 7a and 7b are block diagrams respectively showing the structure of the memory control circuit and cursor control circuit. FIGS. 8a and 8b show a time chart for the explanation of the operation of these circuits.

The memory 4 is composed of five blocks 41, 42, 43, 44 and 45. These blocks have a similar structure and the structure of the block 41 is only shown in detail. Each block comprises memory elements in the form of MOS dynamic shift registers having a memory capacity of eight bits. The present embodiment is adapted to display a character or symbol by a character code consisting of eight bits, and therefore eight MOS dynamic shift registers 1101, 1201,–, 1801 are disposed

in parallel so as to give a character code for displaying a character or symbol. A train of thirteen MOS dynamic shift registers are connected in cascade in each row as **1101, 1102,–, 1113, 1201, 1202,–, 1213,–, 1801, 1802,–, 1813.** The MOS dynamic shift register employed in this embodiment has a memory capacity of eight bits as described above, and eight bits are used for one word which give a character code for one character as will be apparent from the later description. Thus, one block has a memory capacity of 13×8=104 characters and the five blocks have a total memory capacity of 104×5=520 characters to be displayed on the screen.

In each block, these registers are divided into a buffer memory **46** and a main memory **47** which are connected to each other by groups of gates **1114, 1115,–, 1117, 1214, 1215,–, 1217, 1814, 1815,–, 1817.** The output from the buffer memory **46** is delivered to the character address decoder **25** through gates **1118, 1218,–, 1818** described later. The buffer memory **46** has circulating routes **1151, 1251,–, 1851** to the main memory **47.** The gates **1114, 1214,–, 1814** are opened when control signals **481, 482,–, 485** indicating the write-in by the keyboard do not appear and when a control signal **49** is supplied during the period of appearance of the rasters y_1, y_2,–, y_7, thereby circulating the memory contained in the registers **1101, 1201,–, 1801.** The gates **1115, 1215,–, 1815** are opened when the control signals **481, 481,–, 485** indicating the write-in by the keyboard appear, and introduce new data **52** supplied from the keyboard into the registers **1101, 1201,–, 1801** to rewrite the memory contained therein. The gates **1116, 1216,–, 1816** are opened when the computer **3** supplies a control signal **50,** and introduce new data **53** supplied from the computer **3** into the registers **1101, 1201,–, 1801** to rewrite the memory contained therein. The gates **1117, 1217,–, 1817** are opened in response to the application of a control signal **51** that is supplied during the display period (FIG. **5**) in which a raster, for example, y_8 which is not directly utilized for display appears, thereby replacing the memory contained in the buffer memory **46** by the memory contained in the main memory **47.** In other words, the memories contained in the registers connected in cascade are circulated by eight bits. During the flyback period (refer to FIG. **5**), a suitable raster is selected so that the memories may not vanish.

A control signal **97** is supplied when such a scanning line appears to open the gates **1117, 1217,–, 1817** so as to circulate all the date in the memories a predetermined number of times.

Shift pulses for successively transferring the data (memory contents) to be displayed during the display period and shift pulses for circulating the data so as not to erase the memory contents or the registers during the flyback period are supplied to the blocks **41, 42, 43, 44** and **45.** The former shift pulses are designated by **33, 34; 35, 36;** and **37, 38,** while the latter shift pulses are designated by **39** and **40.** During the display period, the shift pulses **33, 34; 35, 36;** and **37, 38** (having a pulse interval of 5 μs. corresponding to the highest operating speed of the shift register employed in this embodiment) are continuously supplied to the buffer memories **46** to renew the character code. However, the shift pulses **33, 34; 35, 36;** and **37, 38** are supplied to the main memories **47** only when gates **59** and **60** are opened in response to the application of the control signal **51.** Reference numerals **91, 92, 93** and **94** designate OR gates. It will be understood that the shift pulses **39** and **40** supplied during the flyback period are simultaneously applied to the buffer memories **46** and main memories **47.** Reference numerals **1118, 1218,–, 1818** designates gates for leading the memory output to the outside. The outputs from the registers **1101, 1201,–, 1801** are delivered to a lead group **24** in response to the appearance of control signals **54, 55, 56, 57** and **58.** The control signals **54, 55, 56, 57** and **58** applied to the respective blocks are out of phase relative to one another, have a pulse width of about 1 μs. as shown in FIG. **8** and are applied at intervals of about 5 μs. Thus, the address supplied to the address decoder **25** is renewed every 1 μs.

Referring next to FIGS. **7** through **10,** timing control signals for the memory **4,** renewal of data and control of cursor will be described. The term "cursor" is used to denote a bright line—appearing on the *i*-th line in FIG. **1,** and the cursor is used to designate a place in which data is to be newly put and a place from which data to be renewed is derived.

At first, the display of characters will be described. A decoder **61** receives the output from the quinary counter **10***a* and delivers five trains of pulses **62, 63, 64, 65** and **66** having a recurrent frequency of 200 kHz. Shift pulse control circuits **67, 68** and **69** for obtaining the shift pulses to be applied during the display period act to suitably combine the pulse trains to deliver two trains of pulses conveniently used for the shifting of the MOS dynamic shift registers. The five trains of pulses are combined with suitable timing so as to avoid the hazard of opening and closure of the gates **1118, 1218,–, 1818** by the control signals **54, 55,–, 58,** that is, to supply the control signals at a time at which the shifting of data in the registers has been completed and the data is completely established. Control signals **70, 71** and **72** from the horizontal position-designating circuit **12** and a control signal **21** from the vertical position-designating circuit **20** are further applied to these circuits **67, 68** and **69** so as to limit the period of delivery of the shift pulses **33, 34; 35, 36;** and **37, 38** to the display period and to control the timing of their delivery. The control signals **70, 71** and **72** have a timing as shown in FIG. **8***a*.

A decoder **95** receives the outputs from the third and fourth counters **17** and **18** so as to deliver the control signal **51** during the display period and when the raster y_8 is scanned. At the same time, the decoder **95** delivers the control signal **97** 26 times which signal appears at suitable intervals during the flyback period and lasts for a period of time during which one raster is scanned. The number of times described above must be *n* times the number of the MOS dynamic shift registers connected in cascade, where *n* is an integer. A circulating shift pulse control circuit **96** receives the control signals **97** and **72** and permits passage therethrough of the pulse trains **62** and **65** when both the control signals **97** and **72** appear so as to deliver the two pulse trains **39** and **40** therefrom.

In the presence of the control signal **97,** a gate signal is applied to the gates **1117, 1217,–, 1817** through the OR-gates **98** so as to circulate the memory contents of the registers and to prevent the memory contents of the registers from being lost during the flyback period.

The control signals **54, 55, 56, 57** and **58** used for the delivery of an output from the memory **4** are delivered from a control circuit **73** which receives the five pulse trains **62, 63, 64, 65** and **66** supplied from the decoder **61** and the outputs **14** and **21** from the horizontal and vertical position-designating circuits **12** and **20.** Thus, as apparent from reference to FIG. **8***a*, character codes of eight bits corresponding to characters or symbols to be displayed by the horizontal rasters y_1, y_2,–, y_7 are supplied from the blocks **41, 42, 43, 44** and **45** to the output lead group **24** of the memory **4.**

Cursor control will next be described. A cursor control circuit **74** generates a horizontal carry-forward pulse HU (shift to the right by one character), a horizontal carry-backward pulse HD (shift to the left by one character), a reset pulse HC (shift to the first character), a vertical carry-upward pulse VU (shift by one line upward), a vertical carry-downward pulse VD (shift by one line downward) and a reset pulse VC (shift to the first line) depending on the manipulation of cursor keys so that these pulses are supplied to a horizontal reversible counter **75** and a vertical reversible counter **76.** The counters **75** and **76** are a divide-by-40 counter and a divide-by-13 counter, respectively. When an overflow takes place in the counter **75,** an output apparatus on a lead **77** to be supplied through an OR-gate **78** to the counter **76** as an adding pulse (vertical carry-upward pulse VU), while when an underflow takes place in the counter **75,** an output appears on a lead **79** to be supplied through an OR-gate **80** to the counter **76** as a deducting pulse. A write-in finish pulse **81** described later is supplied through an OR-gate **82** to the counter **75** as an ad-

ding pulse. A horizontal cursor counter (divide-by-40 counter) **83** counts clock pulses supplied from a control circuit **84** described later. More precisely, the counter **83** detects the position of the cursor on a specific line. When the values counted by the counters **75** and **83** show a coincidence, a horizontal coincidence detection circuit **85** delivers an output. A vertical cursor counter (divide-by-13) **86** counts the rasters y_7 (output y_7 from the vertical dot-producing circuit **22**). More precisely, the counter **86** detects the specific line on which the cursor must be positioned. When the values counted by the counters **76** and **86** show a coincidence, a vertical coincidence detection circuit **87** delivers an output. An AND-gate **88** delivers an output when both the circuits **85** and **87** deliver their output. Accordingly, the appearance of an output from the AND-gate **88** means that the timing of the external cursor control coincides with the timing of the cursor display in the display circuit.

The control circuit **84** described above receives the output **89** from the first counter **9**, the control signal **90** delivered from the horizontal character position-designating circuit **12** and the output y_7 from the vertical dot-producing circuit **22** and permits passage therethrough of the output **89** when both the signal **90** and the output y_7 exist so as to supply the output **89** from the counter **9** to the counter **83** through line **32**. In the cursor control, it is necessary for the write-in of information in the memory to detect the presence of the cursor with a faster timing than when the cursor actually reaches the position on the screen. In view of the above, the control signal **90** is applied with a timing which precedes the control signal **14** designating the horizontal position by five characters as shown in FIG. **8***b*. Accordingly, when the AND-gate **88** delivers its output, the cursor is to be displayed at a time after the scanning line proceeds by five characters from then, and this may be utilized to write new data in a predetermined place in the buffer memory.

Control inputs to a control circuit **101** include the output **90** from the horizontal position designating circuit **12** and the output y_7 from the vertical dot-producing circuit **22** as in the case of the control circuit **84**. In the presence of both the inputs, the control circuit **101** permits passage therethrough of the five pulse trains **62**, **63**, **64**, **65** and **66**. Accordingly, control signals **102**, **103**, **104**, **105** and **106** delivered from the control circuit **101** have a timing which is preceded by five characters compared with the respective control signals **54**, **55**, **56**, **57** and **58** as shown in FIG. **8***b*. Reference numerals **107**, **108**,–, **116** designate AND-gates. Reference numerals **117**, **118**,–, **121** designate flip-flops. In each flip-flop, an output appears at its terminal **1** when a signal is applied from the associated AND-gate to its set terminal S and an output appears at its terminal **0** when a signal is applied from the associated AND-gate to its reset terminal R. Since the AND-gates **107**, **109**, **111**, **113** and **115** are supplied with the output from the AND-gate **88** and the respective control signals **102**, **103**, **104**, **105** and **106**, the flip-flops **117**, **118**,–, **121** are set with a timing faster by five characters than the cursor displayed on the screen. The flip-flops so set supply a signal input to INHIBIT-gates **122**, **123**,–, **126**, and at the same time, supply write-in control signals **127**, **128**,–, **131** to a write-in control circuit described later. The outputs from the gates **107**, **109**, **111**, **113** and **115** supplying the set signal to the flip-flops **117**, **118**,–, **121** are led also to an OR-gate **132** to trigger a one-shot multivibrator **133**. The delay time of the one-shot multivibrator **133** is set at about three characters and its output **134** is delivered from a NOT side terminal. The output **134** is supplied as an input to the AND-gates **108**, **110**, **112**, **114** and **116** which supply the reset signal to the flip-flops **117**, **118**,–, **121**. The control signals **55**, **56**, **57**, **58** and **54** are further supplied to the respective resetting gates **108**, **110**, **112**, **114** and **116**. In addition to the outputs from the flip-flops **117**, **118**,–, **121**, the INHIBIT-gates **122**, **123**,–, **126** are supplied with the control signals **54**, **55**,–, **58** as signal inputs and with the set signals (outputs from the gates **107**, **109**, **111**, **113** and **115**) for the flip-flops as inhibit inputs. Outputs from the INHIBIT-gates **122**, **123**,–, **126** are led to an OR-gate **135** to be derived from the latter as a cursor display signal **136**.

In the lower portion of FIG. **8***b*, there is shown a time chart for displaying the cursor at the sixth character on the first line and for writing new data. Since the cursor is to be displayed at the sixth character, the gate **88** delivers its output at a time when the scanning lines scan the first character on the screen of the cathode-ray tube and a coincidence takes place between the output and the control signal **102** so that the set signal is supplied to the flip-flop **117** through the gate **107**. The output from the gate **107** triggers the one-shot multivibrator **133** through the OR-gate **132** so as to extinguish the output **134** from the multivibrator **133** for a short period of time and to prevent the flip-flop **117** from being reset by the control signal **55** which appears immediately after the control signal **102** which has set the flip-flop **117**. The signal inputs to the INHIBIT-gate **122** are supplied from the flip-flop **117** and from the control circuit **73** as the control signal **54**, but its output is inhibited during a period in which the gate **107** is delivering its output. The INHIBIT-circuit **122** delivers its output to display the cursor at a time at which the control signal **54** is supplied after the output from the gate **107** has disappeared. In other words, the fact that the cursor should be displayed is detected and the cursor is displayed after the period of time corresponding to five characters has elapsed. Since the output **134** is delivered at the time of displaying the cursor, the gate **108** delivers its output as a result of the supply of the control signal **55** after display of the cursor and the flip-flop **117** is reset. Thus, the cursor is displayed only at the predetermined sixth character position on the first line.

During the period in which the flip-flop **117** is set to deliver its output **127**, the gates **1115**, **1215**,–, **1815** are opened as will be described later and new data **52** is supplied to the buffer memory **46**. When the memory contents of the registers are transferred by the shift pulses **33** and **34**, the data in the registers is renewed.

FIGS. **9** and **10** show a write-in control circuit for the renewal of data and a time chart for the explanation of operation of the circuit, respectively. A data key unit **141** includes keys for setting data of eight bits corresponding to 2^0, 2^1,–, 2^7 and a key closed at a time of complete establishment of data to give a strobe signal STB. A one-shot multivibrator **142** is energized by the strobe signal to deliver an output for a limited time period of one-sixtieth second. When the one-shot multivibrator **142** delivers its output, signals delivered from the data key unit **141** are set in flip-flops **152**, **152**,–, **158** through respective gates **143**, **144**,–, **150** so as to thereby form the signal **52** to be applied to the buffer memory. During the period in which the one-shot multivibrator **142** is delivering its output, that is, during the one-sixtieth second period, presence of the cursor is detected and a signal **88** is delivered from the gate **88**. Then, a set signal is supplied to a flip-flop **160** through an AND-gate **159**. When the flip-flop **160** is set, an output appears at its terminal **1** to supply a signal to AND-gates **161**, **162**,–, **165**. The AND-gates **161**, **162**,–, **165** select as to the gates **1115**, **1215**,–, **1815** which block of the blocks **41**, **42**–, **45** of the memory **4** should be opened. This is determined by the write-in control signals **127**, **128**,–, **131** described above. Thus, data in the corresponding buffer memory is renewed in the manner explained with reference to FIG. **8***b*. As apparent from reference to FIG. **8**, write-in of information in the buffer memory has been finished when the cursor is indicated. Therefore, when the cursor signal **136** appears, the cursor signal **136** is applied to a reset terminal R of the flip-flop **160** to reset the same. An output appearing at a terminal **0** in response to resetting of the flip-flop **160** is applied through a suitable delay circuit **166** to reset terminals R of the flip-flops **151**, **152**,–, **158** to reset the same, and at the same time, to energize a one-shot multivibrator **167** for producing the write-in finish signal **81**. The write-in finish signal **81** is applied to the counter **75** through the OR-gate **82** as a cursor carry-forward signal as described with reference to FIG. **7** to add one to the counter and advance the cursor to the right by one

character to indicate the position at which data are to be written next.

It will be apparent that a simple pattern display apparatus may be made according to the present invention when one character space, 8×14 dots, including the line space and character space is used an an element for displaying the so-called special pattern including longitudinal, lateral and oblique lines in lieu of characters or symbols as shown in FIG. **11**. In this case too, data may be stored in the memory **4** according to an eight-bit code as in the case of characters or symbols, and control entirely similar to that used in the character display described above may be carried out. While two sets of longitudinal elements, two sets of lateral elements and two sets of oblique elements making a total of six sets are essentially required for the display of a pattern, it will readily be understood that the number of sets may be increased to display a more detailed pattern.

Further, a memory for displaying a character or symbol and a memory for displaying a pattern may be independently provided to display a character or symbol and a pattern in superimposed relation as seen in FIG. **11** so as to obtain a universal display apparatus which can be applied to various industrial services. In this case, it is desirable that the lines of the pattern do not overlap the lines of the character so that the character can easily be distinguished from the pattern as shown in FIG. **11**. It is therefore convenient to select the timing of the character and pattern at x_2–x_6, y_3–y_9 and x_1–x_8, y_1–y_{14}, respectively.

FIGS. **12***a*, **12***b*, **12***c* and **12***d* show the relation between a basic control circuit **5**, a character-generating circuit **6** and a pattern-generating circuit **6'** adapted to exhibit a pattern and a character simultaneously as seen in FIG. **11**. FIGS. **12***a*, **12***b*, **12***c* and **12***d* are arranged in a relationship as shown in FIG. **13** to provide a complete illustration of the relation between the circuits as in FIG. **3**. In FIGS. **12***a* through **12***d*, lines bearing the same symbols connect the associated parts in the circuits. As apparent from comparison between FIG. **12** and FIG. **3**, the embodiment shown in FIG. **12** includes a memory **4'** and a pattern-generating circuit **6'** which are similar in structure to the memory **4** and a character-generating circuit **6** required for the display of characters, and both are regulated with the same timing. In the illustrated embodiment, the character-generating circuit **6** is adapted to display a character A, while the pattern-generating circuit **6'** is adapted to display an obliquely rightward and upward extending line in FIG. **11**. In FIG. **12**, dashes are affixed to those parts employed for the character display appearing in FIG. **3** to denote the same or equivalent parts employed for the pattern display. An OR-circuit **1000** and a lead **1001** are provided to assemble a character and a pattern in the same video signal.

According to the present invention, a commercial television receiver can be utilized in its existing form in the display section. It is thus possible to effect switchover as desired between display according to the present invention and the reception of broadcasting television. FIG. **14** is a block diagram of an embodiment of the present invention adapted for this purpose. Like reference numerals are used in FIG. **14** to denote like parts appearing in FIG. **2**.

The apparatus includes a keyboard and printer unit **1**, a memory control circuit **2**, a data processing unit **3** such as a computer or data logger, a memory **4**, a basic control circuit **5**, a character-generating circuit **6**, an alarm signal-generating circuit **501**, a display unit **502** including a horizontal oscillation circuit, a vertical oscillation circuit, an amplifying circuit and a video amplifying circuit, an alarm generating section **503** including an audio amplifying circuit, a control circuit **504** of a standard television receiver, an antenna **505** for receiving the television broadcasting and changeover switches **506**, **507**, **508** and **509**. The standard television receiver is designated by the reference numeral **510**. The keyboard and printer unit **1** writes any desired character or symbol or prints a displayed character or symbol for preservation.

The memory control circuit **2** controls the acceptance and delivery of data between the keyboard and printer unit **1**, and computer **3** and the memory **4** and readout of data from the memory **4** for delivery to the character generating circuit **6** and the alarm signal generating circuit **501** for display of characters and generation of an alarm signal. The memory **4** stores the code of characters to be displayed on the screen and effects readout and write-in of data under control of the memory control circuit **2**.

The basic control circuit **5** produces the horizontal and vertical synchronizing signals to be applied to the display unit **502**, and at the same time, applies signals designating the position of characters, space between characters and the spaces between lines to the character-generating circuit **6** and memory control circuit **2**. Further, the basic control circuit **5** applies a control signal to the alarm-signal-generating circuit **501** to designate the time and the code at which the alarm is to be generated.

The character generating circuit **6** generates a video signal according to the timing designated by the basic control circuit **5** on the basis of the code supplied from the memory **4** and delivers the video signal to the display unit **502**. The display unit **502** displays a character on the screen of the cathode-ray tube depending on the video signal described above and the synchronizing signals supplied from the basic control circuit **5**.

The alarm-signal-generating circuit **501** produces an alarm signal according to the timing designated by the basic control circuit **5** on the basis of the code supplied from the memory **4** and delivers the alarm signal to the alarm-generating section **503**.

The alarm-generating section **503** comprises an audio amplifying circuit, an output circuit and a speaker, and the audio signal coming from the control circuit **504** of the standard television receiver **510** and the alarm signal coming from the alarm-signal-generating circuit **501** of the character display apparatus are selectively applied to the alarm-generating section **503** by means of the changeover switch **506** to produce sound.

The switches **507**, **508** and **509** are changeover switches for the video signal, horizontal synchronizing signal and vertical synchronizing signal, respectively. The display unit **502** serves as a television broadcasting receiver when these switches are closed at contacts *a* and as a character display unit when these switches are closed at contacts *b*. These changeover switches **506**, **507**, **508** and **509** can be remotely controlled from the keyboard **1**, a processing unit **3** by a manual control.

A block **520** comprising the circuits **1** through **6** may preferably have a structure the same as that of the embodiment shown in FIGS. **2** and **3** so that a character signal and a received television signal can be selectively displayed. The alarm-signal-generating circuit **501** is controlled by the circuits **4** and **5** so that an alarm signal and an audio signal can be selectively heard. Thus, the apparatus can be made at low cost and a service man for commercial television receivers can perform the required maintenance of the apparatus.

It will be apparent from the foregoing description that the present invention employs a scanning system similar to that of the standard television system. Thus, there is no need to devise a special deflecting circuit and an inexpensive apparatus can be obtained since a receiver according to the standard television system can be satisfactorily incorporated in the apparatus as described above.

By use of the circulating memory, peripheral circuits have a simple structure and hence the control circuit therefor also has a simpler structure. Further, according to the present invention, the memory is divided into a plurality of blocks for the successful control thereof so that a dynamic shift register having a slow operating speed can be satisfactorily employed.

In the embodiments described above, dynamic shift registers having a relatively slow operating speed are employed so that data may merely be transferred from the main memory **47** to the buffer memory **46** during the period of scanning between lines and suitably circulated during the flyback

period. However, with high-speed registers, it is necessary to suitably circulate data during the period of scanning between lines as well as the flyback period and also to suitably circulate data within the main memory **47** so as to avoid loss of memory contents. For this purpose, AND-gates **168** and INHIBIT-gates **169** as shown by the broken lines in FIG. **6** may, for example, be provided to establish the circulating path for the main memory **47** and to cut off the circulating path from the buffer memory **46** to the main memory **47**. In this case, the data should naturally be circulated in such a manner so as not to cause any disorder in the address system as described in the embodiments. The circulating memory operable with high speeds may become somewhat complex compared with those of the embodiments in respect of the control of circulation. However, the number of divided blocks of the memory can be reduced or division of the memory into blocks will become unnecessary to simplify the control in this respect. When, for example, the shift register has an operating speed of 1 MHz, it is unnecessary to divide the memory into five blocks in the case of the described embodiments. Further, due to a high operating speed, it becomes unnecessary in respect of the control of write-in by the cursor too to make cursor detection prior to the actual cursor position as previously described. More precisely, as shown in FIG. **15**, there is a period of time ΔT before a shift pulse ϕ_1 is supplied after the cursor is detected, and this permits write-in thereby simplifying the detection of the cursor and the write-in control circuit. When a high-speed circulating memory is employed to further increase the number of characters that can be displayed, the circulating path shown by the broken lines in FIG. **6** will be difficult to make possible the circulation of a predetermined number of bits. In such a case, the main memory may be divided into a suitable number of small sections and circulation may be made within the individual small sections.

We claim:

1. A display apparatus comprising means for supplying information-representing characters to be displayed memory means for storing said information to be displayed, memory control means for controlling the storage and rewrite of the information in said memory means, character-generating means for generating signals representing characters corresponding to the contents of said memory means, cathode-ray tube display means for displaying a character depending on the output from said character-generating means, said display means being provided with a deflection system and a deflection control system corresponding to that of the standard commercial television receiver, and a basic control circuit having an oscillator generating a specific frequency for applying control signals to said memory control means and character-generating means with a predetermined timing, said memory means comprising a number of component memory means equal to the number of bits forming characters to be displayed, said components memory means being connected in parallel and each component memory means comprising first and second circulating memories connected in cascade, said first circulating memory containing information for one horizontal sweep in a line of the display, said second circulating memory containing information for the remaining lines of the display, the output of said first circulating memory being connected to said character-generating means in control thereof, said memory control means including means for separately controlling said first and second circulating memories.

2. A display apparatus as claimed in claim **1**, in which said second circulating memory is divided into a plurality of blocks which are controlled by separate pulse trains.

3. A display apparatus as claimed in claim **1**, in which there is provided at least one pattern-generating circuit for generating preselected pattern elements and means for switching connections between said character generating circuit and said pattern generating circuit.

4. A display apparatus as claimed in claim **1**, in which there are provided further memory means for preselected pattern elements, which are interconnected with the remaining means in the apparatus so as to allow a parallel operation with the first-mentioned memory means for the information of characters.

5. A display apparatus as claimed in claim **1**, further including means for controlling and detecting the position of a cursor which means includes means for producing an output at a time earlier by predetermined bit time than the time when the cursor actually appears, and means responsive to said output for writing an external signal into said memory means at the address corresponding to the position of said cursor.

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