

Nov. 22, 1955

J. S. HARRIS

2,724,739

CODE CONVERSION SYSTEM

Filed June 16, 1953

4 Sheets-Sheet 1

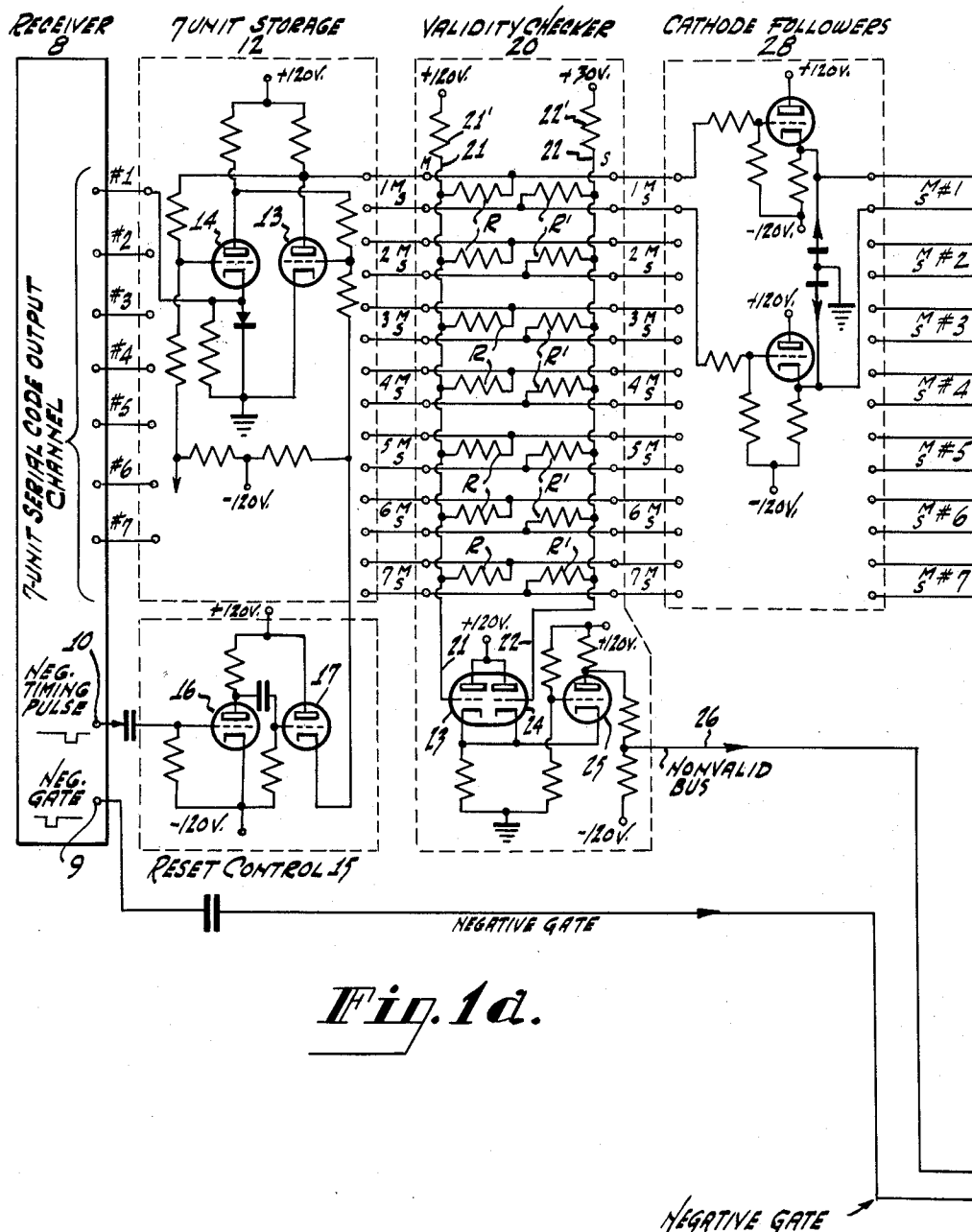


Fig. 1a.

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4 Sheets-Sheet 2

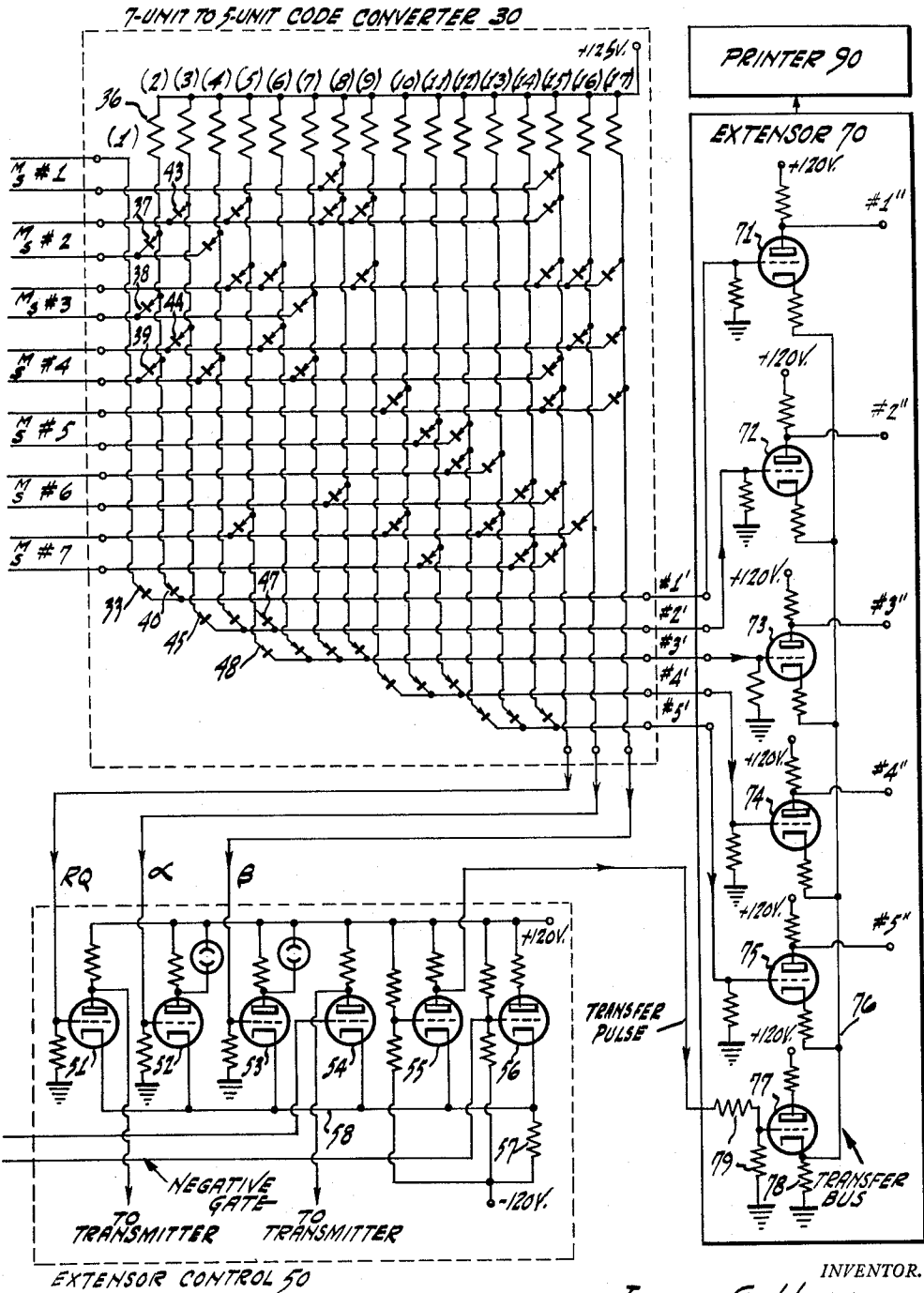


Fig. 1 b.

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Fig. 2.

7-UNIT CODE							5-UNIT CODE						
UNIT 1 2 3 4 5 6 7 BINARY							UNIT 1 2 3 4 5 BINARY						
NUMERICAL							NUMERICAL						
CHARACTER OR FUNCTION							CHARACTER OR FUNCTION						
1	2	4	8	16	32	64	1	2	4	8	16		
M	M	M	S	S	S	7	I	6	S	M	M	S	S
M	M	S	M	S	S	11	SPACE	4	S	S	M	S	S
M	S	M	M	S	S	13	LINE FEED	2	S	M	S	S	S
S	M	M	M	S	S	14	E	1	M	S	S	S	S
M	M	S	S	M	S	19	R	10	S	M	S	M	
M	S	M	S	M	S	21	N	12	S	S	M	M	S
S	M	M	S	M	S	22	RQ						
M	S	S	M	M	S	23	C	14	S	M	M	M	S
S	M	S	M	M	S	26	D	9	M	S	S	M	S
S	S	M	M	M	S	28	B						
M	M	S	S	S	M	35	L	18	S	M	S	S	M
M	S	M	S	S	M	37	H	20	S	S	M	S	M
S	M	M	S	S	M	38	U	7	M	M	M	S	S
M	S	S	M	S	M	41	P	22	S	M	M	S	M
S	M	S	M	S	M	42	S	5	M	S	M	S	S
S	S	M	M	S	M	44	A	3	M	M	S	S	S
M	S	S	S	M	M	49	O	14	S	S	S	M	M
S	M	S	S	M	M	50	FIGS	27	M	M	S	M	M
S	S	M	S	M	M	52	X	29	M	S	M	M	M
S	S	S	M	M	M	56	LTRS	31	M	M	M	M	M
M	M	S	S	S	S	67	G	26	S	M	S	M	M
M	S	M	S	S	S	69	M	28	S	S	M	M	M
S	M	M	S	S	S	70	Z	17	M	S	S	S	M
M	S	S	M	S	S	73	V	30	S	M	M	M	M
S	M	S	M	S	S	74	B	25	M	S	S	M	M
S	S	M	M	S	S	76	Q						
M	S	S	S	M	S	81	T	16	S	S	S	S	M
S	M	S	S	M	S	82	W	19	M	M	S	S	M
S	S	M	S	M	S	84	V	21	M	S	M	S	M
S	S	S	M	M	S	88	Q	23	M	M	M	S	M
M	S	S	S	S	M	97	CAR RET.	8	S	S	S	M	S
S	M	S	S	S	M	98	J	11	M	M	S	M	S
S	S	M	S	S	M	100	F	13	M	S	M	M	S
S	S	S	M	S	M	104	K	15	M	M	M	M	S
S	S	S	S	M	M	112	SPACE	0	S	S	S	S	S

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Fig. 3.

VERT. BUS	7-UNIT CODE								5-UNIT CODE				
	1	2	3	4	5	6	7		1	2	3	4	5
(1)	M	-	-	-	-	-	-	}	S	-	-	-	-
(2)	-	S	S	S	-	-	-						
(3)	-	M	-	M	-	-	-	}					
(4)	-	S	-	S	-	-	-		-	S	-	-	-
(5)	-	M	M	-	-	-	M	}					
	-	M	M	-	-	-	M						
(6)	-	-	M	M	-	-	-	}			S	-	-
(7)	-	-	S	S	-	-	-						
(8)	S	M	-	-	-	S	-	}					
(9)	-	M	M	-	-	-	-						
(10)	-	-	-	-	M	-	M	}			-	S	-
(11)	-	-	-	-	S	-	M						
(12)	S	-	-	-	S	M	-	}					
(13)	-	-	-	-	-	M	M						S
(14)	-	-	-	-	-	S	S	}					
	7-UNIT CODE SUPERVISORY SIGS.								No CORRESPONDING 5-UNIT SIG.				
(15)	S	M	M	S	M	S	S		RQ	SIG.			
(16)	-	-	M	M	-	-	M		IDLE	α			
(17)	-	-	M	M	M	-	-		IDLE	β			

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2,724,739

CODE CONVERSION SYSTEM

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Application June 16, 1953, Serial No. 361,979

10 Claims. (Cl. 178—26)

This invention relates to a system capable of converting a coded signal in the form of n mark and space units per character into another coded signal in the form of p mark and space units per character.

While not limited thereto, this invention is particularly useful in the communications art employing printing telegraph apparatus wherein messages are transmitted over the oceans by radio using a seven-unit protected code for each character ($n=7$) and wherein the same messages are transmitted over land lines using a five-unit printer code for each corresponding character ($p=5$). The seven-unit protected code is used to guard against errors caused by interference encountered on radio channels and is of the type described in Moore and Mathes Reissue Patent 23,028. In this seven-unit protected code, each valid combination consists of three mark and four space units. By employing such a code, the received signals are readily analyzed and—if found to be incorrect because of the absence of the foregoing constant-ratio feature—rejected by the printer “translator.” It is necessary to provide means to quickly and automatically translate the message of seven-unit character signals into the corresponding five-unit character signal. In practice, the conversion has been performed by relay circuits which are becoming inadequate as the speeds with which messages are transmitted are increased. It is therefore a general object of this invention to provide a fast-acting electronic code converter system which is simpler and more reliable than those previously known.

It is another object to provide an improved system for translating a coded signal having a given number of elements in serial form into a coded signal having a different number of elements also in serial form.

It is a further object to provide an improved means to recognize the validity of a signal in a protected-type multi-element code.

In one aspect, the invention comprises a system for use in the communications field to translate a seven-unit protected-code signal to a five-unit code signal suitable for operating a conventional printer. The signal from a receiver comprises seven serial units to represent each message character. The units are either mark or space and they are arranged serially in time. The serial signal is applied to a storage circuit which accumulates the serial units of a character and presents them as a simultaneous signal to a validity checker. The validity checker determines whether the ratio of marks to spaces is $3/4$ as is the case for all valid seven-unit character signals. After passing through the validity checker, the signal is applied through cathode followers to a crystal matrix code converter which converts the signal to a five-unit per character simultaneous signal. This signal is applied to an extensor which translates the signal to serial form for application to a conventional printer. A reset control and an extensor control are included in the system to control the cyclic operation of the system wherein there is one complete cycle for each signal character.

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A feature of the invention is the arrangement of a diode matrix code converter for translating a seven-unit protected code to a five-unit code, the code converter being used in combination with validity checking and control circuits whereby to prevent non-valid and supervisory seven-unit code signals from appearing in the output circuit as erroneous five-unit signals. A validity checker is an essential part of a system receptive to a seven-unit protected code and its cooperation with the code converter after the manner taught herein permits of a greatly simplified system compared with what has been possible heretofore.

Other objects, aspects and features of the invention will be apparent to those skilled in the art from the following description taken together with the appended drawings wherein:

Figure 1a and Figure 1b taken together comprise a circuit diagram, partly in block form, of a system for converting seven-unit serial code signals to five-unit serial signals for operating a printer.

Figure 2 is a chart showing the specific seven-unit code and the equivalent five-unit code presently in use with which the system of Figure 1a and Figure 1b is designed to operate.

Figure 3 is a tabulation derived from the chart of Figure 2 which will be used in explaining the operation of the invention.

The drawings and descriptions are based on the use of conventional thermionic tubes and crystal diodes. Heater circuits for the thermionic cathodes have been omitted as such circuits are well known in the art, and their inclusion might obscure the clarity of the presentation of the invention. For the same reason, the details of the direct current power supply have been omitted. The voltages required at various supply points in the circuit, and the polarities thereof are indicated on the drawing. It is to be understood that the power supply may include the usual filtering and decoupling arrangements to prevent interaction between the circuits fed from the various points. Values of voltage are illustrative only and are not to be construed in a limiting sense. Points of reference potential in the circuits are represented by the symbol for ground. The converter may include thermionic diodes or crystal diodes such as those including germanium.

Referring now to the drawings, Figures 1a and 1b show a system, by way of example, which is receptive to a coded message signal according to the seven-unit code wherein each character is in the form of seven serial units, and which is operative to generate a signal for a printer, the signal being in the five-unit code wherein each character is in the form of five serial units. A receiver 8 to which are applied the seven-unit signals from a remotely located transmitter or sending terminal has seven output terminals, one terminal for each unit of the received seven-unit code message signal. The output terminals are energized in sequence to indicate whether the units are mark or space. A mark is indicated by a negative pulse on the corresponding terminal and a space is indicated by zero voltage on a corresponding terminal. The receiver 8 also has a negative gate output terminal 9 and a negative timing pulse output terminal 10. The gate pulse follows the succession of output pulses on the seven channel output terminals, and the timing pulse follows the gate pulse.

The seven output terminals of receiver 8 are connected to a seven-unit storage device 12 which translates the serial signal into a simultaneous signal whereby all seven units of a character are simultaneously present on the output terminals of the storage device 12. There is a mark output terminal and a space output terminal for each of the seven signal units. A mark is indicated by

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+120 volts on the mark terminal and +30 volts on the space terminal. A space is indicated when the potentials are reversed. The circuit for signal unit No. 1 is shown in the dotted line box 12; the other six circuits within storage device 12 for the other six output leads, No. 2 to No. 7, inclusive, from receiver 8 are the same and are not shown. Vacuum tubes 13 and 14 are connected together to form a bi-stable recipro-conductive circuit. Due to the action of the reset control circuit 15 (described later) tube 13 will be conducting and tube 14 nonconducting prior to receipt of signal units from the receiver 8. Tube 13 is biased to be normally conducting and tube 14 is biased to be normally nonconducting. When a negative pulse corresponding to a mark from output terminal No. 1 of receiver 8 is applied to the cathode of tube 14, tube 14 is rendered conductive, the potential on its plate drops from +120 volts to +30 volts and this drop is coupled to the grid of tube 13 to cut tube 13 off (i. e., to cut off the flow of plate current in tube 13). The resulting high potential (nominally +120 volts) on the plate of tube 13 is connected to the mark output terminal and the low potential (nominally +30 volts) on the plate of tube 14 is connected to the space output terminal. If the output No. 1 of the receiver 8 is zero volts indicating a space, the mark output terminal of storage device 12 is +30 volts and the space output terminal of storage device 12 is +120 volts.

When a valid seven-unit character signal is applied from receiver 8 to storage device 12, the three mark unit signals reverse the conductive states of the tubes 13 and 14 of the corresponding bistable recipro-conductive storage circuits. The four space signals have no effect on the four corresponding storage circuits. As a result, three of the seven output line pairs from storage device 12 have +120 volts on the mark leads and +30 volts on the space leads, and four of the output line pairs have +120 volts on the space leads and +30 volts on the mark leads.

After all seven serial units of a character from receiver 8 have been stored in storage device 12, a negative timing pulse from terminal 10 is applied to the reset control circuit 15. A negative pulse applied to the grid of vacuum tube 16 results in a positive pulse on its plate which is coupled to the grid of vacuum tube 17. The cathode of tube 17 rises with its grid and this rise is coupled to the grids of the seven vacuum tubes 13 (only one is shown). The tubes 13 are thus rendered conductive and tubes 14 are rendered nonconductive so that the storage device 12 is in readiness to store the following seven-unit character.

The output of storage device 12 consists of a separate pair of mark and space terminals for each of the seven units of the signal. Prior to the operation of reset control 15, there is simultaneously present a positive potential of +120 volts on either the mark terminal or on the space terminal of each of the seven pairs of terminals. A potential of +30 volts is present on the other terminal of each pair. The simultaneous output of the storage device 12 is applied to a validity checker 20.

The seven-unit code of the present example is a protected code wherein each character consists of three mark units and four space units. The validity checker 20 analyses each character signal received and if the ratio of marks to spaces is different from 3/4, an error is indicated and the remotely located sending terminal is required to retransmit the character. The validity checker 20 is the subject of my separate copending application Serial No. 368,973 filed on July 20, 1953, now Patent No. 2,688,050, issued on August 31, 1954, and assigned to the assignee of this application.

In the validity checker 20, a mark bus 21 is connected through individual resistors to all seven mark lines, and through a resistor 21' to +120 volts. A space bus 22 is connected through resistors to all seven space lines, and through a resistor 22' to +30 volts. All sixteen resistors

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are identical. The buses 21 and 22 are also connected respectively to the grids of tubes 23 and 24 which may be a duo-triode tube having inter-connected cathodes. The cathodes of tubes 23 and 24 are connected to the cathode of a non-valid tube 25, all three tubes being provided with a common cathode resistor. The grid of non-valid tube 25 has its bias fixed by a voltage divider.

When there is a valid seven-unit character signal of three marks and four spaces on the seven input line pairs to validity checker 20, there is +120 volt potential on three mark leads and +30 volt potential on four mark leads. The seven mark leads are connected through identical resistors R to the mark bus 21. An eighth identical resistor 21' is connected from the +120 volt source to mark bus 21. Since four of these resistors are connected to +120 volts and four are connected to +30 volts, the voltage on the mark bus 21 and on the grid of the tube 23 is halfway between these values, or 75 volts. In like manner, when a valid seven unit signal is applied to the validity checker 20, there is +30 volt potential on three space leads and +120 volt potential on four space leads, and these seven leads are connected through seven identical resistors R' to the space bus 22. An eighth identical resistor 22' is connected from the +30 volt source to space bus 22. (Resistors R, 21' R' and 22' are equal in value.) Since four of the resistors R' and 22' are connected to +30 volts and four are connected to +120 volts, the voltage on space bus 22 is also halfway between these values, or 75 volts. If a non-valid signal having other than three mark units and four space units is applied to the validity checker, the balanced condition described above will not exist and either the mark bus 21 or the space bus 22 will be at a potential greater than 75 volts.

It will be understood that if the validity checker were required to pass signals having a ratio of marks to spaces of unity, the resistors 21' and 22' would have a value of infinity, and that in general resistors 21' and 22' are used to translate the desired mark/space ratio at the input to a potential ratio of unity on buses 21 and 22.

Tubes 23, 24 and 25 are arranged and biased so that when there is +75 volts on the grids of tubes 23 and 24, the cathodes of tubes 23, 24 and 25 are at a potential which allows tube 25 to conduct. The output 26 from the validity checker 20 is then at zero volts. If a non-valid signal is applied to the validity checker 20, the potential on one or the other of the grids of tubes 23 and 24 is higher than 75 volts and the increased current flow through the common cathode resistor increases the cathode potential of tube 25 cutting the tube off. The output voltage on lead 26 then increases from zero volts to +35 volts. The manner in which this output of the validity checker 20 is used to prevent the printing of invalid characters will appear as the description proceeds.

The seven pairs of lines going through the validity checker 20 are applied to cathode followers 28 shown as a dotted line box. There are fourteen identical cathode follower circuits, one for each of the mark and space leads of the seven line pairs from the checker 20, only two of them being shown in the drawing. The cathode follower circuits are well known in the art and are employed here to provide a low impedance signal source for application to the code converter 30. The output of the cathode followers corresponds to the output of storage device 12 except that a mark on a line pair is indicated by +25 volts on the mark lead and zero volts on the space lead. A space on a line pair is indicated by +25 volts on the space lead and zero volts on the mark lead. It will be understood to be within the skill of those in the art to modify the circuits of storage device 12 and validity checker 20 to provide the desired low-impedance source of signals without the need for cathode followers 28.

Code converter 30 is a diode matrix for converting a simultaneous seven-unit code into a simultaneous five-unit code. The simultaneous seven-unit input signal is on

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seven line pairs, one lead of each pair being for mark units and the other lead being for space units. Either the mark lead or the space lead of each pair is energized. A mark condition on a line is indicated if the mark lead is at +25 volts and the space lead is at 0 volts. A space condition is indicated by the reverse potentials. The code converter has five output terminals. Each terminal represents one unit of the five-unit code. A space condition on an output terminal is indicated when the potential on the lead is +25 volts and a mark condition is indicated by a potential of 0 volts. The input to the code converter is in binary form and the output is also in binary form. Patent Number 2,620,395 on a Code Converter issued on December 2, 1952, to A. Snijders shows a code converter having a binary input of resistor elements and a binary output of diode elements. The present code converter has a binary input of diode elements and a binary output of diode elements with a resulting improvement in reliability of operation.

The code converter of this invention employs a very greatly reduced number of diode elements in the matrices than have previously been possible in converting from a seven-unit protected code to a five-unit code. This simplification of the converter results from the combination with the converter 30 of the validity checker 20. A valid seven-unit signal must consist of three mark units and four space units. The validity checker 20 discriminates against non-valid signals. Without the cooperation of a validity checker, the binary-to-numerical section of a seven-unit to a five-unit code converter must define all seven units of the input signal. With the cooperation of a validity checker, the binary-to-numerical section of a seven-unit protected code converter needs to define only the three mark units of each character. Since a 7-unit protected code has

$$\frac{7!}{3!4!} = 35 \text{ variations}$$

the resulting saving in diodes is 4×35 or 140 diodes.

According to this invention, a further simplification is provided by arranging the converter matrix to recognize only the groups of seven-unit combinations (by the inclusion or exclusion of specified binary digits) which result in the inclusion or exclusion of specified binary digits in the five-unit code. With this concept it is only necessary to define sufficient groups of the seven-unit combinations to include only the desired five-unit equivalents, as will become more apparent as the description proceeds.

In the five-unit code there are $2^5 = 32$ variations. Each of these five variations is identified with one of the 26 alphabetic characters or with a signal such as "carriage space," "line feed," "figures," "letters," "carriage return," and "five space." The difference between the 35 variations of the protected seven-unit code and the 32 variations of the five-unit code provides three extra seven-unit signals which are designated RQ, α and β and are used for supervisory purposes. There is no five-unit equivalent for these supervisory seven-unit signals and by providing means in the converter to distinguish the supervisory signals from valid five-unit signals, a still further simplification of the converter results.

The corresponding characters of the presently used seven-unit and five-unit codes are as shown in Figure 2. The characters are arranged in the order of the numerical count of the seven-unit code according to the binary system. From an analysis of the codes it is apparent that if the first unit of the seven-unit code is a mark, or, if the second, third and fourth units of the seven-unit code are spaces, the first unit of the five-unit code must be a space. Further analysis provides the tabulation of Figure 3 showing the conditions of mark and/or space in the seven-unit code which define a space in each of the five positions of the five-unit code, and which define the supervisory signals for which there is no corresponding five-unit code. A similar tabulation could be made for

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the conversion from any other seven-unit code to the five-unit code. Such tabulations may define either the space or the mark condition of each of the five positions of the five-unit code, as desired, it being understood that in the case of space definitions the absence of a space is interpreted as a mark and vice versa.

Referring now to the code converter 30 of Figure 1b, it will be noted that the converter consists of a matrix of input diodes connected between the seven-unit input leads and the seventeen vertical buses, and a matrix of output diodes connected between the seventeen vertical buses and the five-unit output leads. Each vertical bus except the first one is connected through an isolating resistor to a source of +125 volts. The various vertical buses in the converter are labeled (1) through (17) in accordance with the analysis tabulated in Figure 3 wherein each condition is similarly labeled (1) through (17). The diodes in the matrix are represented by a symbol including an arrow pointing in the direction of current flow (as contrasted with electron flow). The diodes may be germanium diodes.

According to the first condition tabulated in Figure 3, when the first unit of the seven-unit code is a mark, the first unit of the five-unit code must be a space. A mark on the No. 1 line pair to the code converter is represented by +25 volts on the mark lead and zero volts on the space lead. The mark lead is connected through the vertical bus (1) and through diode 33 to the five-unit output lead No. 1'. A +25 volts on an output lead represents a space and zero volts represents a mark. A space is indicated by the +25 volts on the output lead No. 1' and the first line of the tabulation of Figure 3 is satisfied.

According to the second condition of Figure 3, if the second, third and fourth units of the seven-unit code are spaces, the first unit of the five-unit code must be a space. In Figure 1a, the vertical bus (2) is connected through diodes 37, 38 and 39 to the space leads of input lines No. 2, No. 3 and No. 4 which are at +25 volts. Current flows from the +125-volt source in converter 30 through resistor 36, vertical bus (2) and diodes 37, 38 and 39 to the respective space leads of input lines No. 2, No. 3 and No. 4. The current flow through resistor 36 causes a 100-volt drop thereacross so that the vertical bus (2) and the output lead No. 1' connected by diode 40 is at a potential of +25 volts to indicate a space on five-unit output lead #1'. The diodes act to make the potential on the vertical bus to which they are connected conform with the lowest potential on the mark or space leads to which the other ends of the diodes are connected. If space leads No. 2 and No. 3 had been at +25 volts but space lead No. 4 had been at zero volts, the drop across resistor 36 would have been 125 volts so that potential on the vertical bus (2) would have been zero volts. Then, assuming zero potential on vertical bus (1), the output lead No. 1' would be at zero volts and would indicate output lead No. 1' to not be a space, i. e., to be a mark.

According to the third condition labeled (3) of Figure 3, if the second and fourth units of the seven-unit code are both marks, the second unit of the five-unit code must be a space. This condition is taken care of in converter 30 by vertical bus (3) and diodes 43 and 44 connected to the mark leads of inputs No. 2 and No. 4. The vertical bus (3) assumes the potential of +25 volts which is on the mark leads of inputs No. 2 and No. 4 and this potential is connected by diode 45 to the No. 2' output lead. The fourth condition (4) of Figure 3 is taken care of by the diodes connected to vertical bus (4).

It will be noted from Figure 3 that if the second, third and seventh units of the seven-unit code are marks, the second and the third units of the five-unit code must be spaces. Therefore these two conditions may be taken care of in the converter with a single vertical bus (5) by connecting the bus through diodes 47 and 48 respectively to the output lead No. 2' and to the output lead No. 3'. The balance of the first fourteen conditions of Figure 3

are taken care of by the balance of the first fourteen vertical buses in the manner described above in connection with vertical buses No. 2 and No. 3.

The conditions labeled (15), (16) and (17) in Figure 3 for the seven-unit code have no counterpart in the five-unit code. These conditions are used for supervisory purposes and are labeled RQ, α and β . Vertical buses (15), (16) and (17) are provided to detect these conditions in the seven-unit code and the vertical buses are connected from the converter 30 directly to an extensor control 50. This arrangement reduces the number of diodes that would otherwise be required in the converter. In the language of the claims, the fourteen conditions of the specific equipment described herein are generally referred to as q conditions, and the three supervisory conditions for which there are no five-unit equivalents are referred to as r conditions.

The greatest reduction in the number of diodes in converter 30 compared with the converters of the prior art results from the combination with the converter of the validity checker 20. All non-valid seven-unit signals are recognized by the validity checker 20 and the output thereof is applied through the extensor or output circuit control to the extensor 70 to prevent the printing of non-valid characters. Therefore the code converter 30 merely has to convert valid seven-unit signals to the corresponding five-unit signal. This permits of the greatly simplified converter of this invention. It will be understood that in telegraphic practice whenever it is necessary to convert from a first code having a given number of units to a code of fewer units, the first code will be a protected code having a predetermined ratio of marks to spaces. A protected code is useful only if some means are provided to check the validity of a received signal. Therefore, a validity checker is an essential part of a system wherein a first protected code is converted to a second code of fewer units, and by a combination of the essential validity checker with the code converter according to this invention, the system is greatly simplified without any resulting disadvantages.

The extensor control 50 includes six vacuum tubes 51 through 56 connected through a common cathode resistor 57 to a source of -120 volts. The plates of all the tubes are connected through individual plate resistors to a source of $+120$ volts. The grid of tube 56 is biased by a voltage divider to $+50$ volts so that in the absence of a 100 -volt negative gate from receiver 8, the tube is conductive and the drop across cathode resistor 57 maintains the cathode bus 58 at a potential of about $+50$ volts so that tubes 51, 52, 53, 54 and 55 are normally cut off. In the absence of supervisory RQ, α and β signals from code converter 30, the grids of tubes 51, 52 and 53 are at ground potential. In the absence of a non-valid signal from validity checker 20, the grid of tube 54 is at zero or ground potential. The grid of tube 55 is biased to $+15$ volts by a voltage divider.

In the operation of the extensor control 50, when a negative gate of 100 volts is supplied from gate terminal 9 of receiver 8 to the grid of tube 56, the tube is cut off and the potential on the cathode bus 58 falls until it reaches a value which is equal to the voltage on the grid of one of the other five tubes. If there is a valid character signal in the system, the potential of the cathode bus 58 will drop until the value equals the $+15$ volts on the grid of tube 55. Tube 55 will then conduct and generate a negative transfer pulse on its plate which is applied to the extensor 70. Tubes 51, 52, 53 and 54 remain cut off because their grids are at zero volts.

If there is a $+35$ volt non-valid signal from validity checker 20 to the grid of tube 54 when a negative gate is applied to the tube 56, the potential of the cathode bus 58 drops from $+50$ volts only to the $+35$ -volt value which renders tube 54 conductive. Tube 55 remains cut off and no transfer pulse is applied to extensor 70.

If there is a $+25$ volt supervisory signal applied from

code converter 30 to the grid of one of tubes 51, 52 and 53, and no $+35$ volt signal applied from validity checker 20 to the grid of tube 54, when a negative gate is applied to tube 56, the potential of the cathode bus 58 drops from $+50$ volts to the $+25$ volt value which renders the corresponding tube 51, 52 or 53 conductive. Tube 55 remains cut off and no transfer pulse is sent to extensor 70. If the conductive tube is tube 51, and RQ signal is generated on its plate and is used for supervisory purposes (not shown). If the conductive tube is tube 52 or tube 53, a neon glow lamp is energized in the plate circuit of the corresponding tube and this is visually interpreted as a supervisory signal.

It is thus apparent that a transfer pulse is applied from the extensor control 50 to the extensor 70 only when a valid seven-unit signal is present in the validity checker 20 and only when the valid seven-unit signal is not one of the three supervisory signals.

The extensor 70 includes six tubes 71 through 75 the grids of which are receptive to the five outputs, respectively, of code converter 30. The plate of each tube 71-75 is connected through an individual plate resistor to a source of $+120$ volts and to one of the output terminals No. 1' through No. 5'. The cathode of each of the tubes is connected through an individual cathode resistor to a transfer bus 76. The transfer bus 76 is connected to the cathode of a cathode follower tube 77 having a cathode resistor 78 connected to ground. The plate of cathode follower 77 is connected to source of $+120$ volts and the grid is connected to receive the transfer pulse from extensor control 50.

In the operation of that part of the extensor 70 shown in Figure 1b, the outputs No. 1' through No. 5' from the converter 30 are applied to the grids of tubes 71-75 respectively. The voltages applied to the grids are either $+25$ volts to indicate a space or zero volts to indicate a mark. Normally $+120$ volts is applied from extensor control 50 to voltage divider 79 to provide a potential of $+50$ volts on the grid of cathode follower 77. The current flow through cathode follower 77 results in the transfer bus 76 being maintained at $+50$ volts and all of tubes 71-75 are thus maintained in a cut-off condition. When a negative transfer pulse is applied to voltage divider 79, the potential on the grid and the cathode of cathode follower 77 and transfer bus 76 falls to $+25$ volts. This allows all of tubes 71-75 which have $+25$ volts on their grids (representing a space) to conduct. The tubes which conduct provide a relatively low voltage to the respective output terminals to indicate a space. The tubes which do not conduct provide a relatively high potential to the respective output terminals to indicate a mark. The output terminals No. 1' through No. 5' indicate by the simultaneous potentials thereon the five-unit character corresponding with the seven-unit character from receiver 8.

The extensor 70 includes means (not shown) to perform additional functions such as the storage of the simultaneous five-element signal, the distribution of the simultaneous signal to serial pulses on a single conductor and the resetting of the storage to receive the following signal. The output of the extensor is a serial five-unit signal which is applied to a conventional telegraph printer 90 which reproduces the message in written or punched tape form.

The operation of the entire system of Figures 1a and 1b may be summarized as follows: A serial seven-unit character signal from receiver 8 is applied to storage 12 and is stored as a simultaneous signal until cleared by reset control 15 operating from a timing pulse from receiver 8. Storage 12 provides an output on seven pairs of leads which are connected to validity checker 20. A signal not having a $3/4$ ratio between marks and spaces results in a positive output from the validity checker on non-valid bus 26. Whether valid or not, the seven-unit signal from the validity checker 20 is applied through

cathode followers 28 to code converter 30. The code converter provides a corresponding five-unit output on five conductors to the extensor 70, and provides an output on three conductors for supervisory signals to the extensor control 50. After the receiver 8 supplies the seven-unit code character, the receiver supplies a negative gate to energize the extensor control 50. If the output from the validity checker 20 to the extensor control 50 indicates that the seven-unit signal stored in the system is a valid seven-unit signal, and if the valid seven-unit signal is not one of the three supervisory signals applied from the converter 30 to the extensor control 50, then the extensor control sends a transfer pulse to the extensor 70 to render the extensor capable of accepting the five-unit output from the code converter 30. If the valid seven unit signal in the system is one of the three supervisory signals for which there is no corresponding five-unit signal, the supervisory signal is taken from the code converter 30, applied to the extensor control 50, and used to perform its supervisory function. The extensor control 50 prevents the extensor 70 from accepting what would be an erroneous five-unit signal from the code converter 30 when a supervisory seven-unit signal is in the system. The validity checker 20, the extensor control 50 and the code converter 30 cooperate to perform the necessary functions with a minimum of circuit components and circuit complexity.

What is claimed is :

1. A code converter system comprising a source of coded signals of a given number of simultaneous units per character, all valid signals in said code having a predetermined ratio between mark and space units, a matrix of diode-connected conductors having input terminals receptive to said source of coded signals and output terminals for equivalent characters in a code of less than said given number of elements, an output circuit coupled to said converter output terminals, and control circuit means coupled to said source over a path excluding said matrix and being receptive to the output from said source and operative to energize said output circuit only when said source supplies a valid coded signal.

2. A code converter system comprising a source of signals having n units per character, a matrix of diode-connected conductors having input terminals coupled to said source and output terminals for equivalent signals having p units per character, an output circuit coupled to said output terminals, and control circuit means having input terminals also coupled to said source and output terminals coupled to said output circuit to selectively energize said output circuit.

3. A code converter system comprising a source of signals having n mark and space units per character, a code converter matrix having input terminals coupled to said source and output terminals for equivalent signals having p mark and space units per character, an output circuit coupled to said converter output terminals, and control circuit means having input terminals coupled to said source and output terminals coupled to said output circuit to energize said output circuit when the signal from said source has a predetermined ratio between mark and space units.

4. A code converter system comprising a source of signals having n mark and space units per character, a code converter matrix having input terminals coupled to said source and character output terminals for equivalent signals having p mark and space units per character and supervisory output terminals for supervisory signals of the n -unit code not having a p -unit equivalent, an output circuit coupled to said character output terminals, and control circuit means having input terminals coupled to said source and to said supervisory output terminals and having output terminals coupled to said output circuit to energize said output circuit only when the signal from said source has a predetermined ratio between mark and

space units, and is not a supervisory signal for which there is no equivalent p -unit character.

5. A code converter system comprising a source of signals having n mark and space units per character, a code converter matrix having input terminals coupled to said source and character output terminals for equivalent signals having p mark and space units per character and supervisory output terminals for signals of the n -unit code not having a p -unit equivalent, an output circuit coupled to said character output terminals, and control circuit means having input terminals coupled to said supervisory output terminals and having output terminals coupled to said output circuit to prevent the passing of an erroneous p -unit signal when a supervisory n -unit signal is applied to the code converter matrix.

6. A code converter system receptive to a character signal with n serially arranged units per character, comprising storage means to store said signal to provide m simultaneous units per character, a code converter matrix having input terminals receptive to the output of said storage means and character output terminals for p -unit signals and supervisory output terminals for input signals for which there is no equivalent p -unit signal, a validity checker having input terminals coupled to the output of said storage means, a source of a gate pulse occurring between each serially arranged character signal, an output circuit coupled to the character output terminals of the code converter, and a control circuit having input terminals coupled to said source of gate pulses, said validity checker and said supervisory output terminals of the code converter and having output terminals coupled to said output circuit to energize the output circuit when the output of the validity checker indicates a predetermined ratio between the mark and space units of the m -unit signal, there is no signal on the supervisory output terminals of the code converter and a gate pulse is received from the gate source.

7. An n -unit to p -unit code converter comprising a source of a simultaneous signal of n -units, said source having n mark terminals and n space terminals grouped in n pairs, each pair having a given potential on the mark terminal to indicate a mark or said given potential on the space terminal to indicate a space, p output terminals, one for each unit of the p -unit code, a number of buses equal to less than the number of valid n -unit signals, an impedance element connecting each bus to a source of unidirectional potential, a means including diodes connecting each bus to those of said source terminals which define one unit of the p -unit code, and diodes connecting each bus to the corresponding output terminal.

8. An n -unit to p -unit code converter comprising a source of a simultaneous signal of n -units, said source having n mark terminals and n space terminals grouped in n pairs, each pair having a given potential on the mark terminal to indicate a mark or said given potential on the space terminal to indicate a space, p output terminals, a number of buses equal to less than the number of valid n -unit signals, diodes connecting each of said buses to those of said source terminals which define one unit of the p -unit code to be a space, and diodes connecting each of said buses to a corresponding output terminal.

9. A code converter to convert from a mark-space code of n -units to a mark-space code of p -units, the codes being such that there are p groups of q conditions of relatively few units of the n -unit code wherein any one condition within a group defines at least one unit of the p -unit code, comprising, a source of simultaneous signal of n -units, said source having n mark terminals and n space terminals grouped in n pairs, each pair having a given potential on the mark terminal to indicate a mark or said given potential on the space terminal to indicate a space, a bus for each of the 2 conditions, p output terminals, one for each unit of the p -unit code and each of said p groups of conditions, a diode connecting each bus to the corresponding output terminal, and diodes con-

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necting each bus to the corresponding mark and/or space terminal of said source having said given potential thereon.

10. A code converter to convert from a mark-space code of n -units to a mark-space code of p -units, the codes being such that there are p groups of q conditions of relatively few units of the n -unit code wherein any one condition within a group defines at least one unit of the p -unit code and wherein there are r conditions of the n -unit code for which there is no equivalent p -unit code, 10 comprising, a source of a simultaneous signal of n -units, said source having n mark terminals and n space terminals grouped in n pairs, each pair having a given potential on the mark terminal to indicate a mark or said given potential on the space terminal to indicate a space, a bus 15 for each of the q conditions and a bus for each of the r conditions, $p+r$ output terminals, diodes connecting said q buses by groups to corresponding ones of said p

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output terminals and diodes connecting said r buses to said r output terminals, means to apply the signals on said source terminals corresponding to said q conditions to corresponding ones of said q buses, and means to apply the signals on said source terminals corresponding to said r conditions to said corresponding r output terminals.

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