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POLYPHASE LOGICAL CIRCUIT EMPLOYING COMPLEMENTARY MISFET'S

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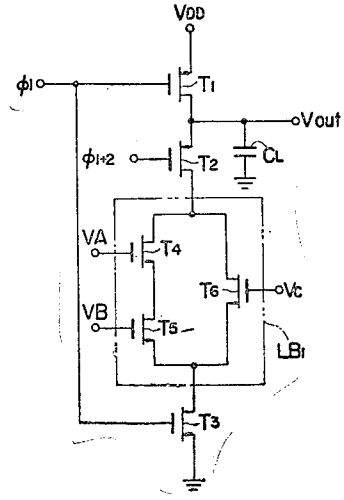
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2 Sheets Drawing. 10 Pages Specification



A complementary MOS logic circuit has a reduced number of transistors. A P-channel MOSFET and an N-channel MOSFET are connected in series with a logical block of a predetermined logical expression between one terminal of a power source and the logical block and between the logical block and the other terminal of the power source, respectively. Means is provided which drives the P-channel and N-channel MOSFETs by a first clock pulse. Means is provided which establishes a current path between the logical block and an output terminal of the complementary MOS logical circuit or between the connection point of the logical block and P-channel MOSFET and the output terminal at timings of the first clock pulse and a second clock pulse differing in phase therefrom.

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2 Sheets-Sheet 1

FIG. 1

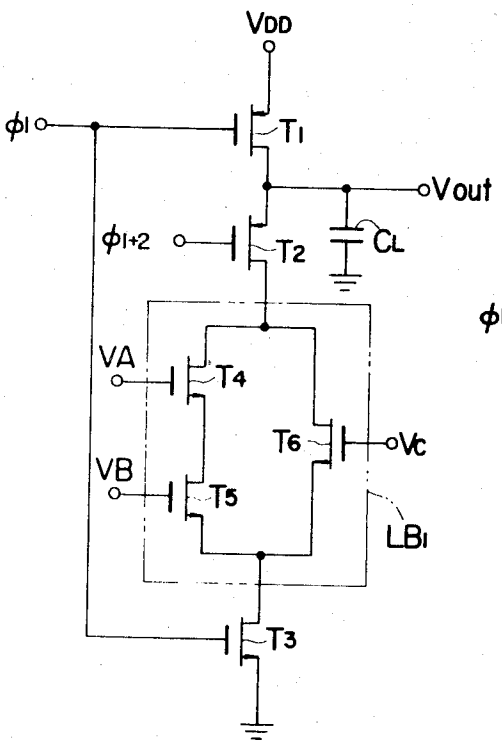


FIG. 2

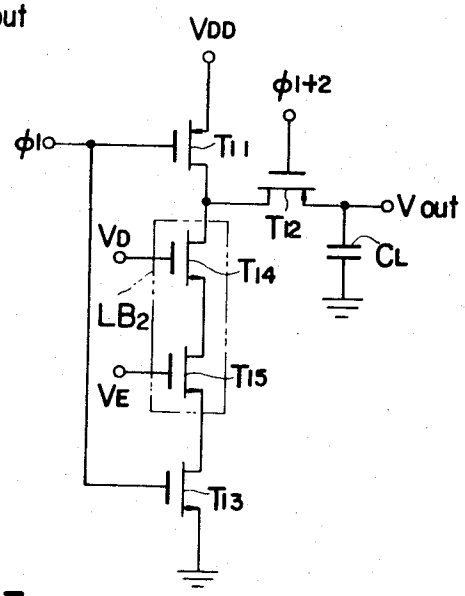
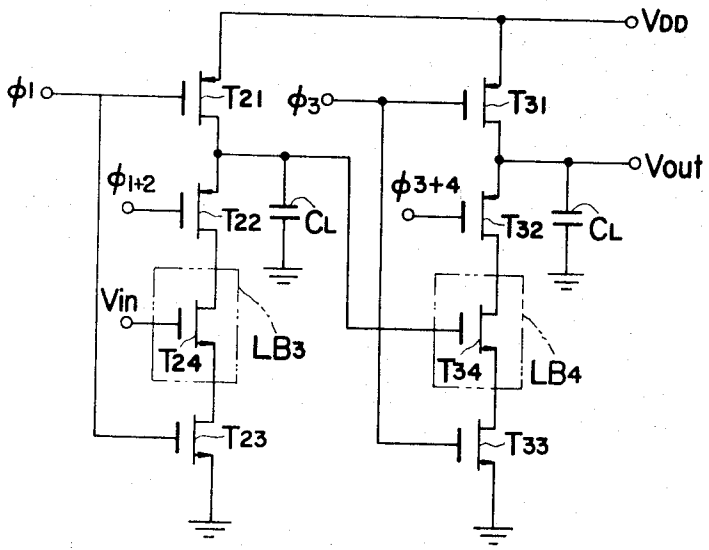


FIG. 3



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FIG. 4

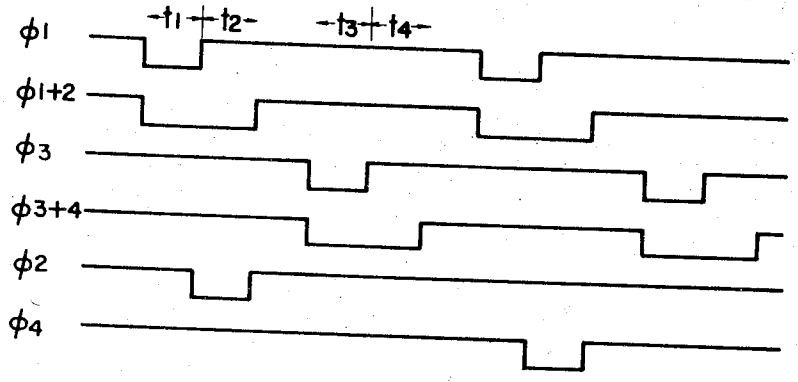


FIG. 5a

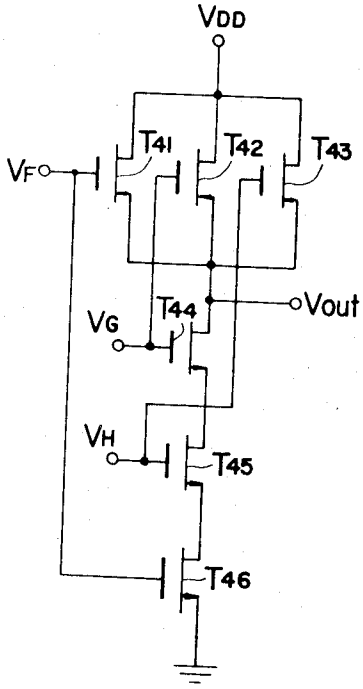


FIG. 5b

