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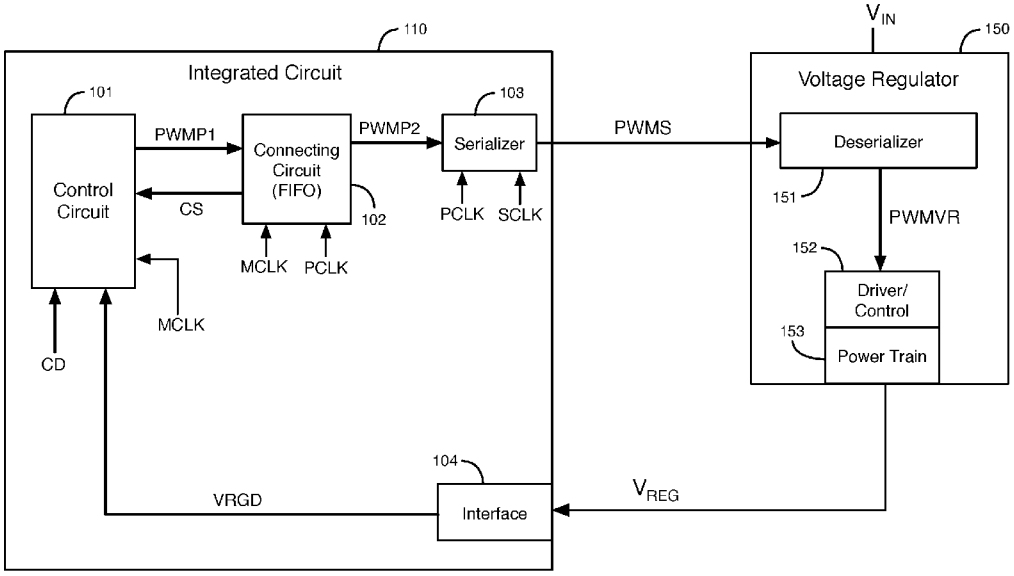


FIG. 1

(57) Abstract: An integrated circuit includes a control circuit, a first-in first-out circuit, and a serializer circuit. The control circuit generates parallel pulse-width modulation data in first parallel pulse-width modulation signals. The first-in first-out circuit stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals. The first-in first-out circuit outputs the stored parallel pulse-width modulation data in second parallel pulse-width modulation signals. The serializer circuit converts the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal.

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Techniques For Generating Pulse-Width Modulation Data

CROSS REFERENCE TO RELATED APPLICATION

[0001] This patent application claims priority to U.S. patent application 15/230,150, filed August 5, 2016, which is incorporated by reference herein in its entirety.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to electronic circuits, and more particularly, to techniques for generating pulse-width modulation data using electronic circuits.

BACKGROUND

[0003] Pulse-width modulation (PWM) is a technique that is used to encode data into a pulsing signal. PWM can be used, for example, to encode data for transmission or to control the power supplied to electrical devices, such as integrated circuits or motors. A voltage regulator may use PWM to control a voltage and a current provided to a load by turning a switch that is coupled between an input voltage source and the load on and off. The duration of time that the switch is on in each switching period of the switch determines the total power supplied to the load.

BRIEF SUMMARY

[0004] According to some embodiments, an integrated circuit includes a control circuit, a first-in first-out circuit, and a serializer circuit. The control circuit generates parallel pulse-width modulation data in first parallel pulse-width modulation signals. The first-in first-out circuit stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals. The first-in first-out circuit outputs the stored parallel pulse-width modulation data in second parallel pulse-width modulation signals. The serializer circuit converts the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal.

[0005] Embodiments of the present invention can be implemented in numerous ways, such as a process, an apparatus, a system, or a device. Various objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 illustrates a pulse-width modulation (PWM) control system for a voltage regulator, according to an embodiment of the present invention.

[0007] Figure 2 illustrates an exemplary waveform of the serial PWM output signal PWMS of the serializer circuit shown in Figure 1, according to an embodiment.

[0008] Figure 3 is a flow chart that illustrates examples of operations that may be performed by the control circuit in the PWM control system of Figure 1, according to an embodiment.

[0009] Figure 4 is a simplified partial block diagram of a field programmable gate array (FPGA) that can include embodiments of the present invention.

DETAILED DESCRIPTION

[0010] A previously known implementation of a circuit that generates a pulse-width modulation (PWM) signal has a counter that operates at a clock frequency that is based on the minimum pulse width that the circuit can generate in a varying logic signal. For example, if the minimum pulse width that the circuit can generate is 1 microsecond, the counter needs to run at 1 megahertz (MHz). A counter that runs at a clock frequency of the minimum pulse width limits the maximum frequency of the PWM output signal. A counter based PWM circuit is not flexible enough to generate PWM signals that are targeted for different protocols.

[0011] According to some embodiments, a system for generating a PWM signal includes a control circuit, a first-in first-out (FIFO) circuit, and a serializer circuit. The control circuit generates parallel pulse-width modulation (PWM) signals that indicate parallel PWM data. The parallel PWM data in the parallel PWM signals is provided from the control circuit to the serializer circuit through the FIFO circuit. The serialier circuit converts the parallel PWM data into serial PWM data and outputs the serial PWM data in a serial PWM signal.

[0012] These embodiments may allow the serial PWM data to be transmitted at a higher data rate than can be generated by the control circuit for the parallel PWM data. These embodiments may allow the control circuit to operate at a lower clock frequency

than the frequency of the serial PWM signal, which may ease the timing requirements imposed on the design of the control circuit. The serialization rate of the serializer circuit may be determined by the ratio between the clock frequency of the control circuit and the data rate of the serial PWM signal. In some embodiments, the control circuit may be programmed to generate PWM data according to different PWM protocols, for example, by programming or re-programming the control circuit using software or different configuration data.

[0013] Figure 1 illustrates a pulse-width modulation (PWM) control system for a voltage regulator, according to an embodiment of the present invention. Figure 1 illustrates an integrated circuit (IC) 110 and a voltage regulator circuit 150. Integrated circuit 110 may be, for example, a microprocessor, a central processing unit, or a programmable logic integrated circuit, to name a few examples. Examples of programmable logic integrated circuits include field programmable gate arrays (FPGAs), programmable logic devices (PLDs), programmable logic arrays (PLAs), etc.

[0014] Integrated circuit (IC) 110 has a PWM control system that includes a control circuit 101, a connecting circuit 102, a serializer circuit 103, and an interface circuit 104. Control circuit 101 functions as a PWM control circuit. Control circuit 101 may be, for example, a micro-controller circuit, a microprocessor circuit, or a central processing unit within IC 110. As another example, control circuit 101 may include an array of programmable logic circuits that are programmed by software or by configuration data to perform the functions of a PWM control circuit.

[0015] Voltage regulator circuit 150 includes deserializer circuit 151, driver and control circuit 152, and power train circuit 153. Voltage regulator circuit 150 may include one or more integrated circuits and/or discrete circuits. Voltage regulator circuit 150 may also be referred to as a power converter circuit or as a DC/DC converter circuit.

[0016] Control circuit 101 generates parallel pulse-width modulation (PWM) data. Control circuit 101 may, for example, be programmed to generate the PWM data by software or by configuration data. The software or configuration data may, for example, be provided to control circuit 101 in signals CD. Control circuit 101 may generate the PWM data in response to a periodic clock signal MCLK that is provided to an input of control circuit 101. The PWM data may, for example, be stored in a data structure array in memory in control circuit 101 or in another area of IC 110. The PWM data generated

by control circuit 101 digitally encodes the duty cycle of a serial PWM signal to be output by serializer circuit 103.

[0017] The PWM data generated by control circuit 101 is output as parallel PWM data in parallel PWM signals PWMP1. Signals PWMP1 may include any suitable number of parallel signals. Parallel signals PWMP1 are provided to inputs of connecting circuit 102. Connecting circuit 102 generates parallel PWM signals PWMP2 based on parallel PWM signals PWMP1. Connecting circuit 102 provides the parallel PWM data indicated by signals PWMP1 to serializer circuit 103 in parallel PWM signals PWMP2.

[0018] Connecting circuit 102 may be, for example, a storage circuit that stores the parallel PWM data indicated by signals PWMP1. As a specific example, connecting circuit 102 may be a first-in first-out (FIFO) circuit. In some embodiments, the FIFO circuit may be part of control circuit 101 or part of serializer circuit 103.

[0019] In embodiments in which connecting circuit 102 is a FIFO circuit, the FIFO circuit in connecting circuit 102 converts the parallel PWM data generated by control circuit 101 in signals PWMP1 from the clock domain of clock signal MCLK to the clock domain of another clock signal PCLK. Clock signals MCLK and PCLK may have different frequencies or phases. The FIFO circuit may be synchronous or asynchronous, depending on whether clock signals MCLK and PCLK are synchronous or asynchronous, respectively. PCLK may be referred to as a parallel clock signal.

[0020] Clock signals MCLK and PCLK are provided to inputs of the FIFO circuit in connecting circuit 102. The FIFO circuit stores the parallel PWM data indicated by signals PWMP1 in response to clock signal MCLK. The FIFO circuit outputs the stored parallel PWM data as signals PWMP2 in response to clock signal PCLK. The FIFO circuit in connecting circuit 102 also generates control signals CS that are provided to control circuit 101. The control signals CS generated by the FIFO circuit may include, for example, a FIFO full signal and a FIFO empty signal. The FIFO full signal indicates when the FIFO circuit is full of data (i.e., the FIFO circuit has no more storage space to store additional data). The FIFO empty signal indicates when the FIFO circuit is empty.

[0021] Parallel PWM signals PWMP2 are provided to inputs of serializer circuit 103. Clock signal PCLK is provided to another input of serializer circuit 103. A third periodic clock signal SCLK is provided to yet another input of serializer circuit 103. Clock signal

SCLK may be referred to as a serial clock signal. Clock signals MCLK, PCLK, and SCLK may, for example, be generated by one or more phase-locked loop or delay-locked loop circuits. The serializer circuit 103 may, for example, be a high-speed serializer circuit (e.g., up to 20 gigahertz (GHz)) such as a SERDES interface or a low voltage differential signaling (LVDS) interface serializer.

[0022] Serializer circuit 103 includes a parallel-to-serial converter circuit that converts the parallel PWM data indicated by signals PWMP2 into serial PWM data in serial PWM signal PWMS in response to clock signals PCLK and/or SCLK. The duty cycle of serial PWM signal PWMS is the serial PWM data generated by the serializer circuit 103. The serialization rate of serializer circuit 103 may, for example, be based on the ratio between the frequency of clock signal PCLK and the frequency of clock signal SCLK or signal PWMS. The serialization rate of serializer circuit 103 may be set to a value that allows the control circuit 101 to operate at a much lower frequency than the frequency of the serial PWM signal PWMS.

[0023] The parallel-to-serial converter circuit in serializer circuit 103 may include a shift register circuit. The parallel PWM data indicated by parallel PWM signals PWMP2 are loaded into the shift register in response to the parallel clock signal PCLK. Parallel PWM data may, for example, be loaded into the shift register in each period of PCLK. The parallel PWM data stored in the shift register is serially shifted out of the shift register as serial PWM data in serial PWM signal PWMS in response to the serial clock signal SCLK. Serial PWM data may, for example, be shifted out of the shift register in each period of SCLK. In an exemplary embodiment, the least significant bit (LSB) of the serial PWM data bits from each group of parallel PWM data bits may be shifted out of the shift register first.

[0024] Serial PWM signal PWMS may be a single-ended signal on one wire or a differential signal on two wires. Serial PWM signal PWMS is transmitted outside IC 110 through one or more external wires to voltage regulator circuit 150. Serializer circuit 103 may, for example, include an output driver circuit that drives serial PWM signal PWMS from IC 110 to voltage regulator circuit 150. Serial PWM signal PWMS is provided to deserializer circuit 151 in voltage regulator 150. Deserializer circuit 151 includes a serial-to-parallel converter circuit (e.g., a shift register) that converts the serial PWM data

indicated by serial PWM signal PWMS into parallel PWM data in parallel PWM signals PWMVR.

[0025] Parallel PWM signals PWMVR are provided to inputs of driver and control circuit 152. Power train circuit 153 includes one or more switch circuits (e.g., switching transistors). Driver and control circuit 152 converts the parallel PWM data indicated by parallel PWM signals PWMVR into one or more drive signals that control the on and off switching of the one or more switch circuits in the power train circuit 153. Thus, driver and control circuit 152 controls the duty cycle(s) of the one or more switch circuits in power train circuit 153 based on the parallel PWM data indicated by parallel PWM signals PWMVR. The parallel PWM data indicated by parallel PWM signals PWMVR is the same PWM data provided by control circuit 101 in signals PWMP1.

[0026] Power train circuit 153 may also include an inductor and a capacitor. Voltage regulator circuit 150 converts an unregulated input voltage V_{IN} into a regulated output voltage V_{REG} at its output. Voltage regulator circuit 150 may, for example, provide current from input voltage V_{IN} through the one or more switch circuits and the inductor to its output at V_{REG}. The capacitor in power train circuit 153 helps to reduce the voltage ripple in voltage V_{REG} that is caused by the switching of the one or more switch circuits in power train circuit 153.

[0027] Voltage V_{REG} is provided through an external wire to interface circuit 104 in IC 110. Interface circuit 104 may, for example, include an analog-to-digital converter circuit that converts the analog value of voltage V_{REG} into a set of digital signals VRGD that indicate the analog value of voltage V_{REG}. Digital signals VRGD are provided to inputs of control circuit 101 in IC 110.

[0028] Control circuit 101 adjusts the values of the parallel PWM data indicated by parallel PWM signals PWMP1 and PWMP2 based on changes in the voltage V_{REG} as indicated by the digital signals VRGD. In response to control circuit 101 adjusting the values of the parallel PWM data indicated by signals PWMP1-PWMP2, serializer circuit 103 changes the duty cycle of signal PWMS. In response to changes in the duty cycle of signal PWMS, voltage regulator circuit 150 varies the parallel PWM data indicated by signals PWMVR, which changes the duty cycle(s) of the one or more switch circuits in power train circuit 153. Changes in the duty cycle(s) of the one or more switch circuits in

power train circuit 153 cause power train circuit 153 to adjust the current provided to the output of voltage regulator circuit 150.

[0029] For example, if the voltage V_{REG} decreases below a threshold voltage, control circuit 101 may adjust the values of the parallel PWM data indicated by parallel PWM signals PWMP1 to cause voltage regulator circuit 150 to provide more current from voltage V_{IN} to its output in order to increase the voltage V_{REG} back to the threshold voltage. If the voltage V_{REG} increases above the threshold voltage, control circuit 101 may adjust the values of the parallel PWM data indicated by parallel PWM signals PWMP1 to cause voltage regulator circuit 150 to provide less current from voltage V_{IN} to its output in order to decrease the voltage V_{REG} back to the threshold voltage. The control circuit 101 may adjust the threshold voltage based on the varying voltage requirements of load circuits that receive voltage V_{REG}.

[0030] In the embodiment of Figure 1, the serial PWM signal PWMS may have a greater frequency than can be generated by control circuit 101 for the parallel PWM data signals PWMP1 if, for example, the frequency of clock signal SCLK is greater than the frequency of clock signal MCLK. The embodiment of Figure 1 may allow control circuit 101 to operate at a lower clock frequency than the frequency of the serial PWM signal PWMS, which may ease the timing requirements imposed on the design of control circuit 101. In some embodiments, the control circuit 101 may be programmed to generate PWM data according to different PWM protocols at different times, for example, by programming or re-programming control circuit 101 using different software or different configuration data provided to control circuit 101 in signals CD.

[0031] Figure 2 illustrates an exemplary waveform of the serial PWM output signal PWMS of serializer circuit 103, according to an embodiment. As shown in the example of Figure 2, signal PWMS has a constant frequency and a varying duty cycle. In the example of Figure 2, serializer circuit 103 has a serial multiplication factor of 10, and signal PWMS has a default duty cycle of 50% after initialization. After initialization, serializer circuit 103 adjusts the duty cycle of signal PWMS in response to control circuit 101 adjusting the parallel PWM data indicated by signals PWMP1-PWMP2 based on changes in voltage V_{REG}, as described above. In the example of Figure 2, serializer circuit 103 increases the duty cycle of signal PWMS from 50% to 90% in response to the parallel PWM data in signals PWMP2 having a hexadecimal value 10'b1111111110 that

indicates a 90% duty cycle. Serializer circuit 103 then decreases the duty cycle of signal PWMS from 90% to 60% in response to the parallel PWM data in signals PWMP2 having a hexadecimal value 10'b1111110000 that indicates a 60% duty cycle. The duty cycle of signal PWMS remains at 60% for at least 3 periods in the example of Figure 2. Control circuit 101 and serializer circuit 103 may, for example, cause the duty cycle of signal PWMS to increase and decrease in response to voltage V_{REG} decreasing and increasing, respectively.

[0032] In some embodiments, different duty cycles in signal PWMS may cause voltage regulator circuit 150 to generate different voltages in V_{REG}. As examples that are not intended to be limiting, duty cycles in signal PWMS of 50%, 90%, and 60% may cause voltage regulator circuit 150 to generate voltages of 0.85 volts, 0.89 volts, and 0.86 volts, respectively, in voltage V_{REG}.

[0033] According to other embodiments, the PWM control system in IC 110 of Figure 1 may be used in other PWM applications. For example, the PWM control system in IC 110 may be used to generate a PWM signal as a modulated data signal for data transmission between integrated circuits in a circuit system. As other examples, the PWM control system in IC 110 may be used to generate a PWM signal for controlling a motor or a photovoltaic solar battery charger. The PWM control system in IC 110 may be used in any system that uses a PWM controller, including any type of power management system.

[0034] Figure 3 is a flow chart that illustrates examples of operations that may be performed by control circuit 101 in the PWM control system in IC 110 of Figure 1, according to an embodiment. In operation 301, control circuit 101 starts the PWM control process, for example, in response to an input signal from a user or from other circuitry in IC 110. In operation 302, control circuit 101 creates an array containing PWM data. The array is a data structure that is stored in memory in control circuit 101 or in another area of IC 110. In operation 303, control circuit 101 determines if the array is empty. If the control circuit 101 determines that the array is empty in operation 303, then the process ends in operation 304. If the control circuit 101 determines that the array is not empty in operation 303, control circuit 101 then determines if the FIFO circuit in connecting circuit 102 is full in operation 305. If the FIFO circuit has no storage space to store additional PWM data without overwriting PWM data that has not been output in

signals PWMP2, then the FIFO circuit asserts a FIFO full signal that is provided to control circuit 101 in signals CS. Thus, control circuit 101 may determine when the FIFO circuit is full based on signals CS.

[0035] If the control circuit 101 determines in operation 305 that the FIFO circuit in connecting circuit 102 is full, control circuit 101 enters a delay mode in operation 306 during which control circuit 101 does not output PWM data for a period of time. After the delay period of time of operation 306, the control circuit 101 repeats operation 305 to determine if the FIFO circuit in connecting circuit 102 is still full. The FIFO circuit continues to output stored parallel PWM data in signals PWMP2, which causes the FIFO circuit to no longer be full after a period of time. If the control circuit 101 determines in operation 305 that the FIFO circuit in connecting circuit 102 is not full, then control circuit 101 loads parallel PWM data into the FIFO circuit from an entry in the array in operation 307. Control circuit 101 then deletes the entry from the array in operation 308 that was just loaded into the FIFO circuit in the previous iteration of operation 307. The control circuit 101 then returns to operation 303 and performs additional iterations of operations 305-308 until the array is empty, and the process ends in operation 304.

[0036] Figure 4 is a simplified partial block diagram of a field programmable gate array (FPGA) 400 that can include embodiments of the present invention. FPGA 400 is an example of an integrated circuit that can be used as integrated circuit 110. FPGA 400 is merely one example of an integrated circuit that can include features of the present invention. Embodiments of the present invention can be used in numerous types of integrated circuits, such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), complex programmable logic devices (CPLDs), programmable logic arrays (PLAs), microprocessors, central processing units, etc.

[0037] FPGA 400 includes a two-dimensional array of programmable logic array blocks (or LABs) 402 that are interconnected by a network of vertical and horizontal interconnect resources of varying length and speed. Each of LABs 402 includes multiple (e.g., 10) logic elements (or LEs).

[0038] A logic element (LE) is a programmable logic circuit that provides for efficient implementation of user defined logic functions. An FPGA has numerous logic elements that can be configured to implement various combinatorial and sequential functions. The logic elements have access to programmable interconnect resources. The programmable

interconnect resources can be programmed to interconnect the logic elements in almost any desired configuration.

[0039] FPGA 400 may also include a distributed memory structure including random access memory (RAM) circuits of varying sizes provided throughout the array. The RAM circuits include, for example, circuits 404, circuits 406, and circuit 408. These memory circuits can also include shift registers and first-in first-out (FIFO) circuits.

[0040] FPGA 400 may further include digital signal processing (DSP) circuits 410 that can implement, for example, multipliers with add or subtract features. Input/output elements (IOEs) 412 located, in this example, around the periphery of the IC, support numerous single-ended and differential input/output standards. IOEs 412 are coupled to pads. Each of the pads is an external terminal of the FPGA.

[0041] The integrated circuits described herein may be part of a data processing system that includes one or more of the following components; a processor; memory; input/output circuitry; and peripheral devices.

[0042] Although the method operations were described in a specific order, it should be understood that other operations may be performed in between described operations, described operations may be adjusted so that they occur at slightly different times or in a different order, or described operations may be distributed in a system that allows the occurrence of the processing operations at various intervals associated with the processing.

[0043] The following examples pertain to further embodiments. Example 1 is an integrated circuit comprising: a control circuit that generates parallel pulse-width modulation data in first parallel pulse-width modulation signals; a first-in first-out circuit that stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals, wherein the first-in first-out circuit outputs the stored parallel pulse-width modulation data in second parallel pulse-width modulation signals; and a serializer circuit that converts the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal.

[0044] In Example 2, the subject matter of Example 1 can optionally include wherein the control circuit is programmed by software or configuration data to generate the parallel pulse-width modulation data.

[0045] In Example 3, the subject matter of any one of Examples 1-2 can optionally include wherein the control circuit is reprogrammable to generate the parallel pulse-width modulation data based on different protocols.

[0046] In Example 4, the subject matter of any one of Examples 1-3 can optionally include wherein the first-in first-out circuit stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals in response to a first clock signal, and wherein the first-in first-out circuit outputs the stored parallel pulse-width modulation data in the second parallel pulse-width modulation signals in response to a second clock signal.

[0047] In Example 5, the subject matter of Example 4 can optionally include wherein the control circuit generates the parallel pulse-width modulation data in response to the first clock signal, and wherein the serializer circuit converts the parallel pulse-width modulation data to the serial pulse-width modulation data in response to the second clock signal and in response to a third clock signal.

[0048] In Example 6, the subject matter of any one of Examples 1-5 can optionally include wherein the first-in first-out circuit generates a full signal that is provided to the control circuit, and wherein the control circuit only provides the parallel pulse-width modulation data to the first-in first-out circuit in the first parallel pulse-width modulation signals in response to the full signal indicating that the first-in first-out circuit is not full.

[0049] In Example 7, the subject matter of any one of Examples 1-6 can optionally include wherein the serializer circuit varies a duty cycle of the serial pulse-width modulation signal based on changes in the parallel pulse-width modulation data generated by the control circuit.

[0050] In Example 8, the subject matter of any one of Examples 1-7 can optionally further include an interface circuit that receives a regulated voltage from a voltage regulator circuit, wherein the interface circuit generates digital signals that indicate the regulated voltage, wherein the digital signals are provided to the control circuit, and

wherein the control circuit adjusts the parallel pulse-width modulation data based on changes in the regulated voltage generated by the voltage regulator circuit.

[0051] In Example 9, the subject matter of any one of Examples 1-8 can optionally include wherein the control circuit comprises programmable logic circuits, and wherein the integrated circuit is a programmable logic integrated circuit.

[0052] Example 10 is an integrated circuit comprising: a control circuit that generates parallel pulse-width modulation data in first parallel pulse-width modulation signals in response to a first clock signal; a first-in first-out circuit that stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals in response to the first clock signal, wherein the first-in first-out circuit outputs the stored parallel pulse-width modulation data in second parallel pulse-width modulation signals in response to a second clock signal; and a serializer circuit that converts the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal in response to the second clock signal.

[0053] In Example 11, the subject matter of Example 10 can optionally include wherein the serializer circuit converts the parallel pulse-width modulation data to the serial pulse-width modulation data in response to a third clock signal, and wherein a frequency of the third clock signal is greater than frequencies of the first and second clock signals.

[0054] In Example 12, the subject matter of any one of Examples 10-11 can optionally include wherein the control circuit is reprogrammable to generate the parallel pulse-width modulation data based on different pulse-width modulation protocols.

[0055] In Example 13, the subject matter of any one of Examples 10-12 can optionally further include an interface circuit that receives a regulated voltage from a voltage regulator circuit, wherein the interface circuit generates digital signals that indicate the regulated voltage, wherein the digital signals are provided to the control circuit, and wherein the control circuit adjusts the parallel pulse-width modulation data based on changes in the regulated voltage as indicated by the digital signals.

[0056] In Example 14, the subject matter of any one of Examples 10-13 can optionally include wherein the control circuit comprises programmable logic circuits, and wherein the integrated circuit is a programmable logic integrated circuit.

[0057] In Example 15, the subject matter of any one of Examples 10-14 can optionally include wherein the serializer circuit varies a duty cycle of the serial pulse-width modulation signal based on changes in the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals.

[0058] Example 16 is a method comprising: generating parallel pulse-width modulation data in first parallel pulse-width modulation signals using a control circuit in an integrated circuit; storing the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals in a first-in first-out circuit in the integrated circuit in response to a first clock signal; outputting the stored parallel pulse-width modulation data from the first-in first-out circuit in second parallel pulse-width modulation signals in response to a second clock signal; and converting the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal using a serializer circuit in the integrated circuit.

[0059] In Example 17, the subject matter of Example 16 can optionally include wherein the control circuit generates the parallel pulse-width modulation data in response to the first clock signal, and wherein the serializer circuit converts the parallel pulse-width modulation data to the serial pulse-width modulation data in response to the second clock signal.

[0060] In Example 18, the subject matter of any one of Examples 16-17 can optionally further include: generating digital signals that indicate a regulated voltage received from a voltage regulator circuit using an interface circuit in the integrated circuit; providing the digital signals to the control circuit; and adjusting the parallel pulse-width modulation data based on changes in the regulated voltage as indicated by the digital signals using the control circuit.

[0061] In Example 19, the subject matter of any one of Examples 16-18 can optionally further include: programming the control circuit to generate the parallel pulse-width modulation data based on a first pulse-width modulation protocol; and reprogramming the control circuit to generate the parallel pulse-width modulation data based on a second pulse-width modulation protocol.

[0062] In Example 20, the subject matter of any one of Examples 16-19 can optionally further include: varying a duty cycle of the serial pulse-width modulation signal based on changes in the parallel pulse-width modulation data using the serializer circuit.

[0063] The foregoing description of the exemplary embodiments of the present invention is not intended to be exhaustive or to limit the present invention to the examples disclosed herein. In some instances, features of the present invention can be employed without a corresponding use of other features as set forth. Many modifications, substitutions, and variations are possible in light of the above teachings, without departing from the scope of the present invention.

What is claimed is:

1. An integrated circuit comprising:

a control circuit that generates parallel pulse-width modulation data in first parallel pulse-width modulation signals;

a first-in first-out circuit that stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals, wherein the first-in first-out circuit outputs the stored parallel pulse-width modulation data in second parallel pulse-width modulation signals; and

a serializer circuit that converts the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal.

2. The integrated circuit of claim 1, wherein the control circuit is programmed by software or configuration data to generate the parallel pulse-width modulation data.

3. The integrated circuit of claim 2, wherein the control circuit is reprogrammable to generate the parallel pulse-width modulation data based on different protocols.

4. The integrated circuit of claim 1, wherein the first-in first-out circuit stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals in response to a first clock signal, and wherein the first-in first-out circuit outputs the stored parallel pulse-width modulation data in the second parallel pulse-width modulation signals in response to a second clock signal.

5. The integrated circuit of claim 4, wherein the control circuit generates the parallel pulse-width modulation data in response to the first clock signal, and wherein the serializer circuit converts the parallel pulse-width modulation data to the serial pulse-width modulation data in response to the second clock signal and in response to a third clock signal.

6. The integrated circuit of claim 1, wherein the first-in first-out circuit generates a full signal that is provided to the control circuit, and wherein the control circuit only provides the parallel pulse-width modulation data to the first-in

first-out circuit in the first parallel pulse-width modulation signals in response to the full signal indicating that the first-in first-out circuit is not full.

7. The integrated circuit of claim 1, wherein the serializer circuit varies a duty cycle of the serial pulse-width modulation signal based on changes in the parallel pulse-width modulation data generated by the control circuit.

8. The integrated circuit of claim 1, further comprising:

an interface circuit that receives a regulated voltage from a voltage regulator circuit, wherein the interface circuit generates digital signals that indicate the regulated voltage, wherein the digital signals are provided to the control circuit, and wherein the control circuit adjusts the parallel pulse-width modulation data based on changes in the regulated voltage generated by the voltage regulator circuit.

9. The integrated circuit of claim 1, wherein the control circuit comprises programmable logic circuits, and wherein the integrated circuit is a programmable logic integrated circuit.

10. An integrated circuit comprising:

a control circuit that generates parallel pulse-width modulation data in first parallel pulse-width modulation signals in response to a first clock signal;

a first-in first-out circuit that stores the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals in response to the first clock signal, wherein the first-in first-out circuit outputs the stored parallel pulse-width modulation data in second parallel pulse-width modulation signals in response to a second clock signal; and

a serializer circuit that converts the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal in response to the second clock signal.

11. The integrated circuit of claim 10, wherein the serializer circuit converts the parallel pulse-width modulation data to the serial pulse-width modulation data in response to a third clock signal, and wherein a frequency of the third clock signal is greater than frequencies of the first and second clock signals.

12. The integrated circuit of claim 10, wherein the control circuit is reprogrammable to generate the parallel pulse-width modulation data based on different pulse-width modulation protocols.

13. The integrated circuit of claim 10, further comprising:

an interface circuit that receives a regulated voltage from a voltage regulator circuit, wherein the interface circuit generates digital signals that indicate the regulated voltage, wherein the digital signals are provided to the control circuit, and wherein the control circuit adjusts the parallel pulse-width modulation data based on changes in the regulated voltage as indicated by the digital signals.

14. The integrated circuit of claim 10, wherein the control circuit comprises programmable logic circuits, and wherein the integrated circuit is a programmable logic integrated circuit.

15. The integrated circuit of claim 10, wherein the serializer circuit varies a duty cycle of the serial pulse-width modulation signal based on changes in the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals.

16. A method comprising:

generating parallel pulse-width modulation data in first parallel pulse-width modulation signals using a control circuit in an integrated circuit;

storing the parallel pulse-width modulation data indicated by the first parallel pulse-width modulation signals in a first-in first-out circuit in the integrated circuit in response to a first clock signal;

outputting the stored parallel pulse-width modulation data from the first-in first-out circuit in second parallel pulse-width modulation signals in response to a second clock signal; and

converting the parallel pulse-width modulation data indicated by the second parallel pulse-width modulation signals to serial pulse-width modulation data in a serial pulse-width modulation signal using a serializer circuit in the integrated circuit.

17. The method of claim 16, wherein the control circuit generates the parallel pulse-width modulation data in response to the first clock signal, and

wherein the serializer circuit converts the parallel pulse-width modulation data to the serial pulse-width modulation data in response to the second clock signal.

18. The method of claim 16, further comprising:

generating digital signals that indicate a regulated voltage received from a voltage regulator circuit using an interface circuit in the integrated circuit;

providing the digital signals to the control circuit; and

adjusting the parallel pulse-width modulation data based on changes in the regulated voltage as indicated by the digital signals using the control circuit.

19. The method of claim 16, further comprising:

programming the control circuit to generate the parallel pulse-width modulation data based on a first pulse-width modulation protocol; and

reprogramming the control circuit to generate the parallel pulse-width modulation data based on a second pulse-width modulation protocol.

20. The method of claim 16, further comprising:

varying a duty cycle of the serial pulse-width modulation signal based on changes in the parallel pulse-width modulation data using the serializer circuit.

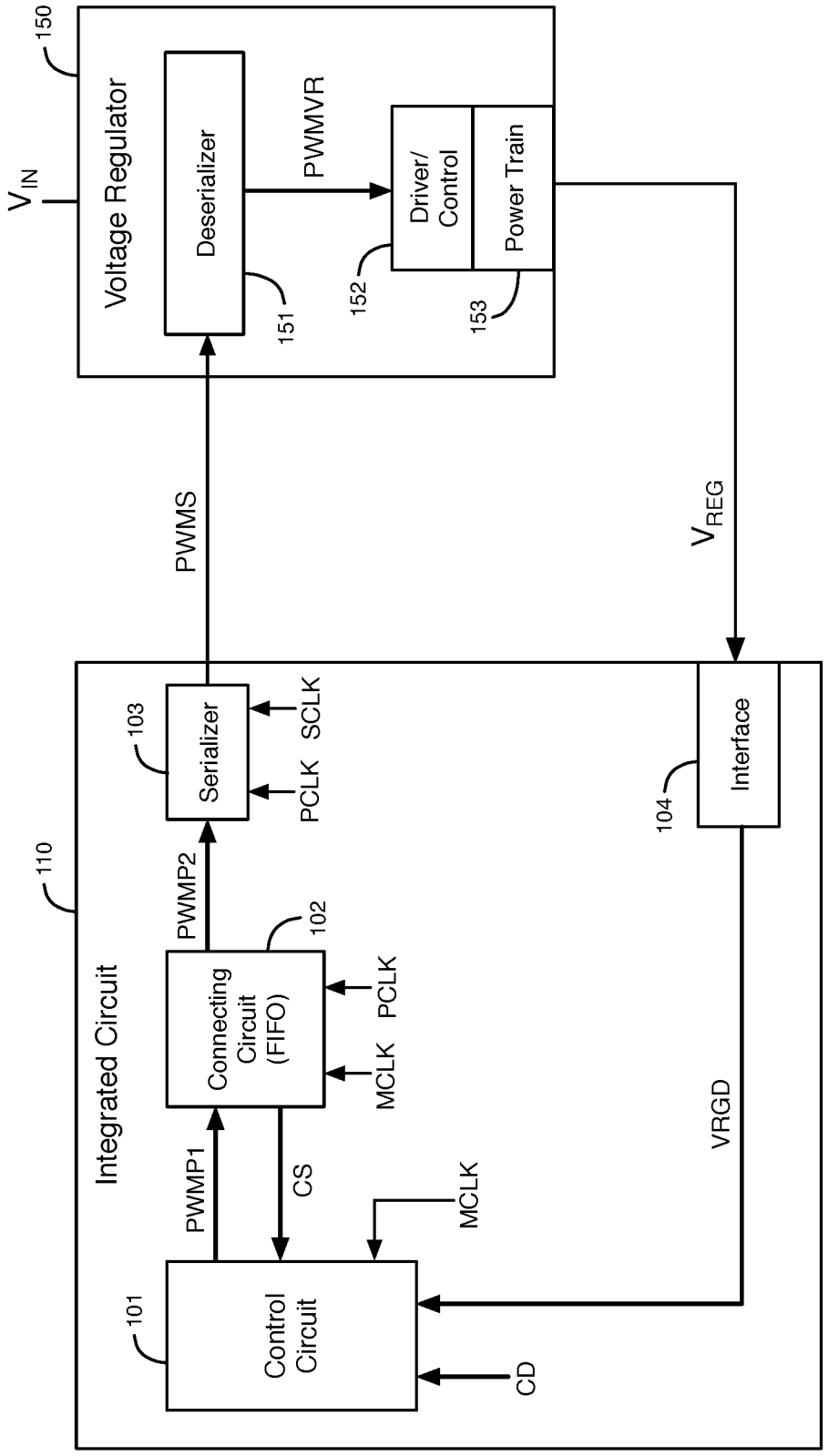

150
Voltage Regulator
V_{IN}
Deserializer
PWMVR
Driver/ Control
Power Train
151
152
153
PWMS
V_{REG}
110
Integrated Circuit
103
Serializer
SCLK
PCLK
104
Interface
PWMP2
102
Connecting Circuit (FIFO)
PCLK
MCLK
PWMP1
CS
MCLK
VRGD
101
Control Circuit
CD

FIG. 1

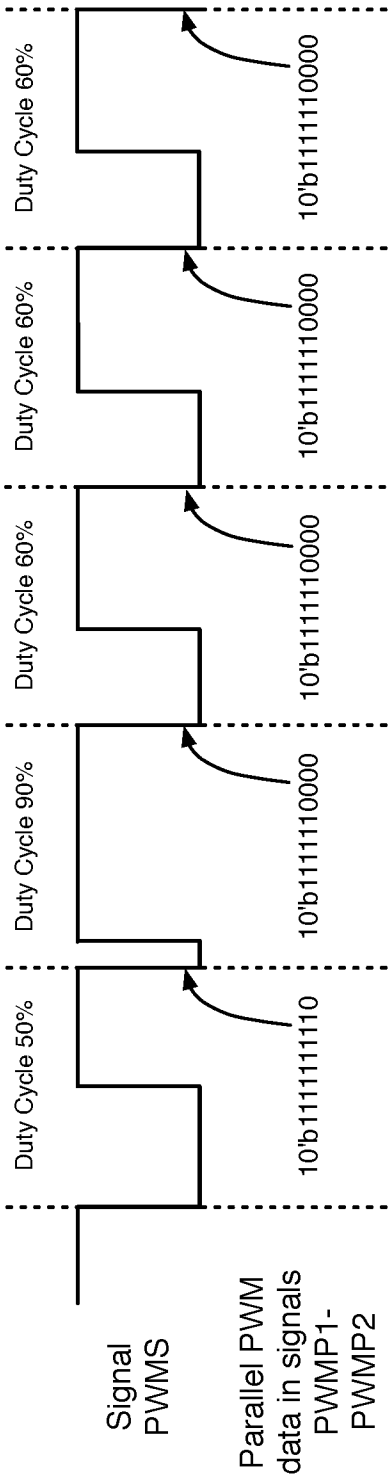

Signal PWMS
Parallel PWM data in signals PWMP1-PWMP2
Duty Cycle 50%
10'b1111111110
Duty Cycle 90%
10'b1111110000
Duty Cycle 60%
10'b1111110000
Duty Cycle 60%
10'b1111110000
Duty Cycle 60%
10'b1111110000

FIG. 2

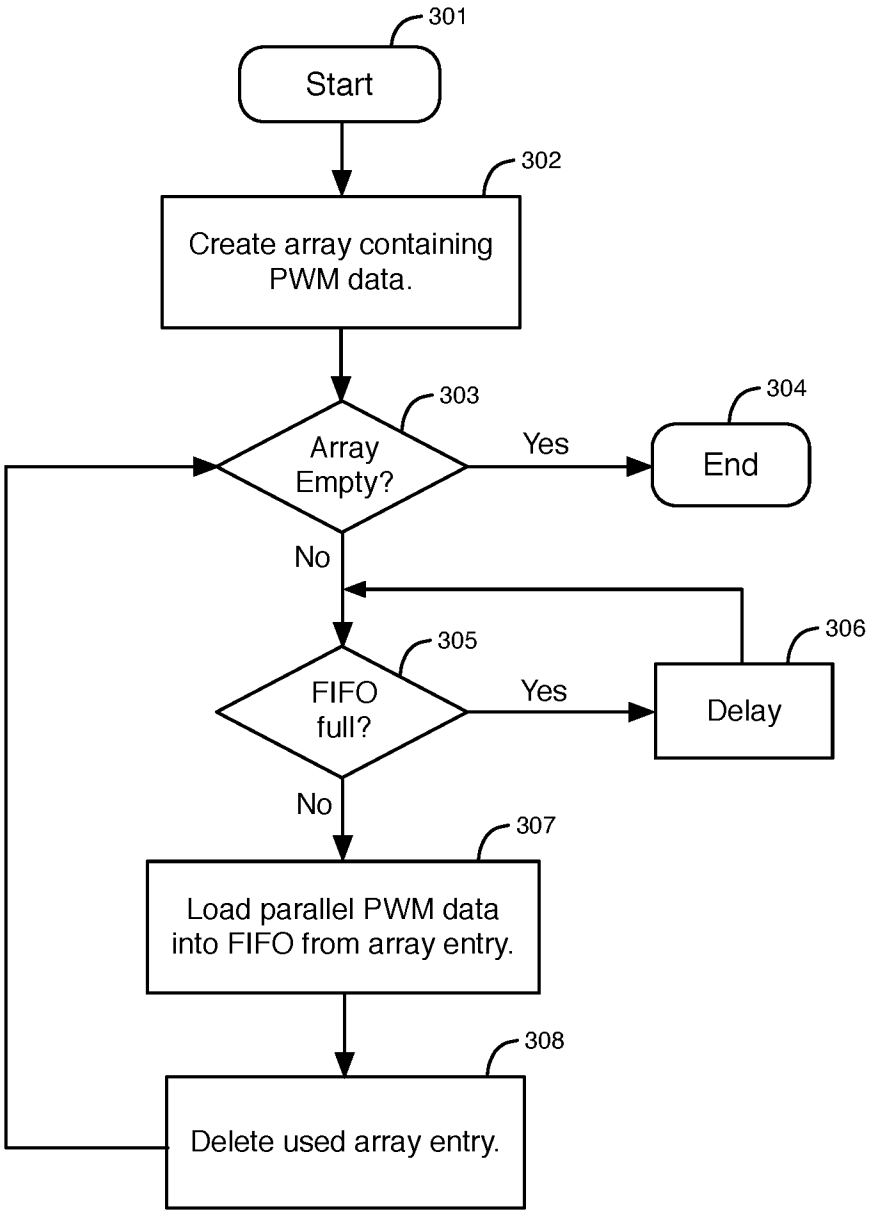

301
Start
302
Create array containing PWM data.
303
Array Empty?
Yes
304
End
No
305
FIFO full?
Yes
306
Delay
No
307
Load parallel PWM data into FIFO from array entry.
308
Delete used array entry.

FIG. 3

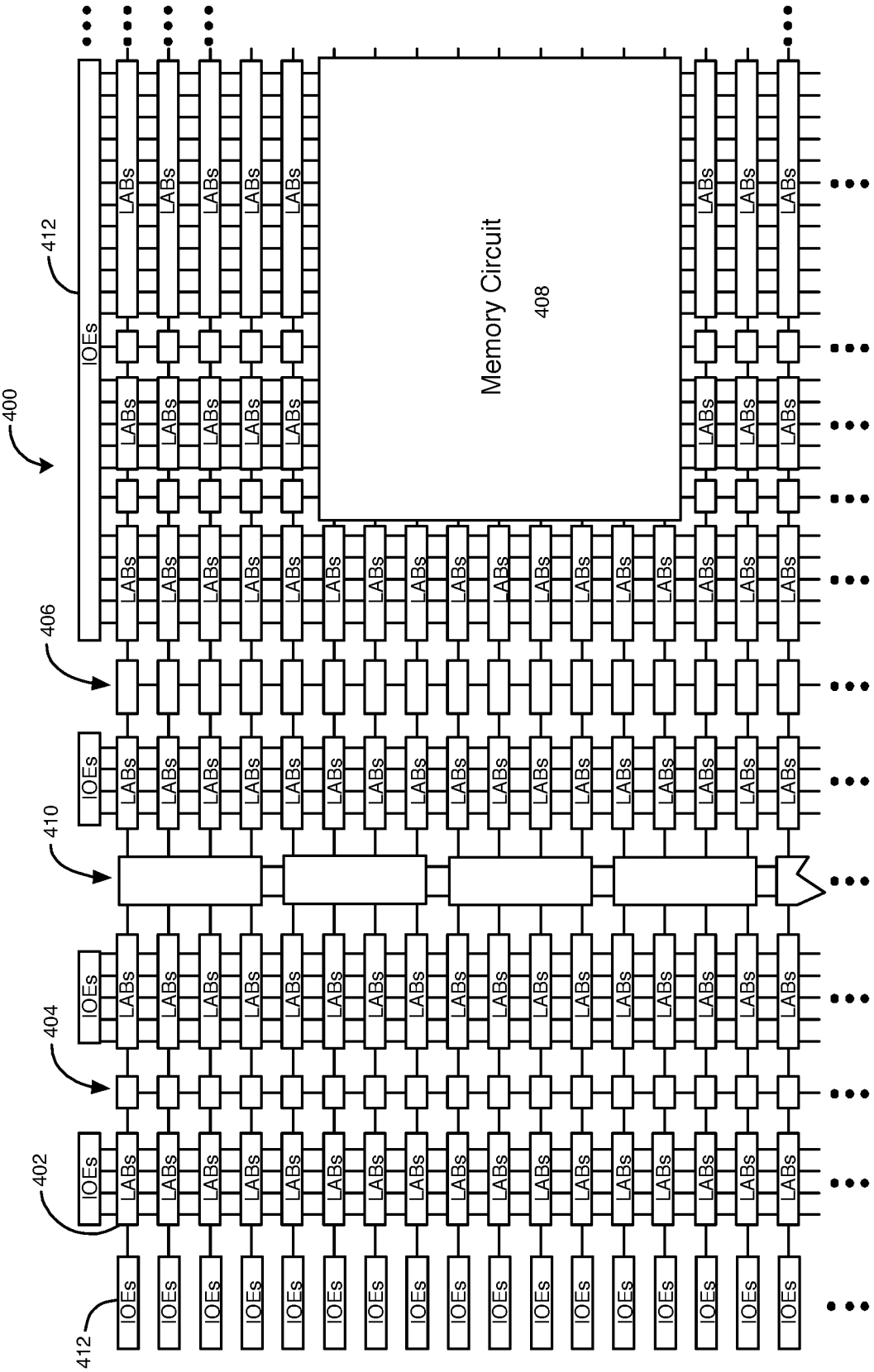


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/041059

A. CLASSIFICATION OF SUBJECT MATTER

H03K 7/08(2006.01)i, H03M 3/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K 7/08; G11C 7/00; G06F 3/00; H03K 19/00; H03F 3/217; H03K 3/017; G05F 1/575; H03M 3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: control circuit, controller, first-in first-out, serializer, pulse width

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2015-0077181 A1 (QUALCOMM INCORPORATED) 19 March 2015 See paragraphs [0024]-[0046] and figures 3-5.	1-20
Y	US 2005-0242858 A1 (DAVID A. FIGOLI et al.) 03 November 2005 See paragraphs [0009], [0026]-[0048] and figure 3.	1-20
A	US 2016-0011611 A1 (SANDISK TECHNOLOGIES INC.) 14 January 2016 See paragraphs [0032]-[0036] and figure 1.	1-20
A	US 2011-0299351 A1 (DAVID P. SCHULTZ et al.) 08 December 2011 See paragraphs [0019]-[0037] and figure 1.	1-20
A	US 2012-0260002 A1 (BRET S. HILDEBRAN et al.) 11 October 2012 See paragraphs [0057]-[0065] and figure 9.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 October 2017 (16.10.2017)	**17 October 2017 (17.10.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/041059

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015-0077181 A1	19/03/2015	US 9197172 B2	24/11/2015
		WO 2015-042062 A2	26/03/2015
		WO 2015-042062 A3	21/05/2015
US 2005-0242858 A1	03/11/2005	None	
US 2016-0011611 A1	14/01/2016	US 9535438 B2	03/01/2017
		WO 2016-007232 A1	14/01/2016
US 2011-0299351 A1	08/12/2011	CN 103039006 A	10/04/2013
		CN 103039006 B	02/09/2015
		EP 2577871 A1	10/04/2013
		EP 2577871 B1	09/09/2015
		JP 2013-531845 A	08/08/2013
		JP 5719926 B2	20/05/2015
		KR 10-1391118 B1	30/04/2014
		US 2011-0298511 A1	08/12/2011
		US 2011-0299347 A1	08/12/2011
		US 2011-0302356 A1	08/12/2011
		US 8270235 B2	18/09/2012
		US 8358553 B2	22/01/2013
		US 8438326 B2	07/05/2013
		US 8446195 B2	21/05/2013
		WO 2011-153107 A1	08/12/2011
US 2012-0260002 A1	11/10/2012	CN 103019163 A	03/04/2013
		CN 103019163 B	20/04/2016
		CN 103064354 A	24/04/2013
		CN 103064354 B	16/03/2016
		CN 104391485 A	04/03/2015
		CN 104391485 B	12/04/2017
		CN 105573192 A	11/05/2016
		CN 105700491 A	22/06/2016
		EP 2511778 A2	17/10/2012
		EP 2511779 A2	17/10/2012
		EP 2511780 A2	17/10/2012
		US 2012-0256566 A1	11/10/2012
		US 2012-0265322 A1	18/10/2012
		US 2014-0237141 A1	21/08/2014
		US 2014-0243999 A1	28/08/2014
		US 2014-0244002 A1	28/08/2014
		US 2014-0365015 A1	11/12/2014
		US 2014-0371877 A1	18/12/2014
		US 2016-0026165 A1	28/01/2016
		US 8762588 B2	24/06/2014
		US 8850092 B2	30/09/2014
		US 8996745 B2	31/03/2015
		US 8996754 B2	31/03/2015
		US 9152136 B2	06/10/2015

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/041059

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 9310788 B2	12/04/2016
		US 9323235 B2	26/04/2016