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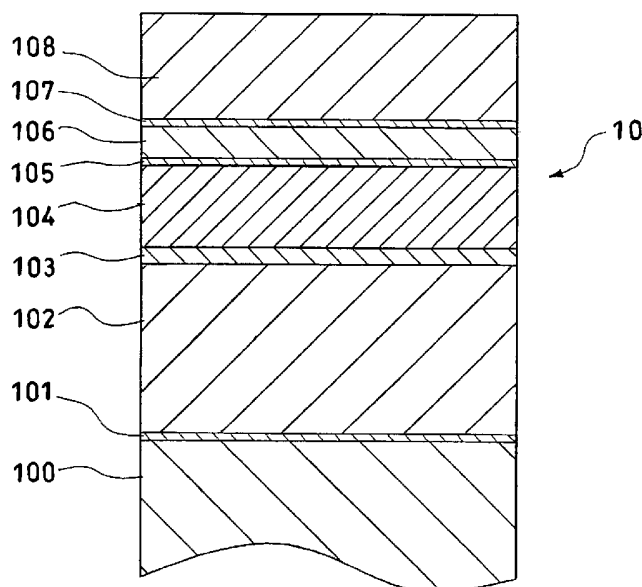
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(54) Title: GALLIUM NITRIDE-BASED SEMICONDUCTOR STACKED STRUCTURE



(57) Abstract: A gallium-nitride-based semiconductor stacked structure includes a sapphire substrate; a lowtemperature-deposited buffer layer which is composed of a Group III nitride material of $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) containing gallium (Ga) in a predominant amount with respect to aluminum (Al), which has been grown at low temperature and which is provided in a junction area thereof joined to a (0001) plane (c-plane) of the sapphire substrate with a single crystal in an as-grown state; and a gallium-nitride (GaN)-based semiconductor layer formed on the low-temperature-deposited buffer layer. The low-temperature-deposited buffer layer is predominantly composed of an as-grown single crystal which has a [1.0.-1.0.] orientation parallel to a [2.-1.1.0.] direction of a lattice forming a (0001) basal plane of the sapphire substrate.

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DESCRIPTION

GALLIUM NITRIDE-BASED SEMICONDUCTOR STACKED STRUCTURE

5 Cross Reference to Related Applications:

This application is an application filed under 35 U.S.C. § 111(a) claiming the benefit pursuant to 35 U.S.C. § 119(e)(1) of the filing dates of Provisional Application No. 60/580,910 filed June 21, 2004 and
10 Japanese Patent Application No. 2004-171108 filed June 9, 2004 pursuant to 35 U.S.C. § 111(b).

Technical Field:

The present invention relates to structural
15 requirements for a buffer layer formed at low temperature and advantageous for fabricating a stacked structure from a gallium-nitride-based Group III-V compound semiconductor layer having improved orientation characteristics, and to a compound semiconductor device
20 including the stacked structure.

Background Art:

Conventionally, gallium nitride (GaN)-based Group III-V compound semiconductors of a zinc-blende crystal
25 type or a Wurtzite crystal type are employed for fabricating semiconductor devices, such as a light-emitting device emitting visible light of short wavelength (see, for example, JP-A HEI 2-288388). Stacked structures for fabricating gallium-nitride-based
30 semiconductor devices are produced by use of a single-crystal substrate composed of a high-heat-resistance aluminum oxide, such as sapphire (α -Al₂O₃ single crystal)

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or a garnet single-crystal (see, for example, JP-A HEI 7-288231).

The above single-crystal substrate composed of aluminum oxide (e.g., sapphire) has lattice constants considerably different from those of a gallium nitride (GaN)-based semiconductor material. Thus, the stacked structure for use in fabrication of gallium-nitride-based semiconductor devices is generally formed via a buffer layer on a single-crystal substrate. The buffer layer for mitigating mismatch in terms of lattice constants is generally called a "low-temperature-deposited buffer layer" since the layer has been conventionally formed at relatively low temperature (see, for example, Book edited by Isamu AKASAKI, "Group III-V Compound Semiconductors," published by Baifukan Co., Ltd., 1st edition, Chapter 13, (May 20, 1995)).

The low-temperature-deposited buffer layer is formed from, for example, gallium nitride (see, for example, JP-A HEI 8-255926). In order to mitigate lattice constant mismatch with respect to a crystalline substrate, the low-temperature-deposited buffer layer is preferably formed of an amorphous material or a polycrystalline material in an as-grown state (see, for example, JP-A HEI 8-255926). Meanwhile, there has been disclosed another technique for forming a low-temperature-deposited buffer layer of a layer having a junction area with respect to a crystalline substrate formed in an as-grown state into a single-crystal layer (see, for example, JP-A HEI 10-321905).

However, the low-temperature-deposited buffer layer formed on the surface of a sapphire substrate has a drawback in that the orientation of the single-crystal

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layer included in the buffer layer is not sufficiently unified on the surface of the sapphire substrate, thereby failing to attain consistent formation, on the substrate, of a GaN-based Group III nitride semiconductor layer
5 having a well-unified orientation and excellent single-crystal characteristics.

Thus, an object of the present invention is to provide a crystal structural feature of a single-crystal layer included in a low-temperature-deposited buffer
10 layer so as to form, on a low-temperature-deposited buffer layer of $\text{Al}_x\text{Ga}_y\text{N}$ ($0 < X, Y < 1, X + Y = 1$) having a single-crystal layer included in the vicinity of a junction interface area thereof in contact with a substrate, a gallium-nitride-based semiconductor layer
15 having excellent single-crystal characteristics that is suitably grown. Another object of the invention is to provide a stacked structure having a GaN-based nitride semiconductor layer of excellent single-crystal characteristics that is formed via a low-temperature-
20 deposited buffer layer including a single-crystal layer having the above crystal feature. Yet another object of the invention is to provide a compound semiconductor device exhibiting excellent characteristics by virtue of employment of the stacked structure.

25

Disclosure of the Invention:

In order to attain the aforementioned objects, a first aspect of the present invention is directed toward a gallium-nitride-based semiconductor stacked structure
30 comprising a sapphire substrate; a low-temperature-deposited buffer layer which is composed of a Group III nitride material of $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1, X + Y = 1$)

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containing gallium (Ga) in a predominant amount with respect to aluminum (Al), which has been grown at low temperature and which is provided in a junction area thereof joined to a (0001) plane (c-plane) of the sapphire substrate with a single crystal in an as-grown state; and a gallium-nitride (GaN)-based semiconductor layer formed on the low-temperature-deposited buffer layer, wherein the low-temperature-deposited buffer layer is predominantly composed of an as-grown single crystal which has a [1.0.-1.0.] orientation parallel to a [2.-1.-1.0.] direction of a lattice forming a (0001) basal plane of the sapphire substrate.

A second aspect of the invention is directed to the gallium-nitride-based semiconductor stacked structure according to the first aspect, which further includes an active layer stacked on the low-temperature-deposited buffer layer and a thin-film layer interposed between the low-temperature-deposited buffer layer and the active layer and composed of a GaN-based Group III nitride semiconductor containing indium (In) or aluminum (Al).

A third aspect of the invention is directed to the gallium-nitride-based semiconductor stacked structure according to the second aspect, wherein the thin-film layer has a layer thickness of 2 nm to 100 nm.

A fourth aspect of the invention is directed to the gallium-nitride-based semiconductor stacked structure according to the second or third aspect, which further includes, between the low-temperature-deposited buffer layer and the active layer, a superlattice structure layer having a thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium (In) or aluminum (Al).

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A fifth aspect of the invention is directed to the gallium-nitride-based semiconductor stacked structure according to any one of the second to fourth aspects, which further includes an aluminum gallium indium nitride layer provided on the low-temperature-deposited buffer layer, wherein the thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium (In) or aluminum (Al) or the superlattice structure layer having the thin-film layer is provided between the active layer and the aluminum gallium indium nitride layer, and wherein the aluminum gallium indium nitride layer is represented by $\text{Al}_\alpha\text{Ga}_\beta\text{In}_{1-\alpha-\beta}\text{N}$ ($0 \leq \alpha$, $\beta \leq 1$, $0 \leq \alpha + \beta \leq 1$).

A sixth aspect of the invention is directed to the gallium-nitride-based semiconductor stacked structure according to any one of the second to fifth aspects, wherein the thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium (In) or aluminum (Al) has an orientation that coincides with that of the single-crystal layer included in the low-temperature-deposited buffer layer.

A seventh aspect of the invention is directed to a method for forming a gallium-nitride-based semiconductor stacked structure comprising the steps of providing a sapphire substrate, forming, on the sapphire substrate, a low-temperature-deposited buffer layer which is composed of a Group III nitride material of $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) containing gallium (Ga) in a predominant amount with respect to aluminum (Al) and which is provided in a junction area thereof joined to a (0001) plane (c-plane) of the sapphire substrate with a single crystal in an as-grown state, and forming a gallium-nitride-based semiconductor layer on the low-temperature-deposited

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buffer layer, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate in such a manner that the junction area is predominantly formed from an as-grown single
5 crystal which has a [1.0.-1.0.] orientation parallel to a [2.-1.-1.0.] direction of a lattice forming the (0001) basal plane of the sapphire substrate.

An eighth aspect of the invention is directed to the method for forming a gallium-nitride-based semiconductor
10 stacked structure according to the seventh aspect, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate at 350°C to 450°C.

A ninth aspect of the invention is directed to the
15 method for forming a gallium-nitride-based semiconductor stacked structure according to the seventh or eighth aspect, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate at a growth rate of 1 nm/min to 3 nm/min.

20 A tenth aspect of the invention is directed to the method for forming a gallium-nitride-based semiconductor stacked structure according to the ninth aspect, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate at a growth
25 rate of 1 nm/min to 3 nm/min controlled through regulation of an amount, per unit time, of a Group III element source including gallium or aluminum supplied to a growth reaction system for growing the low-temperature-deposited buffer layer.

30 An eleventh aspect of the invention is directed to the method for forming a gallium-nitride-based semiconductor stacked structure according to any one of

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the seventh to tenth aspects, wherein the as-grown single crystal which is contained in the low-temperature-deposited buffer layer and which predominantly forms the junction area joined to the sapphire substrate has a thickness of 1 nm or more when formation of the low-temperature-deposited buffer layer has been completed.

A twelfth aspect of the invention is directed to a gallium-nitride-based semiconductor device comprising the gallium-nitride-based semiconductor stacked structure according to any one of the first to sixth aspects, or a gallium-nitride-based semiconductor stacked structure produced through the method according to any one of the seventh to eleventh aspects.

According to the present invention, the single-crystal layer which is provided in an as-grown state in the junction area of the low-temperature-deposited buffer layer joined to the surface of the sapphire substrate attains a well-unified orientation of a GaN-based Group III nitride semiconductor layer deposited on the low-temperature-deposited buffer layer.

The present invention provides a gallium-nitride-based semiconductor stacked structure comprising a sapphire substrate; a low-temperature-deposited buffer layer which is composed of a Group III nitride material, which has been grown at low temperature and which is provided in a junction area thereof joined to a (0001) plane of the sapphire substrate with a single crystal in an as-grown state; and a gallium-nitride-based semiconductor layer formed on the low-temperature-deposited buffer layer. The stacked structure is fabricated from a GaN-based semiconductor layer via the low-temperature-deposited buffer layer containing an as-

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grown single crystal which is composed of a well-unified, hexagonal $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) crystal and which has the [1.0.-1.0.] orientation parallel to the [2.-1.-1.0.] direction of the sapphire substrate.

5 Therefore, the stacked structure can be advantageously fabricated from a GaN-based semiconductor layer having a well-unified orientation and excellent single-crystal characteristics.

According to the present invention, the low-
10 temperature-deposited buffer layer composed of a single-crystal containing gallium in an amount more than that of aluminum is formed at a specific growth temperature and growth rate. Therefore, a single-crystal layer that is well-unified with a specific crystal orientation of the
15 sapphire substrate can be formed. In addition, the single-crystal layer advantageously enhances the orientation of a GaN-based semiconductor single-crystal layer formed on the buffer layer. Through employment of the stacked structure having a well-unified orientation
20 and excellent single-crystal characteristics, semiconductor devices, such as a light-emitting diode, exhibiting excellent emission characteristics, i.e. causing few local breakdowns in the reverse direction, can be effectively produced.

25 The above and other objects, characteristic features and advantages of the present invention will become apparent to those skilled in the art from the description given herein below with reference to the accompanying drawings.

30

Brief Description of the Drawings:

Figure 1 is a schematic cross-section of the

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semiconductor stacked structure of Example 1 of the present invention.

Figure 2 is a schematic plan view of the light-emitting diode (LED) of Example 2 of the present invention.

Figure 3 is a schematic cross-section of the LED of Example 2 of the present invention.

Figure 4 is a schematic cross-section of the LED of Example 3 of the present invention.

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Best Mode for carrying Out the Invention:

The $\text{Al}_x\text{Ga}_y\text{N}$ low-temperature-deposited buffer layer is formed on a sapphire substrate through, for example, a metal-organic chemical vapor deposition (abbreviated as MOCVD) means. For example, an $\text{Al}_x\text{Ga}_y\text{N}$ layer is formed through a MOCVD means by use of a metal-organic (abbreviated as MO) compound, such as trimethylgallium ($(\text{CH}_3)_3\text{Ga}$), triethylgallium ($(\text{C}_2\text{H}_5)_3\text{Ga}$) or trimethylaluminum ($(\text{CH}_3)_3\text{Al}$) as a source. Ammonia (NH_3) or a similar compound may be used as a nitrogen source. Hydrazines which are decomposed at lower temperature may also be employed as nitrogen (N) sources for growing the low-temperature-deposited buffer layer.

When an $\text{Al}_x\text{Ga}_y\text{N}$ low-temperature-deposited buffer layer including a junction portion composed of an as-grown hexagonal single crystal is to be formed on a sapphire substrate, particularly on a (0001) plane (i.e., c-plane), the growth temperature is essentially controlled so as to fall within an appropriate range. Specifically, the growth temperature is preferably controlled to 250°C to 500°C.

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When the growth temperature is lower than 250°C, formation of the $\text{Al}_x\text{Ga}_y\text{N}$ low-temperature-deposited buffer layer is unsatisfactorily attained due to insufficient thermal decomposition of growth sources, whereas when the growth temperature is higher than 500°C, a large number of crystals grow at random, thereby failing to reliably form a low-temperature-deposited buffer layer containing a continuous single crystal that sufficiently and homogeneously covers the substrate surface (e.g., a low-temperature-deposited buffer layer composed of a continuous single crystal in the layer form (single-crystal layer)). Needless to say, both cases are problematic.

The term "as-grown single crystal" refers to a single crystal which is formed in an as-grown state of the low-temperature-deposited buffer layer. Even when the single crystal is subjected to a subsequent film formation step or a device fabrication step, the single crystal contained in the buffer layer is maintained.

More preferably, the $\text{Al}_x\text{Ga}_y\text{N}$ low-temperature-deposited buffer layer is grown at 350°C to 450°C. When the growth temperature falls within the temperature range, the formed low-temperature-deposited buffer layer comes to include, at the junction interface between the buffer layer and the sapphire substrate, an $\text{Al}_x\text{Ga}_y\text{N}$ crystal having a crystal orientation unified in a specific direction.

Particularly when the low-temperature-deposited buffer layer is formed from an $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) crystal containing gallium in an amount greater than that of aluminum, the formed low-temperature-deposited buffer layer contains a single crystal composed of $\text{Al}_x\text{Ga}_y\text{N}$

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($0.5 < Y \leq 1$, $X + Y = 1$) such that the [1.0.-1.0.] orientation of the $\text{Al}_x\text{Ga}_y\text{N}$ crystal is parallel to the [2.-1.-1.0.] (a-axis) direction of the c-plane (basal unit lattice) of the sapphire substrate. Whether or not the
5 formed low-temperature-deposited buffer layer assumes a single crystal may be determined on the basis of appearance of diffraction spots in an electron diffraction image. When a halo or a ring diffraction image appears, the formed layer can be determined to be
10 amorphous or polycrystalline.

When the growth rate is regulated to 1 through 3 nm/min, a single crystal or a single-crystal layer formed of single crystals connected whose orientation is well-unified with respect to a specific crystal axis of the
15 sapphire substrate can be formed more effectively and reliably. The growth rate may be controlled by modifying the amount per unit time (supply rate) of a Group III element (e.g., gallium or aluminum) source supplied to the reaction system for growing the low-temperature-
20 deposited buffer layer. Thus, when the amount of aluminum or gallium supplied to the growth reaction system or the total amount thereof is increased, the growth rate can be increased. In the case where the concentration of gallium exceeds that of aluminum during
25 supply of aluminum and gallium to the growth reaction system, a low-temperature-deposited buffer layer composed of an $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) crystal containing Ga in an amount greater than that of Al can be formed.

The orientation feature of the single-crystal layer
30 included in the low-temperature-deposited buffer layer and present in a junction area thereof joined to the sapphire substrate may be determined through, for example,

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electron diffraction method.

In one determination procedure of the orientation feature, an incident electron beam is made incident on the $\text{Al}_x\text{Ga}_y\text{N}$ low-temperature-deposited buffer layer in parallel to the $[2.-1.-1.0.]$ direction of a sapphire substrate to capture an electron diffraction pattern of the buffer layer. When a reciprocal-lattice image attributable to the $\text{Al}_x\text{Ga}_y\text{N}$ low-temperature-deposited buffer layer as viewed from an orientation of $[1.0.-1.0.]$ appears in the electron diffraction pattern, the $\text{Al}_x\text{Ga}_y\text{N}$ single-crystal layer included in the low-temperature-deposited buffer layer is determined such that the $[1.0.-1.0.]$ orientation of the $\text{Al}_x\text{Ga}_y\text{N}$ single-crystal layer forming the low-temperature-deposited buffer layer is parallel to the $[2.-1.-1.0.]$ direction of the sapphire substrate.

The low-temperature-deposited buffer layer of the present invention may be formed of a single-crystal layer in its entirety.

In other words, an amorphous $\text{Al}_x\text{Ga}_y\text{N}$ may be present on the single-crystal layer included in the low-temperature-deposited buffer layer, as observed in a cross-sectional TEM (transmission electron microscope) image of the low-temperature-deposited buffer layer in an as-grown state. This is because such an amorphous substance is known to be crystallized when a GaN-based semiconductor layer is grown on the low-temperature-deposited buffer layer at a temperature higher than the temperature at which the low-temperature-deposited buffer layer has been grown.

In the above case, since the single crystal or single-crystal layer having the aforementioned well-

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unified orientation is present to serve as an under layer, the unified orientation feature of the under layer is reflected to the amorphous substance, which is advantageous for transforming the amorphous substance to the corresponding crystal having an unified orientation. Specifically, the single-crystal layer that is present in a junction area of the low-temperature deposited buffer layer joined to the surface of the sapphire substrate can also be effectively used for transforming an amorphous substance contained in the low-temperature-deposited buffer layer to the corresponding crystal having an unified orientation, so that an upper layer having an excellent well-unified orientation and single-crystal characteristics can be provided.

The single crystal or layered single crystal (single-crystal layer) present in a junction area which is in contact with the surface of the sapphire substrate has a thickness of at least about 1 nm.

In such a single crystal, constituent atoms (i.e., aluminum, gallium and nitrogen) are chemically bonded tightly with one another and adhere strongly to the sapphire substrate. Therefore, despite the layer thickness being about 1 nm, so long as the single crystal assumes the aforementioned layer form, the single crystal remains on the surface of the sapphire substrate even when the single crystal is placed under high-temperature conditions under which the GaN-based Group III nitride semiconductor layer has been formed on the low-temperature-deposited buffer layer, whereby exposure of the surface of the sapphire substrate is prevented. As a result, the GaN-based Group III nitride semiconductor layer having a well-unified orientation can be formed as

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an upper layer on such a single-crystal layer serving as an under layer.

The GaN-based Group III nitride semiconductor layer which is formed on the low-temperature-deposited buffer layer may be formed through a known vapor growth means, such as the halogen method, the hydride method or MOCVD, or through molecular beam epitaxy.

For example, on the low-temperature-deposited buffer layer of the present invention, the GaN-based Group III nitride semiconductor layers (a) to (g) shown below are sequentially stacked, whereby a GaN-based semiconductor stacked structure for fabricating a light-emitting diode (abbreviated as LED) can be formed. The Group III nitride semiconductor layers (a) to (g) may be grown through different means. However, all the layers including a low-temperature-deposited buffer layer are preferably grown through the same means (e.g., MOCVD) from the viewpoint of production of such a stacked structure.

- 20 (a) A silicon (Si)-doped n-type GaN layer
- (b) A superlattice structure composed of Si-doped n-type gallium indium nitrides ($\text{Ga}_{Y1}\text{In}_{Z1}\text{N}$: $0 < Z1 < 1$, $Y1 + Z1 = 1$) and $\text{Ga}_{Y2}\text{In}_{Z2}\text{N}$: $0 < Z2 < 1$, $Z1 \neq Z2$, $Y2 + Z2 = 1$)
- (c) A quantum well (QW) structure composed of an n-type GaN layer and an n-type layer of $\text{Ga}_{Y3}\text{In}_{Z3}\text{N}$ ($0 < Z3 < 1$, $Z1 < Z3$, $Z2 < Z3$, $Y3 + Z3 = 1$)
- 25 (d) A superlattice structure composed of a layer of $\text{Al}_{X1}\text{Ga}_{Y1}\text{N}$ ($0 \leq X1$, $Y1 \leq 1$, $X1 + Y1 = 1$) and a layer of $\text{Al}_{X2}\text{Ga}_{Y2}\text{N}$ ($0 \leq X2$, $Y2 \leq 1$, $X1 \neq X2$, $X2 + Y2 = 1$)
- 30 (e) A p-type layer of $\text{Al}_{X3}\text{Ga}_{Y3}\text{N}$ ($0 \leq X3$, $Y3 \leq 1$, $X3 < X1$ or $X2$, $X3 + Y3 = 1$)

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(f) A p-type layer of $\text{Al}_{X4}\text{Ga}_{Y4}\text{N}$ ($0 \leq X4, Y4 \leq 1, X4 > X3, X4 + Y4 = 1$)

(g) A p-type GaN layer

Instead of the aforementioned p-type Group III
5 nitride semiconductor layer (e) or (g), or of the p-type
layers (e) through (g), a p-type Group III-V
semiconductor layer(s) may be stacked to form a stacked
structure. In this case, a boron-phosphide-based
semiconductor layer or a similar layer may serve as the
10 p-type Group III-V semiconductor layer. Particularly,
use of boron monophosphide (BP) having a lattice plane
spacing equivalent to the a-axis (= 0.319 nm) of GaN, is
advantageous for producing a stacked structure having a
p-type layer well matched with GaN.

15 The compound semiconductor device of the present
invention is fabricated by appropriately working the
aforementioned GaN-based semiconductor stacked structure
and forming electrodes and other elements.

For example, the uppermost layer of the
20 aforementioned stacked structure composed of the
aforementioned p-type GaN layer (f) is employed as a
contact layer, on which an ohmic electrode is formed. On
the aforementioned n-type Group III nitride semiconductor
layer (a) or (b), the ohmic electrode of the opposite
25 polarity is provided. Through provision of these
electrodes in such a manner, the n-type Group III nitride
semiconductor layer (a) or (b) serves as an n-type
cladding layer, the quantum well structure (c) serves as
a light-emitting layer, and the p-type Group III nitride
30 semiconductor layer (d) or (e) serves as a p-type
cladding layer. A pn-junction double-hetero (DH)
structure LED is fabricated from the layers.

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In the present invention, the constituent layers included in the stacked structure are grown via a low-temperature-deposited buffer layer including a single-crystal layer having a well-unified orientation. Thus, each layer assumes the form of a single-crystal layer having a particularly unified orientation; i.e., having no crystal grain boundaries. In addition, the single-crystal layer included in the low-temperature-deposited buffer layer grown on the sapphire substrate has a surface crystal plane having characteristics identical with those of the surface of the sapphire substrate. Accordingly, a low-temperature-deposited buffer layer including a single-crystal layer having a (0001) crystal plane forming a surface is provided on a sapphire substrate having a (0001) plane forming the surface.

Since the crystal feature of the surface is reflected from the low-temperature-deposited buffer layer to an upper layer, the upper Group III nitride semiconductor layer comes to have a surface crystal having a well-unified crystal plane and orientation. The aforementioned LED fabricated from such a stacked structure exhibits excellent electrical properties. For example, unnecessary leak current caused by crystal grain boundaries, which are formed through, for example, combination of crystal grains having different orientations, can be reduced.

In the case in which a stacked structure for use in a light-emitting device, such as a light-emitting diode (LED) or a laser diode (LD), is formed, a thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium (In) or aluminum (Al) or a superlattice structure layer including the thin-film layer may be

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interposed between a light-emitting layer and the low-temperature-deposited buffer layer of the present invention. The resultant light-emitting layer exhibits excellent crystallinity with few misfit dislocations by virtue of the thin-film layer.

For example, a stacked structure is fabricated by forming a light-emitting layer on a GaN layer provided on a low-temperature-deposited buffer layer via a thin-film layer composed of an aluminum gallium nitride mixed crystal ($\text{Al}_Q\text{Ga}_{1-Q}\text{N}$: $0 < Q \leq 1$). Alternatively, a stacked structure is fabricated by interposing between an n-type light-emitting layer and a low-temperature-deposited buffer layer, a superlattice structure layer including a thin-film layer composed of an n-type gallium indium nitride mixed crystal ($\text{Ga}_Q\text{In}_{1-Q}\text{N}$: $0 \leq Q \leq 1$). Through employment of such a stacked structure, a light-emitting layer which can emit high-intensity light can be produced.

Example 1:

The present invention will next be described in detail by way of Example 1 that shows the case where a GaN-based Group III nitride semiconductor layer is grown on a sapphire substrate via a low-temperature-deposited buffer layer to thereby fabricate a stacked structure.

Figure 1 is a schematic cross-sectional view of a stacked structure 10 as described in Example 1.

Group III nitride semiconductor layers 102 to 108 included in the stacked structure 10 were formed on the (0001) surface of a sapphire substrate 100 via a low-temperature-deposited buffer layer 101 composed of an aluminum gallium nitride mixed crystal ($\text{Al}_{0.10}\text{Ga}_{0.90}\text{N}$). The low-temperature-deposited buffer layer 101 was grown at

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400°C through an atmospheric pressure (near atmospheric pressure) MOCVD means by use of triethylgallium ($(\text{C}_2\text{H}_5)_3\text{Ga}$) as a gallium (Ga) source, trimethylaluminum ($(\text{CH}_3)_3\text{Al}$) as an aluminum (Al) source and ammonia (NH_3) as
5 a nitrogen (N) source. The growth rate was adjusted to 3 nm/min by controlling the total concentration per unit time of $(\text{C}_2\text{H}_5)_3\text{Ga}$ and $(\text{CH}_3)_3\text{Al}$ supplied to the MOCVD reaction system. The thickness of the low-temperature-deposited buffer layer 101 was controlled to 18 nm.

10 The internal crystal structure of the low-temperature-deposited buffer layer 101 was analyzed in an as-grown state through electron diffraction method. The diffraction pattern assumed a spot-like pattern attributed to a region from the (0001) surface of the
15 sapphire substrate 100 to a depth of about 8 nm, indicating that a single crystal was present inside the region of the low-temperature-deposited buffer layer 101 that was joined to the sapphire substrate 100. The electron diffraction pattern also indicated that the
20 single-crystal layer was composed of a hexagonal crystal which was stacked on the (0001) surface of the sapphire substrate such that the (0001) plane of the hexagonal crystal and the (0001) surface of the sapphire substrate were unified in parallel to each other. On the basis of
25 the relationship between diffraction and incident direction of electron beam, the [1.0.-1.0.] orientation of the single-crystal layer was found to be parallel to the [2.-1.-1.0.] direction of the sapphire substrate 100. It was noted that an amorphous substance having a height
30 of about 10 nm was present discretely on the single-crystal layer.

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On the $\text{Al}_{0.10}\text{Ga}_{0.90}\text{N}$ low-temperature-deposited buffer layer 101, the following GaN-based Group III nitride semiconductor layers 102 to 108 corresponding respectively to (1) through (7) were grown through MOCVD to thereby fabricate a stacked structure 10 of the present invention.

- (1) An Si-doped n-type GaN layer 102 (carrier concentration $(n) = 1 \times 10^{18} \text{ cm}^{-3}$, layer thickness $(t) = 5,500 \text{ nm}$)
- 10 (2) A superlattice structure layer 103 formed from twelve Si-doped n-type layers of gallium indium nitride mixed crystal ($\text{Ga}_{0.98}\text{In}_{0.02}\text{N}$, $t = 1.5 \text{ nm}$) and eleven Si-doped n-type layers of gallium indium nitride mixed crystal ($\text{Ga}_{0.99}\text{In}_{0.01}\text{N}$, $t = 1.5 \text{ nm}$)
- 15 (3) A quantum well structure layer 104 formed from eight n-type layers of GaN ($t = 15 \text{ nm}$) and seven n-type layers of $\text{Ga}_{0.95}\text{In}_{0.05}\text{N}$ ($t = 2.0 \text{ nm}$)
- (4) A high-resistive layer 105 composed of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ ($t = 1.5 \text{ nm}$)
- 20 (5) A superlattice structure layer 106 formed from three layers of $\text{Al}_{0.10}\text{Ga}_{0.90}\text{N}$ mixed crystal ($t = 1.5 \text{ nm}$) and four layers of $\text{Al}_{0.10}\text{Ga}_{0.88}\text{In}_{0.02}\text{N}$ mixed crystal ($t = 1.5 \text{ nm}$)
- (6) A p-type layer 107 of $\text{Al}_{0.10}\text{Ga}_{0.90}\text{N}$ (carrier concentration $(p) = 6 \times 10^{17} \text{ cm}^{-3}$, $t = 2.0 \text{ nm}$)
- 25 (7) A p-type layer 108 of $\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$ layer (carrier concentration $(p) = 9 \times 10^{17} \text{ cm}^{-3}$, $t = 350 \text{ nm}$)

Since the aforementioned Group III nitride semiconductor layers (1) to (7) were grown via the low-temperature-deposited buffer layer 101 including a single-crystal layer, all the grown layers assumed the form of single-crystal layers. Through observation based on cross-sectional TEM, no amorphous substance was

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observed in the junction interface between the low-temperature-deposited buffer layer 101 and the n-type GaN layer 102 grown at a higher temperature of 1,080°C, indicating that the n-type GaN layer 102 was considered to be grown so as to be directly joined to the single-crystal layer present in the low-temperature-deposited buffer layer 101 in an as-grown state. Therefore, the amorphous substances scattered on the single-crystal layer present in the low-temperature-deposited buffer layer in an as-grown state may be sublimated during deposition of the n-type GaN layer 102 at a high temperature (1,080°C).

In addition, since the Group III nitride semiconductor layers 102 to 108 were deposited on the low-temperature-deposited buffer layer 101 including a single-crystal layer having a well-unified orientation, all these layers assumed hexagonal single-crystal layers each having a [1.0.-1.0.] orientation parallel to the [2.-1.-1.0.] direction of the sapphire substrate 100. Thus, there was provided a stacked structure 10 including GaN-based Group III nitride semiconductor single-crystal layers 102 to 108 each having a well-unified orientation and excellent single-crystal characteristics.

Example 2:

The present invention will next be described in detail by way of Example 2 showing the case where an LED is fabricated from the stacked structure of the present invention.

Figure 2 is a schematic plan view of a light-emitting diode (LED) 1A of Example 2 fabricated from the stacked structure 10 produced in Example 1. Figure 3 is

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a schematic cross-sectional view of the light-emitting diode (LED) 1A. In Figures 2 and 3, the same constituent elements as shown in Figure 1 are denoted by the same reference numerals.

5 The stacked structure 10 of Example 1 was processed through a conventional plasma etching means, whereby a portion of the surface of the n-type GaN layer 102 provided via the low-temperature-deposited buffer layer 101 was exposed, the portion being exclusively used for
10 an area where an n-type ohmic electrode 201 is to be provided.

 Subsequently, on the surface of the thus exposed portion of the n-type GaN layer 102, tungsten (W) and aluminum (Al) films were sequentially stacked, thereby
15 providing the n-type ohmic electrode 201.

 On the surface of the p-type $\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$ layer 108 serving as the surface of the stacked structure 10, gold (Au)-gallium (Ga)-nickel (Ni) alloy film and nickel oxide film were sequentially deposited and placed in the form
20 of lattice-like pattern, thereby forming a p-type ohmic electrode 202. On a corner of the p-type ohmic electrode 202, a pad electrode 203 having an upper layer formed of gold (Au)-titanium (Ti) alloy film and a nickel (Ni) bottom layer was provided so as to attain electrical
25 connection with the p-type ohmic electrode 202.

 Through the above procedure, there was fabricated a light-emitting diode (LED) 1A having a pn-junction double-hetero (DH) structure, which structure was composed of the n-type GaN layer 102 of Example 1 serving
30 as an n-type cladding layer, the quantum well structure layer 104 (GaN layers/n-type $\text{Ga}_{0.95}\text{In}_{0.05}\text{N}$ layers) serving as a light-emitting layer and the uppermost p-type

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Al_{0.05}Ga_{0.95}N layer 108 serving as a p-type contact layer.

Emission characteristics of the light-emitting diode (LED) 1A were evaluated when forward device operation current (20 mA) was caused to flow between the n-type ohmic electrode 201 and the p-type ohmic electrode 202. The light-emitting diode (LED) 1A was found to emit blue light having a center wavelength of 450 nm. The emission intensity of the LED chip before resin-molding, as determined through a typical integrating sphere, was as high as about 5 mW. The forward voltage (V_f) was found to be as low as 3.3 V.

Since the n-type ohmic electrode 201 and the p-type ohmic electrode 202 were formed on a Group III nitride semiconductor layer having excellent crystallinity via the low-temperature-deposited buffer layer 101 including a single-crystal layer having a well-unified orientation in an as-grown state, the LED exhibited few local breakdowns. Thus, the reverse voltage at a reverse current of 10 μ A was found to be higher than 15 V.

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Example 3:

The present invention will next be described in detail by way of Example 3 showing the case where an LED is fabricated from the stacked structure of the present invention.

The procedure of Example 1 was repeated, except that a low-temperature-deposited buffer layer 101a was fabricated from gallium nitride (GaN) different from that employed in Example 1, to thereby fabricate a stacked structure.

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Figure 4 is a schematic cross-sectional view of a light-emitting diode (LED) 1B.

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The GaN low-temperature-deposited buffer layer 101a was formed at 350°C through an atmospheric pressure (near atmospheric pressure) MOCVD means by use of $(\text{CH}_3)_3\text{Ga}$ and NH_3 as sources. The total thickness of the GaN layer
5 serving as the low-temperature-deposited buffer layer 101a was controlled to 15 nm.

The structural analysis on the basis of a conventional electron diffraction technique revealed that the junction portion of the low-temperature-deposited
10 buffer layer 101a joined to the sapphire substrate 100 was formed, in an as-grown state, of a single-crystal layer composed of a hexagonal GaN having an a-axis unified in parallel to the [0.1.-1.0.] direction of the sapphire substrate. The single-crystal layer was found
15 to cover virtually the entire surface of the (0001) plane of the sapphire substrate. The electron diffraction patterns indicated that the aforementioned alignment feature was maintained over the area of the substrate. On the (0001) surface of the GaN single-crystal layer, an
20 amorphous substance having a generally circular cross-section was present discretely. Since no such amorphous substance was observed on the surface of the GaN low-temperature-deposited buffer layer 101a after formation of the constituent layers of the stacked structure, the
25 amorphous substance may be sublimated during formation of the constituent layers at high temperature.

In a manner similar to that described in relation to Example 2, the stacked structure 10a was etched, and an n-type ohmic electrode 201 and a p-type ohmic electrode
30 202 having the same structure were provided in the same positions. Similarly to Example 2, the thus fabricated light-emitting diode (LED) 1B was found to emit blue

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light having a center wavelength of 450 nm at a forward current of 20 mA. The emission intensity of the LED chip before resin-molding, as determined through a typical integrating sphere, was as high as about 5 mW. The forward voltage (Vf) was found to be as low as 3.3 V. Since the n-type ohmic electrode 201 and the p-type ohmic electrode 202 were formed on a GaN-based single-crystal layer having a well-unified orientation and excellent crystallinity via the low-temperature-deposited buffer layer 101a having the crystal feature according to the present invention, the provided LED exhibited few local breakdowns.

Industrial Applicability:

As has been described in the foregoing, according to the present invention, the low-temperature-deposited buffer layer composed of a single-crystal containing gallium in an amount more than that of aluminum is formed at a specific growth temperature and growth rate. Therefore, a single-crystal layer that is well-unified with a specific crystal orientation of the sapphire substrate can be formed. In addition, the single-crystal layer advantageously enhances the orientation of a GaN-based semiconductor single-crystal layer formed on the buffer layer. Through employment of the stacked structure having a well-unified orientation and excellent single-crystal characteristics, semiconductor devices, such as a light-emitting diode, exhibiting excellent discharge characteristics, i.e. causing few local breakdowns in the reverse direction, can be effectively produced.

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CLAIMS

1. A gallium-nitride-based semiconductor stacked structure comprising:

a sapphire substrate;

a low-temperature-deposited buffer layer which is composed of a Group III nitride material of $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) containing gallium in a predominant amount with respect to aluminum, which has been grown at low temperature and which is provided in a junction area thereof joined to a (0001) plane (c-plane) of the sapphire substrate with a single crystal in an as-grown state; and

a gallium-nitride-based semiconductor layer formed on the low-temperature-deposited buffer layer;

wherein the low-temperature-deposited buffer layer is predominantly composed of an as-grown single crystal which has a [1.0.-1.0.] orientation parallel to a [2.-1.-1.0.] direction of a lattice forming a (0001) bottom plane of the sapphire substrate.

2. A gallium-nitride-based semiconductor stacked structure according to claim 1, further comprising:

an active layer stacked on the low-temperature-deposited buffer layer; and

a thin-film layer interposed between the low-temperature-deposited buffer layer and the active layer and composed of a GaN-based Group III nitride semiconductor containing indium or aluminum.

3. A gallium-nitride-based semiconductor stacked structure according to claim 2, wherein the thin-film

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layer has a layer thickness of 2 nm to 100 nm.

4. A gallium-nitride-based semiconductor stacked structure according to claim 2 or claim 3, further comprising, between the low-temperature-deposited buffer layer and the active layer, a superlattice structure layer having a thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium or aluminum.

5. A gallium-nitride-based semiconductor stacked structure according to any one of claims 2 to 4, further comprising an aluminum gallium indium nitride layer provided on the low-temperature-deposited buffer layer, wherein the thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium or aluminum or the superlattice structure layer having the thin-film layer is provided between the active layer and the aluminum gallium indium nitride layer, and wherein the aluminum gallium indium nitride layer is represented by $\text{Al}_\alpha\text{Ga}_\beta\text{In}_{1-\alpha-\beta}\text{N}$ ($0 \leq \alpha$, $\beta \leq 1$, $0 \leq \alpha + \beta \leq 1$).

6. A gallium-nitride-based semiconductor stacked structure according to any one of claims 2 to 5, wherein the thin-film layer composed of a GaN-based Group III nitride semiconductor containing indium (In) or aluminum (Al) has an orientation that coincides with that of the single-crystal layer included in the low-temperature-deposited buffer layer.

7. A method for forming a gallium-nitride-based semiconductor stacked structure comprising the steps of:

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providing a sapphire substrate;

forming, on the sapphire substrate, a low-temperature-deposited buffer layer which is composed of a Group III nitride material of $\text{Al}_x\text{Ga}_y\text{N}$ ($0.5 < Y \leq 1$, $X + Y = 1$) containing gallium (Ga) in a predominant amount with respect to aluminum (Al) and which is provided in a junction area thereof joined to a (0001) plane (c-plane) of the sapphire substrate with a single crystal in an as-grown state; and

forming a gallium-nitride-based semiconductor layer on the low-temperature-deposited buffer layer;

wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate in such a manner that the junction area is predominantly formed of an as-grown single crystal which has a [1.0.-1.0.] orientation parallel to a [2.-1.-1.0.] direction of a lattice forming the (0001) plane of the sapphire substrate.

8. A method for forming a gallium-nitride-based semiconductor stacked structure according to claim 7, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate at 350°C to 450°C.

9. A method for forming a gallium-nitride-based semiconductor stacked structure according to claim 7 or claim 8, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate at a growth rate of 1 nm/min to 3 nm/min.

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10. A method for forming a gallium-nitride-based semiconductor stacked structure according to claim 9, wherein the low-temperature-deposited buffer layer is formed on the (0001) plane of the sapphire substrate at a growth rate of 1 nm/min to 3 nm/min controlled through regulation of an amount, per unit time, of a Group III element source including gallium or aluminum supplied to a growth reaction system for growing the low-temperature-deposited buffer layer.

11. A method for forming a gallium-nitride-based semiconductor stacked structure according to any one of claims 7 to 10, wherein the as-grown single crystal which is contained in the low-temperature-deposited buffer layer and which predominantly forms the junction area joined to the sapphire substrate has a thickness of 1 nm or more when formation of the low-temperature-deposited buffer layer has been completed.

12. A gallium-nitride-based semiconductor device comprising the gallium-nitride-based semiconductor stacked structure according to any one of claims 1 to 6, or a gallium-nitride-based semiconductor stacked structure produced through the method according to any one of claims 7 to 11.

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FIG. 1

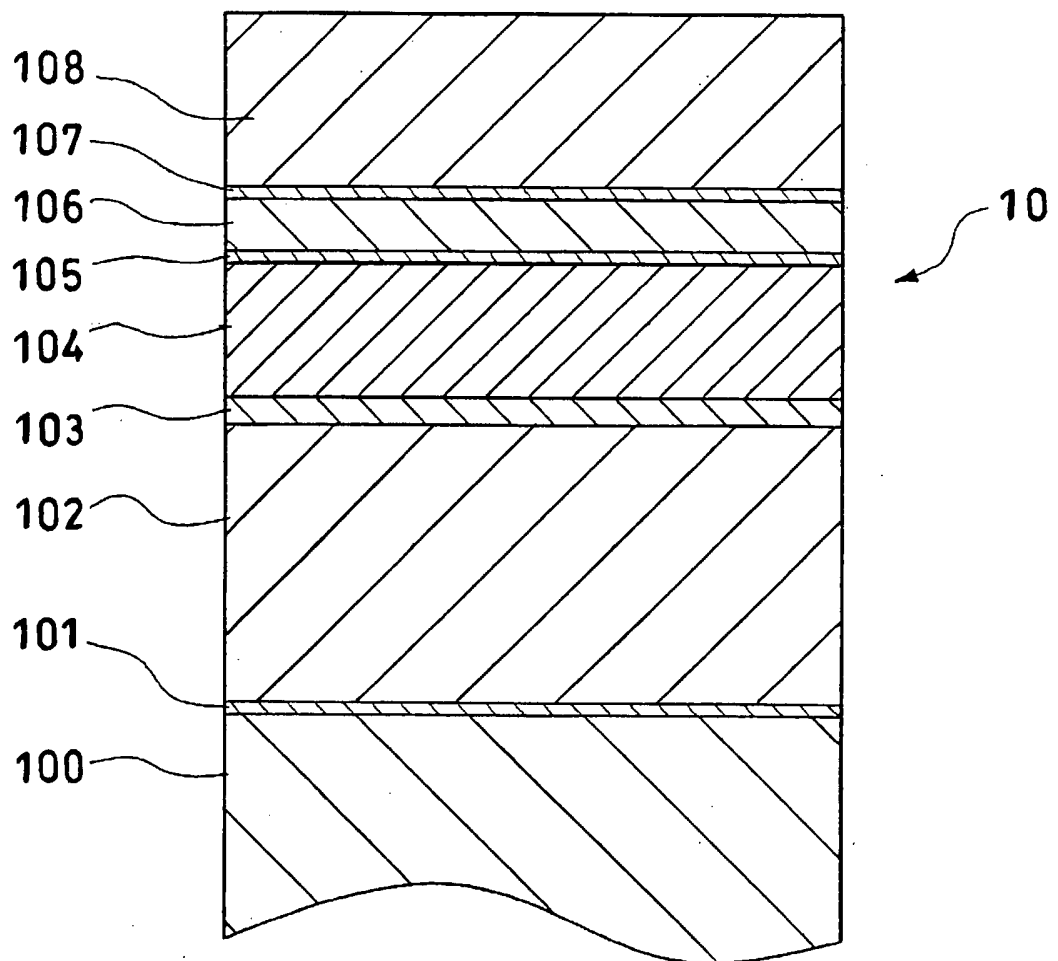


FIG. 2

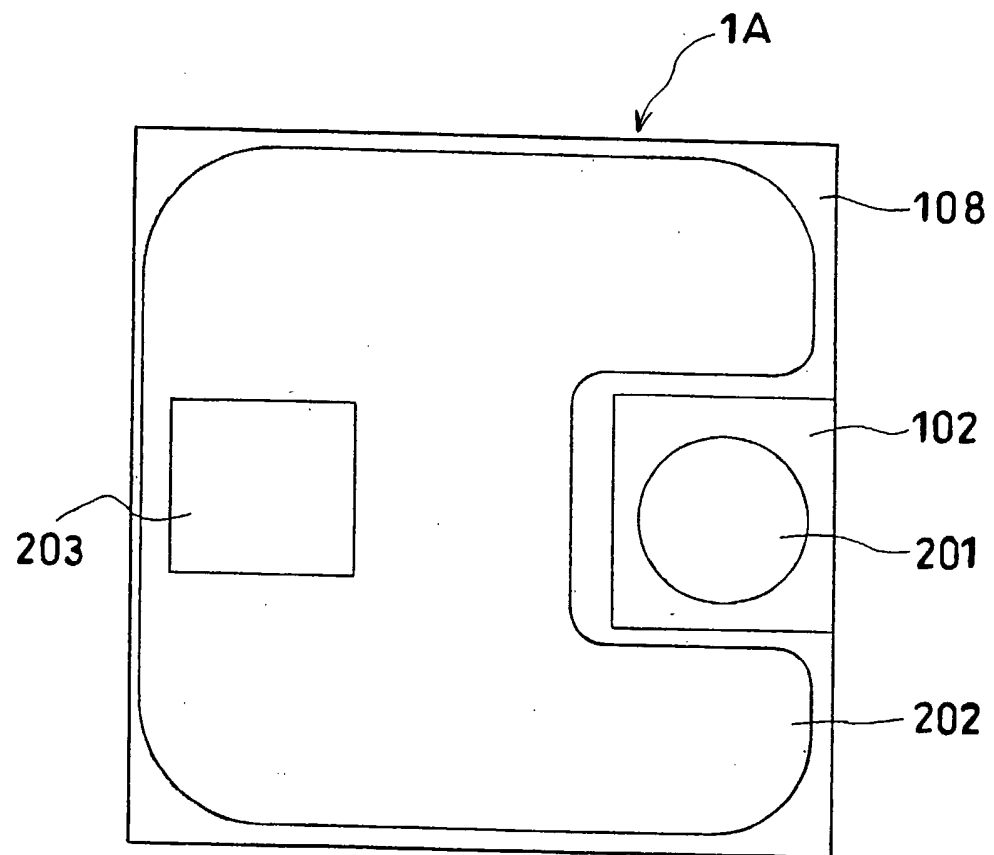
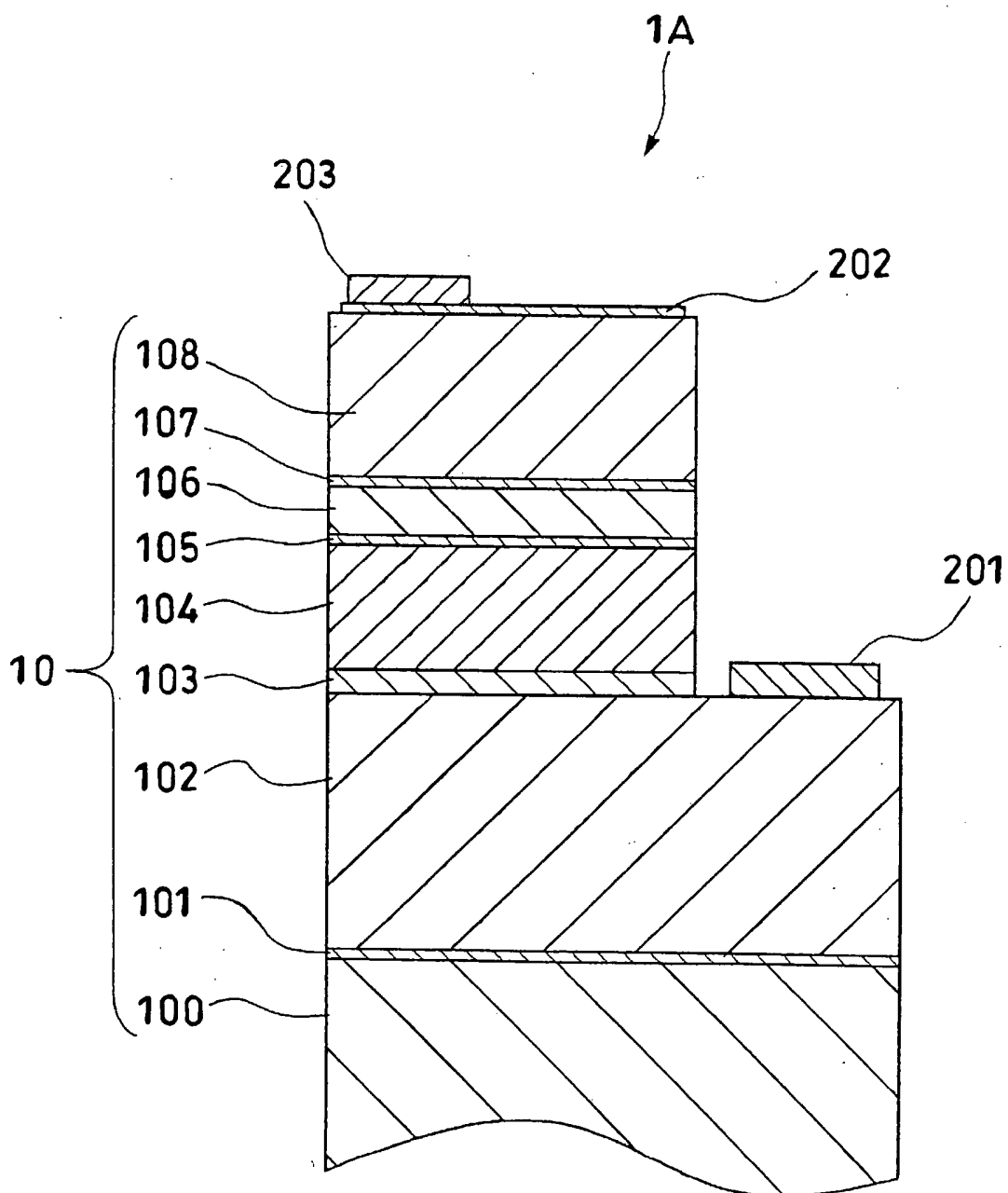
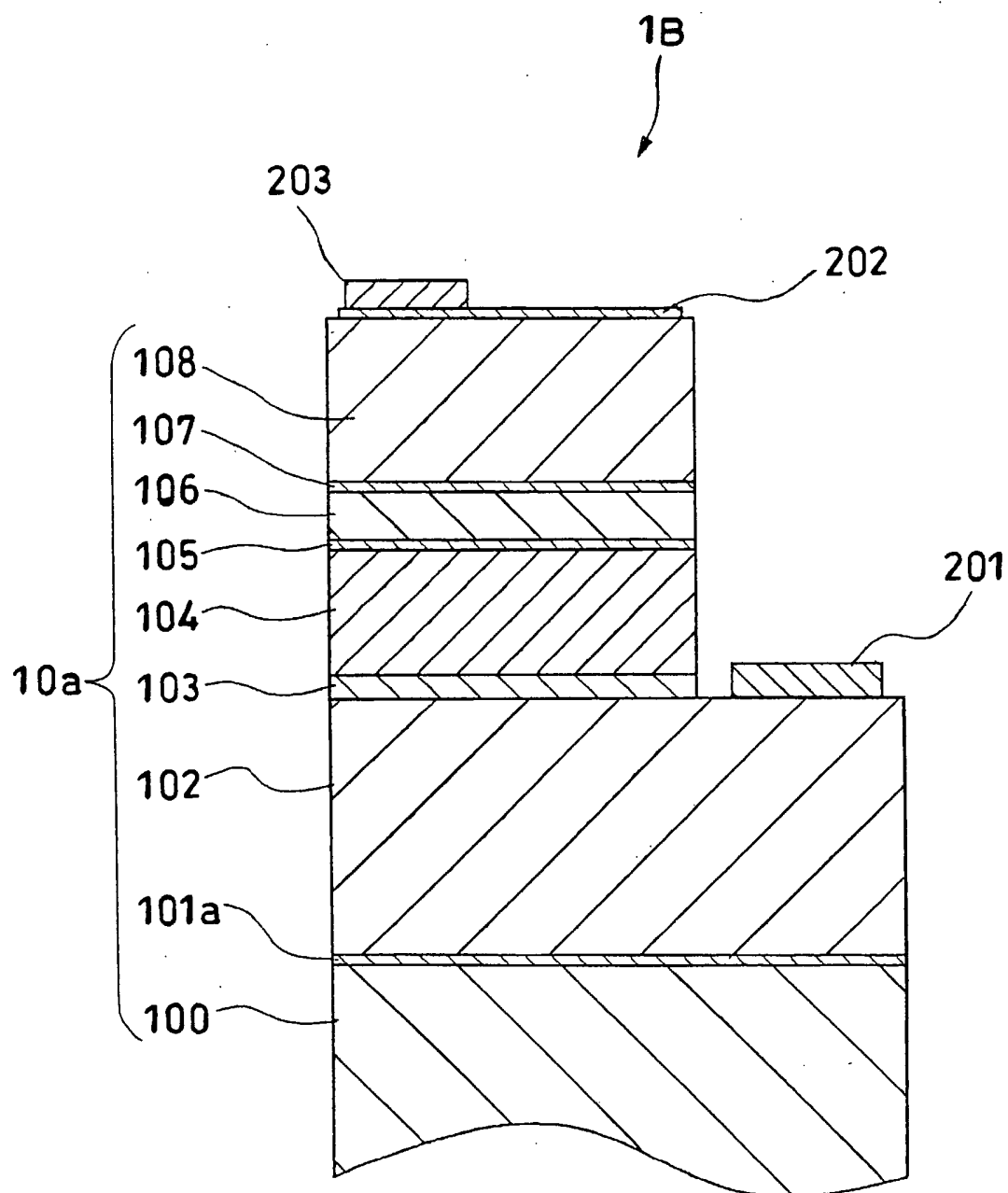


FIG. 3



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FIG. 4



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2005/010991

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl.⁷ H01L33/00, 21/205

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl.⁷ H01L33/00, 21/205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2005
 Registered utility model specifications of Japan 1996-2005
 Published registered utility model applications of Japan 1994-2005

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	JP 2002-134786 A (Nichia Corporation.) 2002.05.10, [0027] - [0035], fig1 (None Family)	1-3, 6, 7
X	JP 2004-111997 A (Nichia Corporation.) 2004.04.08, [0115] - [0127] & U S 2004/0165635 A & EP 14063 60 A1 & WO 2002/101894 A1	1, 2, 4-7

☒ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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Date of the actual completion of the international search

09.09.2005

Date of mailing of the international search report

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INTERNATIONALSEARCHREPORT

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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