(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 051 342**
B1

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **29.01.86**

(51) Int. Cl.⁴: **G 10 L 9/18**

(21) Application number: **81201230.0**

(22) Date of filing: **30.10.81**

(54) **Multichannel digital speech synthesizer employing adjustable parameters.**

(30) Priority: **31.10.80 NL 8005989**

(43) Date of publication of application:
12.05.82 Bulletin 82/19

(45) Publication of the grant of the patent:
29.01.86 Bulletin 86/05

(84) Designated Contracting States:
BE DE FR GB SE

(56) References cited:
EP-A-0 016 427
US-A-3 715 512
US-A-3 975 587

ICASSP 79, PROCEEDINGS OF A IEEE INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH AND SIGNAL PROCESSING (April 2-4, 1979, WASHINGTON), NEW YORK (US), L. NEBBIA et al.: "Eight-channel digital speech synthesizer based on LPC techniques", pages 884-886

(73) Proprietor: **Staat der Nederlanden (Staatsbedrijf der Posterijen, Telegrafie en Telefonie)**
P.O. Box 430
NL-2260 AK Leidschendam (NL)

(72) Inventor: **Maathuis, Petrus Gerardus Maria**
Edelsteenweg 15
NL-2651 SP Berkel en Rodenrijs (NL)
Inventor: **Oberman, Maarten Roelof**
Bergluststraat 6a
NL-3054 BM Rotterdam (NL)

Courier Press, Leamington Spa, England.

EP 0 051 342 B1

Description

The invention relates to a digital multichannel speech synthesizer operating according to the linear-predictive-coding method, comprising:

- a speech generator including a digital noise generator, an adjustable digital pitch generator, and a controllable change-over switch for selectively connecting one of said generators to an output;
- an adjustable digital filter adapted to produce in combination with said speech generator digital speech signals for each of a number of speech signals;
- means for adjusting said speech generator and for controlling said switch by control signals; and
- means for generating interpolated parameters.

A multichannel synthesizer of the kind described above is known from Icassp 79, Proceedings Of An IEEE International Conference On Acoustics, Speech and Signal Processing (April 2—4, 1979, Washington), L. Nebbia et al.: "Eight-channel digital speech synthesizer based on LPC techniques, pages 884—886.

The prior art as disclosed in the article mentioned above describes multichannel synthesizers suitable for applications in which good quality audio responses over a number of time-division channels are required. Although with such prior art multichannel synthesizers a satisfactory performance is achievable, the transmission capacity of the multichannel transmission path between a sending side and a receiving side of a communication section is not exploited to its full extent, while the quality of the synthesized speech is invariable. More in particular this prior art has the deficiency that with decreased traffic load on said transmission path, the amount of idle transmission time, i.e. time segments during which useful information is not transferred, increases and consequently the transmission efficiency declines.

It is an object of the present invention to improve the overall performance of a multichannel synthesizer of the aforementioned kind in that an improved transmission efficiency and an improved quality of synthesized speech are achievable. In other words it is an object of the present invention to effect an advantageous trade-off between quality and quantity, thereby more efficiently exploiting the transmission time available on the multichannel transmission path.

A digital multichannel speech synthesizer is according to the invention characterized in that said speech generator in combination with control means are adapted to selectively vary the number of bits involved in the computation of each parameter and/or the number of parameters effective for generating synthesized speech, in dependence on the multichannel load; said control means comprising:

- a pre-processing unit having included therein means to separate control signals from a multichannel speech input, means to derive from said control signals data representing the number of interpolations to be carried out between successively received frames on said input, and means to carry out said number of interpolations; and
- a store to temporarily store the coded speech signals for the control of said adjustable filter.

A multichannel synthesizer structured in accordance with the principles of the present invention inherently has the options to selectively control a) the number of interpolations between successively received samples of speech (set of parameters), and b) the number and/or "width dimension" (number of bits) of the parameters (filter coefficients) included in the respective speech samples. Therefore the quality of the synthesized speech can be improved when the traffic load is lowered.

An embodiment of a digital multichannel speech synthesizer is according to the present invention characterized thereby that said pre-processing unit further comprises

- a function decoder adapted to decode control signals from said input;
- registers, a converter, a fraction table and a counter, which in combination are effective to determine the number of interpolations to be carried out on the basis of data in said control signals;
- a microprocessor, which in response to data derived from said fraction table and data from a speech data input controls the computation of the number of interpolations; and
- an adder-multiplier for carrying out the interpolations under control of said microprocessor and to transfer the interpolated parameters to a computing unit included in said control means via lines.

The above embodiment is illustrative of a specific structure for the implementation of interpolation processes wherein on the basis of knowledge about the time available between successively received samples of speech, a correspondingly varied number of interpolations is carried out.

A further embodiment of a digital multichannel speech synthesizer is according to the present invention characterized thereby that said means for adjusting said speech generator in combination with said control means include

- a series-to-parallel converter, which under control of a central processing unit selectively varies the number of bits included within the parameters provided at its input, in dependence on the multichannel load; and
- an auxiliary control unit, which under control of said central processing unit is effective to cause a computing unit to compute a number

of parameters depending on the multichannel load.

The further embodiment described above is illustrative of a specific structure by which on the basis of knowledge about the traffic load of the multichannel transmission path, (and therefore on the basis of available transmission time) the number of coefficients and/or the number of bits per coefficient can be correspondingly varied.

The above-mentioned and other features and objects of this invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawing, in which:

Fig. 1 is a general block diagram of a speech synthesizer;

Fig. 2 is a block diagram of the speech synthesizer according to the invention;

Fig. 3 illustrates a preferred embodiment of the pre-processing unit of the device according to the invention;

Fig. 4 illustrates a preferred embodiment of the computing unit of the device according to the invention;

Fig. 5 is the flow-chart of the pre-processing unit (9) of the device of Fig. 2 and

Fig. 6 is the flow-chart of the central processing unit (11) of the device of Fig. 2.

Fig. 1 is a general block diagram of a speech synthesizer. The adjusting parameters for the device are designated by the letters a, b, c and d. The circuit comprises a digital noise source 1, which generates white noise for unvoiced speech components, and a digital pitch generator 2, which generates the fundamental frequency for voiced speech components and is adjusted according to parameter a. The choice between generators 1 and 2 is made by switch 3 as controlled by parameter b. Then the digital signal is applied successively to an adjustable digital ladder filter 4, controlled by parameter c, and a digital volume regulator 5, controlled by parameter d. A digital-to-analog converter 6 converts the digital signal into an analog signal. Fig. 2 is a block diagram of the device according to the invention. A digital input signal incorporating the parameters a, b, c and d is applied to input 7 of the speech synthesizer and led to a buffer 8. The parameters a, b, c and d have been determined by the "linear predictive coding" method and can come from a storage medium, in the case of a message that has to be repeated regularly or from a transmission line. A preprocessing unit 9 ensures the reading of the parameters and their storage in portion 10.1 of store 10, the interpolation of two successive groups of parameters, the transfer of the interpolation results to other parts of the circuit and the passing of control data to the central processing unit 11.

The data stored in store portion 10.1 can be transferred to a second store portion 10.2, when the preceding data stored in 10.2 have been processed. Processing takes place in a computing unit 12, which employs the interpolated data for adjusting the ladder filter (Fig. 1; 4) incorporated in the computing unit. In the meantime store portion 10.1 is filled again. The computing unit 12 of this embodiment can compute the digital speech signals for 16 speech channels simultaneously. These digital speech signals are stored in "first-in-first-out" buffers 13.1... 13.16 (one signal per channel) and then led to digital-to-analog converters 6.1... 6.16, respectively. The computing unit 12 is controlled in conformity with fixed rules by a control unit 14, which receives its instructions from the central processing unit 11.

Fig. 3 illustrates a preferred embodiment of the pre-processing unit 9 according to the invention, and store portion 10.1. The data coming from the buffer (Fig. 2; 8) are led to a series-to-parallel converter 15. The discriminator 16 infers from the first few bits of a 24-bit frame whether this frame contains speech data or control information, in which cases a data buffer 17 or a control buffer 18 is opened, respectively. The speech data are led from the data buffer 17 via a data bus 19 to a microprocessor 20, which is connected to the central processing unit (Fig. 2; 11) via a control bus 21 and an address bus 22. Store 23 (RAM) and decoding store 24 (ROM) are also connected to this data bus. Further, the circuit comprises an adder-multiplier 25 for carrying out parts of interpolation calculations.

The group of parameters comprises, as has already been observed, the following four:

a. the pitch, for which the data are led via output 27 to the computing unit (Fig. 2; 12);

b. the voiced/unvoiced decision, for which the data are also led to said computing unit via output 26;

c. the reflection coefficients K_1^n to K_M^n, 1st and Mth reflection coefficient, respectively, of the nth group of parameters read, the data of which are led to store portion 10.1, while the data transferred to store portion 10.2 are being handled;

d. the volume of output signal C^n, the data of which are also led to store portion 10.1.

The data for parameters a and b have no effect upon the ladder filter (Fig. 1; 4), so that they can be handled in a different manner and need not pass the store 10, as will be described hereinafter.

The function of the speech data portion of the circuit of Fig. 3 is described as separating the parameters a, b, c and d and interpolating the parameters c and d. Interpolation is necessary, because the speech information arrives in bursts and because annoying clicks could occur without interpolation. Every time a group of data n is written in register 23, the interpolation with the preceding group of data, n−1, is carried out by the microprocessor 20 with the aid of the adder-multiplier 25 and store 24 in accordance with the formula

$$K_i^{nl}=K_i^{n-1}\cdot\left[\frac{L-l}{L}\right]+K_i^n\left[\frac{l}{L}\right], \qquad (1)$$

in which l=0... L−1, L being the number of

interpolations desired. I indicates the number of a group interpolated between the groups n−1 (I=0) and n (I=L). The coefficients

$$\frac{L-I}{L}$$

and

$$\frac{I}{L}$$

are generated by the microprocessor 20.

The reflection coefficients interpolated on the basis of rule (1) and the interpolated volume are led to store 10.1.

According to the invention, the pre-processing unit comprises means for adjusting the quality of the speech reproduced according to the degree of occupation of the transmission medium. Therefore, at the transmitting end, relevant data are sent along with the control signals. These data are interpreted in the function decoder 28. Further, the circuit comprises a register 29, for recording the number of interpolations to be carried out by the microprocessor 20 on the unvoiced part of the speech, and a register 30, which has an analogous function with regard to the voiced part of the speech. Registers 29 and 30 are connected to ROM store 31, which converts the number of interpolations to be carried out into a signal for positioning counter 32, stepping in synchronism with a counter incorporated in microprocessor 20. The position of counter 32 is passed to a fraction table 33 (ROM), connected via a selector 34 to control bus 21 and address bus 22. Under the control of the central processing unit (Fig. 2; 11), the number of interpolations to be carried out by the microprocessor 20 can be fixed. The circuit of Fig. 3 also contains registers 35 and 36 for recording adjusting data for the adjustable filter incorporated in the computing unit (Fig. 2; 12). The adjusting data for unvoiced speech are stored in register 35, those for voiced speech in register 36. A ROM 37, converts the adjusting data into positioning data for counter 38. Via selector 39 the counter position is passed to buses 21 and 22, after which the number of calculations to be carried out by the control unit (Fig. 2: 14) is fixed under the control of the central processing unit (Fig. 2; 11).

Furthermore, the circuit may contain a register 40 for recording a signal indicating that the next one or two frames contain no speech. The relevant data can be passed via selector 41 and buses 21 and 22 to the central processing unit (Fig. 2; 11), so that the computing unit (Fig. 2; 12) can spend the time thus saved in dealing with other channels. The circuit may comprise a register 42 and a selector 43 for recording the signal indicating that one or two new frames contain the same information as the preceding frame, so that the new frames need not be transmitted. Because the preceding frame is in the buffer (Fig. 2; 8) for interpolation purposes, repetition will suffice, so that transmission capacity is saved. In an analogous way information concerning the degree of compression and expansion of the speech signal can be received and handled.

Fig. 4 illustrates a preferred elaboration of store 10.2, computing unit 12, buffers 13 and control unit 14. The data stored in 10.1 (Fig. 2) are transferred to store 10.2 under the control of the central processing unit 11. The data stored in 10.2, containing the information for computing the digital signal to be supplied to the buffers 13, are led to multipliers 44 and 45 working in parallel, adder-subtractor 46, AND-circuit 47 and D-flip-flop 48. Selector 49 determines the number of bits to be calculated per PCM-word and a round-off factor. D-flip-flop 50 ensures in a well-known manner the adaptation to bus traffic. The results of a first calculation are written, for sixteen separate channels, in buffers 51, from which they can be output via D-flip-flops 52. The voiced/unvoiced and pitch data are sent via output 26 to electronic switch 3 and via output 27 to generator 2, respectively, and combined by means of D-flip-flop 53 with the digital signal to be calculated. The whole algorithm can be represented by the following formulae:

$$Y_m(i)=Y_{m+1}(i)-K_m b_m(i-1) \qquad (2)$$

and

$$b_{m+1}(i)=b_m(i-1)+K_m Y_m \qquad (3)$$

in which

$$m=M-1,\ldots,o \qquad (4)$$

and

$$b_o(i)=Y_o(i) \qquad (5)$$

Multipliers 44 and 45 ensure the multiplications and adder-subtractor 46 carries out the adding and subtracting operations. The intermediate results of the operations are put away, every time, in the 51-buffer associated with the channel dealt with. Every time one sample has been calculated, its value is multiplied by the volume factor C_n. The various operations carried out on the data from store 10.2 are controlled by a programmable store (PROM) 54, which, under the control of a counter 55, makes a step every time after the calculation of one PCM-sample for each of the 16 channels. The stepping of counter 55 is timed by clock 56. Store 54 supplies the data required for carrying out the various operations via a control bus 57 and the address data for store 10 via address bus 58. The last instruction in store 54 relates to writing the calculated final results in buffers 13 and signalling to the central processing unit 11 (Fig. 2) that the programme has finished. Then, under the control of central processing unit 11 (Fig. 2), a fresh set of data is transferred from store 10.1 to store 10.2, clock 56 being started in

order to carry out again the programme contained in store 54. The data produced by the programme will only be stored when the central processing unit 11 (Fig. 2) has found that the buffers 13 are not full. After the data have been stored in buffers 13, the programme is started again under the control of the central processing unit 11. Thus the invention provides a relatively simple device for generating, from an input signal produced by the LPC-method referred to hereinabove, an analog signal for a large number of channels. The pre-processing unit 9 and the central processing unit 11 comprise microcomputers, for which the flow-charts are given in Figs. 5 and 6, respectively. The arrangement is not relevant for a good understanding of the invention, so that the flow-chart need not be described in detail. After a start command the microprogramme stored in the control unit 14 (Fig. 4) is carried out.

As soon as counter 55 (Fig. 4) has reached its final position, the last instruction contained in store 54 passes the signal "End of programme" to the central processing unit 11, which checks whether buffers 13 are full. In the affirmative case the programme is stopped. If there is space left in buffers 13, the next PCM-word is calculated.

Claims

1. Digital multichannel speech synthesizer operating according to the linear-predictive-coding method, comprising:

- a speech generator including: a digital noise generator (1), an adjustable digital pitch generator (2), and a controllable change-over switch (3) for selectively connecting one of said generators (1, 2) to an output;
- an adjustable digital filter (4) adapted to produce in combination with said speech generator digital speech signals for each of a number of speech signals;
- means (a, b) for adjusting said speech generator and for controlling said switch by control signals; and
- means for generating interpolated parameters, characterized in that said means for adjusting said speech generator in combination with control means (9; 10.1, 10.2; 11, 14, 12) are adapted to selectively vary the number of bits involved in the computation of each parameter and/or the number of parameters effective for generating synthesized speech, in dependence on the multichannel load; said control means comprising:
- a pre-processing unit (9) having included therein—means (16, 18) to separate control signals from a multichannel speech input, means (28, 29, 30, 31, 32, 33) to derive from said control signals data representing the number of interpolations to be carried out between successively received frames on said input, and means (20, 23, 24, 25) to carry out said number of interpolations; and
- a store (10) to temporarily store the coded speech signals for the control of said adjustable filter.

2. Synthesizer according to claim 1, characterized in that said pre-processing unit (9) further comprises

- a function decoder (28) adapted to decode control signals from said input;
- registers (29, 30), a converter (31), a fraction table (33) and a counter (32), which in combination are effective to determine the number of interpolations to be carried out on the basis of data in said control signals;
- a microprocessor (20), which in response to data derived from said fraction table (33) and data from a speech data input (19) controls the computation of the number of interpolations; and
- an adder-multiplier (25) for carrying out the interpolations under control of said microprocessor (20) and to transfer the interpolated parameters to a computing unit (12) included in said control means (9; 10.1, 10.2; 11; 14; 12) via lines (26, 27).

3. Synthesizer according to claim 2, characterized in that said means for adjusting said speech generator in combination with said control means (9; 10.1, 10.2; 11; 14; 12) include

- a series-to-parallel converter (15), which under control of a central processing unit (11) selectively varies the number of bits included within the parameters provided at its input, in dependence on the multi-channel load; and
- an auxiliary control unit (14), which under control of said central processing unit (11) is effective to cause a computing unit (12) to compute a number of parameters depending on the multichannel load.

Patentansprüche

1. Digitaler Mehrkanal-Sprachsynthesizer, der nach dem linear vorhersagenden Kodierverfahren arbeitet, umfassend:

- einen Sprachgenerator enthaltend: einen digitalen Geräuschgenerator (1), einen einstellbaren, digitalen Tonhöhegenerator (2) und einen steuerbaren Umschalter (3), um wahlweise einen dieser Generatoren (1, 2) mit einem Ausgang zu verbinden;
- ein einstellbares digitales Filter (4), um in Kombination mit dem Sprachgenerator digitale Sprachsignale für jedes einer Mehrzahl von Sprachsignalen zu erzeugen;
- Mittel (a, b) zum Einstellen dieses Sprachgenerators und zum Steuern dieses Umschalters mittels Steuersignalen; und
- Mittel zum Erzeugen interpolierter Parameter, dadurch gekennzeichnet, dass die Mittel zum Einstellen des Sprachgenerators, zusammen

mit Regelmitteln (9; 10.1; 10.2; 11; 14; 12), so ausgebildet sind, dass sie selektiv die Anzahl der zum Errechnen jedes Parameters benützten Bits und/oder die Anzahl der zur Erzeugung synthetisierter Sprache benützten Parameter variieren in Abhängigkeit der Mehrkanal-Belastung; wobei die Regelmittel umfassen:

— eine Vorbehandlungseinheit (9) enthaltend Mittel (16, 18) zum Trennen von Steuersignalen von einem Mehrkanal-Spracheingang, Mittel (28, 29, 30, 31, 32, 33) zum Ableiten von die Anzahl der zwischen aufeinanderfolgend an diesem Eingang empfangenen Rahmen auszuführenden Interpolationen darstellenden Daten aus diesen Steuersignalen, und Mittel (20, 23, 24, 25) um diese Anzahl Interpolationen auszuführen; und
— einen Speicher (10) zum vorübergehenden Speichern der kodierten Sprachsignale für die Steuerung des einstellbaren Filters.

2. Synthsizer nach Anspruch 1, dadurch gekennzeichnet, dass die Vorbehandlungseinheit (9) zudem umfasst:

— einen Funktionsdekoder (28) zum Dekodieren von Steuersignalen von diesem Eingang;
— Register (29, 30), einen Wandler (31), eine Bruchtabelle (33) und einen Zähler (32), die im Zusammenwirken die Anzahl von auszuführenden Interpolationen auf Grund von Daten in diesen Steuersignalen ermitteln;
— einen Microprocessor (20), der in Antwort auf aus der Bruchtabelle (33) ermittelten Daten und auf Daten von einem Sprachdateneingang (19) die Berechnung der Anzahl Interpolationen steuert; und
— einen Addierer-Multiplizierer (25) zur Durchführung der Interpolationen unter Kontrolle dieses Microprocessors (20) und zum Weiterleiten der interpolierten Parameter an eine Recheneinheit (12) dieser Regelmittel (9; 10.1; 10.2; 11; 14; 12) über Verbindungsleitungen (26, 27).

3. Synthesizer nach Anspruch 2, dadurch gekennzeichnet, dass die Mittel zum Einstellen des Sprachgenerators zusammen mit den Regelmitteln (9; 10.1; 10.2; 11; 14; 12) umfassen:

— einen Serie-Parallel-Umwandler (15), der, gesteuert durch einen zentralen Processor (11), abhängig von der Mehrkanalbelastung selektiv die Anzahl der in den an seinem Eingang vorhandenen Parametern enthaltenen Bits variiert; und
— eine Hilfsregeleinheit (14), die, gesteuert durch den zentralen Processor (11), eine Recheneinheit (12) veranlasst, die Anzahl Parameter abhängig von der Mehrkanalbelastung zu errechnen.

Revendications

1. Synthétiseur numérique de parole pour plusieurs canaux fonctionnant selon le procédé du codage prédictif linéaire, comprenant:

— un générateur de signaux de parole comportant: un générateur de bruit numérique (1), un générateur de hauteur de son numérique ajustable (2), et un commutateur réglable (3) servant à connecter sélectivement l'un desdits générateurs (1, 2) à une sortie;
— un filtre numérique ajustable (4) conçu pour produire, en combinaison avec ledit générateur de signaux de parole, des signaux de parole numériques pour chaque signal d'un certain nombre de signaux de parole;
— des moyens (a, b) servant à ajuster le générateur de signaux de parole et à commander ledit commutateur au moyen de signaux de commande; et
— des moyens servant à produire des paramètres interpolés, caractérisé en ce que lesdits moyens d'ajustement dudit générateur de signaux de parole en combinaison avec des moyens de commande (9; 10.1, 10.2; 11, 14, 12) sont conçus pour faire varier sélectivement le nombre de bits intervenant dans le calcul de chaque paramètre et, ou bien, le nombre de paramètres pour la production des signaux de parole synthétisés, en fonction de la charge des canaux; lesdits moyens de commande comprenant:
— une unité de prétraitement (9) comportant des moyens (16, 18) permettant de séparer des signaux de commande d'un signal d'entrée formé de signaux de parole à plusieurs canaux, des moyens (28, 29, 30, 31, 32, 33) permettant d'extraire desdits signaux de commande des données représentant le nombre d'interpolations à effectuer entre blocs successivement reçus sur ledit signal d'entrée, et des moyens (20, 23, 24, 25) permettant d'effectuer ledit nombre d'interpolations; et
— une mémoire (10) servant à emmagasiner temporairement les signaux de parole codés en vue de la commande dudit filtre ajustable.

2. Synthétiseur selon la revendication 1, caractérisé en ce que ladite unité de prétraitement (9) comprend en outre:

— un décodeur de fonction (28) conçu pour décoder des signaux de commande à partir dudit signal d'entrée;
— des registres (29, 30), un convertisseur (31), une table de fractions (33) et un compteur (32) qui, en combinaison, peuvent déterminer le nombre d'interpolations à effectuer sur la base des données contenues dans lesdits signaux de commande;
— un microprocesseur (29), qui, en réponse aux données extraites de ladite table de fractions (33) et des données venant d'un signal

d'entrée de données de signaux de parole (19), commande le calcul du nombre d'interpolations; et un additionneur-multiplicateur (25) servant à effectuer les interpolations sous commande dudit microprocesseur (20) et à transférer les paramètres interpolés à une unité de calcul (12) incluse dans lesdits moyens de commande (9; 10.1, 10.2, 11; 14; 12) via des lignes (26, 27).

3. Synthétiseur selon la revendication 2, caractérisé en ce que lesdites moyens servant à ajuster ledit générateur de signaux de parole en combinaison avec lesdits moyens de commande (9; 10.1, 10.2; 11; 14; 12) comporte:

— un convertisseur série-parallèle (15) qui, sous commande d'une unité centrale de traitement (11) fait sélectivement varier le nombre de bits inclus à l'intérieur des paramètres présents à son entrée, en fonction de la charge des canaux; et une unité de commande auxiliaire (14), qui, sous commande de ladite unité centrale de traitement (11) permet d'amener une unité de calcul (12) à calculer un nombre de paramètres en fonction de la charge des canaux.

FIG. 1

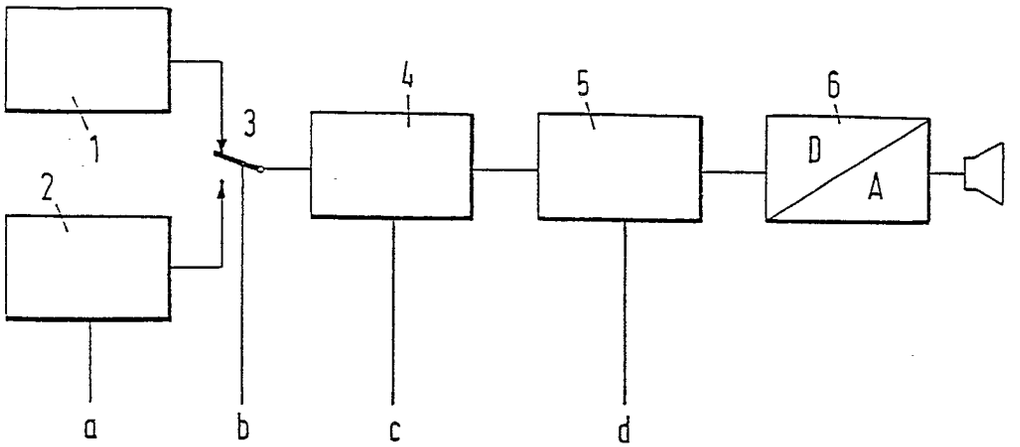
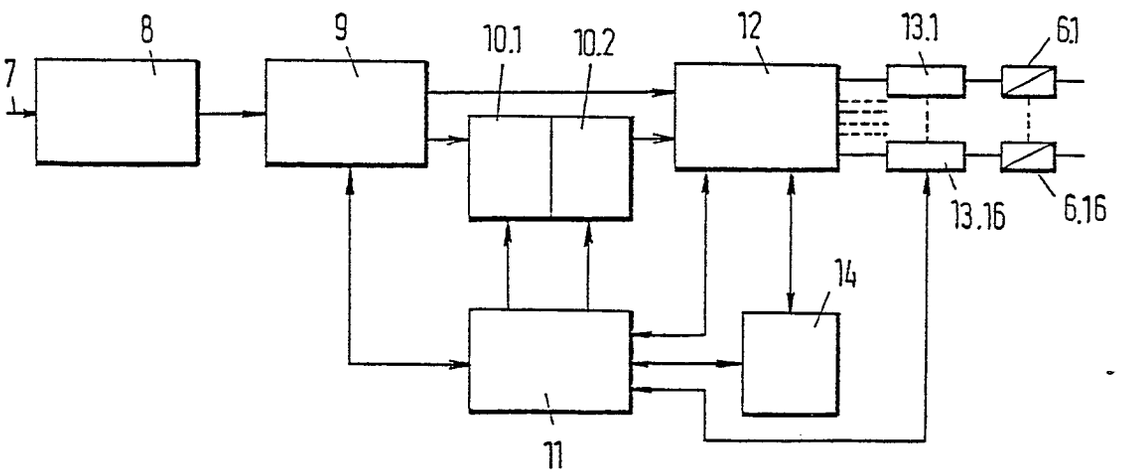


FIG. 2



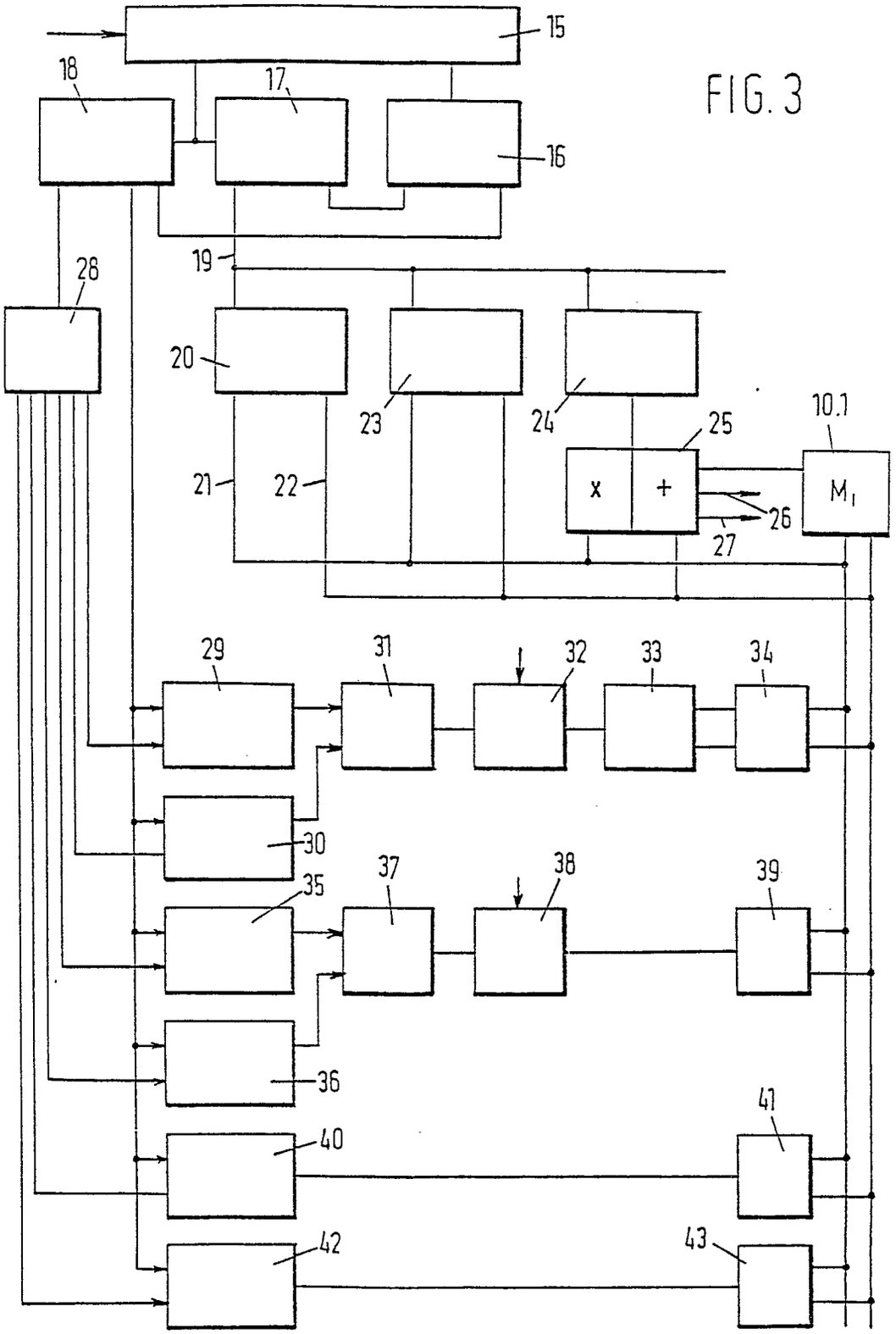

15
18
17
16
19
28
20
23
24
25
10.1
21
22
x
+
M_1
26
27
29
31
32
33
34
30
37
38
39
35
36
41
40
42
43

FIG. 3

FIG.4

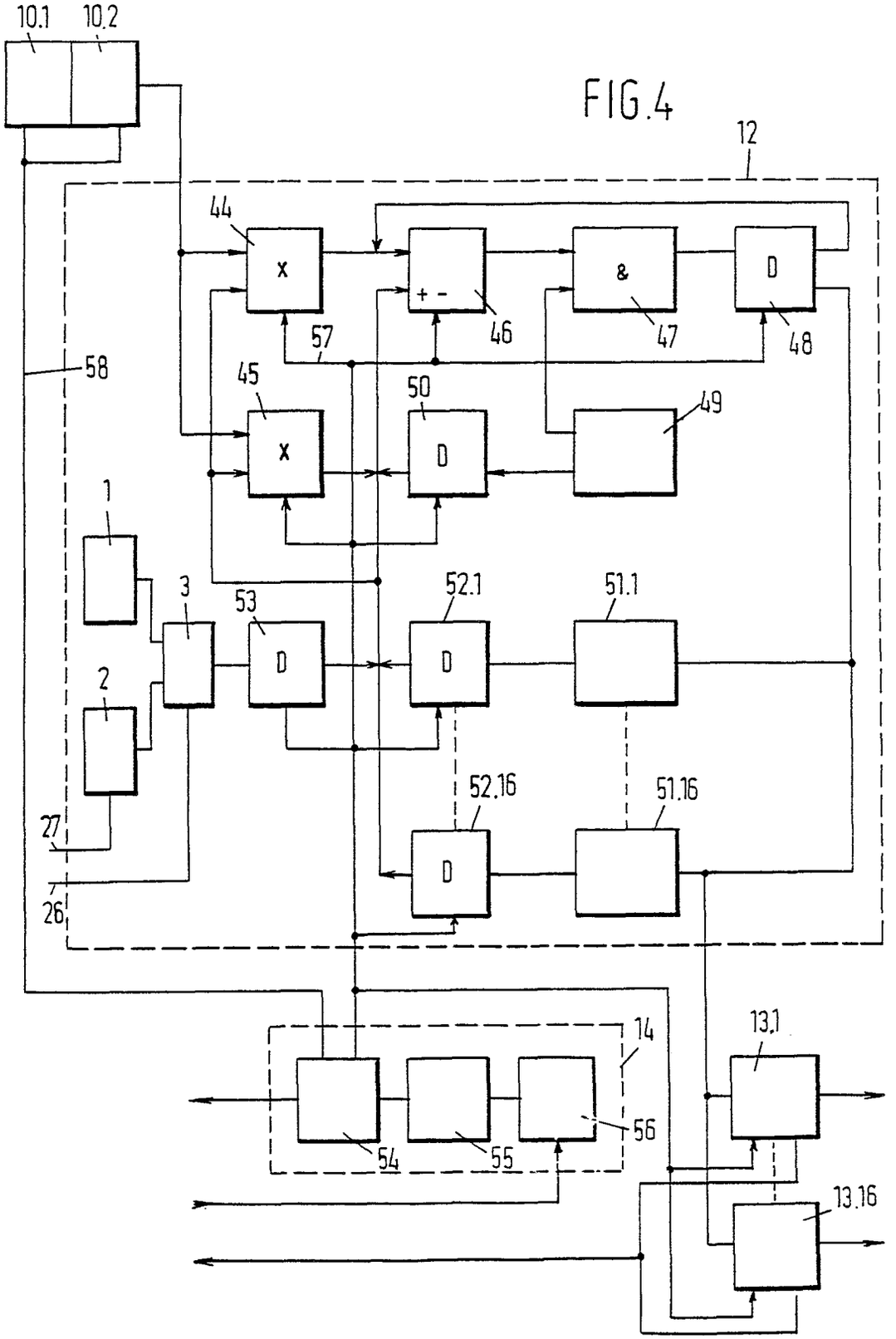

10.1
10.2
12
44
X
+ -
&
D
46
47
48
57
58
45
X
50
D
49
1
3
53
D
52.1
D
51.1
2
52.16
51.16
27
D
26
14
13.1
54
55
56
13.16

FIG 5A

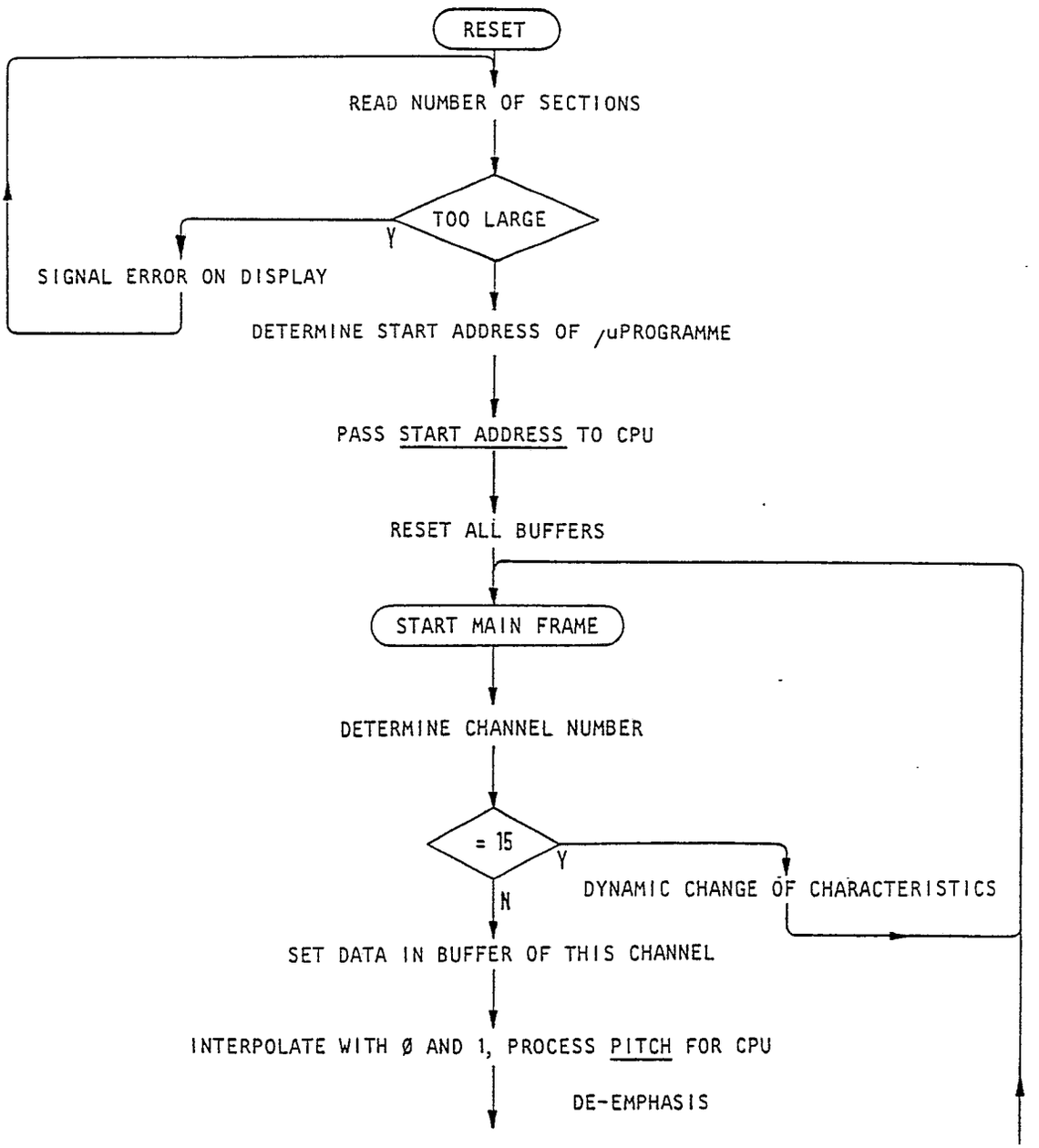

RESET
READ NUMBER OF SECTIONS
TOO LARGE
Y
SIGNAL ERROR ON DISPLAY
DETERMINE START ADDRESS OF µPROGRAMME
PASS START ADDRESS TO CPU
RESET ALL BUFFERS
START MAIN FRAME
DETERMINE CHANNEL NUMBER
= 15
Y
DYNAMIC CHANGE OF CHARACTERISTICS
N
SET DATA IN BUFFER OF THIS CHANNEL
INTERPOLATE WITH Ø AND 1, PROCESS PITCH FOR CPU
DE-EMPHASIS

FIG. 5B

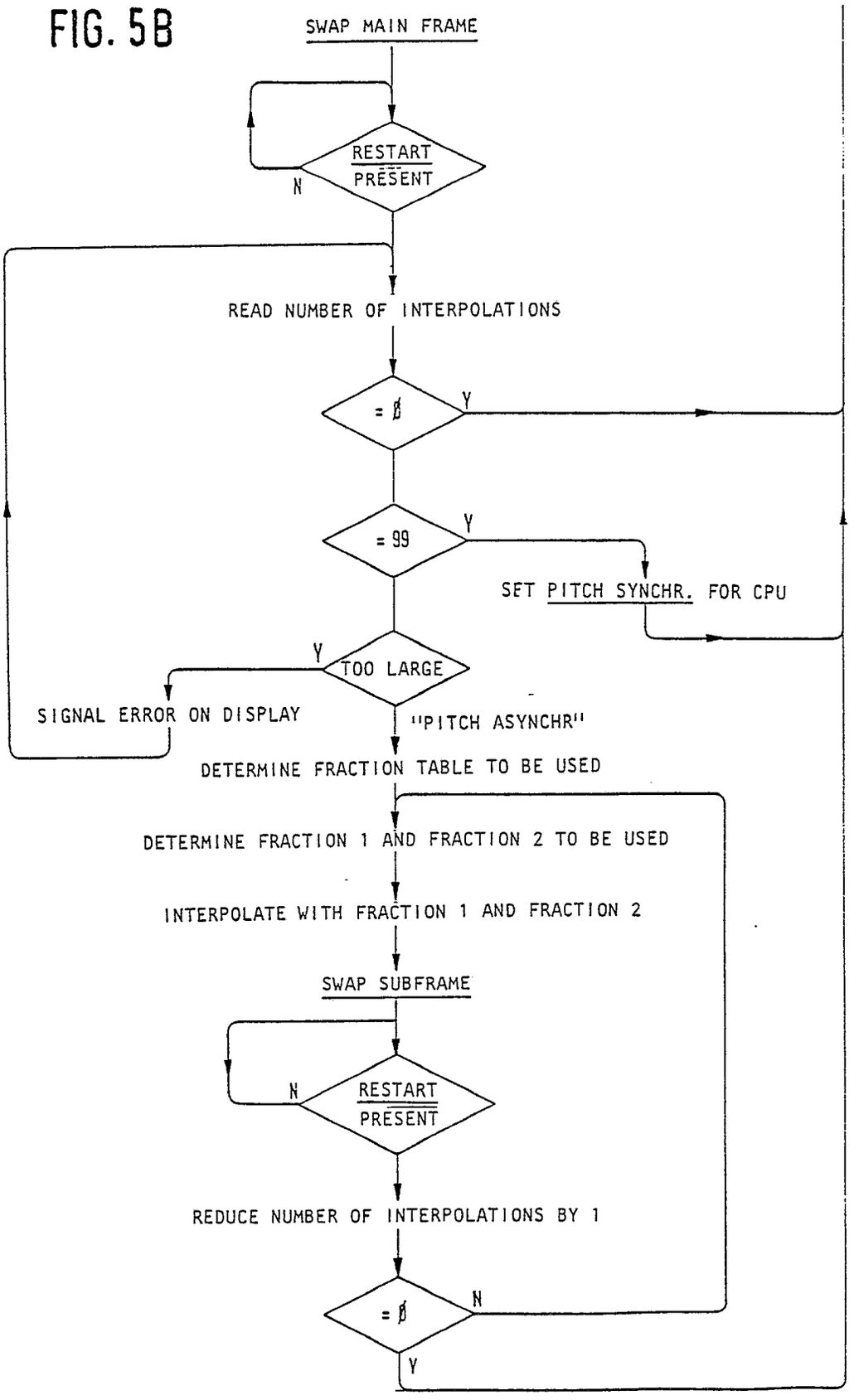
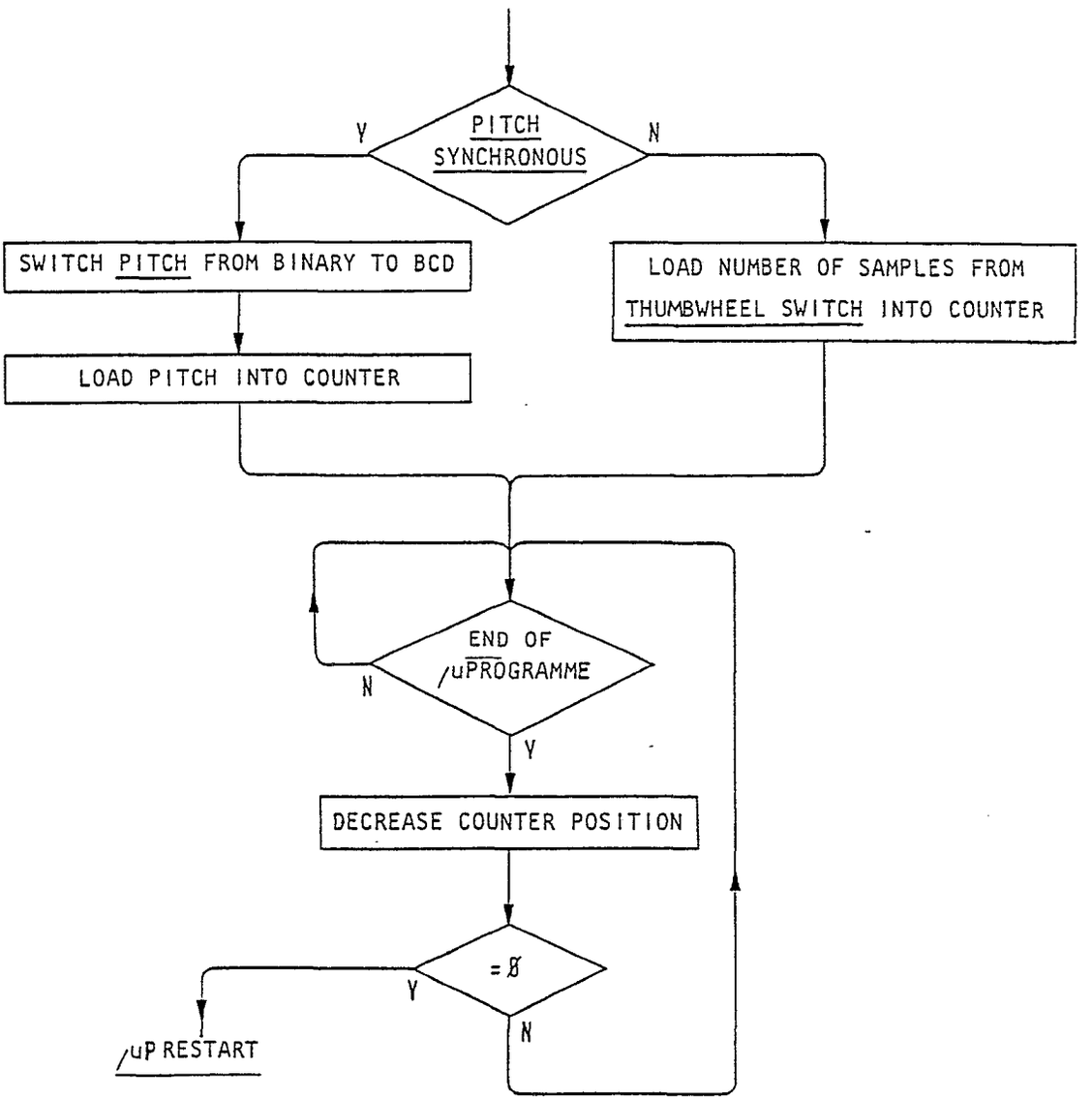

SWAP MAIN FRAME
RESTART PRESENT
N
READ NUMBER OF INTERPOLATIONS
= Ø
Y
= 99
Y
SET PITCH SYNCHR. FOR CPU
Y
TOO LARGE
SIGNAL ERROR ON DISPLAY
"PITCH ASYNCHR"
DETERMINE FRACTION TABLE TO BE USED
DETERMINE FRACTION 1 AND FRACTION 2 TO BE USED
INTERPOLATE WITH FRACTION 1 AND FRACTION 2
SWAP SUBFRAME
N
RESTART PRESENT
REDUCE NUMBER OF INTERPOLATIONS BY 1
= Ø
N
Y

FIG. 6



COUNTER COUNTS REMAINING NUMBER OF SAMPLES IN THIS FRAME