

[54] **TRAFFIC CONTROL SYSTEM**
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 [58] Field of Search..... **340/31, 37**

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[57] **ABSTRACT**

The traffic system includes a vehicle and pedestrian section and may be used for complex traffic flow conditions. A three phase traffic controller is disclosed defining phases A, B, and C. Each section of the system is provided with an indicator panel, a binary counter for indicating phase and interval timing, timing circuitry, and relay drive circuitry for actuating traffic signals. Separate gate and memory circuits are also used for each phase. The operation of the system is such that if the system is in any phase such as phase C and there are no calls from the other phases it remains in phase C. If there is a call from another phase and there are no vehicles being detected or prior pedestrian signals being displayed in phase C it moves to that other phase. If phase C is still detecting vehicles or displaying prior pedestrian signals a predetermined time period elapses before the system selects the phase that has called. The system also has the capability of skipping phases that have not called by going from C directly to B skipping A if A has not called.

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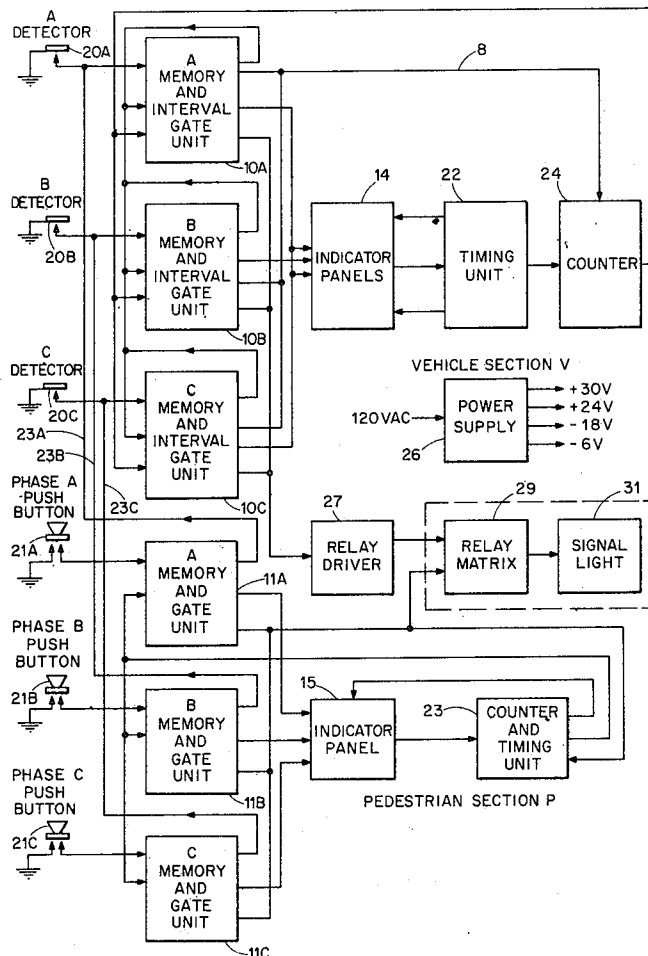
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21 Claims, 8 Drawing Figures



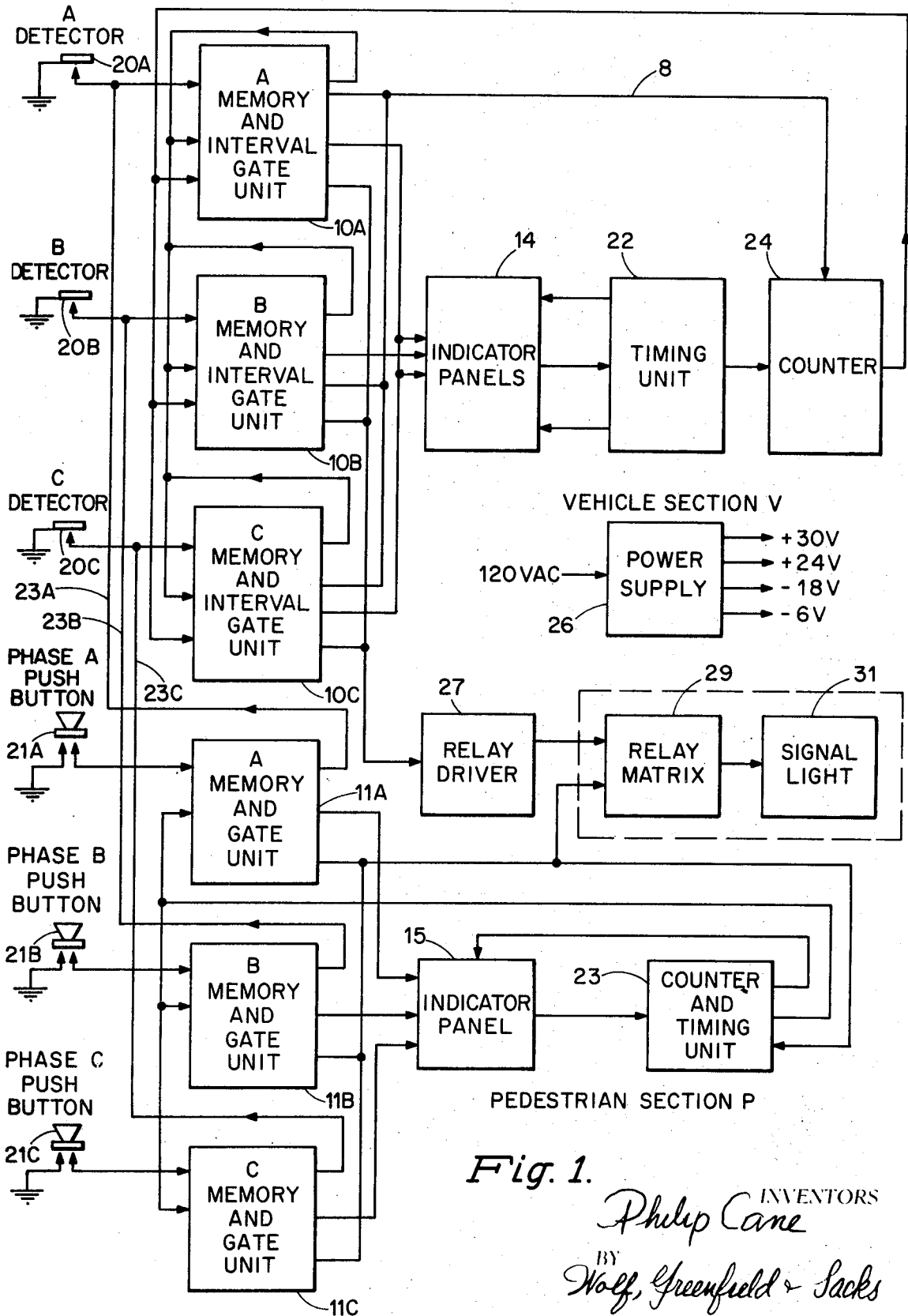


Fig. 1.

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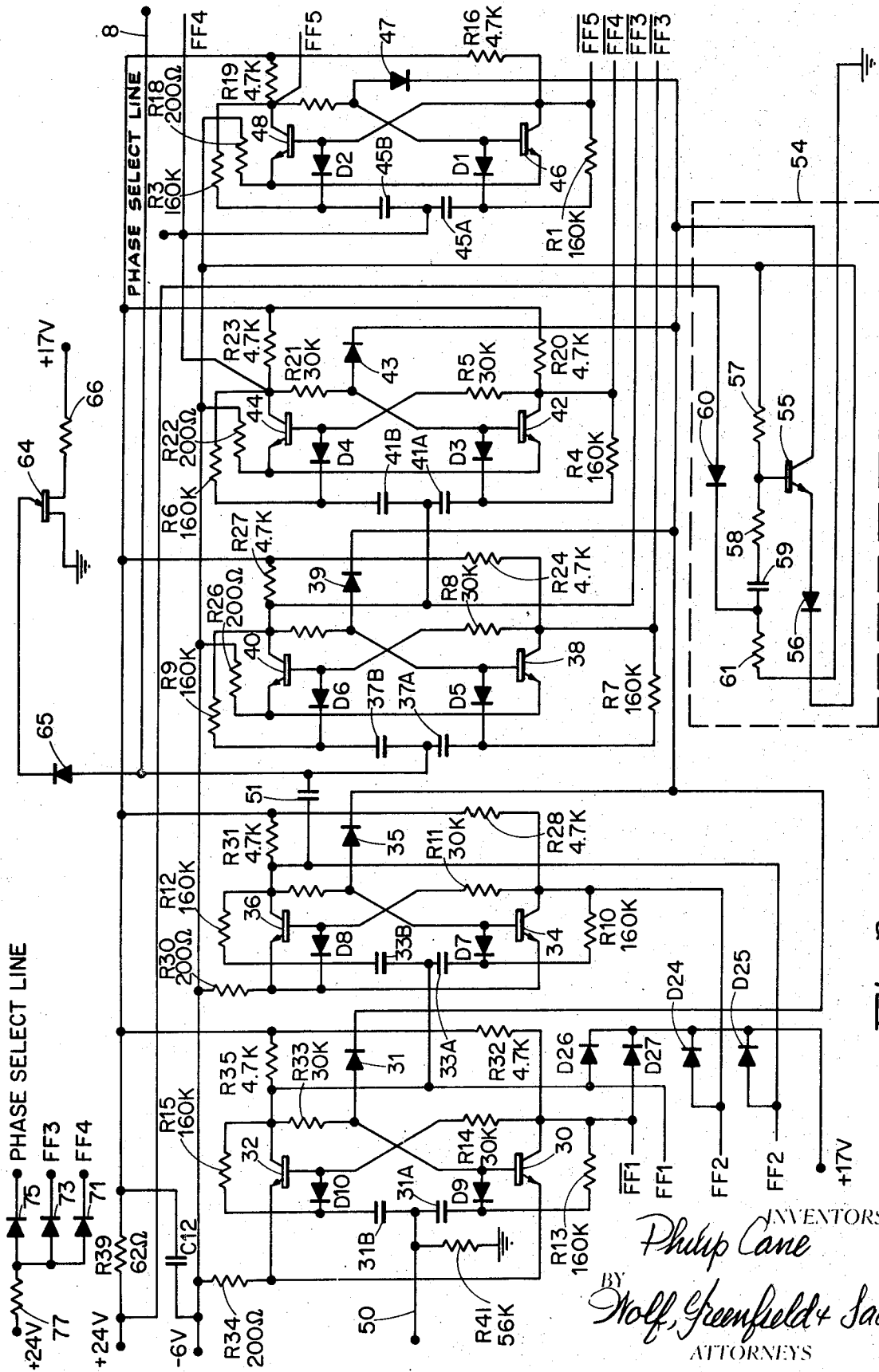


Fig. 2.

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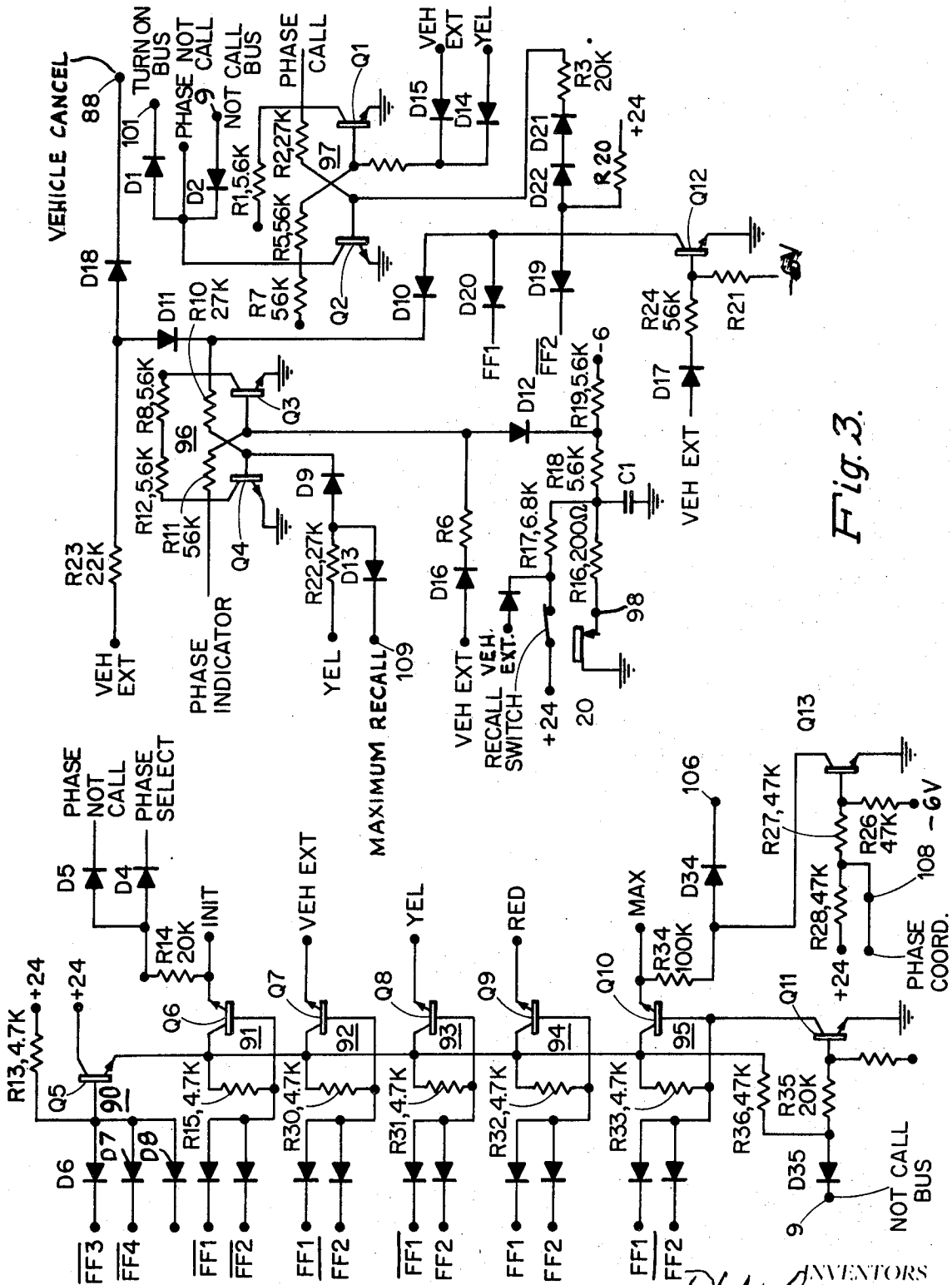


Fig. 3.

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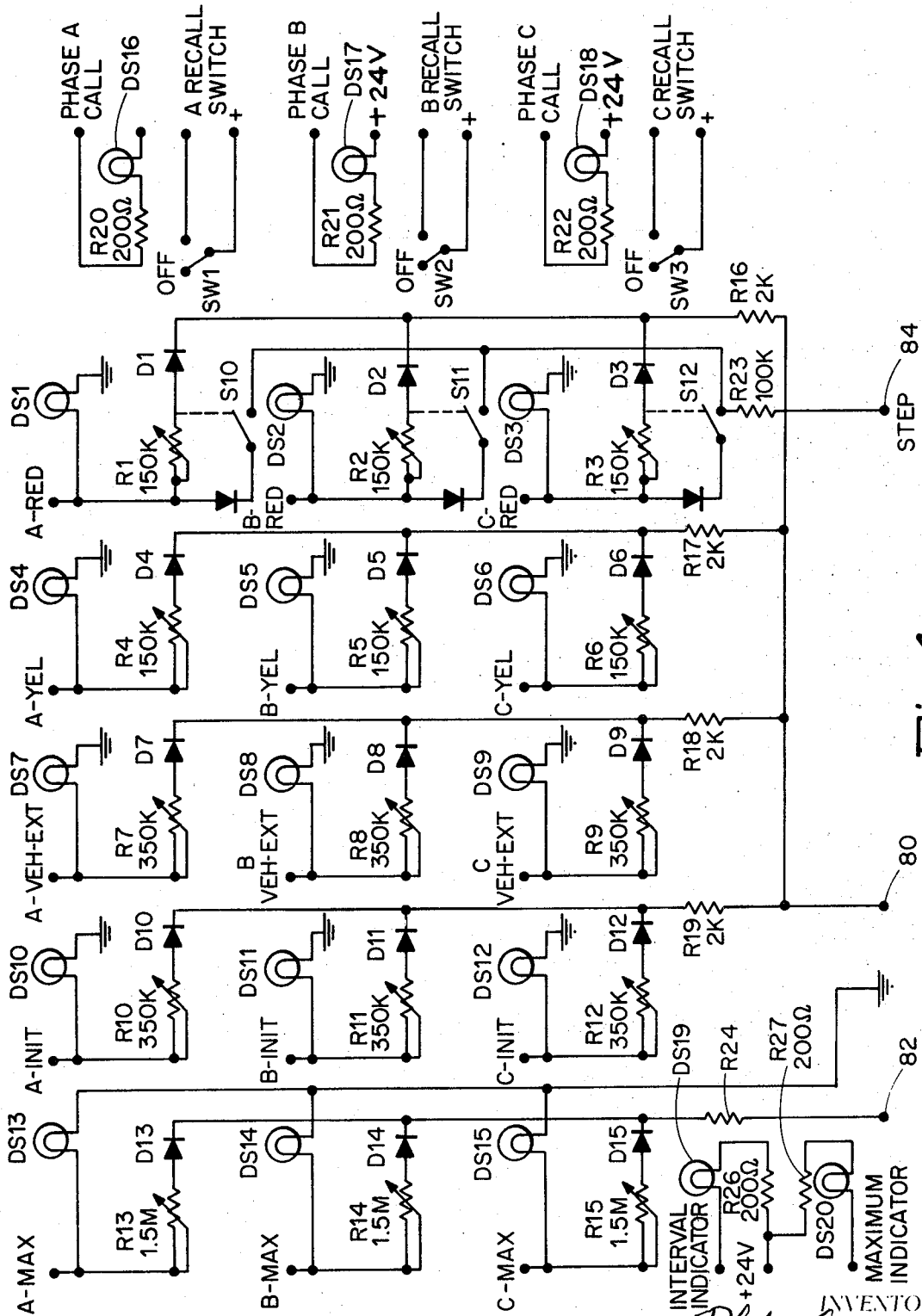


Fig. 4.

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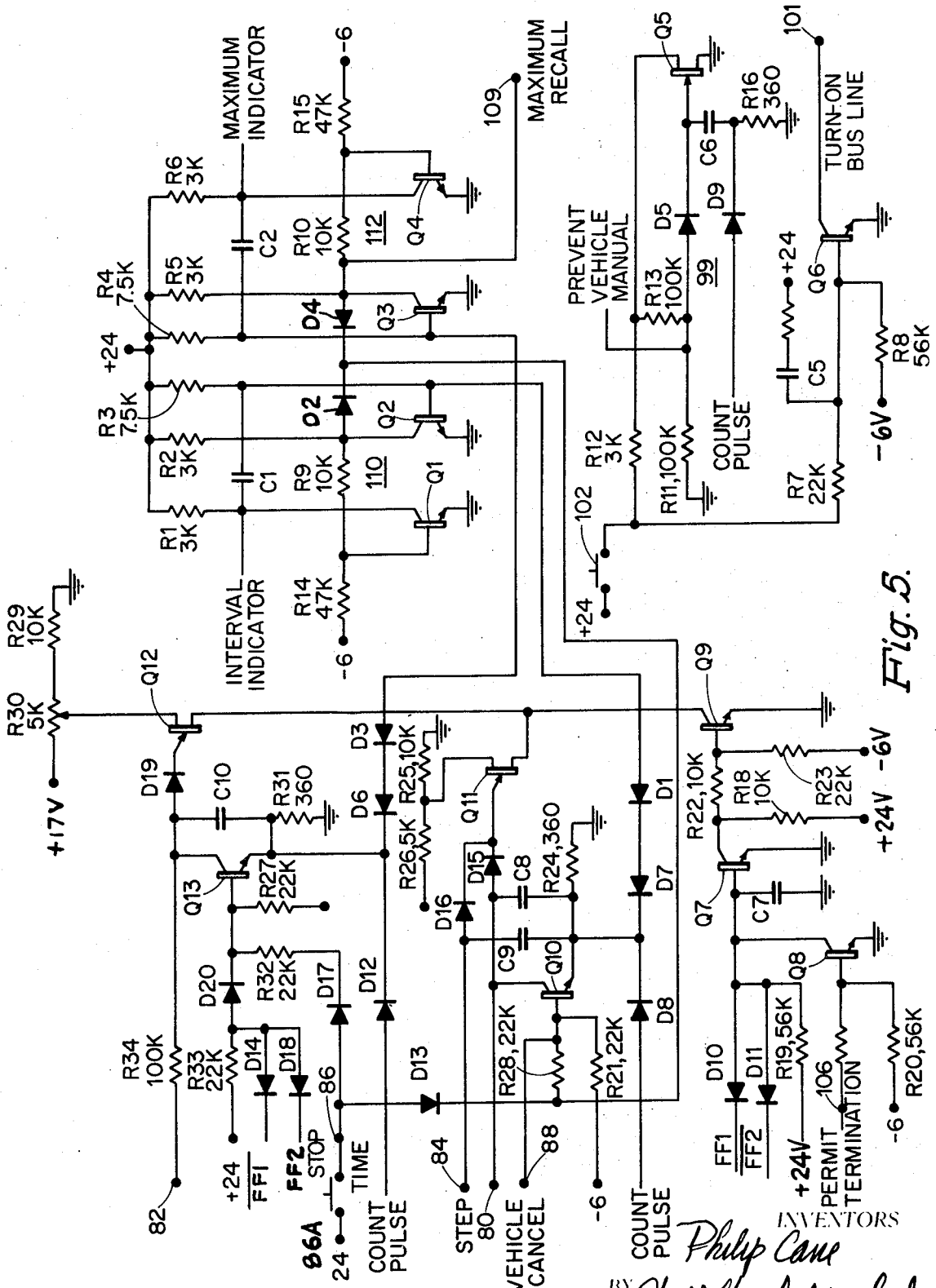


Fig. 5.

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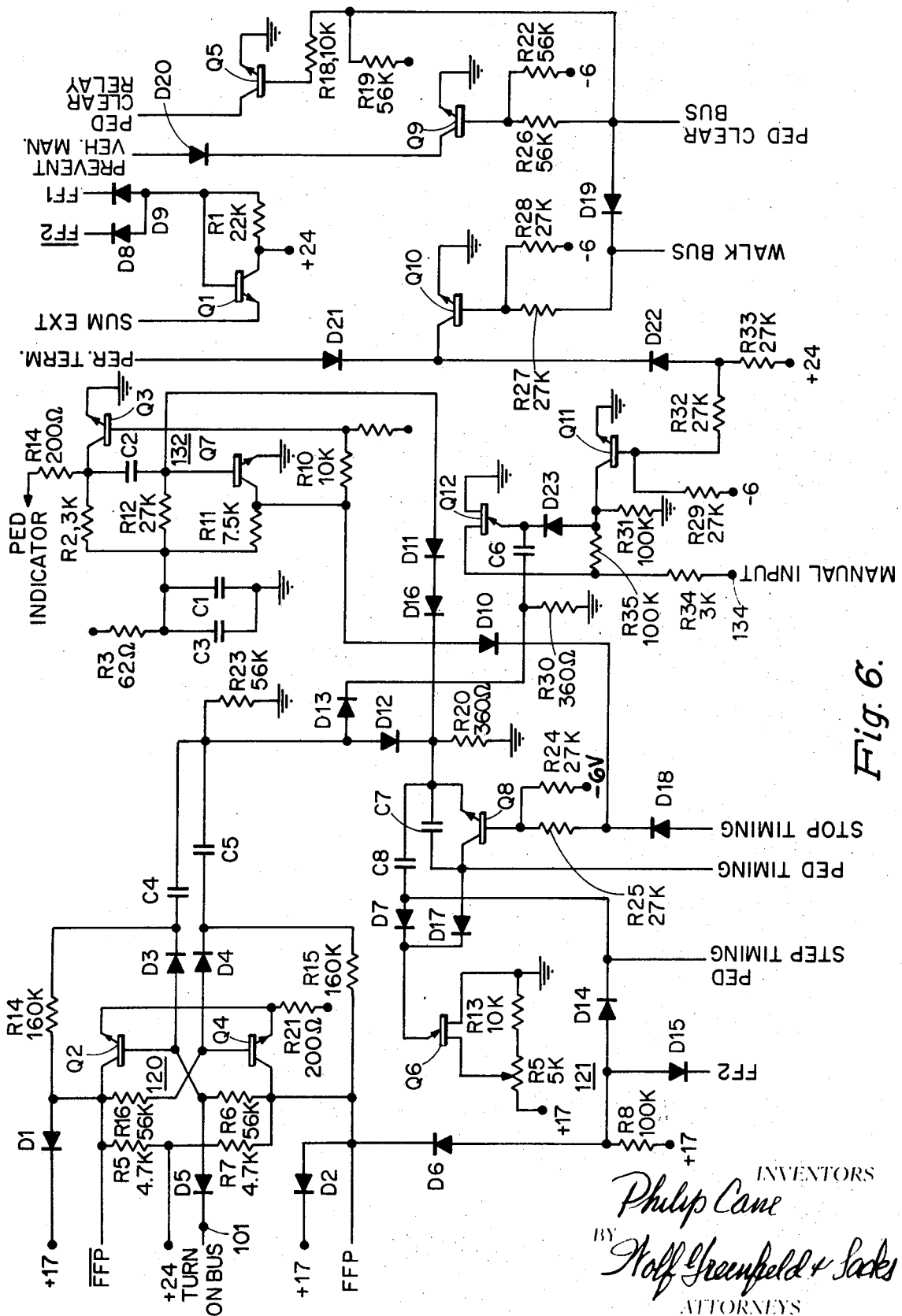


Fig. 6.

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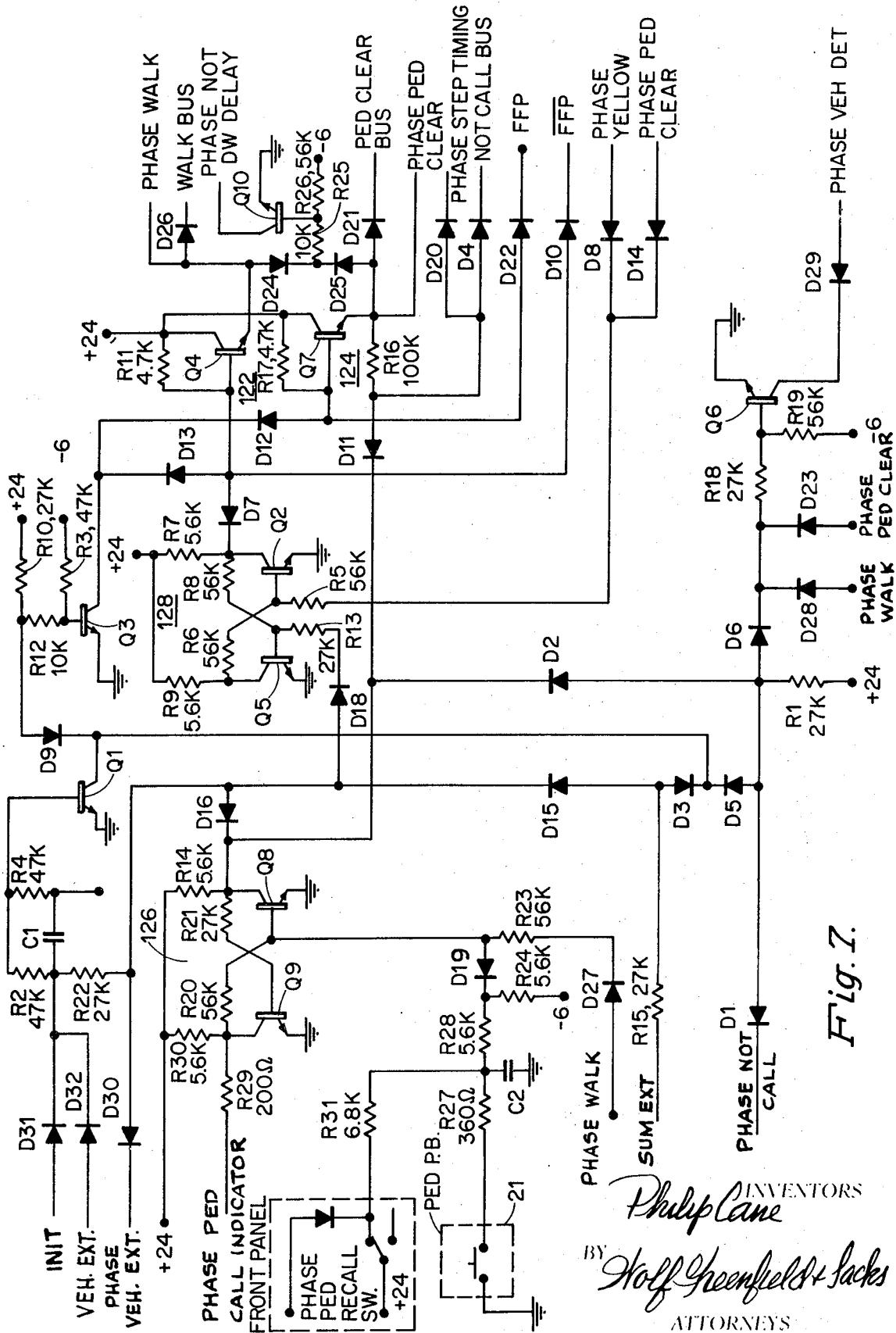


Fig. 1.

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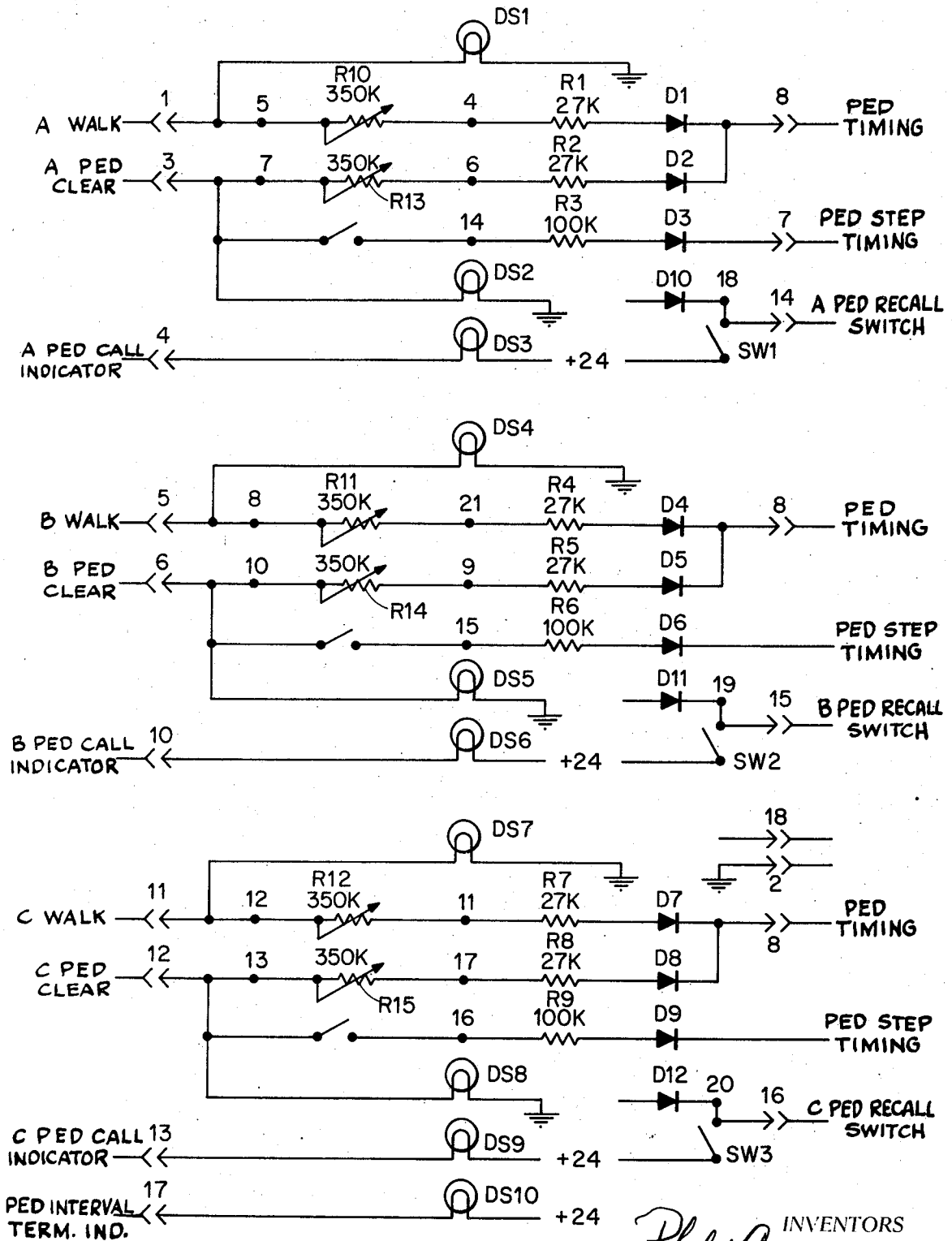


Fig. 8.

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TRAFFIC CONTROL SYSTEM

BACKGROUND OF THE INVENTION

The present invention pertains in general to a traffic control system that is particularly useful where complex traffic flow conditions exist.

There has been a rapid increase in the number of vehicles used on highways. Thus, the effective regulation of traffic flow conditions has become more difficult. The usual two phase system for operating a standard intersection with a main street and a cross street is often inadequate. Therefore, a traffic control system for effectively regulating complex traffic flow conditions is becoming more necessary.

Accordingly, it is an object of the invention to provide an improved traffic system for controlling a plurality of traffic control conditions.

It is another object of the invention to provide a traffic control system in accordance with the preceding object in which means are associated with multiphases for storing a phase call indication.

It is a further object of the invention to provide a multiphase traffic control system including means associated with each traffic flow condition for requesting that traffic flow condition.

Another object of the invention is to provide means associated with each traffic flow condition for extending the time period of that condition (phase) when vehicles are being detected within that phase and a call is received from another phase.

A further object of the invention is to provide a traffic control system that is capable of both pedestrian and vehicle actuable operation.

Still a further object of the invention is to provide a traffic control system according to the preceding objects that is effective in operation, simple in construction, reliable and may be built relatively inexpensively.

SUMMARY OF THE INVENTION

According to the invention, a traffic control system is provided for establishing a plurality of traffic flow conditions. The system includes means for initially establishing a first traffic flow condition, means associated with each traffic flow condition for selecting that traffic flow condition, means associated with each traffic flow condition for maintaining that condition for at least a predetermined minimum time interval, and means responsive to the termination of said time interval for selecting the next traffic flow condition.

One feature of the invention is the capability of using actuated detectors and/or pedestrian signals associated with each phase that register in a memory circuit the actuation of that phase detector. Logic means may be provided to retain the system in a called phase when vehicles and or pedestrians continue to be detected in that phase up to a maximum predetermined time interval. After this interval the controller moves to the next traffic flow condition. Another feature of the invention is the capability of the controller to stay in a previously called phase for an indefinite interval when no other phase is called. This indefinite interval terminates when another phase does call. Further features of the invention that may be provided are recall means associated with each phase for returning to that phase when no other phase is calling, and pedestrian actuation means associated with each phase including storage means that provides for automatic pedestrian operation.

BRIEF DESCRIPTION OF THE DRAWINGS

Numerous other objects, advantages and features of the invention will be apparent upon a reading of the following detailed specification in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of a preferred embodiment of a traffic system of the invention;

FIG. 2 is a circuit diagram of a preferred vehicle counter;

FIG. 3 is a circuit diagram of a vehicle memory and interval gate unit for one phase of the system;

FIG. 4 is a circuit diagram of a vehicle indicator panel associated with the traffic controller;

FIG. 5 is a circuit diagram of a vehicle timing unit for the traffic control system;

FIG. 6 is a circuit diagram of a pedestrian counter and timing unit for the traffic control system;

FIG. 7 is a circuit diagram of a pedestrian memory and gate unit for the system; and

FIG. 8 is a circuit diagram of a pedestrian indicator panel.

DETAILED DESCRIPTION

General

FIG. 1 is a block diagram illustrating a three phase traffic control system constructed according to the invention, including a pedestrian section P and vehicle section V. The three phases of each section are considered as phases A, B, and C and may be respectively associated with two cross streets and a main street of heavier traffic flow. For example, in vehicle section V each phase has an associated vehicle detector and is partitioned into discrete vehicle timing intervals which may be designated as the INITIAL, (INIT.), VEHICLE EXTENSION (VEH. EXT.), YELLOW (YEL.) and ALL RED (RED) intervals. Each phase includes these intervals and the controller is adapted to sequence through each interval under control of the vehicle counter 24. A MAXIMUM (MAX) time interval is also associated with each phase and is adapted to extend the VEH EXT interval under certain circumstances, discussed in more detail hereinafter.

The pedestrian section P of the controller includes pedestrian actuators 21A, 21B, and 21C associated with respective phases A, B and C. Time intervals are also defined for the pedestrian operation. These intervals are WALK, WALK CLEAR and DONT WALK.

Signal light unit 31 controls conventional red, yellow and green signal lights for each phase. On a per phase basis, the signal lights are green during the INITIAL and VEHICLE EXTENSION intervals, yellow during the YELLOW interval and red during the ALL RED interval. Typical time interval ranges for the different intervals are shown in Table I below including those for pedestrian intervals.

TABLE I

Interval	Range
INITIAL	2 - 30 seconds
VEHICLE EXTENSION	2 - 30 seconds
YELLOW	1 - 12 seconds
ALL RED	0 - 12 seconds
MAXIMUM	10 - 120 seconds
WALK	2 - 30 seconds
WALK CLEAR	2 - 30 seconds

The vehicle and pedestrian intervals for any one phase along with associated signals are shown below in Table II.

TABLE II

Vehicle Interval	Signals	Pedestrian Interval	
		Signals	Signals
INITIAL	Green	Walk	Walk
VEHICLE EXTENSION	Green	Walk Clear	Walk Clear
VEHICLE EXTENSION	Green	Dont Walk	Dont Walk
YELLOW	Yellow	Dont Walk	Dont Walk
ALL RED	Red	Dont Walk	Dont Walk

All other phases will show "Red" and "Dont Walk" during the sequence listed above for the selected phase.

On a per phase basis the vehicle and pedestrian signals associated with that phase are positioned at an intersection so that vehicles and pedestrians associated with the phase travel in the same direction. For example, if phase C refers to a main traffic street, the associated phase C pedestrian section operates to allow pedestrians to walk with the traffic of phase C, and not across the main street. Thus, the pedestrian push button can be thought of as a second call detector associated with its phase.

The sequence shown in Table II may vary somewhat as to the concurrence of the INIT. and VEH EXT intervals with the WALK and WALK CLEAR intervals. The concurrence of these intervals with each other depends somewhat on the timing settings of the intervals. The INIT and WALK begin simultaneously, but may be of different time duration. Thus the INIT may be completed before the WALK times out. In this event, some of the WALK period takes place during the VEH EXT period. Other timing value arrangements may cause slightly different combinations of intervals. It is expected that the operator will set the various timing controls to provide for reasonable relationships, however, the system is designed so that neither the WALK or WALK CLEAR can extend into the YEL interval.

The traffic controller may also be provided with recall means associated with either vehicle or pedestrian operation, or both. Each vehicle phase has a recall switch which when set reverts the controller to that phase for the INIT Green plus one VEH EXT interval. If vehicles are actuating the detector on that phase the traffic extends the period to its maximum preset interval. Similarly, a recall switch may be included for each pedestrian phase. Operation of this recall switch causes a call to be registered with its associated phase so that the system reverts to that phase.

Referring again to FIG. 1, vehicle section V includes three vehicle actuated detectors 20A, 20B and 20C, one associated with each phase. These detectors are shown schematically as switches that close completing a path to ground when a vehicle is sensed. These detectors connect also to their corresponding memory and interval gate units 10A, 10B and 10C. The vehicle detectors may be of conventional design. An imbedded inductive loop detector could be used or, in the alternative, a mechanical detector.

The pedestrian section P includes three pedestrian push bottoms 21A, 21B and 21C, one associated with each pedestrian phase. When the pedestrian push but-

ton is actuated it connects one side of the push button switch to ground. The buttons 21A, 21B and 21C also connect to their corresponding memory and gate units 11A, 11B and 11C, respectively. The push buttons may be of conventional design.

The general organization of vehicle section V of the traffic system, as indicated in FIG. 1 also includes indicator panel 14 with interval timing resistors, interval and maximum timing unit 22 and counter 24. Similarly, pedestrian section P includes indicator panel 15, and counter and timing unit 23. A D.C. power source 26 is provided to supply power to the circuitry of the traffic system. Relay driver 27, relay matrix 29 and signal light unit 31 may make up the remainder of the traffic controller and may all be of conventional design.

The block diagram of FIG. 1 is somewhat simplified in that it does not show all the possible interconnections so as to simplify the design and not obscure the invention. These connections not specifically shown in FIG. 1 are discussed in detail with reference to the circuit diagrams shown in the remaining figures.

Detector calls are stored in the memory portion of their respective memory and gate units 10A, 10B and 10C. These units are shown in detail in FIG. 3. The interval gates of each unit 10 decode the outputs of counter 24 to establish which phase is in operation and which time interval is in control. The Not Call Bus line 9 connects from the memory circuits, to the Interval Gates of each phase. This output is combined with the counter outputs to enable the operation of the MAX output of the phase. The outputs of the Interval Gates are applied to the timing resistors of front panel 14 as well as to the input of relay driver unit 27. Indicator panel 14 is shown in detail in FIG. 4.

The timing resistors of indicator panel 14 connect to timing unit 22 which is shown in more detail in FIG. 5. The completion of a timing interval provides a negative pulse from the output of unit 22 (count pulse) which triggers counter 24 into its next position. This changes the counter-stage outputs, which are then decoded by the Interval Gates of units 10A, 10B and 10C to provide the next interval. Counter 24 is also operated directly from phase to phase (skipping all intervening intervals) by means of a signal developed at the proper time on phase select line 8 by a combination of the phase INIT output and the absence of a call of that phase. For example, after completing phase A RED, counter 24 goes into a phase B INIT interval. If there is no call for phase B, a voltage on phase select line 8 drives counter 24 into the phase C INIT position. The dwell time in phase B is so short that there is no time for the signal lamps to respond so that, to the observer, the timer has not been in phase B at all.

The negative "count" pulses from the timing unit 22 in addition to pulsing counter 24 operate mono-stable multivibrators associated with unit 22. The interval and maximum termination indicators (DS19 and DS20 of FIG. 4) on indicator panel 14 are driven from these mono-stable multivibrators and light briefly as their associated multivibrators operate indicating the occurrence of a count pulse.

The relay driver 27 is controlled by outputs from the interval gates and includes amplifiers which operate relay matrix unit 29, to produce the proper signal light outputs and sequence for signal light unit 31.

The power supply 26 converts the 120V A.C. line voltage into ± 30 , $+24V$, $\pm 18V$ and $-6V$ D.C. voltages.

In the pedestrian section P of FIG. 1 pedestrian calls from buttons 21A, 21B and 21C are stored in their associated memory circuits of units 11A, 11B and 11C. These units, in turn initiate a call to the vehicular memory circuits along lines 23A, 23B, and 23C, respectively. The output from each of the memory and gate units 11 enables the WALK interval during the proper time for the correct phase.

The interval gates of each unit 11 decode the outputs from the counter part of counter and timing unit 23. These outputs are logically combined with the phase INIT or VEH EXT and the combined output is used to drive relay matrix 29 and is also fed to the timing resistors of front panel 15 in a manner similar to the operation of the vehicle section V.

The outputs from the timing resistors of front panel 15 are applied to the counter and timing unit 23. Thus, unit 23 develops a negative pulse at the completion of a timing interval which steps the pedestrian counter into the next position, in a similar manner to the operation of the vehicle counter.

VEHICLE SECTION

The heart of the vehicle section of the controller is the five-stage counter 24 shown in FIG. 2 in detail. The basic structure of counter 24 is of conventional design and comprises transistor pairs including transistors 30, 32; 34, 36; 38, 40; 42, 44; and 46, 48. The first transistor pair 30, 32 is the first stage of the counter and is the one that receives the count pulse on input line 50. Each stage of the counter includes associated input coupling capacitors 31A, 31B; 33A, 33B; 37A, 37B; 41A, 41B; 45A, 45B, input pulse-directing diodes D1 to D10 and associated typical biasing resistors. There are essentially three inputs to counter 24, one on count pulse line 50, one on phase select line 8 and one from initial reset circuit 54.

The first two stages including transistors 30, 32, 34, and 36 delineate the intervals of all phases namely INIT, VEH EXT, YEL and RED, while the next three stages including transistors 38, 40, 42, 44, 46 and 48 delineate each phase. For a three or four phase system the last stage is unnecessary. Each stage has two outputs—a true output, denoted as FF and false output noted as \overline{FF} . When FF is logical ZERO, \overline{FF} is logical ONE, and vice versa. For example, when transistor 32 is conducting FF1 is logical ZERO. The next negative count pulse received on line 50 is applied to the junction of capacitors 31A and 31B and drives transistor 32 out of conduction. This action drives transistor 30 into conduction through cross coupling resistor R33. When transistor 30 conducts its collector voltage is low and thus $\overline{FF1}$ is logical ZERO, while FF1 assumes the logical ONE stage. The next count pulse on line 50 drives transistor 30 off and FF1 reverts to the logical ZERO state. This negative going transition of the FF1 output is coupled to the junction of capacitors 33A and 33B and causes the second stage (transistors 34 and 36) of counter 24 to change its conduction pattern.

The third stage of counter 24 including transistors 38 and 40 is actuated when transistor 36 goes from a non-conductive to a conducting condition. It may also be affected by a negative pulse coupled into it from unijunc-

tion transistor 64. Assuming transistor 36 is in conduction and that a positive pulse is applied to phase select line 8, capacitor 51 charges until it reaches the breakdown value of uni-junction transistor 64. The resulting negative going pulse passing through capacitors 37A, 37B drives transistors 38 and 40 into their opposite states. In one embodiment capacitor 51 may be connected to ground instead of to the collector of transistor 36. With such an arrangement a change to conduction of transistor 36 cannot affect the state of transistors 38 and 40 which thus can only be pulsed by the action of transistor 64.

Initial reset circuit 54 sets the initial position of counter 24 when power is turned on. When the power switch (not shown) is thrown on, transistor 55 is driven into conduction from the $+24$ volt source through diode 60, capacitor 59, and resistor 58. This causes the bases of transistors 30, 34, 38, 42 and 46 to be driven out of conduction by means of respective diodes 31, 35, 39, 43 and 47 through transistor 55 and diodes 56 to the -6 volt supply. The traffic controller is thus started in the phase A INIT interval. After a short time capacitor 59 charges and transistor 55 is no longer driven into conduction but is cut off through resistor 57 to the -6 volt supply. Counter 24 is then free to respond to the count and phase select pulses on lines 50 and 8, respectively.

A circuit used to limit the counter to three phase operation is also shown in FIG. 2. This circuit includes diodes 71, 73 and 75 and resistor 77. A phase select pulse is produced on line 8 when counter 24 tries to assume a fourth phase position. For that condition FF3 and FF4 are temporarily high and a positive pulse is applied from the $+24$ volt supply through resistor 77 and diode 75 to phase select line 8. This circuit thus causes the traffic system to essentially skip from phase C to phase A.

The outputs of each counter stage are utilized in various AND circuits associated with each phase for providing phase interval outputs. These AND gates are shown in detail in FIG. 3 for one phase. These counter outputs are also used in other parts of the system including pedestrian section P.

Referring now to FIG. 3 there is shown the memory and interval gate unit 10 for one of the three phases. Identical circuits may be used for the other two phases. The decoding for each phase is provided by decode AND gate 90 which includes diodes D6 and D7 and transistor Q5. In FIG. 3 the cathodes of diode D6 and D7 are illustratively shown connected to the $\overline{FF3}$ and $\overline{FF4}$ outputs of counter 24, thus decoding phase A. The anodes of diodes D6 and D7 couple to the base of emitter follower transistor Q5. Transistor Q5 conducts and provides an output at its emitter if the cathodes of diodes D6 and D7 are both logical ONE'S. The third and fourth stages of counter 24 (FF3, $\overline{FF3}$; FF4, $\overline{FF4}$ outputs) are connected to diodes D6 and D7 in a different decode pattern for each phase to provide an output from transistor Q5. Diode D8 may be used when more phases are needed, in which case it would connect to either FF5 or $\overline{FF5}$. Table III shows the counter outputs for three phase operation.

TABLE III

PHASE	FF3	FF4
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	7	8
A	0	0
B	1	0
C	0	1

The output of AND gate 90 which is taken at the emitter of transistor Q5 enables AND gates 91 through 95 by providing a positive voltage at the collectors of emitter follower transistors Q6, Q7, Q8, Q9 and Q10. There will be an output from AND gate 91 (transistor Q6), for example, when there is an output from transistor Q5 and FF1 and FF2 are both logical ONE. Transistor Q6 is thus in conduction and the phase INIT output of gate 91 is high for the selected phase. The outputs from each of the interval emitter follower gates is summarized in Table IV.

TABLE IV

INTERVAL	FF1	FF2
Initial	0	0
Vehicle Extension	1	0
Yellow	0	1
All Red	1	1

AND gate 95 which includes emitter follower transistor Q10 provides an output during the VEH EXT interval (FF1 and FF2 both high) of the selected phase when a call has been registered in another phase. In FIG. 3 transistor Q11 has its base coupled to Not Call Bus line 9. When a call is registered from another phase, line 9 goes to a ZERO, turning off transistor Q11 and thereby allowing transistor Q10 to conduct and provide a phase MAX output at the output of AND gate 95 (emitter of transistor Q10).

FIG. 3 also shows the memory circuits for one phase of operation. The memory circuits include two bistable multi-vibrators 96 and 97 respectively including transistors Q3 and Q4, and transistors Q1 and Q2. Multivibrator 96 may be referred to as the detector (DET) flip-flop as it is responsive to its associated vehicle detector, and is set (transistor Q4 conducting) when detector terminal 98 is grounded by vehicle detector switch 20. When this is done a negative potential is applied by way of diode D12 to turn transistor Q3 off, thus setting DET flip-flop 96. During that phase VEH EXT interval, a positive voltage is applied to the base of transistor Q3 by way of diode D16 and resistor R6 thereby turning transistor Q3 on (resetting flip-flop 96). Thus, the DET flip-flop is left in a reset state when no vehicles are detected and the controller proceeds to the next phase. This indicates that no call is registered in its phase.

During the phase Vehicle Extension interval an operation of the vehicle detector overcomes the positive voltage applied to the base of transistor Q3 by way of diode D16, thus causing it to be non-conducting during the duration of vehicle detections, but to return to its conducting condition immediately thereafter. DET flip-flop 96 is set also by way of diode D9 during the phase YEL interval provided a Maximum recall pulse has occurred on terminal 109 via diode D13. The Maximum recall signal is generated from the maximum multivibrator 112 of FIG. 5 and is discussed in more detail later.

DET flip-flop 96 is also set from its associated recall switch (SW1, SW2 or SW3 shown in FIG. 4) located on indicator panel 14 and shown schematically in FIG. 3. One output of the DET flip-flop is used via diode D18 during the VEH EXT interval applied through R23 to vehicle cancel terminal 88 to affect the timing circuits shown in FIG. 5. In essence this vehicle cancel output prevents the timing circuitry from generating a count pulse when vehicles are still being detected in that phase (except after the maximum interval has elapsed).

The multivibrator 97 which may be referred to as CALL flip-flop 97 includes transistors Q1 and Q2. Flip-flop 97 is set as a result of the setting of DET flip-flop 96 and any extension other than its own extension. Thus, when we are in VEH EXT interval FF1 and FF2 are high and diodes D19 and D20 are back-biased. If a vehicle has been detected DET flip-flop 96 is set and diode D10 is also back-biased. As long as we are not in the same phase VEH EXT interval transistor Q12 is off and the forward current through resistors R3 and R20 and diodes D21 and D22 renders transistor Q2 conductive. This indicates a phase call. For this condition CALL flip-flop 97 has a high "phase Call" output at the collector of transistor Q1. The other low outputs are from the "phase not call" and through diode D2 to the Not Call Bus line 9. CALL flip-flop 97 is reset during its own phase Vehicle Extension, by way of diode D15, and is held reset during the phase YEL by way of diode D14. Flip-flop 97 is set during turn-on, through diode D1 from the Turn on Bus line 101. FIG. 5 shows the Turn on Bus circuit 99 which connects between the manual control button 102 and the Turn on Bus.

The outputs from the AND gates 91 through 95 shown in FIG. 3, are applied to the timing potentiometers on indicator panel 14 shown in FIG. 4. The respective phase INIT outputs, for example, are applied to potentiometers R10, R11 and R12. The timing potentiometers are adjustable and can be set for different time ranges. If the A INIT output goes high it is applied through the interval timing potentiometer R10 and diode D10 to the interval timing charge terminal 80. The A Max, B Max, C Max outputs are circuited through the maximum timing potentiometers R13, R14, and R15 to the maximum timing charge terminal 82. In addition, if the zero time switches S10, S11 and S12 associated with the potentiometers R1, R2 and R3 respectively are closed, the voltage applied to the RED intervals will, be connected from terminal 84 to STEP input of the timing circuit of FIG. 5. These terminals 80, 82 and 84 are connected to similarly labelled circuits points on the timing circuit of FIG. 5.

Referring now to FIG. 5 there is shown an embodiment of the timing circuitry of the invention. The purpose of the circuitry is to supply negative pulses which will pulse counter 24. This pulse is labelled the "count pulse" and is generated at the anode of either diode D8 or diode D12. Both of these anodes connect to line 50 of counter 24. The turn on bus circuit 99 of FIG. 5 which includes transistors Q5 and Q6 also generates a count pulse under manual control.

The pulse generating circuit includes uni-junction transistors Q11 and Q12. Both of these transistors have typical base and emitter electrode, as shown. When the voltage between the emitter E and base B1 is low the resistance between E and B1 approaches an open cir-

cuit value. When the E-B1 voltage difference increases to a specific proportion of the B1-B2 voltage difference, the E-B1 resistance becomes quite low. This low value of resistance remains until the E-B1 voltage value approaches zero, whereupon the E-B1 resistance resumes its open circuit value.

The timing circuit operation of FIG. 5 may now be traced. Assuming that counter 24 is in the position to provide an A INIT output; this output will be impressed on the A INIT timing potentiometer R10 of FIG. 4 and thence by way of terminal 80 to the interval timing charge circuit including capacitor C8 and diode D15 of FIG. 5. Capacitor C8 charges until it reaches the discharge or breakdown value of transistor Q11. At that time, capacitor C8 discharges through diode D15, transistors Q11, Q9 and resistor R24. Thus, a negative pulse is fed through diode D8 to input line 50 of counter 24.

In a similar way, a negative pulse may be generated when a step current is received on terminal 84. This causes the discharge of capacitor C9 through diode D16 to transistors Q11, Q9 and resistor R24. Since the value of capacitor C9 is small in comparison to the capacitance value of capacitor C8, it takes a very short time to charge it to the breakdown value of transistor Q11, thus providing a shortened step interval.

In FIG. 5 transistor Q10 is connected with its collector and emitter across capacitor C8 to discharge it without causing a negative pulse by way of diode D8 since the discharge path is not through resistor R24. Transistor Q10 is normally cut off by means of resistor R21 which connect to the -6 volt supply. A positive voltage either from the stop time terminal 86 through diode D13 or from the vehicle cancel terminal 86 through diode D13 or from the vehicle cancel terminal 88 turns transistor Q10 on. The vehicle cancel voltage on terminal 88 is obtained from any one of the phase CALL flip-flops 97 during the phase VEH EXT period. The positive input on terminal 86 may be from a manually operated switch 86A as shown.

Transistor Q10 in FIG. 5 is also driven into conduction via diode D2 or diode D4, which are associated with the termination multivibrators 110 and 112 respectively. As indicated in FIG. 5 mono-stable multivibrator 110 includes transistors Q1 and Q2 and typical cross-coupling capacitor C1. Similarly, mono-stable multivibrator 112 includes transistors Q3 and Q4 and typical cross-coupling capacitor C2. Both of these multivibrators may be of conventional design, and in FIG. 5 are constructed to have the same "ON" time.

The maximum timing circuitry associated with transistors Q12 and Q13 operates in a similar manner to the interval timing circuitry associated with transistor Q11. The maximum interval is determined by the value of capacitor C10 and the maximum timing potentiometers on panel 14, namely resistors R13, R14 or R15. Capacitor C10 is charged from the MAX timing circuits of the front panel through resistor R34. The negative count pulse appears at diode D12 when transistor 12 conducts and capacitor C10 discharges through diode D19, transistors Q12, Q9 and resistor R31.

Transistor Q13 is connected with its collector and emitter across capacitor C10 to discharge it. Transistor Q13 is normally cut off but is driven into conduction

from terminal 86 via diode D17; and also through diode D20 in all YEL intervals or when FF1 and FF2 are both high.

It is noted that neither transistor Q12 nor Q11 can provide a discharge path unless transistor Q9, the permit termination transistor, is turned on.

Referring still to FIG. 5, during all VEH EXT intervals FF1 and FF2 have logical ONE values, diodes D10 and D11 are backbiased, and transistor Q7 is driven into conduction by the +24 source through resistor R19. With transistor Q7 on, its collector is low. Thus, transistor Q9, is cut off through resistor R23 from the -6 volt supply. However, when the permit termination terminal 106 is positive transistor Q8 conducts, preventing transistor Q7 from conducting; hence transistor Q9 is driven on from the +24 volt source through resistors R18 and R22.

Transistor Q9 conducts in every counter interval position therefore, except the Vehicle Extension positions. Further, transistor Q9 conducts regardless of the interval position when a permit termination voltage is received on terminal 106. The permit termination voltage is obtained from the gate circuits of FIG. 3 when the MAX Interval is in effect and the coordination circuit is in its enable state.

The coordination circuit shown in FIG. 3 is optional but may be included to permit synchronous or offset timing among a group of controllers. With the use of this circuit the controller is adapted to remain in the VEH EXT interval even if the maximum timing has expired, thereby indicating it should move to the next interval, until the coordination circuit is in its enable condition. Various types of coordination are possible based on the voltage to be used. For ground coordination, for example, transistor Q13 is normally conducting, holding the anode of diode D34 at ground. A ground pulse applied to the phase coordination terminal 108 permits transistor Q13 to be cut off by way of resistor R26 to the -6 volt supply, and as a result, a drive voltage is available to the permit termination terminal 106 through diode D34. This drive voltage then allows conduction of transistor Q9, FIG. 5, and the generation of a count pulse.

As previously mentioned, the termination multivibrators 110 and 112 of FIG. 5 are mono-stable multivibrators. Transistor Q2 of multivibrator 110 is normally in conduction by resistor R3 to the +24 volt source. When transistor Q11 conducts, as described before, a negative pulse appears across resistor R24, and is transmitted through diodes D7 and D1 to turn off transistor Q2. The positive voltage that appears at the collector of transistor Q2 is applied through diode D2 and resistor R28 to transistor Q10. This action completes the discharge of capacitor C8 so that the next timing interval will begin with capacitor C8 completely discharged. At the same time that transistor Q2 is cut off, transistor Q1 is driven into conduction through resistor R9. This causes the interval termination indicator DS19 of the front panel (FIG. 4) to light for a predetermined interval. A short time after completion of the negative pulse obtained from resistor R24, the voltage across transistor R3 reasserts itself after capacitor C1 is charged through resistor R3, thereby driving transistor Q2 into conduction. Thus, each termination of the interval timer causes a momen-

tary operation of the interval termination indicator DS19 and causes a total discharge of the interval charging capacitor C8.

Maximum termination multivibrator 122 which includes transistor Q3 and Q4 acts in similar manner to multivibrator 110. Transistor Q3 which is normally on is cut off by the negative pulse developed across resistor R31. The resulting pulse at the collector of transistor Q3 drives transistor Q13 into conduction through diodes D4 and D17 and resistor R32. Transistor Q10 is turned on at the same time by way of resistor R28 thereby discharging capacitor C8. Thus, each maximum timer termination reduces the charge on the interval timing capacitor C8 to zero and the maximum termination indicator DS20 of FIG. 4 lights briefly.

In FIG. 5 the positive pulse at the collector of transistor Q3 provides a Maximum Recall Signal on terminal 109. This voltage is applied to the cathode of diode D13 of each timing circuit one of which is shown in FIG. 3. If this occurs during the phase YEL interval a positive voltage sets transistor Q4 of flip-flop 96 through diode D9. In the operation of the controller, the maximum timer count pulse causes counter 24 to go into the YEL interval. At the same time, multivibrator 112 has a maximum recall output which goes positive and remains positive for a short time after the inception of yellow. This combination of phase Yellow and Maximum Recall drives DET flip-flop 96 into the set position thereby denoting a recall to that phase at a later time.

The initial setting of the traffic controller may be provided by Turn on Bus circuit 99 shown in FIG. 5. The sequence may also be controlled by the manual control button 102, which is adapted to generate one count pulse per button depression and to also bring bus line 101 to ground when button 102 is depressed. When the button is pushed a positive voltage is supplied from the +24 volt supply to one side of resistor R12 and also through resistor R7 to the base of transistor Q6. This positive voltage turns on transistor Q6 and pulls the Turn-On Bus line 101 to ground thereby initially setting all CALL flip-flops 97, one of which is shown in FIG. 3, to indicate a call of all phases. This positive voltage from button 102 also charges capacitor C6 at a certain rate determined in part by the value of capacitor C6 and resistor R13. The final voltage to which capacitor C6 is charged depends on the voltage divider of resistors R11 and R13. This voltage is normally insufficient to trigger unijunction transistor Q5 in FIG. 5. When the manual control button 102 is released the voltage at the base electrode of transistor Q5 is reduced to approximately zero volts. Capacitor C6 then discharges through transistor Q5 and a negative pulse is fed to input line 50 of counter 24, FIG. 2.

Circuit 99 is particularly designed to eliminate switch bounce problems and to assure that only one count pulse is produced for each button 102, release. This operation is provided by transistor Q5 and capacitor C6 primarily. With the arrangement shown if the button is pushed a pulse can only be generated after capacitor C6 is charged. Once the first pulse occurs thus, another one is prevented from occurring until capacitor C6 charges again.

VEHICLE OPERATION

In the operation of the traffic controller of this invention, it may be understood that at power turn-on transistor Q6, FIG. 5 has been turned on momentarily while capacitor C5 is initially charged and causes the bus line 101 to go to ground, thereby setting all phase CALL flip-flops 97. This forces a call condition for all phases. The controller then steps through each interval of each phase resetting the CALL flip-flop 97 of each phase until the phase C-Vehicle Extension interval is reached. Up until this time it is assumed that no vehicles have been detected by the three detectors 20A, 20B and 20C.

Therefore, the Not Call Bus line 9 is a ONE and we cannot permit any termination as transistor Q11 in FIG. 3 is ON, holding transistor Q10 off and not permitting an output from permit termination terminal 106. If while the controller is in the phase C Vehicle Extension interval a vehicle detection is received in phase C, that DET flip-flop 96 sets but that CALL flip-flop 97 cannot as transistor Q12 (FIG. 3) is conducting by way of the positive applied through diode D17. In effect, no call is received from the phase that the controller is in and thus it cannot be removed from phase C Vehicle Extension until either phase A or phase B calls or, in other words, a vehicle is detected in those phases.

Therefore, it may be assumed that a vehicle call is received from phase B. This would occur when its detector flip-flop 96 gets set and, as we are in a VEH EXT interval, the CALL flip-flop 97 is also set. This action immediately reverts line 9 to a ZERO and permits an output from permit termination terminal 106 shown in FIG. 3. This output is coupled to the timing circuits shown in FIG. 5, turning on transistors Q8 and Q9 and allowing a count pulse which steps the controller into the next interval or the YEL interval of phase C. The controller then automatically sequences through the C YEL interval and the C ALL RED interval. When the counter tends to assume a fictitious phase D interval the circuit of FIG. 2 including diodes 71, 73 and 75 prevents this by immediately generating a phase select pulse on line 8 which reverts counter 24 to the phase A INIT interval.

Until now the Not Call Bus line 9 is still at a ZERO level because the phase B call still exists. However, as there is no call from phase A that phase "not call" signal taken at the negation output of its associated flip-flop 97 is high. A phase select signal is, thus generated on phase select line 8 in FIG. 3 because diode D5 is back-biased and diode D4 forward biased. This moves the controller to the phase B INIT interval position. At that point there is a phase call on phase B so no further phase select pulses are generated on line 8 of FIG. 3. The next count pulse would jump the controller to the phase B VEH EXT interval. If, at that time no vehicles are detected the phase B DET and CALL flip-flop 96 and 97 respectively, are reset. A termination pulse on terminal 106 is not generated, now is a count pulse, so the controller stays in the phase B VEH EXT interval until a further call is received.

If recall switches are used associated with each phase, that phase is continuously recalled. For example, if phase C is the heavy traffic phase it may be desirable to recall to this phase by opening the recall

switch associated therewith. This sets DET flip-flop 96 and calls that phase. These recall switches are shown in FIG. 4 as switches SW1, SW2 and SW3.

It may alternatively be assumed that when the traffic controller steps into the phase B VEH EXT interval that vehicles are still being detected by the phase B vehicle detector 20B. The DET flip-flop 96 associated with phase B would therefore be set. The CALL flip-flop 97 also associated with that phase would not set, however, as the controller is still in its own phase VEH EXT interval. However, the setting of DET flip-flop 96 during the same phase vehicle extension interval generates a vehicle cancel signal at terminal 88 which is coupled to the timing circuitry shown in FIG. 5 thereby inhibiting any count pulses. This inhibit is provided by keeping transistor Q10 on as long as Vehicle Cancel is high.

If a call is received from phase C, for example, and vehicles are still being detected in phase B, the maximum timing circuitry including transistors Q12, Q13 of FIG. 5 goes into operation. The Call from phase C generates a permit termination signal on terminal 106 from the circuitry of FIG. 3. However, a count pulse is not generated by way of diode D8, FIG. 5 as the vehicle cancel input drives transistor Q10 into conduction for each vehicle and capacitor C8 is discharged. It is possible to generate a count pulse, however, from the maximum timing circuitry of FIG. 5. The maximum timer period, determined in part by the values of resistors R13, R14 and R15 on panel 15 eventually times out and generates a count pulse and also a Maximum Recall signal at terminal 109 from the maximum termination multivibrator 112. The count pulse jumps the controller out of the phase B VEH EXT to the phase B YEL interval.

The controller eventually reaches the phase C INIT interval and as phase C has generated a call, the controller at least temporarily stays in phase C.

PEDESTRIAN SECTION

Referring now to FIGS. 1, 6, 7 and 8 there is shown the pedestrian section P of the traffic control system. Pedestrian section P includes memory and gate units 11A, 11B and 11C for each phase, counter and timing unit 23, and indicator panel 15.

The pedestrian counter 120 shown in FIG. 6, unlike the vehicle counter, is only a single stage counter including transistors Q2 and Q4. It has two outputs $\overline{\text{FFP}}$ and FFP taken respectively, at the collectors of transistors Q2 and Q4. These outputs are clamped to not more than +17 volts by means of diodes D2 and D1. In the normal operation of the timer, the counter should be in the $\overline{\text{FFP}}=0$ position when the vehicle timer section is in Yellow. This logically indicates the absence of pedestrians on phase A, for example, when the controller is leaving its phase A VEH EXT interval. This is provided by AND circuit 121 comprising resistors R8 and diode D15 whose cathode is connected to the FF2 output of the vehicle counter 24. The FF2 output is high during all Yellow and Red intervals. This FF2 connection from the vehicle section synchronizes operation of the pedestrian operation with the vehicle operation by forcing the counter 120 to a "no pedestrian condition" when FF2 goes high. The output of AND circuit 121 is coupled through diode D14 to one side of

capacitor C8, the pedestrian step timing capacitor, and through diode D7 to the emitter of transistor Q6, the timing unijunction transistor. Thus, if the timer of FIG. 6 reaches any yellow position and, if the FFP output is high, a pulse is developed via diode D12 to drive transistors Q2 and Q4 into the $\overline{\text{FFP}}=0$ position. If FFP already is ZERO no pulse is generated. This action guarantees that the pedestrian counter 120 provides an output $\overline{\text{FFP}}=1$ when the vehicle section of the timer goes into any phase INIT position.

Referring now to FIG. 7, there is shown memory and gate circuitry for one pedestrian phase. Each of the pedestrian phases includes AND gates 122 and 124 having respective emitter follower transistors Q4 and Q7. Transistor Q4 may be referred to as the WALK emitter follower and transistor Q7 as the PED CLEAR or WALK CLEAR emitter follower.

Transistor Q4 of FIG. 7 provides an output (emitter goes high) when the following conditions concurrently occur, namely, $\overline{\text{FFP}}=1$ through diode D10; a pedestrian call has been registered in MEM flip-flop 126 and the auxiliary (AUX MEM) flip-flop 128 is set; and when the same phase is in the INIT or the VEH EXT interval through diodes D31 or D32 to transistors Q1, Q3 and diode D13.

This WALK output from the emitter of transistor Q4 is applied to transistor Q10 through diode D24 and resistor R25. It is also directly coupled to the WALK timing potentiometer such as R10 in FIG. 8 and to the WALK indicator DS1 associated with that phase shown on front panel 15. Transistor Q7 similarly provides an output to transistor Q10 when $\overline{\text{FFP}}=1$ (through diode D22) and when the same phase is in the INIT or VEH EXT interval, via diode D12 from transistors Q1 and Q3.

The PED CLEAR output from transistor Q7 is also applied to the ped clear relay driver transistor Q5 of FIG. 6 by way of diode D21 (Ped Clear Bus). The output is also applied to its own phase relay driver transistor Q10 through diode D25, to the timing potentiometer such as R13 in FIG. 8 and to the PED CLEAR indicator such as indicator DS2 on front panel 15.

There is a pedestrian memory circuit for each of the pedestrian phases namely phases A, B and C. The memory circuit has associated with it an auxiliary memory circuit. The memory circuit shown in FIG. 7 includes a MEM flip-flop 126 comprising transistors Q8 and Q9 and an AUX MEM flip-flop 128 comprising transistors Q2 and Q5. Flip-flop 126 is responsive to the pedestrian push button 21 which permits a negative pulse through diode D19 to turn off transistor Q8 thus setting flip-flop 126. During the associated phase WALK interval a positive pulse applied to the base of transistor Q8 through diode D27 and resistor R23, turns transistor Q8 on thereby resetting flip-flop 126. Transistor Q8 cannot then be set off again by pedestrian actions in that phase until the phase WALK interval is completed. Thus, the phase under consideration cannot register another pedestrian call until that phase WALK is over.

The auxiliary memory flip-flop 128 is set with transistor Q5 on and transistor Q2 off when a call has been registered from the pedestrian push button and the vehicle section of the controller is in any extension called "sum extension" except its own extension. Flip-

flop 128 is also set when a call has been registered from the pedestrian push button 21, the vehicle section is in the phase INIT or phase VEH EXT and the Not Call Bus line 9 (indicating there is no call on any other phase) is high.

In summary, flip-flop 128 is set providing there is a pedestrian call and the timer is in any extension except its own; or if it is in its own extension, then there must be no call from any other phase. The auxiliary memory flip-flop 128 is reset at the outset of phase PED CLEAR, or under some modes of operation by phase YEL.

A call to the pedestrian phase will result in a call to the same vehicle phase under the condition that the vehicle section of the timer is not in its own INIT or its own VEH EXT interval, and further that there is no call on that phase. Thus, if phase C is in operation and a pedestrian actuation occurs on phase B, the phase B vehicle section receives a call. This is assuming, of course, that no call by way of a vehicle detector has been registered in phase B.

In FIG. 7, the collector of transistor Q6 is connected to its corresponding phase vehicle detector input so that when transistor Q6 is on it grounds the detector input thereby representing the presence of a vehicle. Transistor Q6 is normally held off by the -6 volts applied through resistor R19. However, if the cathode of diode D2 is high (flip-flop 126 set), the cathode of diode D5 is high (transistor Q1 is off - not in phase INIT or phase EXT) and the cathode of diode D1 is also high (no call in that phase) then transistor Q6 will be driven on by the +24 volts through resistor R1, diode D6 and resistor R18. The conduction of transistor Q6 grounds the associated vehicle detector.

There is a constant call to the phase vehicle detector by way of transistor Q6 of FIG. 7 during phase WALK and phase PED CLEAR by way of diodes D28 and D23. When the anodes of either of these diodes goes positive transistor Q6 conducts. This will assure at least one vehicle interval (maximum setting permitting) after the PED CLEAR interval. If it is desired to eliminate the additional period, these diodes may be removed, in which case the vehicle timing is not strictly synchronized to the pedestrian timing. Under this circumstance, if the interval timings are inadvertently set so that the INIT, plus the VEH EXT intervals exceeds the WALK interval, the WALK indication will be terminated when the phase YEL appears since transistor Q2 is driven into conduction at that instant.

The pedestrian section P has the capability of cancelling the PED CLEAR interval if a pedestrian call is received by the associated phase during the PED CLEAR interval and there is no call from any other phase. In FIG. 7 resistor R16 is fed from transistor Q7 during the PED CLEAR interval and is gated through diode D11 to memory flip-flop 126, and through diode D4 to the not call bus line 9. If both flip-flop 126 is set (pedestrian call) and there are no calls from any other phases (vehicle or pedestrian), a voltage is applied to the ped step timing circuit by way of diode D20 to drive counter 120 into the WALK position (FFP=1). If this type of operation is not desired, then diode D20 should be removed.

Obviously, from the discussion of the pedestrian section, many different features may be adopted for use

with the vehicle section of the control system. The use of many of these features depends upon the particular traffic flow situation.

The timing circuits for the pedestrian section are similar to those used for the vehicle section. The timing relations depend upon the RC charging characteristics and the breakdown ability of the uni-junction transistors Q6 and Q12 shown in FIG. 6. Transistor Q6 is the pedestrian timing uni-junction, capacitor C7 the timing capacitor, capacitor C8 the step timing capacitor and resistor R20 the resistor across which the negative "count" pulse is developed. Diode D12 feeds the pulse to the counter, and diodes D16 and D11 feed the same negative pulse to the pedestrian mono-stable multivibrator 132 which includes transistors Q3 and Q7 of FIG. 6. Transistor Q8 is the discharge transistor for capacitor C7 and is normally held off by the -6 volts through resistor R24 but is driven on to discharge capacitor C7.

The pedestrian multivibrator 132 is a mono-stable (one shot) multivibrator, similar to those used in vehicle section V of the timer. Transistor Q7 is normally held on by means of resistor R12; being driven off momentarily by the negative pulse through diodes D16 and D11. The pedestrian interval termination indicator such as indicator DS2 in FIG. 8 lights momentarily as transistor Q3 turns on. A positive pulse is available at the collector of transistor Q7, which through diode D10 and resistor R25 drives transistor Q8 into conduction to discharge capacitor C7 in a similar manner to the discharge of capacitor C8 in FIG. 5.

Transistor Q1 of FIG. 6 provides an output for all Extension intervals. It is driven from the +24 volt supply through resistor R1 and is gated from counter outputs FF1 and FF2. This "sum of extensions" output is used as previously described.

The permit termination of the pedestrian circuitry is taken at the anode of diode D21. This is applied to terminal 106 (transistor Q8) of FIG. 5. Terminal 106 is shorted to ground when transistor Q10 of FIG. 6 is on, so that the WALK and PED CLEAR intervals are not superceded by the MAX interval. If this type of operation is not desired, diode D21 may be removed. Transistor Q10 is driven into conduction from the Walk Bus and from the Ped Clear Bus.

The manual control is designed to operate in conjunction with the vehicle manual control, however, if it is desired to obtain a Walk signal manually, then the Ped Recall switch should be operated for the phase in question, if the pedestrian has not operated the push-button. The pedestrian recall switches shown in FIGS. 7 and 8 operate similarly to the vehicle recall switches discussed previously.

The negative pulse to operate the pedestrian counter 120 of FIG. 6 is obtained at the junction of capacitor C6 and resistor R30 as a result of the breakdown of transistor Q12. The momentary contact manual control terminal 134 when switched to a positive voltage by a switch (not shown), for example, places a charge on capacitor C6 by means of the voltage divider of resistors R35 and R31. This charge can only appear when the controller is in the WALK or PED CLEAR position since transistor Q11 is on except during these two positions and resistor 33 is normally grounded by diode D22 and transistor Q10. During the PED CLEAR inter-

val, the Vehicle Manual is prevented from stepping the vehicle timer out of the extension period. Transistor Q9 provides this action. (output from Q9 is coupled to circuit 99, FIG. 5 to prevent count pulse). The result is that manual operation provides the following sequence for the phase involved.

PED Interval	WALK	WALK CLEAR	(Pedestrian Clear)
VEH Interval	INIT	EXT	EXT YEL RED
VEH Signals	Green	Green	Green Yellow Red
PED Signals	Walk	Dont Walk	Dont Dont
Walk	Walk	Walk	Dont

Having described certain features of the invention particularly with reference to only a single embodiment thereof, other modifications of, and departures from the invention should become readily apparent. For example, a number of logic gates have been shown as represented by diode-resistor logic; other arrangements could be used such as TTL logic. A binary counter using bipolar transistor has been shown; however, other semiconductor counters could be used such as one including field effect transistors or MOS transistors. In addition, the counter could contain virtually any number of stages depending on the number of intervals and phases needed. Also, the vehicle section can be operated without using a pedestrian section, if desired. For this operation, the connections from each pedestrian memory unit to be associated vehicle detector would be non-existent.

It is evident that those skilled in the art may now make numerous uses and modifications of the specific embodiments described herein without departing from the inventive concepts. Consequently, the invention is to be constructed as embracing each and every novel feature and novel combination of features present in or possessed by the apparatus and techniques herein disclosed and limited solely by the spirit and scope of the appended claims.

What is claimed is:

1. A multi-phase traffic control system for controlling the operation of traffic signal means associated with each phase comprising:

counter means having a first portion allocated to phase control, a second portion allocated to interval control within a phase, an input terminal for receiving an incrementing signal, and a select line for receiving a signal to change from one phase of operation to the next;

a plurality of circuit means one being associated with each phase and each including;

detecting means including means for registering a call,

decoding means coupled from the second portion of the counter means for demarcating each interval of its associated phase and defining a call sensing interval,

and means coupled from the decoding means and the registering means for generating the phase change signal in the absence of a registered call and when entering the call sensing interval,

and timing means including interval timing circuit means associated with each phase and means coupled to said counter means for generating an incrementing signal upon termination of the timed interval to thereby change at least the second portion of the counter means.

2. The system of claim 1 wherein said counter means includes a binary counter, said first portion includes two stages for allocating up to four phases, and said second portion includes two stages for allocating up to four intervals.

3. The system of claim 1 wherein said detecting means includes a vehicle actuable detector means for indicating the presence of a vehicle.

4. The system of claim 3 wherein said registering means includes a bistable detector means having one output indicative of the presence of a vehicle and a second output indicative of the absence of a vehicle.

5. The system of claim 4 wherein said registering means includes a bistable call means having an output for generating a phase call signal when the system is in another phase.

6. The system of claim 1 wherein said means for generating the phase change signal includes an AND circuit which is responsive to the presence of the call sensing interval and the absence of a registered call.

7. The system of claim 6 wherein said AND circuit includes a diode-resistor circuit.

8. The system of claim 1 wherein said phase change signal causes said counter means to change from the call sensing interval of one phase to the call sensing interval of the next phase skipping all intervening intervals.

9. The system of claim 1 wherein said timing means includes maximum timing circuitry enabling the system to remain in one phase up to a maximum predetermined time when a call has been received for another phase.

10. The system of claim 1 comprising a bus means coupling to an output of each registering means.

11. A multi-phase traffic control system for controlling the operation of traffic signal means associated with each phase comprising:

counter means having a first portion allocated to phase control, a second portion allocated to interval control within a phase, and an input terminal for receiving an incrementing signal;

a plurality of circuit means one being associated with each phase of operation;

each said circuit means including decoding means coupled from the second portion of the counter means for demarcating each interval of its associated phase, and detector means having means for registering a call;

timing means including interval timing circuit means associated with each phase, means coupled to the input terminal of the counter means capable of generating an incrementing signal upon termination of the timed interval, and means for enabling said means for generating;

bus means coupled to an output of each registering means and assuming a first state when no calls are registered on detector means for other phases and a second state when at least one call has been registered for detector means associated with another phase;

and means responsive to the second state of said bus means for permitting a termination of the occupied interval by activating the means for enabling.

12. The system of claim 11 comprising rectifier means coupled from said bus means to each registering means.

13. The system of claim 11 wherein said decoding means includes gate means defining a maximum interval, said timing means include a maximum timing circuit means, and said means for permitting a termination includes logic means which inhibits said enabling means during said maximum interval as long as said bus means is in its first state.

14. The system of claim 11 wherein said counter means includes a multi-stage binary counter, and said counter means has a select line for receiving a signal to change from one phase to the next phase.

15. The system of claim 14 wherein said decoding means includes gate means defining a call sensing interval and each said circuit means includes means coupled from the decoding means and the registering means for generating the phase change signal in the absence of a registered call for its associated phase and when entering the call sensing interval.

16. In a multi-phase traffic control system including a multi-stage counter means having a first portion allocated to phase control and a second portion allocated to interval control, a plurality of detector circuit means one being associated with each phase of operation, means for applying power to the system, and timing means capable of generating a signal coupled to said counter means for incrementing said counter means, the improvement comprising:

circuit means coupled to said means for applying and said counter means and responsive to said means for applying for setting said counter means to an initial count indicative of an initial interval of a phase.

17. The system of claim 16 wherein said circuit

means for setting comprises conductor means coupled to each stage of said counter means, a current-controlled semiconductor device and a charging means.

18. The system of claim 17 wherein said semiconductor device includes a transistor and said charging means includes a capacitor coupled to an input terminal of the transistor, said conductor means being coupled to an output terminal of said transistor, wherein when power is applied said capacitor charges, said transistor only initially conducts and a setting signal is transmitted via said conductor means to said counter means.

19. In a multi-phase traffic control system including a multi-stage counter means having an input terminal for receiving an incrementing signal, a plurality of detector circuit means one being associated with each phase, and timing means capable of generating the incrementing signal, the improvement comprising:

manually operable circuit means for generating an incrementing signal including switch means and means for generating said signal upon release of said switch means.

20. The system of claim 19 wherein said means for generating includes a transistor and a capacitor coupled to the control electrode of the transistor, wherein upon actuation of said switch means said capacitor charges to a voltage insufficient to cause conduction of said transistor but upon release of said switch means said capacitor discharges and generates said signal.

21. The system of claim 19 comprising turn on bus means coupled to said manually operable circuit means and each said detector circuit means for setting each said detector circuit means to a call condition when said manually operable circuit means is actuated.

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