A frequency conversion circuit includes four analog switching elements (46, 48, 52, 54) coupled. Each switching element is logic controlled to open or close, i.e., to have either a high or low conductivity to pass or block analog currents of either polarity. Effectively, a signal received on the dual input (40, 42) may be enabled in inverted or non-inverted form onto the dual output (60, 62), depending on the control of the switches. The circuit may be used for producing a telephone ringing signal from an AC input signal. The circuit is coupled to receive an AC input signal, such as a 60 Hz signal derived from AC line power. The switching elements are alternately opened and closed during a predetermined sequence of half-cycles of the AC input signal. The circuit produces an output signal having a sequence of consecutive positive half-cycles and a sequence of consecutive negative half-cycles. Each switching element preferably includes a MOSFET switch stage providing either high or low impedance between two switch electrodes, a current amplifier (76, 78) for providing a gate voltage to the MOSFET switch stage, and a storage circuit including a capacitor (102) for storing energy while the switching element is open.
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TELEPHONE RINGING SIGNAL GENERATOR

FIELD OF THE INVENTION:

The present invention generally relates to the field of telephone circuitry. More specifically, the invention relates to circuits for producing a telephone ringing signal at low cost and power consumption.

BACKGROUND OF THE INVENTION:

Many circuits for generating a telephone ringing signal have been implemented. Essentially, a telephone ringing signal is a periodic signal at around 20 Hz. The signal need not be precisely sinusoidal, but should have a strong 20 Hz component in its frequency spectrum.

Conventional AC powered telephone ringing signal generating circuits have had several drawbacks. First, these circuits have required considerable power dissipation, leading to large quantities of heat which must be dissipated. As a consequence, large surface areas for heat sinking have been required.

Many conventional circuits have included well-known rectifier-filter power supplies for producing DC power from an AC source. A large, bulky filter capacitor has been required. Such filter capacitors have rendered ineffective the winding resistance of the isolation power transformer for protecting against an inrush current resulting if the output terminals are short-circuited. These circuits have had the added drawback that a highly irregular current-waveform load has been supplied to an isolation power transformer. This current waveform has required heavy transformers for dissipating large quantities of power.

One conventional type of ringing signal generating circuit includes a signal oscillator and a linear amplifier. A conventional rectifier power supply includes an isolation transformer 2, a bridge rectifier
4, and a filter capacitor 6. This rectifier power supply provides power to the amplifier, and perhaps also to the oscillator. The oscillator is shown in block diagram form as 8.

The conventional amplifier circuit shown includes a differential amplifier comprising transistors 10 and 12 in an emitter-follower configuration. An NPN transistor 14 and a PNP transistor 16 are coupled emitter-to-emitter to produce an output node for the circuit. AC and DC feedback is provided from the output node through a resistor 18 to the base of the transistor 10. A voltage divider biases the base of the transistor 12 to a predetermined fraction of the DC supply voltage. A resistor 20 has a value which, in tandem with the resistor 18, biases the base of the transistor 10 to the same potential as that of the transistor 12 when the output node is midway between the power supply potentials. An integrating amplifier including a transistor 22 and a capacitor 24 provides current or voltage gain between the differential amplifier (the transistors 10 and 12) and the complementary output pair (the transistors 14 and 16).

This circuit has the advantages that a high quality sine wave output is produced, and the levels of generated electromagnetic interference are small. On the other hand, this circuit has several drawbacks. First, the transistors 14 and 16 operate in essentially a Class B linear mode. As a consequence, they dissipate significant heat. They must be large in order to avoid secondary breakdown, unless a low power supply voltage is used and a step-up isolation transformer is added at the output. Such a step-up transformer adds cost, weight, and size to the circuit. Second, linear amplifiers are susceptible to damage from rapid discharge of the filter capacitor if the output is short-circuited. Again, protective circuitry adds to the cost of the circuit.
Third, the transformer 2 is inefficiently utilized, since the load current in the secondary winding differs in waveform from the voltage across the primary. A choke-input filter added to overcome this problem adds to the bulk and cost of the circuit. Finally, the maximum undistorted output voltage swing varies with the AC line voltage. For maximum efficiency, the amplifier gain should be controlled to track the line voltage. Controlling circuitry adds to the cost of the circuit, but if it is omitted, power dissipation of the transistors 14 and 16 increases under high-line conditions. Either one of these situations is undesirable.

A second conventional type of ringing signal generating circuit is shown in FIG. 2. This circuit is called a DC chopper. It employs essentially the same power supply as that of FIG. 1. Similar components are numbered similarly. A controller 26 produces two control signals A and B, shown in a timing diagram in FIG. 3. The signal B has a relatively large duty cycle. When B is high, a bipolar transistor 28 is turned on, drawing current through a series of resistors 30, 32, and 34. A voltage at the junction between the resistors 32 and 34 drops, turning a MOSFET 36 off. The signal A has a shorter duty cycle. The time interval during which A is high is centered within that during which B is high. When A is high, a MOSFET 38 is turned on. Turning on either of the MOSFETs 36, 38 causes its drain-source impedance to go low, so the output waveform in FIG. 3 results. When either MOSFET is on, the output node of the circuit is shorted to the respective power supply line. When neither MOSFET is on, the output node approaches an open-circuit condition, and so tends to seek an intermediate voltage.
The circuit of FIG. 2 operates in a switching mode rather than a linear mode. Power dissipation is reduced. Secondary breakdown is not a problem for a circuit having a MOSFET output. The circuit is less susceptible to output overloads or short circuits. A low-value series output resistor can adequately protect the output devices. A larger value resistor would be required for a linear amplifier, adding undesirable output impedance. On the other hand, the circuit of FIG. 2 cannot produce a sinusoidal output signal, and the rapid edge transitions shown in FIG. 3 can cause electromagnetic interference.

SUMMARY OF THE INVENTION:

These drawbacks in conventional circuits are overcome by providing, in accordance with the invention, a frequency conversion circuit which includes four analog switching elements. Each switching element is logic controlled to open or close, i.e., to have either a low or high conductivity to block or pass analog currents of either polarity. The circuits are coupled to enable either of two lines of a dual input through to either of two lines of a dual output. Effectively, a signal received on the dual input may be enabled in inverted or non-inverted form onto the dual output, depending on the control of the switches.

The circuit may be used for producing a telephone ringing signal from an AC input signal. The circuit is coupled to receive an AC input signal, such as a 60 Hz signal derived from AC line power. The switching elements are alternately opened and closed during a predetermined sequence of half-cycles of the AC input signal. The circuit produces an output signal having a sequence of consecutive positive half-cycles and a sequence of consecutive negative half-cycles. Assuming that the AC line frequency is 60 Hz, a 20 Hz ringing
signal includes three consecutive positive half-cycles, the second one being inverted from the original negative phase, and three consecutive negative half-cycles, the second one or the fifth one overall being inverted from the original positive half-cycle.

Each switching element preferably includes a MOSFET switch stage providing either high or low impedance between two switch electrodes, a current amplifier for providing a gate voltage to the MOSFET switch stage, and a storage circuit including a capacitor for storing energy while the switching element is open.

A ringing signal generating circuit according to the invention dissipates less power than prior art circuits. As a consequence, no large heat sinking surfaces are required, and overall size is reduced. The circuit handles analog signals such as sinusoidal signals, so electromagnetic noise which would be produced by abrupt digital state changes is reduced. Also, the risk of damage to the circuit due to a short circuit is reduced.

Many of the bulky components of prior art circuits have been eliminated. Thus, the physical size and cost of the circuit is reduced. Also, power consumption is reduced and there is less heat to be dissipated. A circuit according to the invention lends itself well to hybridization or monolithic integration.

**BRIEF DESCRIPTION OF THE DRAWINGS:**

FIG. 1 is a schematic diagram of a conventional telephone ringing signal generating circuit including an oscillator and a linear amplifier;

FIG. 2 is a schematic diagram of a conventional telephone ringing signal generating circuit including a DC chopper;

FIG. 3 is a timing diagram illustrating the operation of the circuit of FIG. 2;
FIG. 4 is a schematic diagram of a telephone ringing signal generating circuit according to the invention;

FIG. 5 is a timing diagram illustrating the operation of the circuit of FIG. 4 for various DC values at control inputs of the circuit;

FIG. 6 is a timing diagram illustrating operation of the circuit of FIG. 4 in a method according to the invention;

FIG. 7 is a detailed schematic diagram of a first embodiment of a switching element, four of which are shown in FIG. 4;

FIG. 8 is a schematic diagram of four of the switching elements of FIG. 7, showing how they are coupled within the circuit of FIG. 4;

FIG. 9 is a detailed schematic diagram of a second embodiment of a switching element, four of which are shown in FIG. 4; and

FIG. 10 is a schematic diagram of four of the switching elements of FIG. 9, showing how they are coupled within the circuit of FIG. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS:

FIG. 4 is a simplified schematic diagram of a preferred embodiment of the invention. In accordance with the invention, this embodiment produces a 20 Hz telephone ringing signal from a standard 60 Hz AC sinusoidal line voltage. The overall operation of the circuit of FIG. 4 will be better understood through reference to the timing diagrams of FIGS. 5 and 6. The overall operation will be explained first. Afterward, a more detailed description of certain preferred components of the circuit of FIG. 4 will be given.

An AC line voltage is applied at input terminals 40 and 42. These terminals are coupled to a primary winding of an isolation transformer 44. A secondary winding of the transformer 44 is coupled to two inputs 45 and 46 of
a switching network 47. In accordance with the invention, the switching network includes four switching elements. The switching elements are represented symbolically in FIG. 4, but detailed schematic diagrams for preferred embodiments are given below. Each of the four switching elements has two electrodes. Each switching element operates to open or close its electrodes responsive to a control signal. Each switching element has a control input. Two control signals 56 and 58 are provided for operating the switching elements. The switching network 47 has two outputs 60 and 62.

The switching elements within the switching network 47 are coupled as follows. A first switching element 48 has a first electrode coupled to the input 45 and a control input coupled to the control input 56. A second switching element 50 has a first electrode coupled to the input 45 and a control input coupled to the control input 58. A third switching element 52 has a first electrode coupled to the second electrode of the first switching element 48, a second electrode coupled to the input 46, and a control input coupled to the control input 58. A fourth switching element 54 has a first electrode coupled to the second electrode of the first switching element 50, a second electrode coupled to the input 46, and a control input coupled to the control input 56. The outputs 60 and 62 of the switching network 47 are respectively coupled to the second electrodes of the switching elements 50 and 48.

As will be discussed below, responsive to control signals provided over the control inputs 56, 58, the switching elements 48, 50, 52, 54 open or close. That is, the first and second electrodes of each switch are either coupled together or decoupled. Suitable operation of the switching elements may thus couple the input 45 to the output 60, and the input 46 to the output 62, or vice
versa. If a sinusoidal input signal is received across the inputs 45 and 46, then the signal appears at the outputs 60 and 62 in either an inverted or non-inverted form, depending on the state of the switching elements. This is illustrated in the timing diagram of FIG. 5. The first line is an input sinusoidal waveform at the inputs 45 and 46. The remaining four lines are signals seen at the outputs 60, 62, for the four different steady-state control input values. The second line corresponds with control signals A and B at the control inputs 56 and 58 both having the value 0. In this case, all four of the switching elements are open. As a result, no sinusoidal signal appears at the outputs 60, 62. The third line corresponds with the control signal A at the input 58 having the value 1, and the signal B at the input 56 having the value 0. The switching elements 50 and 52 are then closed, coupling the input 45 through to the output 60 and the input 46 through to the 62. The switching elements 48 and 54 remain open. The result is that the input sinusoid (first line) is coupled through to the outputs 60, 62 in non-inverted form, as shown in the third line.

The fourth line corresponds with the control signal A having the value 0, and the control signal B having the value 1. The switching elements 48 and 54 are closed, coupling the input 45 to the output 62 and the input 46 to the output 60. The switching elements 50 and 52 are open. The result now is that the input sinusoid is inverted, as shown in the fourth line of FIG. 5. The final case, corresponding to the fifth line, is that in which both A and B are high, and all four of the switches are closed. This case is deemed invalid, since the two inputs 45 and 46 are shorted to each other at both of the outputs 60 and 62.
In summary, operation of the switching elements as described above makes it possible to provide an inverted or non-inverted version of an input analog signal at an output. In accordance with the invention, control signals are provided having values which vary in synchronization with the input sinusoidal waveform in a manner shown in the timing diagram of FIG. 6. FIG. 6 shows the input waveform, the control signals A and B (at the control inputs 58 and 56), and the resultant signal provided at the outputs 60 and 62. For clear understanding of FIG. 6, the first line may be visualized as a sequence of six half-cycles. The control signal A at the input 58 is high during the first, third, fourth, and sixth half-cycles and low during the second and fifth. The control signal B at the input 56 is just the opposite. Thus, the input sinusoid (first line) is inverted during the second and fifth half-cycles, and not otherwise.

The resulting output signal is as shown on the fourth line, a series of three positive half-cycles followed by a series of three negative half-cycles. It will be understood that the waveforms, etc., shown in FIG. 6 are repeated. Thus, operation of the circuit of FIG. 4 as shown in FIG. 6 effectively divides the frequency of the input sinusoidal waveform (first line) by 3 to produce the output waveform (fourth line). Of course, the output waveform is not sinusoidal, but has a spectrum of higher frequency components. In practical use, however, the lowest frequency component, having a period equal to three times the period of the input sinusoid, may be used for practical applications.

One such application forms a practical object of the invention. A telephone ringing signal is typically 20 Hz. AC line power, such as that available from an ordinary wall socket, is 60 Hz. Thus, a divide-by-three circuit may be used to produce a 20 Hz ringing signal.
from a 60 Hz input signal derived from the line power. As shown, the isolation transformer 44 may be used to provide the required 60 Hz input signal. While a low pass filter may be coupled at the outputs 60, 62 to smooth out the output signal, i.e., remove higher frequency components, it is usually not necessary that this be done.

It will be understood also, that suitable control signals A and B may be used to divide the input sinusoid by a value other than 3, if other output frequencies are desired. For instance, if A is high during first, third, sixth, and eighth half-cycles and low otherwise, and B is the opposite, then an output signal having four positive half-cycles followed by four negative half-cycles, i.e., a signal divided by four, may be produced. Also, the period of the signal to be produced need not be an integral multiple of the period of the input signal. For instance, a sinusoidal input signal could be divided into quarter-cycles. If the signal is not inverted during the first and fourth quarter-cycles but inverted during the second and third quarter-cycles, the output signal would have two positive phases and two negative phases alternating with each other. Thus, an output signal having a series of frequency components including a fundamental at half the period, and therefore twice the frequency of the input signal would be produced.

Two preferred embodiments of the switching elements 48,50, 52, and 54 will now be considered in more detail. FIGs. 7 and 9 are detailed schematic diagrams of each preferred circuit embodiment. FIGs. 8 and 10 show four each of the respective preferred circuits as they would be coupled together to produce the switching network 47 shown in FIG. 4. Some of the components are common to both of the preferred circuit embodiments. Such common
components are numbered similarly in FIGs. 7 and 9. For the most part, numbers for individual components are omitted from FIGs. 8 and 10.

It has been found that if the switching elements are fully static, i.e., able to be held indefinitely in a continuously conductive condition, implementation of the switching elements tends to be costly. However, the switching elements are to be used for frequency conversion in which each switching element cycles between closed and open states. Therefore, a circuit topology has been developed in accordance with the invention in which a voltage drop during the open state provides a source of energy for use as needed during the closed state. This energy source will be discussed in connection with the discussion of the circuit topology which follows.

Each of the preferred circuits includes a control input element, a current amplifier, an FET switching stage, and a bridge. In FIG. 7, the control input element is shown as an optical coupling device 64 including a light emitting diode (LED) 66 and a phototransistor 68. A control input generally shown as 70 includes a first control input 72 coupled to an anode of the LED 66 and a second control input 74 coupled to a cathode of the LED 66. Since separate input connections to the anode and cathode are provided, an input control signal may be provided to the LEDs of two circuits in series, thus achieving lower current consumption than for the parallel-connected case. A current of about 5 ma is typical. As an alternative, the cathode of the LED 66 could be coupled to ground, or through a current limiting resistor to ground. In this case, the control signal would be coupled in parallel to the anodes of the LED 66 of each circuit.
The control input signal is provided to the anode of the LED 66 through the input 72. A high input signal value causes the LED 66 to emit light. This provides base drive to the phototransistor 68, and causes a current to emerge from the emitter of the transistor 68. This current is not present when a low control signal is provided to the LED anode, and no light is emitted.

The current amplifier includes a first transistor 76 and a second transistor 78. The transistors 76, 78 are preferably NPN and PNP types, respectively, and have their bases and emitters respectively coupled to each other as shown. The bases are coupled to receive the current from the phototransistor 68. Due to the coupled emitters, each transistor is capable of operating as an emitter follower. A current sink resistor 80 is coupled between the base and collector of the transistor 78.

A MOSFET switching stage includes, in the embodiment of FIG. 7, two MOSFETs 84 and 86. Sources of the MOSFETs 84, 86 are coupled together, and drains of the MOSFETs 84, 86 are respectively coupled to switch electrodes 88 and 90. Gates of the MOSFETs 84, 86 are coupled through a current limit resistor 82 to the coupled emitters of the transistors 76, 78.

When a high control signal is received by the LED 66, current from the transistor 68 causes a voltage drop across the resistor 80. This raises the base voltages of the transistors 76 and 78. The transistor 78 is turned off, and the transistor 76 is turned on. Due to emitter-follower action of the transistor 76, a positive voltage is produced at the junction between the emitters. Current from the transistor 76 flows through the current limit resistor 82 to the gates of the MOSFETs 84 and 86. The resistor 82 limits the rate of gate capacitance charging, and thereby limits the generation of electrical noise during MOSFET switching. The MOSFETs 84 and 86 have insulated gates and gate-to-source capacitances, so
the current is stored by the capacitances as a charge, and the voltage of the gates goes up. Preferably the components have such values that the gate voltages are raised to a viable ON voltage, typically at least 4 volts relative to the sources, within a short time, typically less than 500 microseconds. As a result, drain-to-source channels of the MOSFETs 84, 86 are enhanced, and conductivity through the channels goes from a low value to a high value. This has the effect of closing the switching element, i.e., shorting the switch electrodes 88 and 90 together.

When a low control signal is received by the LED 66, no current is produced by the transistor 68. The base voltages of the transistors 76, 78 fall via resistor 80, turning the transistor 76 off and the transistor 78 on. Emitter-follower action of the transistor 78 amplifies current flow through the resistor 80. Thus, the stored charge in the gate capacitances of the MOSFETs 84, 86 is bled off through the transistor 78. Preferably the discharge is quick enough that the gates reach an OFF voltage, typically less than 2 volts relative to the sources, within a short time, typically less than 500 microseconds. The drain-to-source channels of the MOSFETs 84, 86 are depleted, and the conductivity of the MOSFETs drops to a low value. This has the effect of opening the switching element, i.e., decoupling the switch electrodes 88, 90.

As stated above, the cyclical operation of the switching element makes it possible to store a DC supply voltage during the OFF state. The bridge rectifier in the circuit of FIG. 7 includes two parasitic diodes 92 and 94 coupled between the respective drains and sources of the MOSFETs 84, 86. While the parasitic diodes 92, 94 are shown as separate components, in practice they are implemented within the structure of the MOSFETs. The diodes 92, 94 allow only a unipolar OFF state. They are
back-to-back, i.e., coupled anode-to-anode. As a result, a drain-to-drain OFF state of the pair of MOSFETs 84, 86 has integrity regardless of the polarity of the applied voltage. Also, in the ON state each MOSFET is conductive either drain-to-source or source-to-drain, although in one of the two cases the parasitic diode is reverse biased. Thus the ON integrity is also preserved.

The bridge rectifier also includes two diodes 96 and 98 which are coupled cathode-to-cathode. The bridge has two input terminals which coincide with the switch electrodes 88 and 90. The bridge also has two output terminals. A negative output terminal coincides with the sources of the MOSFETs 84, 86, and a positive output terminal coincides with the coupled cathodes of the diodes 96, 98. While the switching element is open, any AC voltage across the switch electrodes 88, 90 is rectified at the cathode-to-cathode junction of the diodes 96, 98. This rectified voltage causes a current flow through a resistor 100 into a storage capacitor 102. A Zener diode 104 is coupled across the capacitor 102 such that its reverse bias breakdown voltage limits a voltage across the capacitor 102 so that no unsafe voltage will be applied to the MOSFET gates. The diodes 96, 98 also prevent the capacitor 102 from discharging through the resistor 100 while the switching element is ON, i.e., closed.

The capacitor 102 preferably has a value large enough that it can maintain a usable fraction of its initial charge during the longest anticipated ON state of the switching element, as defined by the desired frequency conversion and the form of the control signal to be provided at the control input 70. On the other hand, the capacitor should have a value small enough that it can charge all the way up to the Zener diode clamping voltage within a half-cycle of the input waveform. The resistor 100 could be made low in value to increase the
rate of charging of the capacitor 102. Preferably, however, the resistor should be large in value to maintain a high impedance OFF state and to reduce the power dissipation across the resistor 100 so that it can be physically small.

Turning now to FIG. 8, there is shown a switching network 47 as per FIG. 4, implemented using four of the switching elements of FIG. 7. Each switching element is numbered consistently with FIG. 4. Individual components within the four switching elements are shown, but not numbered unless specifically referred to. It will be understood that components shown within the four switching elements are consistent with the detailed description given in connection with FIG. 7.

The control inputs will be discussed first. As stated above, two control inputs coupled to the anode and cathode of the LED 66 are provided, so that a series current path running between the LEDs 66 of different switching elements may be made. Thus, the A control input 58 runs to the control input 72 of the switching element 50, through the LED, from the input 74 of the switching element 50 to the input 72 of the switching element 52, through the LED, from the input 74 of the switching element 52 to ground. Similarly, the B control input 56 runs to the control input 72 of the switching element 48, through the LED, from the input 74 of the switching element 48 to the input 72 of the switching element 54, through the LED, from the input 74 of the switching element 54 to ground.

The input 45 from the secondary winding of the transformer 44 is coupled to the switch electrodes 88 of the switching elements 48 and 50. The input 46 from the secondary winding of the transformer 44 is coupled to the switch electrodes 90 of the switching elements 52 and 54. The switch electrode 90 of the switching element 48 is coupled to the switch electrode 88 of the switching
element 52 and to the switching network output 62. Similarly, the switch electrode 90 of the switching element 50 is coupled to the switch electrode 88 of the switching element 54 and to the switching network output 60. Thus, the result is a switching network consistent with that shown in simplified schematic form in FIG. 4.

Turning now to FIG. 9, there is shown a second preferred embodiment of the switching element. For the most part, circuit components in the circuit of FIG. 9 correspond with components of FIG. 7, and are numbered similarly. The circuit of FIG. 9 is less expensive than that of FIG. 7 due to a reduced number of components.

In the circuit of FIG. 9, the MOSFET 86 is eliminated, and the MOSFET 84 by itself serves as a MOSFET switch stage for providing a high or low conductivity between the switch electrodes 88, 90. A bridge rectifier 106 is coupled between the drain and source of the MOSFET 84 and the switch electrodes 88, 90 in order to provide a current flow through the drain and source of the MOSFET 84 which is independent of a direction of current flow through the switch electrodes 88, 90. Because of this independence of current direction, the MOSFET 86 may be eliminated. Also, there is no longer a need for a bridge rectifier made up of the diodes 92 through 98 as was provided in FIG. 7. Rather, supply voltage for charging the capacitor 102 during the OFF, i.e., open, state of the switching element is provided from the bridge rectifier 106 through a diode 108. This diode prevents the capacitor 102 from discharging through the resistor 100 while the switching element is ON, i.e., closed.

FIG. 10 is a detailed schematic diagram showing four of the circuits of FIG. 9 coupled to form the switching network 47 of FIG. 4. FIG. 10 is in essentially the same form as FIG. 8. Components are numbered in FIG. 10 the same way that comparable components are numbered in FIG.
8. It will thus be understood that the explanatory discussion given above in connection with FIG. 8 applies equally to FIG. 10. Thus, it will not be repeated here.

In summary, a circuit according to the invention as described and claimed herein may be used for producing a telephone ringing signal by frequency conversion. Specifically, a sinusoidal input waveform having a predetermined frequency, such as ordinary 60 Hz AC line power, may be frequency converted to a desired frequency for a telephone ringing signal, such as 20 Hz, by inverting the input waveform at predetermined intervals. The resulting waveform need not be purely sinusoidal, but should be periodic at the desired frequency, and should have a frequency component of substantial magnitude at the desired frequency.

A circuit for generating the telephone ringing signal according to the invention includes four switching elements arranged in a bridge configuration and controlled by control signals to open or close at time intervals corresponding with desired phases of the input waveform. Thus, the input waveform is enabled to a dual output in inverted or non-inverted form at appropriate phases of the input waveform.

Such a circuit is advantageous over conventional circuits in that it provides an analog output, avoids electromagnetic noise caused by rapid state changes, does not dissipate a large amount of power to require bulky, expensive heat sinks or other components, reduces a hazard of damage to the circuit due to a short circuit at the outputs. The circuit in accordance with the invention also provides additional advantages which are clear from the foregoing detailed description.
While I have shown and described an embodiment in accordance with the present invention, it is to be understood that the invention is not limited thereto, but is susceptible to numerous changes and modifications as known to a person skilled in the art. I therefore do not wish to be limited to the details shown and described herein, but rather intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.
WHAT IS CLAIMED IS:

1. A frequency conversion circuit comprising:
   a dual input for receiving an input periodic waveform having a first period, a positive phase, and a negative phase;
   a switching network having first and second inputs coupled to the dual input and first and second outputs, the switching network including (a) a first switching element having a first switch electrode coupled to the first input and a second switch electrode coupled to the first output, (b) a second switching element having a first switch electrode coupled to the first input and a second switch electrode coupled to the second output, (c) a third switching element having a first switch electrode coupled to the first output and a second switch electrode coupled to the second input, and (d) a fourth switching element having a first switch electrode coupled to the second output and a second switch electrode coupled to the second input; and
   means for opening and closing the switching elements by coupling and decoupling the respective first and second switch electrodes of the switching elements of the switching network in (a) a first configuration wherein the input periodic waveform is provided at the first and second outputs in non-inverted form, and (b) a second configuration wherein the input periodic waveform is provided at the first and second outputs in inverted form, at respective times corresponding with predetermined phases of the input periodic waveform to produce an output periodic waveform having a second period and including, within each period, a predetermined number of consecutive positive phases and a predetermined number of consecutive negative phases.

2. A circuit as recited in claim 1 further comprising an isolation transformer at the dual input.
3. A circuit as recited in claim 1 wherein the means for opening and closing include, within each switching element:

means for coupling and decoupling the first and second switch electrodes responsive to first and second values of a control signal provided to the switching element; and

means for providing a first control signal to the first and fourth switching elements and a second control signal to the second and third switching elements, wherein the first signal has the first value and the second signal has the second value to produce the second configuration, and the first signal has the second value and the second signal has the first value to produce the first configuration.

4. A circuit as recited in claim 3 wherein, for each switching element, the means for coupling and decoupling include:

an optical isolating device having an input coupled to receive the control signal and an output at which is provided a current having a value related to the value of the control signal; and

a current amplifier coupled to receive and amplify the current from the optical isolating device.

5. A circuit as recited in claim 4 wherein the optical isolating device includes:

an LED having an anode coupled to receive the control signal including a control current and a cathode coupled to provide the control current, whereby LEDs from a plurality of switching elements may be coupled in series to receive the control signal and control current; and
a phototransistor disposed to receive light from the
LED and produce a current related to the value of the
control signal.

6. A circuit as recited in claim 4 wherein, for
each switching element, the means for coupling and
decoupling further include:

a MOSFET switch stage including at least one MOSFET
having a gate and a drain-to-source channel coupled
between the first and second switch electrodes; and
means for providing a first voltage to the gate
responsive to the first value of the control signal to
couple the first and second switch electrodes, and a
second voltage responsive to the second value of the
control signal to decouple the first and second
electrodes.

7. A circuit as recited in claim 4 wherein each
switching element further includes means for storing
power while the switching element is open and for
providing the stored power to the optical isolating
device and to the current amplifier while the switching
element is closed.

8. A circuit as recited in claim 7 wherein the
means for storing power includes:

a bridge rectifier having first and second inputs
coupled respectively to the first and second switch
electrodes and a first output;

a current limiting resistor having a first end
coupled to the first output of the bridge rectifier and
a second end; and

a storage capacitor having a first end coupled to
the second end of the current limiting resistor and a
second end coupled to said bridge rectifier.
9. A circuit as recited in claim 8 wherein the means for storing power further includes a Zener diode coupled in parallel with the storage capacitor, the Zener diode having a reverse bias breakdown voltage for clamping a voltage across the storage capacitor to a value which operates the switching element safely.

10. A circuit as recited in claim 9, wherein:
each switching element includes first and second MOSFETs each having a drain-to-source channel, a conduction path between the first and second switch electrodes running through the drain-to-source channels of the MOSFETs; and
the bridge rectifier includes first and second parasitic diodes respectively implemented within a structure of the MOSFETs and coupled in series between the first and second inputs of the bridge rectifier, third and fourth diodes coupled in series between the first and second inputs of the bridge rectifier, the first output being between the third and fourth diodes.

11. A circuit as recited in claim 9 wherein:
each switching element includes a MOSFET having a drain and a source;
the bridge rectifier includes first and second inputs respectively coupled to the first and second switch electrodes, and first and second outputs respectively coupled to the drain and source of the MOSFET, and
a current blocking diode having an anode coupled to the first output of the bridge rectifier and a cathode coupled to the first end of the current limiting resistor.
12. A circuit for producing a telephone ringing signal comprising:
   first and second AC inputs for receiving an alternating current (AC) waveform;
   first and second control inputs for receiving first and second control signals, each control signal having first and second values;
   first, second, third, and fourth switching elements, each switching element including first and second electrodes, a control electrode, and means for coupling and decoupling the first and second electrodes responsive, respectively, to a first value and a second value received at the control electrode; and
   first and second outputs;
   wherein:
   (a) the first electrodes of the first and second switching elements are each coupled to the first AC input,
   (b) the second electrode of the first switching element is coupled to the first electrode of the third switching element and to the first output,
   (c) the second electrode of the second switching element is coupled to the first electrode of the fourth switching element and to the second output,
   (d) the second electrodes of the third and fourth switching elements are each coupled to the second AC input,
   (e) the control electrodes of the first and fourth switching elements are each coupled to the first control input, and
   (f) the control electrodes of the second and third switching elements are each coupled to the second control input.
13. A circuit as recited in claim 12 wherein, for each switching element, the control electrode includes first and second terminals and a control element coupled therebetween.

14. A circuit as recited in claim 13 wherein, for each switching element, the control element includes an LED coupled between the first and second terminals to produce light related to the value of the control signal provided to the control electrode, and a photosensitive element disposed adjacent to the LED to receive light therefrom and produce a current related to the light received from the LED.

15. A circuit as recited in claim 13 further comprising:

first coupling means for coupling (a) the first control input to the first terminal of one of the first and fourth switching elements, (b) the second terminal of the one of the first and fourth switching elements to the first terminal of the other of the first and fourth switching elements, and (c) the second terminal of the other of the first and fourth switching elements to ground; and

second coupling means for coupling (a) the second control input to the first terminal of one of the second and third switching elements, (b) the second terminal of the one of the second and third switching elements to the first terminal of the other of the second and third switching elements, and (c) the second terminal of the other of the second and third switching elements to ground.
16. A circuit as recited in claim 12 wherein each switching element includes:
   a control input element which produces a current related to the value of the control signal received at the control input;
   a current amplifier coupled to receive and amplify the current produced by the control input element, thereby producing an amplified current;
   a MOSFET switch stage having an input coupled to the current amplifier such that an input capacitance of the MOSFET switch stage is charged by the amplified current, a conductivity of the MOSFET switch stage being related to the value received at the control input; and
   an energy storage circuit coupled to the MOSFET switch stage and to the current amplifier.

17. A circuit as recited in claim 16 wherein, for each switching element, the control input element includes an optical isolating element including an LED coupled between the first and second terminals and a photosensitive element disposed adjacent to the LED to receive light therefrom and produce a current related to the light received from the LED.

18. A circuit as recited in claim 17 wherein the photosensitive element is a phototransistor.

19. A circuit as recited in claim 16 wherein the current amplifier includes:
   a first transistor coupled to provide current to the MOSFET switch stage responsive to the ON value; and
   a second transistor coupled to bleed current from the MOSFET switch stage responsive to the OFF value.
20. A circuit as recited in claim 19 wherein the
current amplifier has a current gain:
such that, responsive to a control input element
current corresponding to the ON value at the control
input, the current amplifier provides enough current to
charge the input capacitance of the MOSFET switch stage
to a predetermined ON voltage within a predetermined
time; and
such that, responsive to a control input element
current corresponding to the OFF value at the control
input, the current amplifier bleeds enough current to
discharge the input capacitance of the MOSFET switch
stage to a predetermined OFF voltage within a
predetermined time.

21. A circuit as recited in claim 20 wherein the
predetermined ON voltage of the MOSFET switch stage is at
least 4 volts, the predetermined OFF voltage of the
MOSFET switch stage is at most 2 volts, and the
predetermined time is at most 500 microseconds.

22. A circuit as recited in claim 19 wherein:
the first transistor is an NPN bipolar transistor
having a collector, a base, and an emitter;
the second transistor is a PNP bipolar transistor
having an emitter coupled to the emitter of the first
transistor, a base coupled to the base of the first
transistor, and a collector;
the bases of the first and second transistors are
coupled to the control input element to receive base
current therefrom; and
the circuit further comprises:
a first resistor coupled between the base and the
collector of the second transistor for providing a bias
voltage to the bases of the first and second transistors
responsive to current from the control input element; and
a second resistor coupled between the emitters of
the first and second transistors and the MOSFET switch
stage for conducting current from the first transistor to
charge the MOSFET switch stage capacitance and for
bleeding the charge from the MOSFET switch stage to the
second transistor.

23. A circuit as recited in claim 16 wherein the
power storage circuit includes a bridge rectifier having
first and second inputs and first and second outputs.

24. A circuit as recited in claim 23 wherein:
the MOSFET switch stage includes:
a first MOSFET having a drain coupled to the first
input of the bridge rectifier, a source, a gate coupled
to the current amplifier, and a gate-to-source
capacitance, wherein current from the current amplifier
charges the gate-to-source capacitance, and
a second MOSFET having a drain coupled to the second
input of the bridge rectifier, a source coupled to the
source of the first MOSFET, a gate coupled to the current
amplifier, and a gate-to-source capacitance, wherein
current from the current amplifier charges the gate-to-
source capacitance; and
the bridge rectifier includes first and second
parasitic diodes implemented as part of a structure of
the first and second MOSFETs, respectively, to be coupled
between the drain and source of the respective MOSFETs.

25. A circuit as recited in claim 24 wherein the
power storage circuit further includes:
a storage capacitor; and
a resistor coupled between the first output of the
bridge rectifier and the storage capacitor.
26. A circuit as recited in claim 25 wherein the bridge rectifier includes:
   a third diode having an anode coupled to the first switch electrode and a cathode coupled to a first end of the resistor; and
   a fourth diode having an anode coupled to the second switch electrode and a cathode coupled to the first end of the resistor.

27. A circuit as recited in claim 25 wherein the energy storage circuit further comprises a Zener diode having a cathode coupled to a second end of the resistor and to a first end of the capacitor, and an anode coupled to a second end of the capacitor, the Zener diode having a predetermined reverse bias breakdown voltage for clamping a voltage across the capacitor to a safe value for the gates of the MOSFETs.

28. A circuit as recited in claim 23 wherein the MOSFET switch stage includes a first MOSFET having a drain and a source respectively coupled to the first and second outputs of the bridge rectifier.

29. A circuit as recited in claim 28 wherein the power storage circuit further includes:
   a diode having an anode coupled to the first output of the bridge rectifier and a cathode;
   a storage capacitor; and
   a resistor having a first end coupled to the cathode of the diode and a second end coupled to the storage capacitor.
30. A circuit as recited in claim 29 wherein the power storage circuit further comprises a Zener diode having a cathode coupled to a second end of the resistor and to a first end of the capacitor, and an anode coupled to a second end of the capacitor, the Zener diode having a predetermined reverse bias breakdown voltage for clamping a voltage across the capacitor to a safe value for the gate of the MOSFET.

31. A method for producing a telephone ringing signal from an alternating current (AC) input signal received at a dual line AC input including first and second circuit inputs using a circuit including four switching elements, each having first and second switch electrodes, a control input, and a dual output including first and second circuit outputs, wherein:
(a) the first switch electrodes of the first and second switching elements are each coupled to the first circuit input,
(b) the second switch electrode of the first switching element is coupled to the first switch electrode of the third switching element and to the first circuit output,
(c) the second switch electrode of the second switching element is coupled to the first circuit electrode of the fourth switching element and to the second circuit output, and
(d) the second switch electrodes of the third and fourth switching elements are each coupled to the second circuit input,
the method comprising the steps of:
defining a predetermined sequence of time intervals whose total length make up a period of the desired telephone ringing signal and whose time intervals individually correspond with respective positive and negative phases of the AC input signal;
applying a first value to the control inputs of the first and fourth switching elements and a second value to the control inputs of the second and third switching elements during a first time interval to close the first and fourth switching elements and to open the second and third switching elements, whereby an output signal at the circuit output is a non-inverted form of the input signal during the first time interval;

applying the second value to the control inputs of the first and fourth switching elements and the first value to the control inputs of the second and third switching elements during a second time interval to open the first and fourth switching elements and close the second and third switching elements, whereby an output signal at the circuit output is an inverted form of the AC input during the second time interval; and

repeating the steps of applying over the time intervals of the sequence, whereby the output signal, over one period of the desired ringing signal, consists of a consecutive sequence of positive phases and a consecutive sequence of negative phases.

32. A method as recited in claim 31 wherein the step of defining includes defining time intervals corresponding with positive and negative half-cycles of the AC input signal.

33. A method as recited in claim 32 wherein:

the step of applying during the first time interval includes applying during second and fifth ones of six consecutive half-cycles of the AC input, and

the step of applying during the second time interval includes applying during first, third, fourth, and sixth ones of the six consecutive half-cycles of the AC input,
whereby the output signal has a period three times as great as a period of the AC input, and, for each period, has three lobes of a first polarity during the first, second, and third half-cycles, and three lobes of a second polarity during the fourth, fifth, and sixth half-cycles.

34. A frequency conversion method for producing a periodic signal having a second period from an alternating current (AC) input signal having a first period received at a dual line AC input including first and second circuit inputs using a circuit including four switching elements, each having first and second switch electrodes, a control input, and a dual output including first and second circuit outputs, wherein:
(a) the first switch electrodes of the first and second switching elements are each coupled to the first circuit input,
(b) the second switch electrode of the first switching element is coupled to the first switch electrode of the third switching element and to the first circuit output,
(c) the second switch electrode of the second switching element is coupled to the first circuit electrode of the fourth switching element and to the second circuit output, and
(d) the second switch electrodes of the third and fourth switching elements are each coupled to the second circuit input,
the method comprising the steps of:
defining a predetermined sequence of time intervals whose total length make up the second period and whose time intervals individually correspond with respective positive and negative phases of the AC input signal;
applying a first value to the control inputs of the first and fourth switching elements and a second value to the control inputs of the second and third switching elements during a first time interval to close the first and fourth switching elements and to open the second and third switching elements, whereby an output signal at the circuit output is a non-inverted form of the input signal during the first time interval;

applying the second value to the control inputs of the first and fourth switching elements and the first value to the control inputs of the second and third switching elements during a second time interval to open the first and fourth switching elements and close the second and third switching elements, whereby an output signal at the circuit output is an inverted form of the AC input during the second time interval; and

repeating the steps of applying over the time intervals of the sequence, whereby the output signal, over one second period, consists of a consecutive sequence of positive phases and a consecutive sequence of negative phases.

35. A method as recited in claim 34 wherein the step of defining includes defining time intervals corresponding with positive and negative half-cycles of the AC input signal.
INTERNATIONAL SEARCH REPORT

INTERNATIONAL APPLICATION NO. PCT/US92/10379

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H04M 3/02
US CL : 379/418

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S.: 379/418 379/372, 373, 374, 375, 375, 253

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>US-A, 4,500,844 (Lisco) 19 February 1985 Column 6, line 56-Column 8, line 8.</td>
<td>1-3, 12, 13, 15</td>
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Further documents are listed in the continuation of Box C.

Date of the actual completion of the international search

07 March 1993

Date of mailing of the international search report

06 APR 1993

Authorized officer

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<td>A</td>
<td>DE,A, 0,230,127 (Nachrichtentechnik) 20 November 1985 Abstract and figure.</td>
<td>1-35</td>
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