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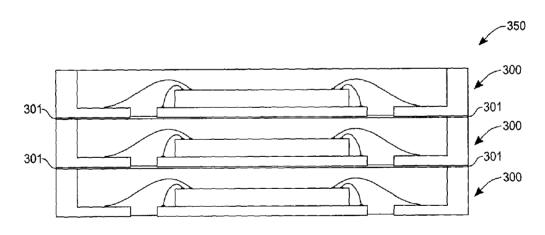
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
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(54) Title: STACKABLE PACKAGES FOR THREE-DIMENSIONAL PACKAGING OF SEMICONDUCTOR DICE



 $Fig._3B$

(57) Abstract: An apparatus and a method for packaging semiconductor devices. The apparatus includes a substrate strip component (201A-201E) of a leadless three-dimensional stackable semiconductor package (300) having mounting contacts on, for example, four peripheral edges. The substrate strip may either be fabricated for mounting a single electrical component (e.g., an integrated circuit die 209) or a plurality of substrate strips may be laid out in an X-Y matrix pattern which may later be singulated (215) into individual package strip for leadless packages. Three-dimensional stacking (350) is achieved by a bonding area (301) on an uppermost portion of the sidewall (203). The sidewall of the strip is high enough to enclose an encapsulant (213) covering a later mounted integrated circuit die and associated bonding wires (211).



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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)				
C. DOC	UMENTS CONSIDERED TO BE RELEVANT			
Category *	Citation of document, with indication, where appropriate, of the relevant passages			Relevant to claim No.
х	US 5,422,514 (Griswold et al.) 6 June 1995 (06.06.1995) Fig. 2, 3			1-3, 7, 9, 15-17
у				4-6, 8, 10-14
у	US 5,541,449 (Crane, Jr. et al.) 30 July 1996 (30.07.1996) column 24 lines 16-26.			4-6, 8, 9-14
Further documents are listed in the continuation of Box C.			See patent family annex.	
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