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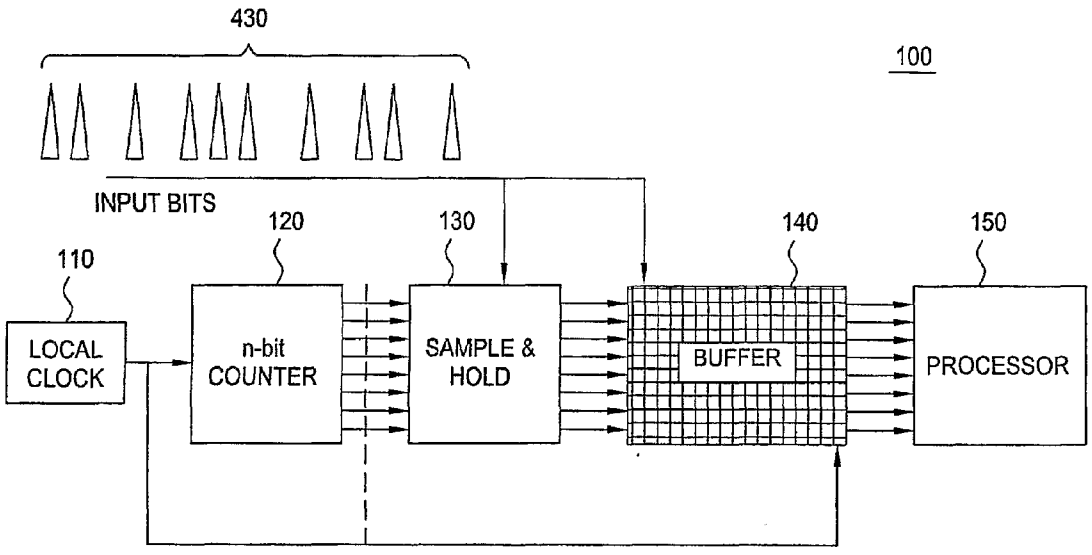
(54) **Title:** RECEIVER SCHEME FOR SYNCHRONOUS DIGITAL TRANSMISSION



(57) **Abstract:** A method, apparatus and system for improving the tolerance for timing jitter noise by eliminating the need to recover clock information from the input signal. There is no need to communicate clock synchronization information between transmit and receive gateways. In addition, the new receiving scheme can work in burst mode in its true sense, i.e., recovering data bits from the first incoming bit after an arbitrary period of time without transmitting.

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RECEIVER SCHEME FOR SYNCHRONOUS DIGITAL TRANSMISSION

FIELD OF THE INVENTION

The invention is related to the field of digital transmission, and in particular, to a receiver scheme for synchronous optical network.

BACKGROUND OF THE INVENTION

Current digital receivers typically include a clock recovery circuit, a sample/hold circuit, and a comparator. An input signal having a pulse train is received and processed by the digital receiver to extract therefrom a data stream. Briefly, the clock recovery circuit recovers a clock from the input signal. The sample/hold circuit uses the recovered clock to sample the input pulse train and produce a steady signal level for processing by the comparator. The comparator compares the analog value of the sampled signal to a threshold value to determine the sample value, which may be further processed by demodulators and the like. This process is repeated for each clock cycle.

Operation of current digital receivers may be degraded in the presence of an input signal experiencing timing jitter. This is because the timing jitter causes the clock recovery circuit to select clock events that may be inaccurate, which in turn causes the data slicing level used by the comparator to be inaccurate, resulting in a bit errors that may or may not be correctable. Moreover, several bit periods are usually necessary for a recovered clock to be stable. Thus, due to clock recovery errors and/or the time necessary to establish a stable clock, the recovery of a burst mode digital transmission signal is difficult.

SUMMARY

The present invention improves upon the prior art by providing a digital receiver that is well adapted to both burst mode and continuous mode digital signal reception. Specifically, a digital receiver according to the present invention provides a sequence of time stamps which are associated by a sample and hold circuit with a sequence of pulses within an input pulse train. The input pulse train includes a sequence of pulses that represents the information being transmitted. The sample and hold circuit contains a time stamp provided by a counter. Each pulse triggers the sample and hold circuit to release the time stamp to a buffer. Thus, the buffer includes a series of time stamps

associated with the series of pulses of the input pulse train. The input pulse train can be recreated using the time stamp information. The transmitted values of the input pulse train are then determined by a processor using the time stamps associated with input pulse train. In this manner, errors normally associated with an improper data slice level of a comparator are avoided.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a block diagram of a receiver according to an embodiment of the present invention;

FIG. 2 depicts a flow diagram of a reception method according to an embodiment of the present invention;

FIG. 3 depicts a flow diagram of a processing method according to an embodiment of the present invention; and

FIG. 4 depicts a timing diagram illustrating the operation of a receiver according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention will be primarily described within the context of a synchronous digital receiver; however, those skilled in the art and informed by the teachings herein will realize that the invention is also applicable to any apparatus and method that involves synchronizing received signals.

FIG. 1 depicts a block diagram of a receiver according to one embodiment of the present invention. The incoming signal is an input pulse train, which includes either optical or electrical input signals. The receiver 100 is a synchronous digital receiver that is designed for either optical or electrical input signals. In one embodiment, the receiver receives an optical input signal. The gates of the receiver are optical gates. In another embodiment, the input signal is electrical signal, or the input signal is first converted to an electrical signal. The receiver in this embodiment includes electronic gates.

The receiver 100 of FIG. 1 receives the input pulse train and includes a local clock 110, an n-bit counter 120, a sample/hold circuit (S&H) 130, a buffer 140 and a processor 150.

The local clock 110 provides fixed clocking signals at regular intervals (clock cycles) to digitize the time of the arrival of input pulses. The local clock is communicated to the n-bit counter 120 and the output of the buffer 150. In one embodiment, the clock 110 is a local oscillator.

The n-bit counter 120 receives the local clock 110 and produces an n-bit value, which is incremented at every clock cycle. The counter 120 functions as a timer. The counter 120 recalls the time of the pulses of the pulse train by incrementing an n-bit value for every incoming clock pulse from the local clock 110. The counter 120 then communicates the n-bit value to the S&H 130 as the time stamp of pulse of the pulse train.

The S&H 130 is triggered by incoming pulses from the input pulse train to hold the current count from the counter 120 as the time stamp. Each input pulse that is received by the S&H 130 enables the S&H such that it holds the time stamp for transmission to buffer 140. In one embodiment, the S&H holds the time stamp from the counter 120, which is transmitted by the counter output to the buffer 140. The time stamp represents the arrival time of the input pulses of the pulse train at the next clock cycle.

The buffer 140 stores the time stamp values from the S&H 130. In one embodiment, the buffer 140 is a first-in-first-out (FIFO) buffer having a plurality of shift registers. Other buffers, queues, and memory devices may be used in conjunction with the respective buffers, queues or memory controllers to perform the equivalent FIFO function. The contents in the buffer 140 are released to the processor 150 at a fixed rate determined by the local clock 110. In one embodiment, shift registers of the FIFO buffer 140 are triggered by input pulses from the local clock. At each cycle of the local clock, the FIFO buffer 140 transmits a time stamp value from the S&H 130 to the FIFO buffer 140 if there is a value stored in the S&H 130. The time stamp value is stored in a first shift register of the FIFO buffer. If there is no pulse at the input pulse train, then the S&H 130 will not have a time stamp value for that clock cycle because no pulse triggers the S&H 130 to store the time stamp. At a future clock cycle when the next pulse of the pulse train is received, the S&H stores the time stamp corresponding to

that pulse. At the following clock cycle, the S&H sends the time stamp value of that pulse to the FIFO buffer. In the FIFO buffer, the value in the first shift register passes to the second shift register, and the new value from the S&H is stored in the first shift register. The local clock triggers the passing of time stamp values in the shift register. At the output of the buffer 140 or the last shift register, the time stamp value that is stored is transmitted from the buffer 140 to the processor 150. Thus, the time stamp value is communicated to the processor 150. In another embodiment, the local clock maybe a global clock or a timer.

The processor 150 processes the time stamp value using an algorithm to recover the incoming digital bits of the input signal described below in FIG. 3. By obtaining all the time stamp values, the processor realizes all the time slots containing the "1" bit. After appending the "0" bits to the remaining time slots, the original information are recovered.

In another embodiment, the receiver takes a random incoming bit sequence (b_n; $n \geq 0$), with $b_0 = 1$ and the arriving time relative to the first bit is (T_n) with $T_n < T_{n+1}$. Consider the time interval ($\Delta T_n = T_n - T_{n-1} > 0$, $n > 0$), one has $\overline{\Delta T_n} = T$, where 1/T is the digital transmission rate. Assuming (t_k) is the subset of (T_n) so that (b_k) is all 1s in the sequence. Then, the closest integers to (t_k/T) can be considered as time slots where "1" is being transmitted. If there are empty time slots in between neighboring 1s, then the symbol transmitted at those time slots are zeros. For example, assume the input bit sequence is (10010111) with nominal data rate of 1 in arbitrary unit. There are total of five ones in this eight bit sequence. The arriving times for these ones are for example 0.0016, 3.0994, 5.2204, 6.1892, and 6.881. The closest integers are 0, 3, 5, 6, and 7. Therefore the bit sequence is (10010111).

For extremely large jitter, it is possible for one integer to appear multiple times. This event indicates that one or more neighboring bits are non-distinguishable in arrival time. If local clock has a finer time resolution than data rate, then multiple possibilities can be narrowed down and the correct bit recovery. In the situation where two or more possibilities cannot be eliminated, then the situation indicates that multiple possibilities exist.

FIG. 2 depicts a flow diagram of the receiver according to one embodiment of the present invention. The flow diagram 200 describes a method the receiver determines the input signal without obtaining a clock signal from the input pulse train.

At step 210, the receiver receives the input signal such as a binary pulse train including binary pulses, which can be either electrical pulses or optical pulses.

At step 220, the receiver records an arrival time of each pulse of the incoming pulse train. In one embodiment, for every clock cycle there is a pulse in the pulse train, the value of the local clock is stored as the time stamp for that pulse. Thus, each pulse has associated with it a time stamp.

At step 230, a buffer is used to store the time stamps associated with the incoming pulses. In one embodiment, the buffer is a FIFO buffer. In other embodiments, other kinds of buffers, memories or queues are used. The purpose of the buffer is to not overload the processor if too many pulses are received at one time. The size of the buffer is selected depending on the amount of information to be received and the transmission speed with respect to the processor speed.

At step 240, the buffer transmits the time stamp values to the processor. In one embodiment, the buffer is a FIFO buffer and its output portion for transmission to the processor is triggered by the local clock. The oldest received time stamp is transmitted to the processor when a new time stamp is received by the buffer.

At step 250, the processing algorithm of the processor will process the time stamp values communicated by the buffer in step 240. The algorithm (further described in FIG. 3) determines the time slots of the pulses of the incoming pulse train.

At step 260, the processing algorithm uses the time stamp values of the input pulses of the input pulse train to determine the time slots of the pulses. By knowing the time stamps of the pulses, any time slots with no pulses are also determined. With the knowledge of recovered pulses, the input pulse train is recovered.

FIG. 3 depicts a flow diagram of a processing algorithm according to one embodiment of the present invention. In one embodiment, the processing algorithm 300 is used in the processor 150.

At step 310, a relative arrival time t_n of a pulse is communicated from the buffer 140 to the processor 150. The arrival time is the time stamp of a clock cycle associated with a pulse that is received by the receiver.

At step 320, the relative arrival time is used to determine the slot number of the pulse of the input pulse train. In one embodiment, the slot number N is calculated by multiplying the relative arrival time with the transmission rate: ($N=t_n/T$). The calculation allows the receiver to use the slot numbers to realize the relative positions of

the pulses. By analyzing the time stamp value, the processor determines the time slots with 1's.

At step 330, the processor determines all the time slots that do not contain 1's and appends 0's to those slot numbers. As a result of adding 0's to the slots, the processor obtains a stream of 1's and 0's representative of the transmitted signal that is received by the receiver.

At step 340, the processor outputs the recovered data derived from the received time stamps.

FIG. 4 depicts the timing diagram illustrating the operations of the receiver according to one embodiment of the present invention. The diagram 400 is a representation of the signals received by the receiver and shows how the receiver corrects for jitter in the received pulse train.

The first set of timing traces 410 represents the signals at the output of the n-bit counter. In one embodiment, a 3-bit counter is used and is represented by signals 412, 415 and 418. The combination of the three signals will represent the time slots 0 to 15.

Numbers shown in the top row 420 indicate the numbering of the time slots 420_0 to 420_{15}. The top three timing traces are three outputs of the n-bit counter in the example discussed above. The vertical dotted lines are the interval where the pulse should come into the receiver.

Input pulse train 420 is received by receiver 100 and the pulses are shown by 420_2, 420_5, 420_7, 420_8, 420_9. The diagram shows incoming data pulses 420_2, 420_5, 420_7, 420_8, 420_9 with significant timing jitter. Those pulses are either before or after the time slot. Nonetheless, the buffer 140 will be filled with time stamps of 1s in the input sequence, (010)(101)(111)(000)(001). Therefore the incoming bit sequence (10010111) can be successfully recovered.

In one embodiment, assume the incoming data rate of 40 Gb/s. The incoming bits are scrambled so that the longest consequent zeros or ones would be less than 8 bits. Further assume a 3-bit counter as the timer. The local oscillator runs at nominal 40 GHz, which is the same clock rate that generates the incoming data. The clocks are assumed to be at least Stratum-3/3E compatible, therefore ensuring long term frequency accuracy. In real operation, a clock recovery based on high-Q filters can always be used to track any long term frequency drift between incoming data and local clock. However, benefiting from the frequency accuracy of Stratum-3/3E or higher tier clocks, receiving

the burst-mode allows the receiver to start receiving with the first bit without the need to recover any clock signal. Again, take the example of input bit sequence as (10010111) and assume when the first bit 1 triggers S&H, the timer yields a random time stamp (010). As illustrated from Fig. 4, the subsequent time stamps for incoming pulses are (101),(111),(000), and (001). This indicates the bit slots for ones starting from bit slot No.2 are 2, 5, 7, 8, 9 and the recovered bit sequence is therefore (10010111). It can be seen that due to the operation of logical gates, the receiver can tolerate some large timing jitters.

The present invention of a receiver scheme for synchronous digital transmission is based on fast logical gate operations. The scheme can tolerate uniformly distributed jitter within 50% of the bit period. The scheme can recover burst-mode bit sequences on the first bit. For short data packets, the proposed receiving scheme does not need the recovered clock. Recovered clock is only helpful to track the possible long-term frequency drift between transmitter and receiver clocks. In addition, since the operation of proposed receiver only requires logical gate operations, with all optical implementations of logical gates, the proposed receiver scheme can also be implemented all optically.

While the foregoing is directed to various embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof. As such, the appropriate scope of the invention is to be determined according to the claims, which follow.

What is claimed is

1. A digital receiver for receiving digital information transmitted in an input pulse train, comprising:

a counter for providing a sequence of time stamps to a sample and hold circuit;

the sample and hold circuit for sequentially holding a time stamp from the sequence of time stamps, wherein each pulse from the input pulse train allows the corresponding time stamp to be stored in a buffer; and

a processor for determining the digital information by analyzing the time stamps stored in the buffer.

2. The receiver of claim 1, further comprising a local clock communicably coupled to the counter.

3. The receiver of claim 1, further comprising optical logic gates adapted to process an optical pulse train.

4. The receiver of claim 1, further comprises electrical logic gates adapted to processes an electrical pulse train.

5. The receiver of claim 1, wherein the controller determines the binary value of a time slot by the time stamp and the digital transmission rate.

6. The method of claim 7, wherein each time slot includes a time slot number N which is determined by $N=t_n/T$, where t_n is the arrival time of the n^{th} pulse and 1/T is the digital transmission rate.

\7. A method for recovering data from a sequence of received pulses, comprising:

recording the arrival times of at least two pulses within said received pulses;

storing the arrival time of each pulse in a buffer;

determining from the arrival times a temporal relationship of the at least two pulses; and

assigning a binary value to a time slot determined by the temporal relationship of the pulses.

8. The method of claim 7, wherein the determining and assigning steps further comprises:

extracting from the buffer a first arrival time associated with the first of the at least two pulses;

determining a first time slot number using the first arrival time;

assigning a logical "1" to the time slot associated with the first time slot number;

extracting from the buffer a second arrival time associated with the second of the at least two pulses;

determining a second time slot number using the second arrival time;

assigning a logical "1" to the time slot associated with a second time slot number; and

assigning a logical "0" to each time slot temporally positioned between the first and second time slots, the time slots having been assigned a logical "1" representing time slots associated with a valid input pulse.

9. The method of claim 7, wherein each time slot includes a time slot number N which is determined by $N=t_n/T$, where t_n is the arrival time of the n^{th} pulse and 1/T is the digital transmission rate.

10. An apparatus for improving tolerance of input signal timing jitter, comprising:

means for recording the arrival times of at least two pulses within said input signal;

means for storing the arrival time of each pulse in a buffer;

means for determining from the stored arrival times a temporal relationship of the at least two pulses; and

means for assigning a binary value to a time slot determined by the temporal relationship of the pulses.

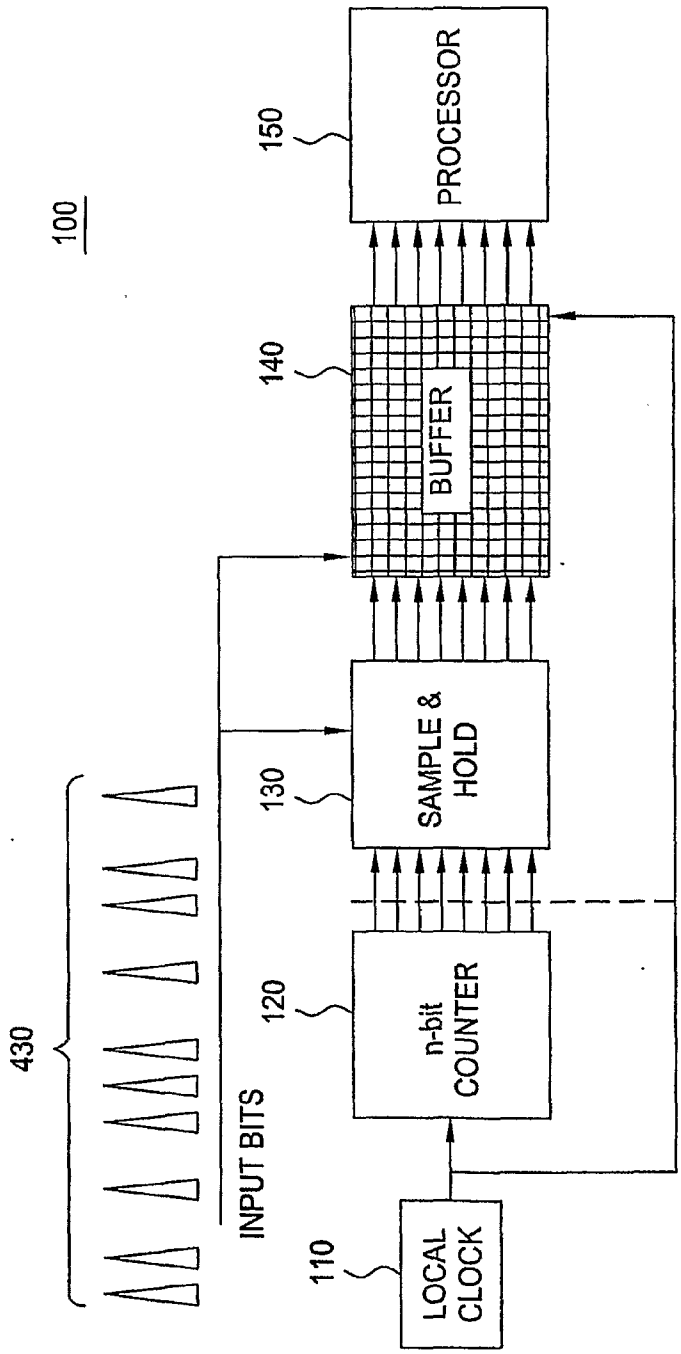
100
150
PROCESSOR
140
BUFFER
130
SAMPLE & HOLD
120
n-bit COUNTER
110
LOCAL CLOCK
INPUT BITS
430

FIG. 1

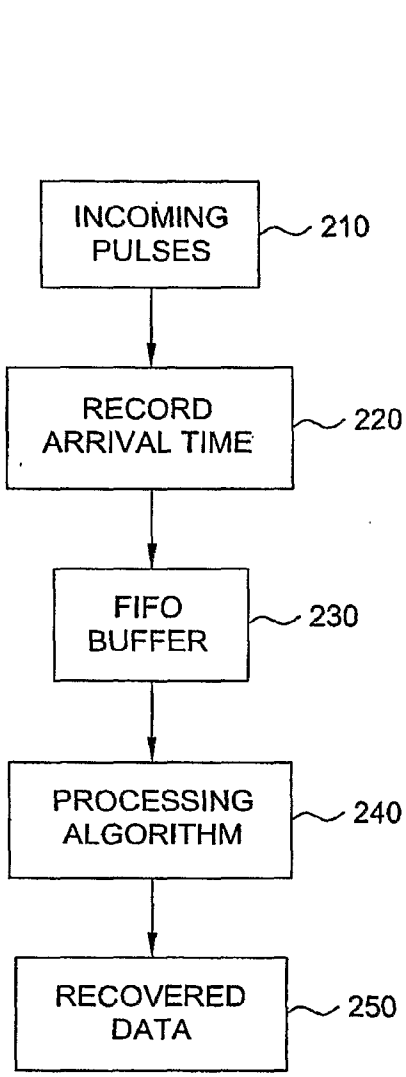
200
INCOMING PULSES
210
RECORD ARRIVAL TIME
220
FIFO BUFFER
230
PROCESSING ALGORITHM
240
RECOVERED DATA
250

FIG. 2

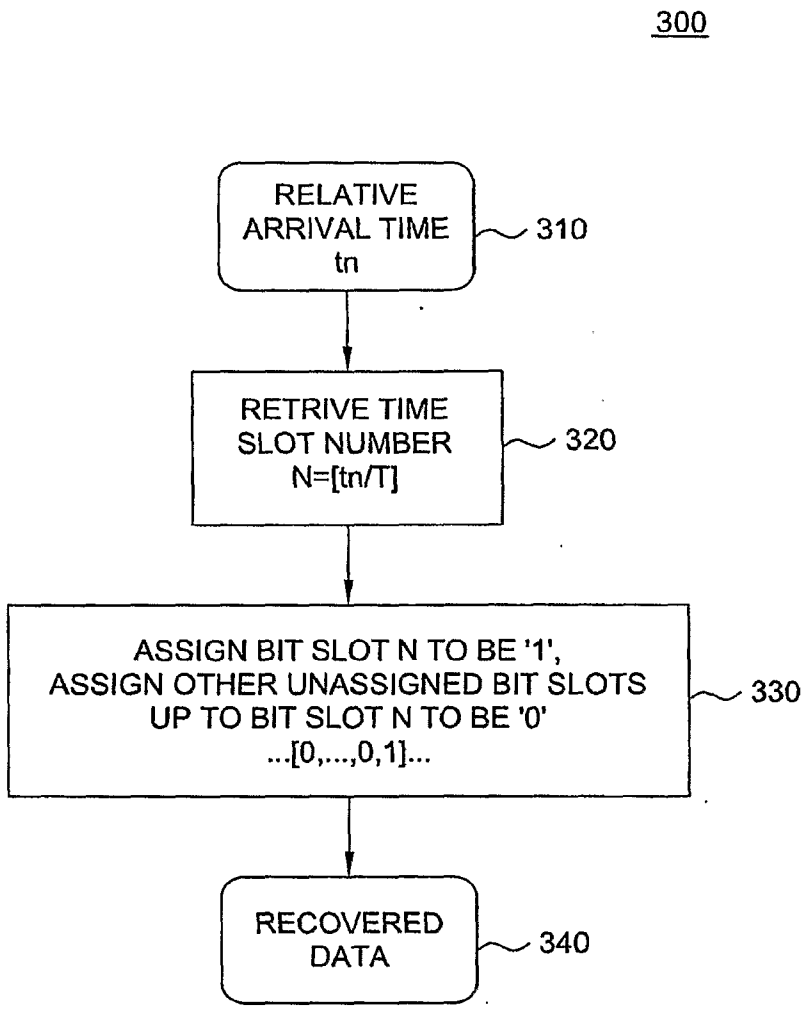
300
RELATIVE ARRIVAL TIME tn
310
RETRIVE TIME SLOT NUMBER N=[tn/T]
320
ASSIGN BIT SLOT N TO BE '1', ASSIGN OTHER UNASSIGNED BIT SLOTS UP TO BIT SLOT N TO BE '0' ...[0,...,0,1]...
330
RECOVERED DATA
340

FIG. 3

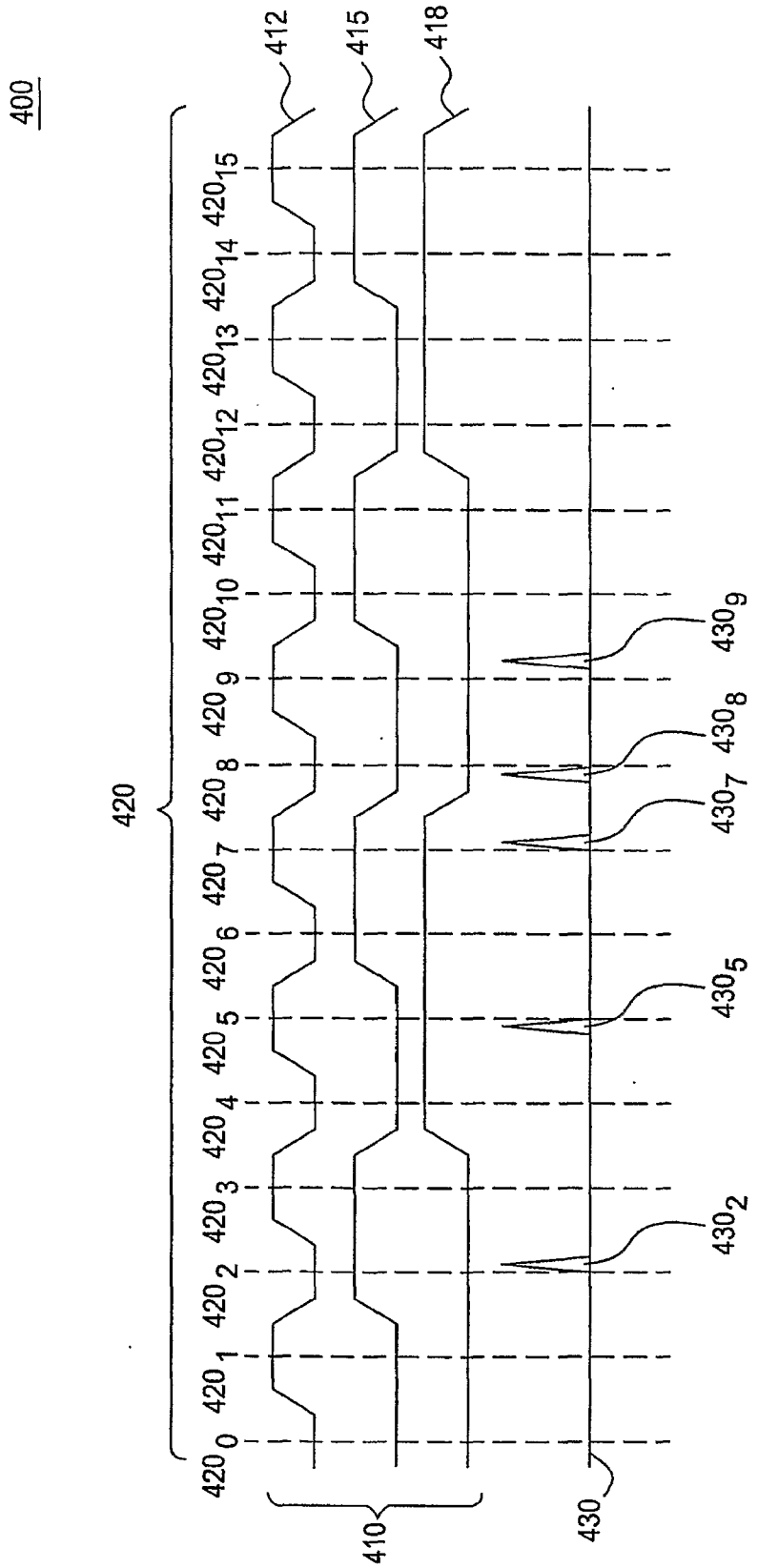
400
420
420_0
420_1
420_2
420_3
420_4
420_5
420_6
420_7
420_8
420_9
420_{10}
420_{11}
420_{12}
420_{13}
420_{14}
420_{15}
410
412
415
418
430
430_2
430_5
430_7
430_8
430_9

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/004855

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L7/033

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L G01R G01S H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/264612 A1 (ALLEN DANIEL J [US]) 30 December 2004 (2004-12-30) abstract paragraph [0005] paragraph [0020] paragraph [0023] - paragraph [0024] paragraph [0054] paragraph [0056] paragraph [0059]	1-4
A	EP 0 452 023 A2 (RAYTHEON CO [US]) 16 October 1991 (1991-10-16) page 3, line 40 - line 42 page 4, line 7 - line 28	1,7,10

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 July 2007	09/07/2007

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/004855

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 04 260248 A (NIPPON TELEGRAPH & TELEPHONE; IWATSU ELECTRIC CO LTD) 16 September 1992 (1992-09-16) abstract	1,7,10
A	US 5 121 413 A (VOEGTLY CARL H [US] ET AL) 9 June 1992 (1992-06-09) column 2, line 7 - line 14	1,7,10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/004855

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004264612 A1	30-12-2004	NONE	
EP 0452023 A2	16-10-1991	US 5091917 A	25-02-1992
JP 4260248 A	16-09-1992	NONE	
US 5121413 A	09-06-1992	NONE	