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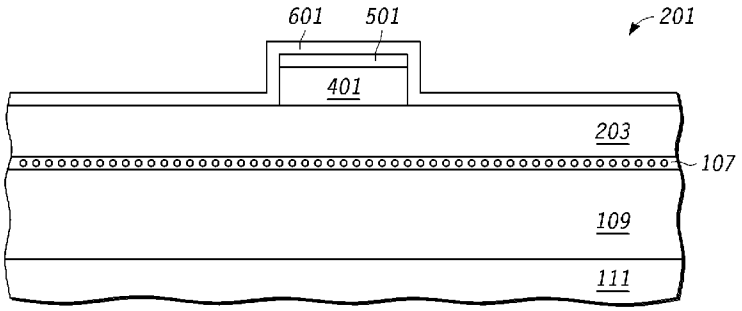
(54) **Title:** BACK-GATED SEMICONDUCTOR DEVICE WITH A STORAGE LAYER AND METHODS FOR FORMING THEREOF



(57) **Abstract:** A method of making a semiconductor device includes providing a first wafer (103) and providing a second wafer (101) having a first side and a second side, the second wafer (101) including a semiconductor substrate (105), a storage layer (107), and a layer of gate material (105). The storage layer (107) may be located between the semiconductor structure (105) and the layer of the gate material (105) and the storage layer (107) may be located closer to the first side of the second wafer (101) than the semiconductor structure (105). The method further includes boding the first side of the second wafer (101) to the first wafer (103). The method further includes removing a first portion of the semiconductor structure (105) to leave a layer of the semiconductor structure (105) after the bonding. The method further includes forming a transistor having a channel region (203), wherein at least a portion of the channel region (203) is formed from the layer of the semiconductor structure.

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BACK-GATED SEMICONDUCTOR DEVICE WITH A STORAGE LAYER AND METHODS FOR FORMING THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates in general to semiconductor devices and more specifically to a back-gated semiconductor device with a storage layer and methods for forming thereof.

Description of the Related Art

[0002] Traditional single gate and double gate Fully Depleted Semiconductor-on-Insulator (FDSOI) transistors have advantages related to reduced short channel effects and reduced un-wanted parasitic capacitances. However, when used as a non-volatile memory these transistors require programming, such as hot carrier injection (HCI) programming. HCI programming results in generation of holes because of impact ionization. Because of the floating nature of the body in such FDSOI devices, however, holes generated due to impact ionization may accumulate in the body of such FDSOI devices. Accumulated holes may then generate enough potential to cause problems, such as snap-back of the FDSOI devices.

[0003] Thus, there is a need for improved FDSOI transistors and methods of forming thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0005] Figure 1 is a side view of one embodiment of two wafers being bonded together to form a resultant wafer, consistent with one embodiment of the invention;

[0006] Figure 2 shows a side view of one embodiment of a bonded wafer, consistent with one embodiment of the invention;

[0007] Figure 3 shows a partial cross-sectional side view of one embodiment of a wafer during a stage in its manufacture, consistent with one embodiment of the invention;

[0008] Figure 4 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0009] Figure 5 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0010] Figure 6 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0011] Figure 7 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0012] Figure 8 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0013] Figure 9 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0014] Figure 10 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0015] Figure 11 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0016] Figure 12 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0017] Figure 13 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention;

[0018] Figure 14 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention; and

[0019] Figure 15 shows a partial cross-sectional side view of one embodiment of a wafer during another stage in its manufacture, consistent with one embodiment of the invention.

[0020] Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

DETAILED DESCRIPTION

[0021] The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

[0022] A back-gated non-volatile memory (NVM) device with its channel available for contacting to overcome the typical problem of charge accumulation associated with NVMs in semiconductor on insulator (SOI) substrates is provided. A substrate supports the gate. A storage layer is formed on the gate, which may be nanocrystals encapsulated in an insulating layer, but could be of another type such as nitride. A channel is formed on the storage layer. A conductive region, which can be conveniently contacted, is formed on the channel. This results in an escape path for minority carriers that are generated during programming, thereby avoiding charge accumulation in or near the channel. This is achievable with a method that includes bonding two wafers, cleaving away most of one of the wafers, forming the conductive region after the cleaving, and epitaxially growing the source/drains laterally from the channel while the conductive region is isolated from this growth with a sidewall spacer.

[0023] Figure 1 shows a side view of two wafers 101 and 103 that are to be bonded together to form a resultant wafer (201 of Figure 2), from which non-volatile memory cells may be formed, for example. Wafer 101 includes a layer 109 of gate material, a storage layer 107, and semiconductor substrate 105. By way of example, substrate 105 is made of monocrystaline silicon, but in other embodiments, may be made of other types of semiconductor materials such as silicon carbon, silicon germanium, germanium, type III-V semiconductor materials, type II-VI semiconductor materials, and combinations thereof including multiple layers of different semiconductor materials. In some embodiments, semiconductor material of substrate 105 may be strained. Storage layer 107 may be a thin

film storage layer or stack and may be made of any suitable material, such as nitrides or nanocrystals. Nanocrystals, such as metal nanocrystals, semiconductor (e.g., silicon, germanium, gallium arsenide) nanocrystals, or a combination thereof may be used. Storage layer 107 may be formed by a chemical vapor deposition process, a sputtering process, or another suitable deposition process.

[0024] Referring still to Figure 1, by way of example, layer 109 includes doped polysilicon, but may be made of other materials such as, amorphous silicon, tungsten, tungsten silicon, germanium, amorphous germanium, titanium, titanium nitride, titanium silicon, titanium silicon nitride, tantalum, tantalum silicon, tantalum silicon nitride, other silicide materials, other metals, or combinations thereof including multiple layers of different conductive materials. An insulator 111 may be formed (e.g., grown or deposited) on layer 109. In one embodiment, insulator 111 includes silicon oxide, but may include other materials such as e.g. PSG, FSG, silicon nitride, and/or other types of dielectric including high thermal, conductive dielectric materials.

[0025] Wafer 103 may include a substrate 115 (e.g., silicon) with an insulator 113 formed on it. In one embodiment, the material of insulator 113 is the same as the material of insulator 111. By way of example, wafer 103 includes a metal layer (not shown) at a location in the middle of insulator 113. This metal layer may be utilized for noise reduction in analog devices built from resultant wafer 201.

[0026] Wafer 101 is shown inverted so as to be bonded to wafer 103 in the orientation shown in Figure 1. In one embodiment, insulator 111 is bonded to insulator 113 with a bonding material. In other embodiments, wafer 101 may be bonded to wafer 103 using other bonding techniques. For example, in one embodiment, wafer 101 may be bonded to wafer 103 by electrostatic bonding followed by thermal bonding or pressure bonding.

[0027] In some embodiments, wafer 101 does not include insulator 111 where layer 109 is bonded to insulator 113. In other embodiments, wafer 103 does not include insulator 113 where insulator 111 is bonded to substrate 115.

[0028] Wafer 101 may include a stress layer 106 formed by implanting a dopant (e.g. H+) into substrate 105. In some embodiments, the dopant is implanted prior to the formation of storage layer 107, but in other embodiments, may be implanted at other times including after

the formation of storage layer 107 and prior to the formation of layer 109, after the formation of layer 109 and prior to the formation of insulator 111, or after the formation of insulator 111. In other embodiments, the dopant for forming stress layer 106 may be implanted after wafer 103 has been bonded to wafer 101.

[0029] Figure 2 shows a side view of resultant wafer 201 after wafer 103 and 101 have been bonded together. The view in Figure 2 also shows wafer 201 after a top portion of substrate 105 has been removed, e.g., by cleaving. By way of example, cleaving is performed by dividing substrate 105 at stress layer 106. Layer 203 is the remaining portion of substrate 105 after the cleaving. One advantage of forming the layer by cleaving is that it may allow for a channel region to be formed from a relatively pure and crystalline structure as opposed to a semiconductor layer that is grown or deposited on a dielectric.

[0030] Figure 3 shows a partial side cross-sectional view of wafer 201. Not shown in the view of Figure 3 (or in subsequent Figures) are insulator 113 and substrate 115. After substrate 105 is cleaved to form layer 203, an oxide layer 303 is formed over layer 203. Layer 303 may be thicker than layer 203. Next, as shown in Figure 4, a layer of polysilicon, to form conductive region 401, may be deposited over oxide layer 303 after a middle portion of oxide layer 303 is patterned and then etched away. Thus, polysilicon layer is deposited directly on the transistor channel. The polysilicon layer may be doped in-situ or doped by implantation. Appropriate doping materials may be used depending on the type of device being manufactured. Conductive region 401 may be used as a well contact. If necessary, an appropriate pre-clean may be performed to remove any interfacial oxide layer. Conductive region 401 may remove minority carriers, such as holes from the channel region 203 of a transistor formed from wafer 201.

[0031] Next, as shown in Figure 5, polysilicon layer forming conductive region 401 may be planarized by chemical-mechanical polishing, for example. Furthermore, a portion from top part of polysilicon layer forming conductive region 401 may be etched and a nitride cap 501 may be formed on top of conductive region 401. In one embodiment, nitride cap 501 should be at least as thick as layer 203 so that nitride cap 501 may serve as an implant mask during implantation described with respect to Figure 7. This would ensure the doping of layer 401 is unaltered during implantation. Referring now to Figure 6, a liner 601, such as an oxide liner may be formed after oxide layer 303 is removed.

[0032] Next, as shown in Figure 7, two implants 701 may be performed. First, amorphization implants may be performed in portions 707/709. By way of example, germanium may be used to perform amorphization implants. Second, source/drain implants may be performed in portions 703/705 to form source/drain extensions. Appropriate n-type or p-type dopants may be used as part of this step. The region (203) under conductive region 401 may serve as a channel region. Referring now to Figure 8, a spacer 801 may be formed on the sidewalls of conductive region 401 (lined by liner 601). Spacer 801 may be made of multiple layers of dielectric materials. Spacer 801 may protect certain portions of portions 703/705 during subsequent processing. Next, exposed portions of portions 703/705 may be etched away.

[0033] Next, as shown in Figure 9, a second spacer 901 may be formed to protect sidewalls of portions 703/705. Furthermore, portions 707/709 implanted with amorphization implants may be etched away. Referring now to Figure 10, an oxide layer 1001 may be deposited on wafer 201. Next, as shown in Figure 11, selected portions of oxide layer 1001 may be etched away. Etching of selected portions of oxide layer 1001 may result in partial etching of liner 601, as well. Figure 12 shows a partial cross-sectional side view of wafer 201 after structures 1201 and 1203 are epitaxially grown on the exposed sidewalls of channel region (including portion 203).

[0034] Referring to Figure 13 now, an amorphous silicon layer 1301/1303 may be deposited. Amorphous silicon layer 1301/1303 may be subjected to chemical mechanical polishing and etched back. Next, as shown in Figure 14, a photoresist layer 1401 may be formed on top of a selected portion of wafer 201 and source/drain implants 1403 may be made forming doped source/drain regions 1405 and 1411. Next, as shown in Figure 15, silicides 1501, 1503, and 1505 may be formed after nitride cap 501 is stripped. Gate silicide 1503 may be formed on top of conductive region 401. By way of example, silicides may be formed using a silicide implantation (e.g., cobalt or nickel) followed by a heat treatment. Alternatively, silicides may be formed by depositing a layer of metal over the wafer and reacting the metal with the underlying material.

[0035] By way of example, the semiconductor device formed on wafer 201 may be used as a non-volatile memory. The non-volatile memory may include cells formed of the semiconductor device, which may be programmed using techniques such as, hot carrier

injection. For example, using HCI, one bit per cell may be stored in storage layer 107 by applying a positive bias voltage to gate 109, applying a positive voltage to drain region 1411, grounding source region 1405, and applying a negative voltage to conductive region 401 or grounding conductive region 401. HCI programming may result in generation of minority carriers, such as holes because of impact ionization. Conductive region 401 may provide an escape path for holes thereby preventing accumulation of holes in channel region 203.

[0036] In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

[0037] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS:

What is claimed is:

1. A method of making a semiconductor device, comprising:
providing a first wafer;
providing a second wafer having a first side and a second side, the second wafer including a semiconductor structure, a storage layer, and a layer of gate material, the storage layer is located between the semiconductor structure and the layer of gate material, the storage layer is located closer to the first side of the second wafer than the semiconductor structure;
bonding the first side of the second wafer to the first wafer;
removing a first portion of the semiconductor structure to leave a layer of the semiconductor structure after the bonding; and
forming a transistor having a channel region, wherein at least a portion of the channel region is formed from the layer of the semiconductor structure.

2. The method of claim 1, wherein forming the transistor is further characterized as forming a conductive region adjoining the channel region for use as a well contact.

3. The method of claim 2, wherein forming the conductive region comprises:
forming a sacrificial layer on the channel region;
patterning the sacrificial layer to form an opening to the channel region;
depositing a doped semiconductor material to fill the opening;
removing the doped semiconductor material around the opening; and
removing the sacrificial layer to leave the conductive region.

4. The method of claim 3, wherein forming the transistor is further characterized as epitaxially growing semiconductor regions adjacent to the channel for use as source/drains of the transistor.

5. The method of claim 4, wherein forming the transistor is further characterized as converting areas of the gate material adjacent to the channel region to being amorphous areas and etching the amorphous areas to leave a gate of the transistor.

6. The method of claim 5, wherein the converting areas of the gate material further comprises implanting the areas of gate material adjacent to the channel region.

7. A semiconductor device structure, comprising:

a substrate;

a gate over the substrate;

a storage layer over the gate;

a channel region over the storage layer;

source/drain regions laterally adjacent to the channel; and

a conductive region over and in direct contact with the channel region and overlapping the channel region.

8. The semiconductor device of claim 7, wherein the storage layer comprises nanocrystals.

9. The semiconductor device of claim 7 further comprising a sidewall spacer laterally adjacent to the conductive region.

10. The semiconductor device of claim 7, wherein the conductive region comprises means for a well contact.

11. The semiconductor device of claim 7, wherein the conductive region comprises polysilicon and the channel region comprises monocrystalline silicon.

12. The semiconductor device of claim 7 further comprising silicide layers on the gate and the source/drains.

13. The semiconductor device of claim 7, wherein the source/drain regions comprise monocrystalline regions adjacent to the channel and polysilicon regions adjacent to the monocrystalline regions.

14. A non-volatile memory cell, comprising:
    a substrate;
    a control gate on the substrate;
    a storage layer on the control gate;
    a monocrystalline channel region on the storage layer; and
    a conductive region extending upward from the channel region for removing minority carriers from the channel.

15. The non-volatile memory cell of claim 14, wherein the conductive region is further characterized as being polycrystalline.

16. The non-volatile memory cell of claim 14, wherein the control gate comprises polysilicon.

17. The non-volatile memory cell of claim 14, wherein the storage layer comprises nanocrystals.

18. The non-volatile memory cell of claim 14 further comprising:
    a drain on a first side of the channel; and
    a source on a second side of the channel, wherein the source and drain are monocrystalline adjacent to the channel.

19. The non-volatile memory of claim 14, further comprising a first silicide layer on a portion of the source, a second silicide layer on a portion of the drain, and a third silicide layer on a portion of the conductive region.

20. The non-volatile memory cell of claim 14 further comprising a sidewall spacer adjacent to a side of the conductive region.

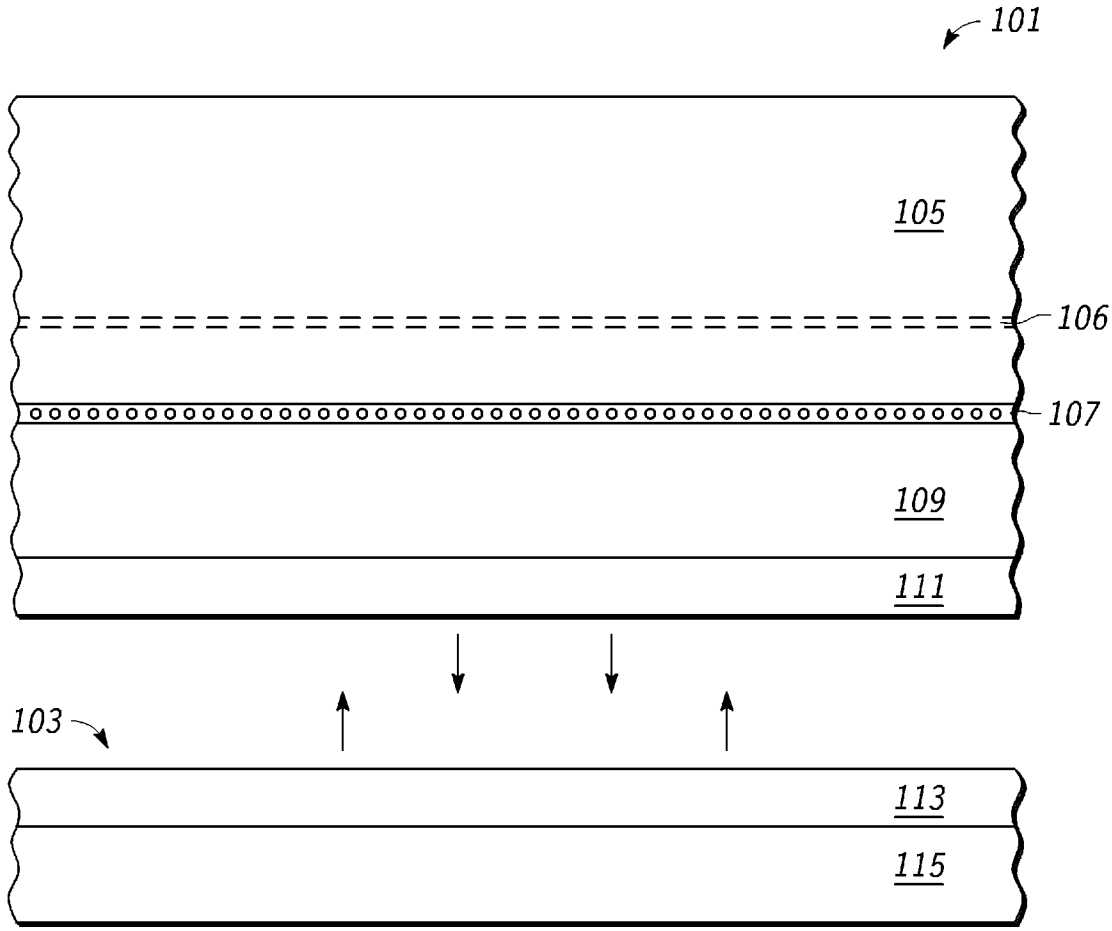

FIG. 1

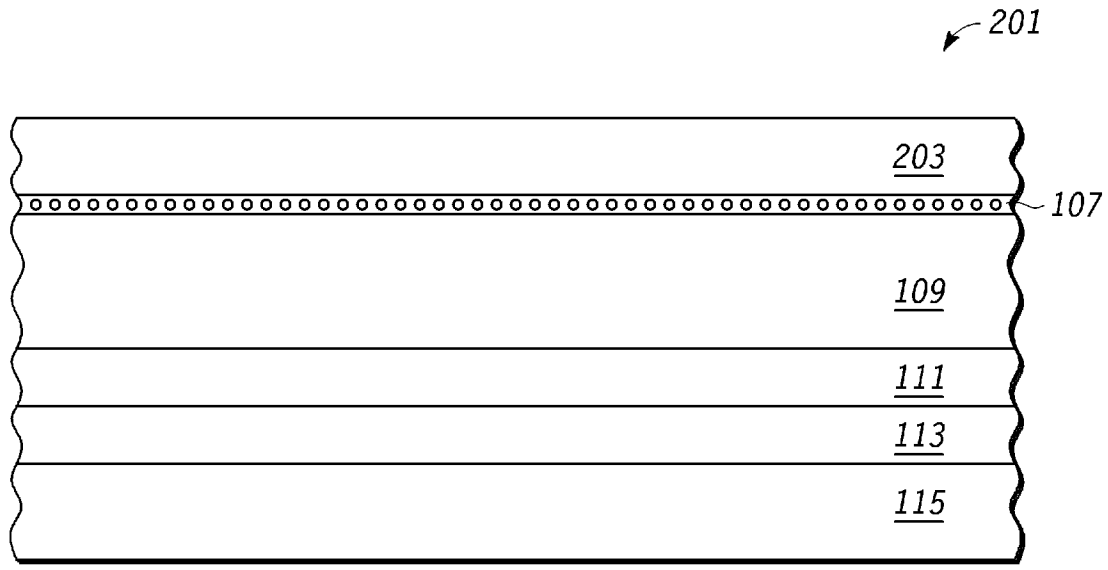

FIG. 2

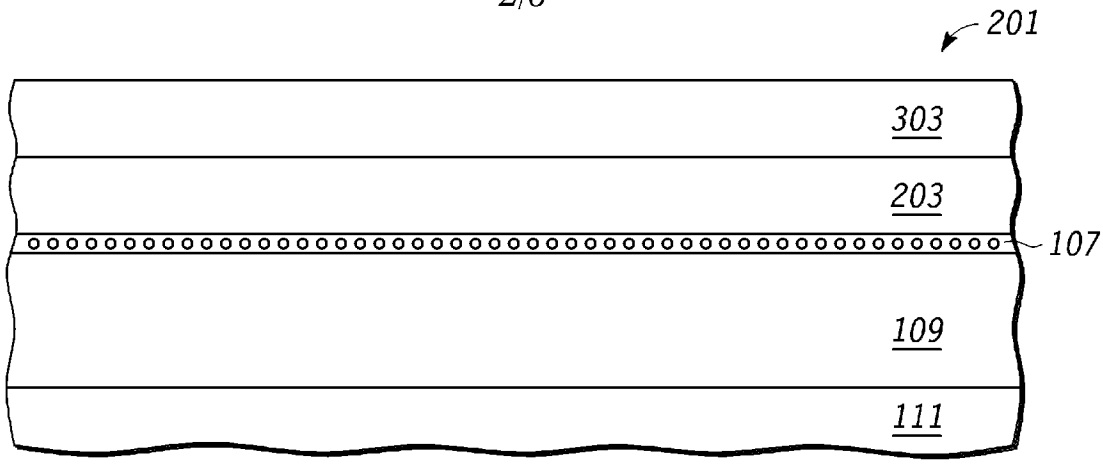

FIG. 3

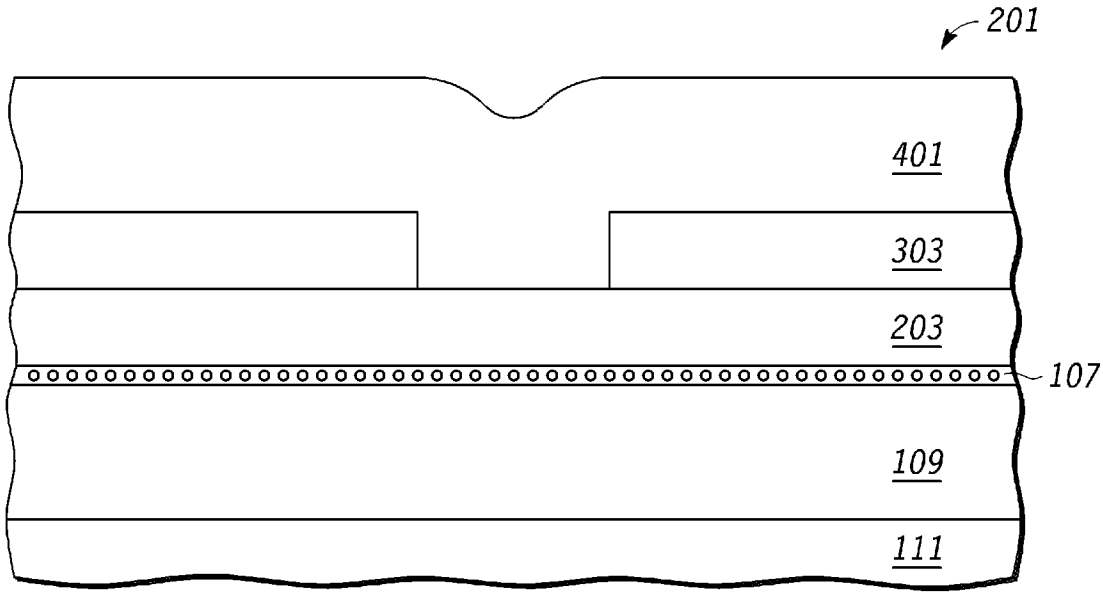

FIG. 4

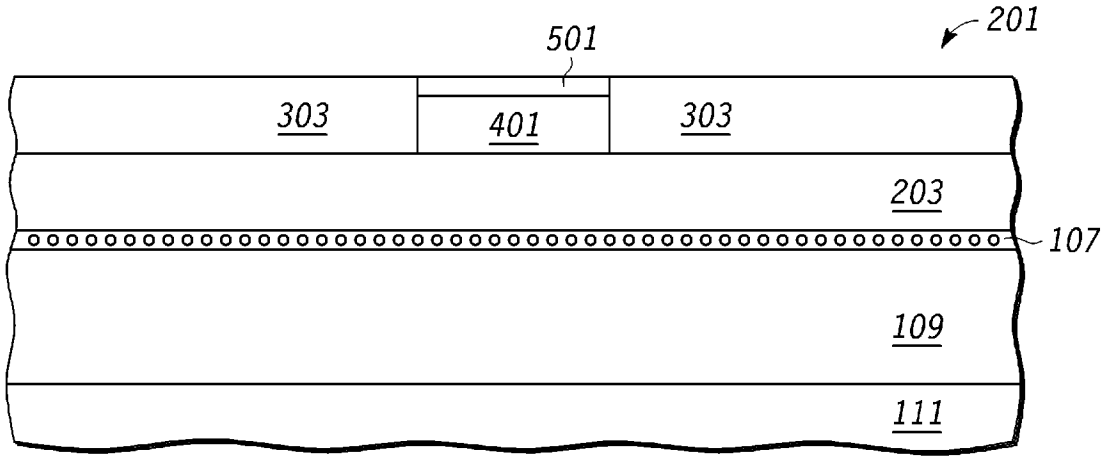

FIG. 5

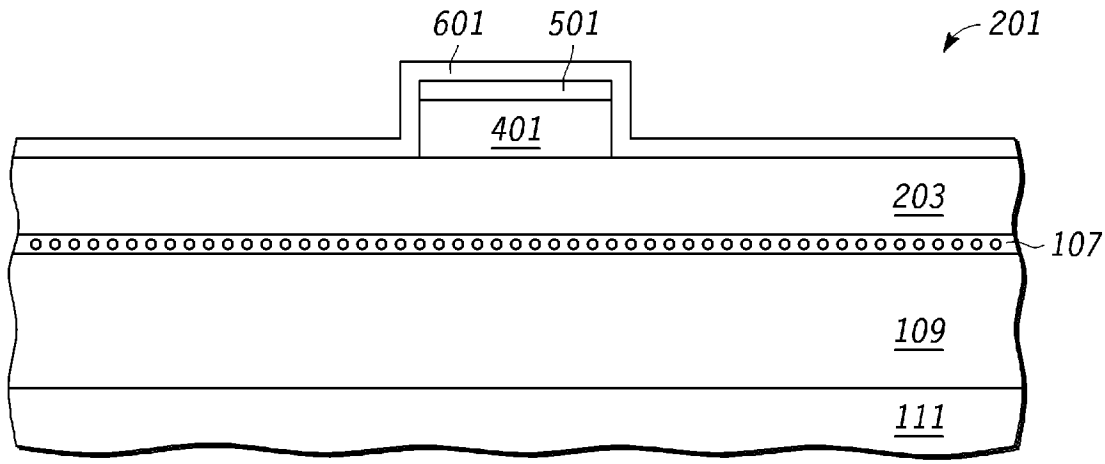

FIG. 6

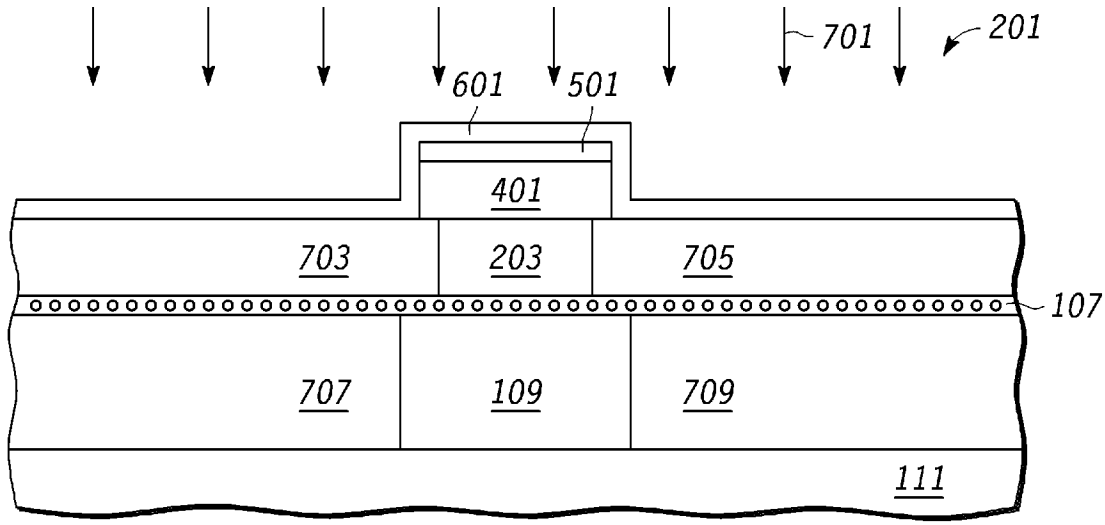

FIG. 7

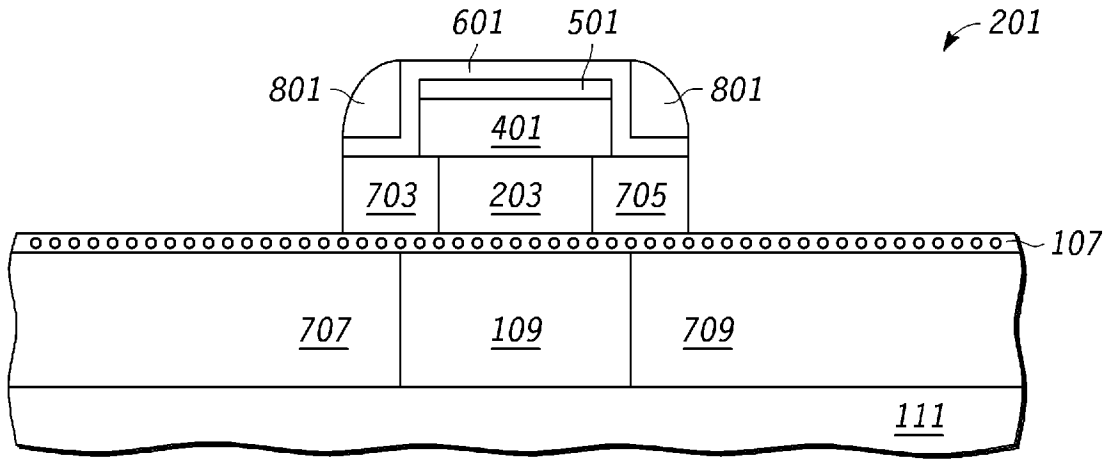

FIG. 8

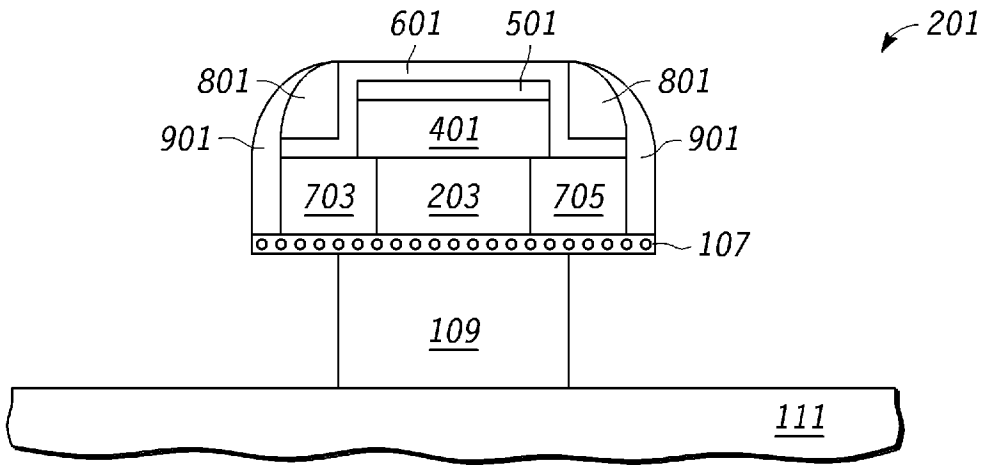

FIG. 9

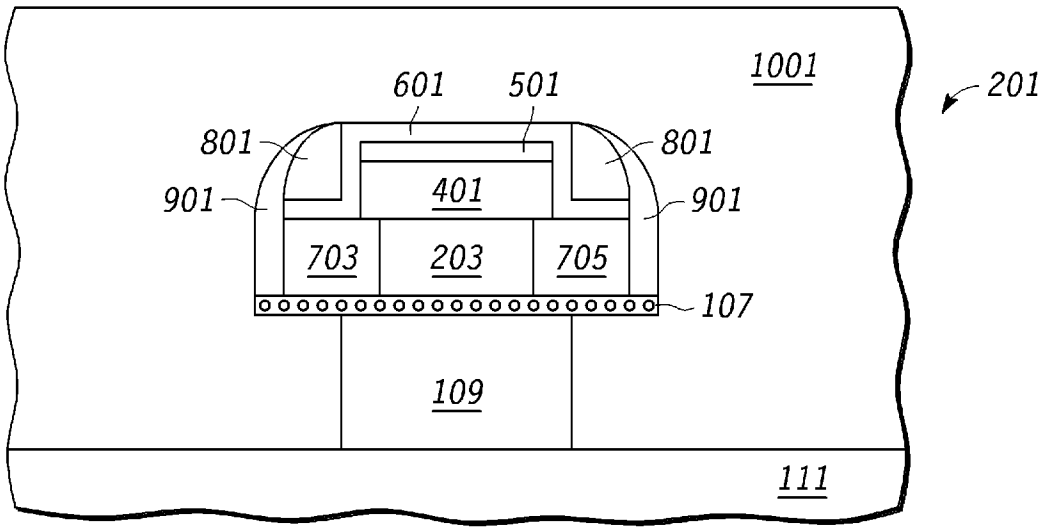

FIG. 10

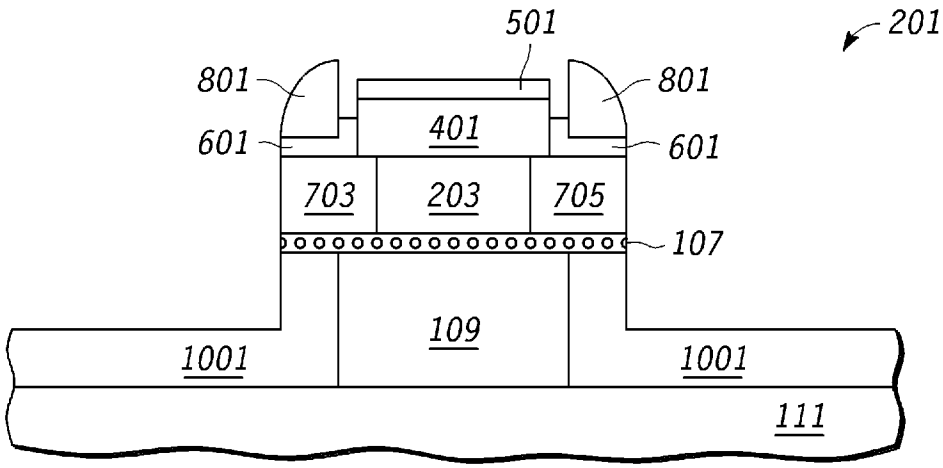

FIG. 11

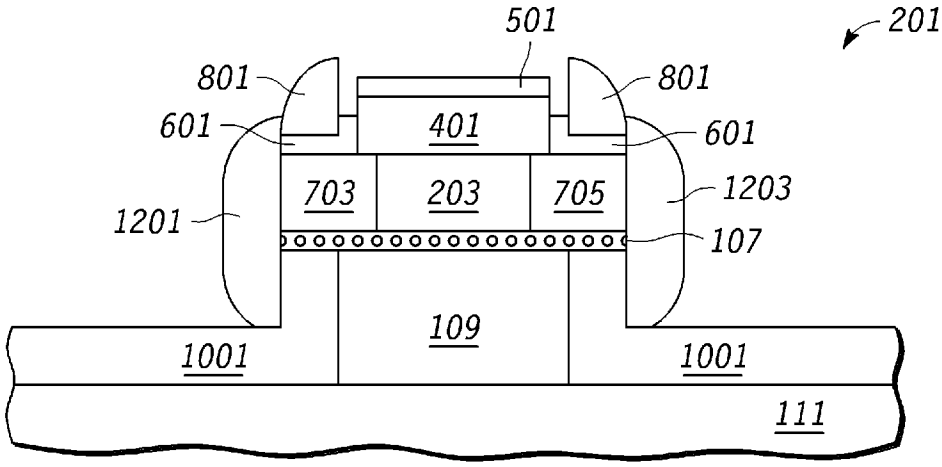

FIG. 12

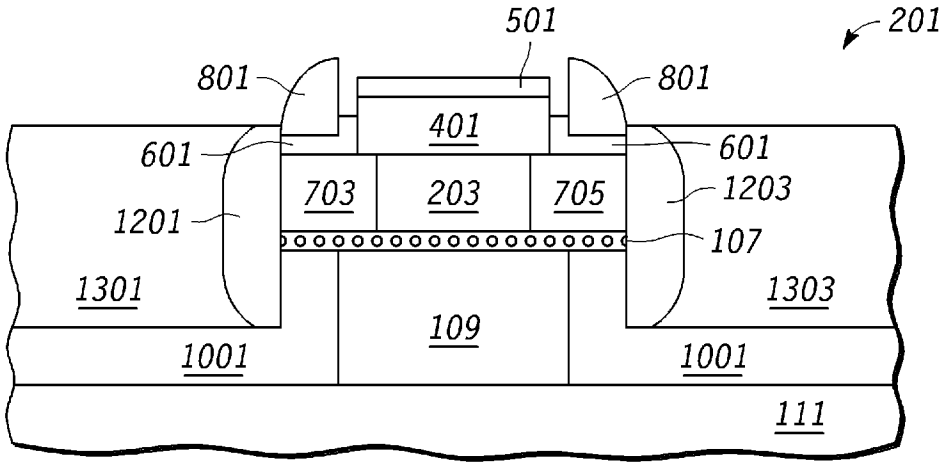

FIG. 13

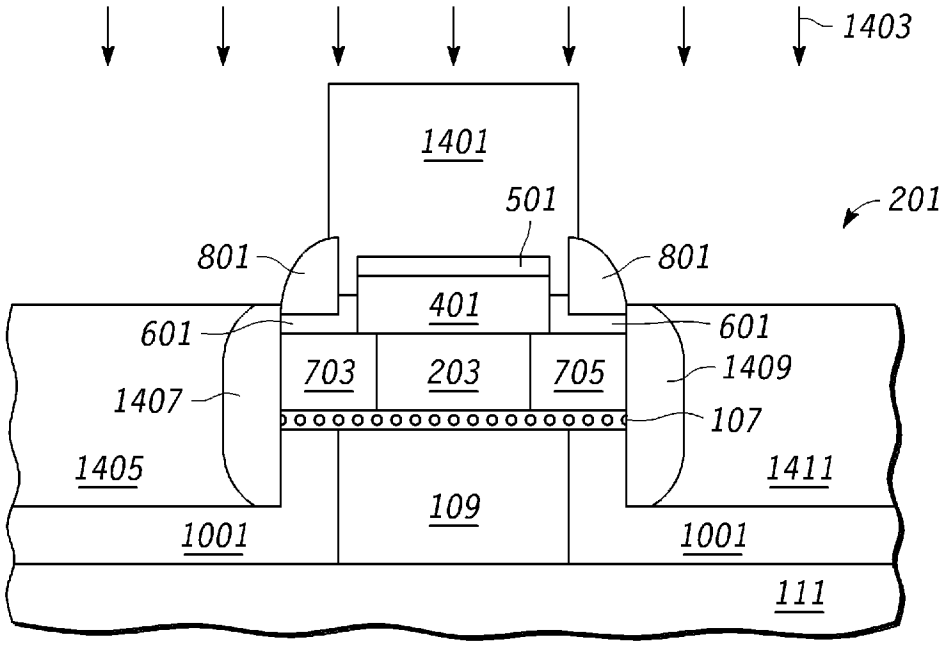

FIG. 14

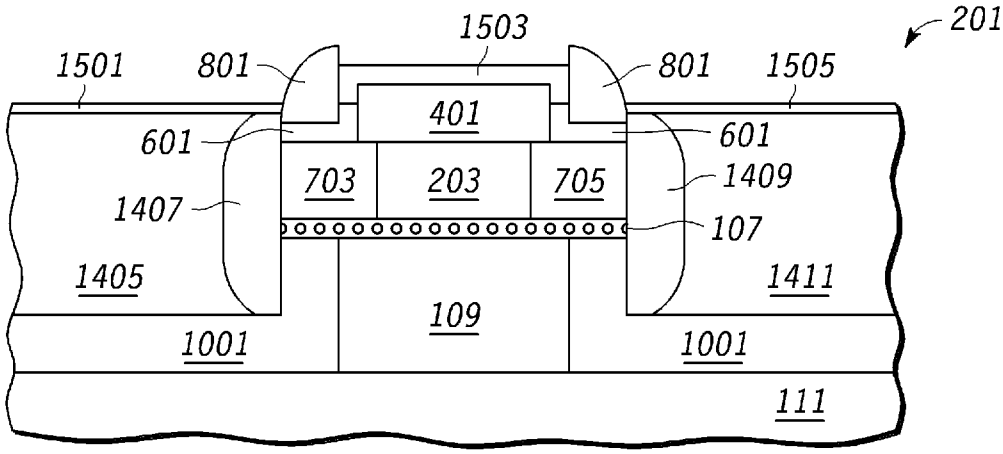
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FIG. 15