(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 June 2017 (29.06.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/111840 A1

(51) International Patent Classification:
H01L 23/12 (2006.01) *H01L 23/48* (2006.01)

(21) International Application Number:
PCT/US2015/000398

(22) International Filing Date:
26 December 2015 (26.12.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95054 (US).

(72) Inventors; and

(71) Applicants : **SANKMAN, Robert, L.** [US/US]; 13202 South 34th Way, Phoenix, AZ 85044 (US). **ELSHERBINI, Adel, A.** [EG/US]; C5-1-H2, 5000 West Chandler Boulevard, Chandler, AZ 85226 (US).

(74) Agents: **VAN NESS, Mark, C.** et al.; Blakely Sokoloff Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, CA 94085 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: CONDUCTIVE BASE EMBEDDED INTERCONNECT

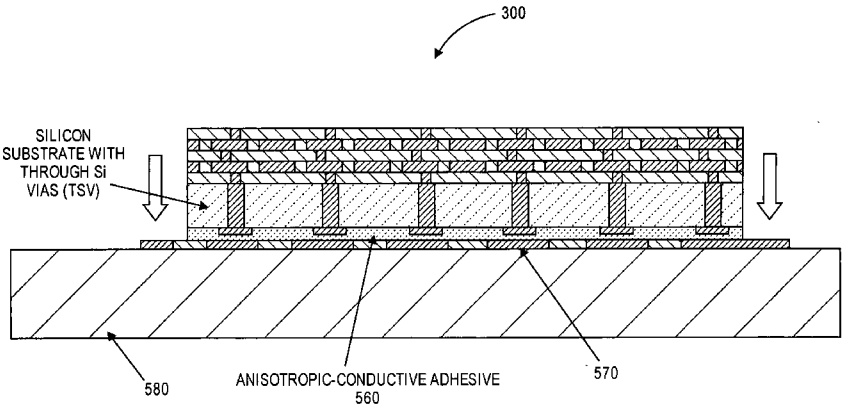

FIG. 5

(57) Abstract: Embodiments are generally directed to a conductive base embedded interconnect. An embodiment of an apparatus includes a substrate; an embedded interconnect layer in a first side of the substrate, the embedded interconnect layer including a plurality of contacts; and one or more conductive paths through the substrate, the one or more conductive paths being connected with the embedded interconnect layers.

WO 2017/111840 A1

CONDUCTIVE BASE EMBEDDED INTERCONNECT

TECHNICAL FIELD

[0001] Embodiments described herein generally relate to the field of electronic devices and, more particularly, to a conductive base embedded interconnect.

BACKGROUND

[0002] In the fabrication of electronic devices, the interfaces of devices with other devices become more complex as the device structure increases. One structure that is utilized to provide an in-package high density interconnect of chips is the Embedded Multi-Die Interconnect Bridge (EMIB) of Intel Corporation.

[0003] However, the use of such an embedded interconnect can be enhanced by providing power through the bridge via vertical connections. For example, a current interconnect bridge structure has horizontal wires supplying power to contact bumps, such as to provide power to a die that is above the bridge. The interconnect bridge structure does not include a vertical conduction path, and power to the bump contacts above the bridge is supplied laterally from outside the bridge. A vertical current path for power delivery offers an enhanced solution with a lower resistance and inductance than the lateral paths.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments described here are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

[0005] **Figure 1** is an illustration of a conductive base embedded interconnect according to an embodiment;

[0006] **Figure 2** is an illustration of an embedded multi-chip interconnect bridge (EMIB);

[0007] **Figures 3A-3F** illustrate fabrication of a conductive base interconnect bridge on a silicon substrate using through silicon via technology according to an embodiment;

[0008] **Figure 4A-4E** illustrate fabrication of a conductive base interconnect bridge on a conductive substrate according to an embodiment;

[0009] **Figure 5** illustrates coupling of a conductive base interconnect bridge on a silicon substrate using through silicon via technology with an organic substrate according to an embodiment;

[0010] **Figure 6** illustrates coupling of a conductive base interconnect bridge on a silicon substrate using through silicon via technology with an organic substrate according to an embodiment;

[0011] **Figure 7** is a flowchart to illustrate fabrication of a conductive path for an interconnect bridge on a silicon substrate using through silicon via technology according to an embodiment; and

[0012] **Figure 8** is a flowchart to illustrate fabrication of a conductive path for an interconnect bridge on a conductive substrate according to an embodiment.

DETAILED DESCRIPTION

[0013] Embodiments described herein are generally directed to conductive base embedded interconnect.

[0014] For the purposes of this description:

[0015] "Through silicon via" or "TSV" refers to a vertical (perpendicular to a surface) electrical connection (or via) that passes through a silicon wafer or die.

[0016] "Substrate" or "wafer" refers to a slice of a substance, including a slice of semiconductor material, such as silicon, used in electronics for the fabrication of integrated circuits and in photovoltaics for conventional, wafer-based solar cells.

[0017] "Embedded interconnects" means interconnects that are embedded within a substrate. Embedded interconnects include, but is not limited to, the Embedded Multi-Die Interconnect Bridge of Intel Corporation. An Embedded Multi-Die Interconnect Bridge is generally referred to as an EMIB or interconnect bridge herein

[0018] In some embodiments, an apparatus, system, or method includes a conductive base embedded interconnect. In some embodiments, an embedded interconnect, including but not limited to an EMIB, includes one or more conductive paths from below the embedded interconnect to a surface contact for the embedded interconnection. In some embodiments, a conductive path provides power via a conductive base that is formed below the embedded interconnect.

[0019] An EMIB provides a high density interconnect within a package for connection of chips, wherein EMIB includes a fine network of metal and dielectric layers, the layers being embedded below a surface of a substrate, with bump contacts above the metal and dielectric layers. However, certain of the bumps require a connection with a power supply.

[0020] However, a current EMIB solution lacks a vertical conduction path that originates from the organic substrate layers directly below the Interconnect Bridge, and then through the Interconnect Bridge to its top surface. To provide a connection to a power supply, power to the bumps above the interconnect bridge are supplied laterally from outside the bridge. This structure creates relatively long paths for power, with supply noise due to the inductance and resistance of these paths.

[0021] In some embodiments, a conduction base embedded interconnect bridge provides a conductive path from the organic substrate wires to the interconnect bridge and ultimately to the topside contacts. In some embodiments, a conductive path includes one of:

[0022] (1) A conductive path for the bridge including multiple through silicon vias (TSVs) and an electrical connection between the plurality of TSVs utilizing a conductive film, wherein the conductive film may include an anisotropic (directional dependent) conductive adhesive film. The connection utilizing the TSVs and conductive film provides a multiple independent current paths to the interconnect bridge.

[0023] (2) A conductive path for the bridge utilizing a conductive substrate, wherein the conductive path is connected via ohmic contacts and a conductive adhesive film. The connection utilizing the conductive substrate provides a single conductive path to the interconnect bridge.

[0024] The conductive paths for the bridge apply known technologies for chip packaging, which such technologies are applied to create a conductive path for an EMIB. In some embodiments, such technologies may be tailored for application in a conductive interconnect bridge by adjusting CTE (Coefficient of Thermal Expansion), Tg (Glass Transition Temperature relating to temperature at which material transitions between liquid and glassy state), and other key material properties. In some embodiments, material of a conductive substrate includes material with a CTE that is in or near the range of the CTE of silicon (CTE ~3 ppm/°C) (parts per million per degree Celsius) and an organic substrate (CTE ~15

ppm/°C). Materials may include, but are not limited to, copper (CTE ~3 ppm/°C), stainless steel (CTE ~10 to 17 ppm/°C), nickel (CTE ~13 ppm/°C), or other various metal alloys. However, embodiments are not limited to particular conductive substrate materials.

[0025] An ohmic contact is a non-rectifying junction, and herein refers to the ohmic contact of a metal to a semiconductor material. Ohmic contacts are also well understood in fields including semiconductor packaging.

[0026] In some embodiments, a conductive adhesive includes conductive particles (such as particles of metal) in the adhesive. In some embodiments, the conductive adhesive is anisotropic (directionally dependent), wherein pressure will cause the conductive particles in a direction of a force to make contact and create an electrical connections. However, particles in a different direction from the force will not be forced together and will not create an electrical connection. In this manner, multiple independent connections between TSVs and substrate wires may be made without inducing a short between the TSVs as the rest of the adhesive will act as an insulator.

[0027] **Figure 1** is an illustration of a conductive base embedded interconnect according to an embodiment. Figure 1 provides a general illustration of an embodiment, wherein more specific embodiments are illustrated in Figures 3A to 6.

[0028] In some embodiments, an apparatus may include an interconnect bridge structure coupled with substrate wires 140 of an organic substrate 150. In some embodiments, the bridge structure includes metal and dielectric layers embedded within a bridge substrate 120.

[0029] In some embodiments, an apparatus, system, or process provides for one or more conductive paths 130 through the bridge substrate 120. In some embodiments, the one or more conductive paths may include multiple conductive paths enabled with multiple through silicon vias, such as illustrated in Figures 3A to 3F. In some embodiments, the one or more conductive paths may include a single conductive path through a conductive substrate, such as illustrated in Figure 4A to 4E.

[0030] **Figure 2** is an illustration of an embedded multi-chip interconnect bridge (EMIB). In Figure 2, a EMIB 200 includes a silicon substrate 210; metal and dielectric layers 220 embedded in the substrate 210, the metal layers including

contacts on a surface of the substrate; and a backside adhesive 230 for coupling with a substrate below (which is not illustrated in Figure 2).

[0031] However, in a conventional structure, there is no conductive path through the substrate 210 to provide a connection between the metal layers 220 and wire connections of the attached substrate below.

[0032] **Figures 3A-3F** illustrate fabrication of a conductive base interconnect bridge on a silicon substrate using through silicon via technology according to an embodiment.

[0033] Figure 3A: A silicon wafer 310 is fabricated for a substrate of the interconnect bridge.

[0034] Figure 3B: Multiple through silicon vias 315 are formed in the silicon wafer 310, where the through silicon vias 315 may be formed by a means known by those of skill in the art.

[0035] Figure 3C: Processing of frontside layers, whereby metal and dielectric layers 320 are embedded in a top surface of the silicon wafer 310 to connect with the through silicon vias 315 and provide a conductive path to contacts on the surface of the silicon wafer 310.

[0036] Figure 3D: The silicon wafer 310 is processed (removing a layer of silicon) to reveal the through silicon vias 315.

[0037] Figure 3E: A backside RDL (redistribution layer) is attached to provide connection with the frontside layers 320 by way of the through silicon vias.

[0038] Figure 3F: A conductive adhesive 330 is attached to the backside of the silicon substrate 310, thereby generating the conductive base embedded interconnect 300. In some embodiments, the adhesive 330 is an anisotropic conductive adhesive containing conductive particles.

[0039] **Figure 4A-4E** illustrate fabrication of a conductive base interconnect bridge on a conductive substrate according to an embodiment.

[0040] Figure 4A: A carrier wafer 450 is provided for the fabrication of the interconnect bridge.

[0041] Figure 4B: A conductive bridge substrate 410 is bonded to the carrier 450.

[0042] Figure 4C: Processing of frontside layers, whereby metal and dielectric layers 420 are embedded in a top surface of the bridge substrate 410 to

provide ohmic contact between the metal layers of the frontside layers 420 and the conductive base.

[0043] Figure 4D: The bridge substrate 410 is de-bonded from the carrier wafer 450.

[0044] Figure 4E: A conductive adhesive 430 is attached to the backside of the bridge substrate 410, thereby generating the conductive base embedded interconnect 410.

[0045] **Figure 5** illustrates coupling of a conductive base interconnect bridge on a silicon substrate using through silicon via technology with an organic substrate according to an embodiment. In some embodiments, a conductive base interconnect bridge 300, such as illustrated in Figure 3F, is attached with a metal wire layer 570 in a cavity of an organic substrate 580 utilizing an anisotropic conductive adhesive 560. In some embodiments, the pressure applied in the attachment of the interconnect bridge 300 with the organic substrate 580 generates an electrical connection between an RDL layer of the conductive base interconnect bridge 300 and the wires of the wire layer 570 while maintaining insulation between the through silicon vias.

[0046] **Figure 6** illustrates coupling of a conductive base interconnect bridge on a silicon substrate using through silicon via technology with an organic substrate according to an embodiment. In some embodiments, a conductive base interconnect bridge 400, such as illustrated in Figure 4E, is attached with a metal wire layer 670 in a cavity of an organic substrate 680 utilizing a conductive adhesive 665. In some embodiments, the conductive adhesive 665 creates a conductive path from the wire layer 670 to the upper contacts of the interconnect bridge 400 utilizing the ohmic contact 590 between the frontside layer and conductive bridge substrate of the interconnect bridge 400.

[0047] **Figure 7** is a flowchart to illustrate fabrication of a conductive path for an interconnect bridge on a silicon substrate using through silicon via technology according to an embodiment. In some embodiments, a fabrication process 700 may include the following:

[0048] 704: Fabrication of a silicon wafer as a substrate for the interconnect bridge.

[0049] 706: Formation of multiple through silicon vias in the silicon wafer.

[0050] 708: Processing of frontside layers including embedding metal and dielectric layers in a top surface of the silicon wafer.

[0051] 710: Revealing the through silicon vias by processing of the silicon wafer.

[0052] 712: Forming a back side RDL (redistribution layer) on the silicon bridge substrate.

[0053] 714: Application of anisotropic conductive adhesive to backside of silicon bridge substrate.

[0054] 716: Coupling of silicon bridge substrate with organic substrate.

[0055] 718: Producing multiple conductive paths between interconnect bridge and organic substrate wires via the through the silicon vias, RDL, and conductive adhesive, while maintaining insulation between the through silicon vias.

[0056] **Figure 8** is a flowchart to illustrate fabrication of a conductive path for an interconnect bridge on a conductive substrate according to an embodiment. In some embodiments, a fabrication process 800 may include the following:

[0057] 804: Providing carrier wafer for the fabrication of an interconnect bridge.

[0058] 806: Bonding conductive bridge substrate to the carrier.

[0059] 808: Processing frontside layers, whereby metal and dielectric layers are embedded in a top surface of the bridge substrate.

[0060] 810: De-bonding bridge substrate the carrier wafer.

[0061] 812: Applying conductive adhesive to the backside of the bridge substrate.

[0062] 814: Coupling bridge substrate with the organic substrate.

[0063] 816: Producing conductive path with organic substrate wires via ohmic contract with frontside layer, conductive substrate, and conductive adhesive.

[0064] In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the described embodiments. It will be apparent, however, to one skilled in the art that embodiments may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form. There may be intermediate structure between illustrated components. The components described or illustrated herein may have additional inputs or outputs that are not illustrated or described.

[0065] Various embodiments may include various processes. These processes may be performed by hardware components or may be embodied in computer program or machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the processes. Alternatively, the processes may be performed by a combination of hardware and software.

[0066] Portions of various embodiments may be provided as a computer program product, which may include a computer-readable medium having stored thereon computer program instructions, which may be used to program a computer (or other electronic devices) for execution by one or more processors to perform a process according to certain embodiments. The computer-readable medium may include, but is not limited to, magnetic disks, optical disks, read-only memory (ROM), random access memory (RAM), erasable programmable read-only memory (EPROM), electrically-erasable programmable read-only memory (EEPROM), magnetic or optical cards, flash memory, or other type of computer-readable medium suitable for storing electronic instructions. Moreover, embodiments may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer.

[0067] Many of the methods are described in their most basic form, but processes can be added to or deleted from any of the methods and information can be added or subtracted from any of the described messages without departing from the basic scope of the present embodiments. It will be apparent to those skilled in the art that many further modifications and adaptations can be made. The particular embodiments are not provided to limit the concept but to illustrate it. The scope of the embodiments is not to be determined by the specific examples provided above but only by the claims below.

[0068] If it is said that an element "A" is coupled to or with element "B," element A may be directly coupled to element B or be indirectly coupled through, for example, element C. When the specification or claims state that a component, feature, structure, process, or characteristic A "causes" a component, feature, structure, process, or characteristic B, it means that "A" is at least a partial cause of "B" but that there may also be at least one other component, feature, structure, process, or characteristic that assists in causing "B." If the specification indicates that a component, feature, structure, process, or characteristic "may",

"might", or "could" be included, that particular component, feature, structure, process, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, this does not mean there is only one of the described elements.

[0069] An embodiment is an implementation or example. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. It should be appreciated that in the foregoing description of exemplary embodiments, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various novel aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed embodiments requires more features than are expressly recited in each claim. Rather, as the following claims reflect, novel aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims are hereby expressly incorporated into this description, with each claim standing on its own as a separate embodiment.

[0070] In some embodiments, an apparatus includes a substrate; an embedded interconnect layer in a first side of the substrate, the embedded interconnect layer including a plurality of contacts; and one or more conductive paths through the substrate, the one or more conductive paths being connected with the embedded interconnect layers.

[0071] In some embodiments, the substrate is a silicon substrate including a plurality of through silicon vias, the embedded interconnect layer being coupled to a first end of the plurality of through silicon vias, and the apparatus further including a redistribution layer coupled with a second end of the plurality of through silicon vias at the second side of the silicon substrate.

[0072] In some embodiments, the apparatus is coupled with a wire layer of an organic substrate using a conductive adhesive applied to the second side of the silicon substrate. In some embodiments, the conductive adhesive is an anisotropic

conductive adhesive, wherein applying pressure to the anisotropic conductive adhesive creates an electrical connection by compression of conductive particles.

[0073] In some embodiments, the one or more conductive paths include a plurality of conductive paths from the wire layer of the organic substrate to the embedded interconnect layer through the through silicon vias.

[0074] In some embodiments, the substrate is a conductive substrate, the embedded interconnect layer having an ohmic contact with the conductive substrate.

[0075] In some embodiments, the apparatus is coupled with a wire layer of an organic substrate using a conductive adhesive applied to the second side of the conductive substrate.

[0076] In some embodiments, the one of more conductive paths include a single conductive path from the wire layer of the organic substrate to the embedded interconnect layer through the conductive substrate.

[0077] In some embodiments, a method includes fabricating a substrate; embedding metal and dielectric layers in a first side of the substrate, the embedded interconnect layer including a plurality of contacts; and generating one or more conductive paths through the substrate, the one or more conductive paths being connected with the embedded interconnect layers.

[0078] In some embodiments, fabricating the substrate includes fabricating a silicon substrate, and the method further including forming a plurality of through silicon via through the silicon substrate, the embedded interconnect layer being coupled to a first end of the plurality of through silicon vias.

[0079] In some embodiments, the method further includes processing the silicon substrate to expose the through silicon vias on a second, opposite side of the silicon substrate.

[0080] In some embodiments, the method further includes forming a redistribution layer (RDL) coupled with a second end of the plurality of through silicon vias at the second side of the silicon substrate.

[0081] In some embodiments, the method further includes applying a conductive adhesive to the second side of the silicon substrate, and coupling the silicon substrate with a wire layer of an organic substrate using the conductive adhesive.

[0082] In some embodiments, the method further includes the conductive adhesive is an anisotropic conductive adhesive, further comprising applying pressure

to the anisotropic conductive adhesive to create an electrical connection by compression of conductive particles.

[0083] In some embodiments, generating the one or more conductive paths includes generating a plurality of conductive paths from the wire layer of the organic substrate to the embedded interconnect layer through the through silicon vias.

[0084] In some embodiments, fabricating the substrate includes bonding a conductive bridge substrate to a carrier wafer; embedding the metal and dielectric layers in a first side of the conductive bridge substrate; and de-bonding the conductive bridge substrate from the carrier wafer.

[0085] In some embodiments, the method further includes applying a conductive adhesive to a second side of the conductive bridge substrate, and coupling the silicon substrate with a wire layer of an organic substrate using the conductive adhesive.

[0086] In some embodiments, generating the one or more conductive paths includes generating a single conductive path from the wire layer of the organic substrate to the embedded interconnect layer through the conductive bridge substrate.

[0087] In some embodiments, a package includes a plurality of chips; an organic substrate; and an interconnect bridge coupled with the organic substrate to connect one or more of the plurality of chips, the interconnect bridge including a substrate, an embedded interconnect layer in a first side of the substrate, the embedded interconnect layer including a plurality of contacts, and one or more conductive paths through the substrate to the organic substrate, the one or more conductive paths being connected with the embedded interconnect layers.

[0088] In some embodiments, the substrate is a silicon substrate including a plurality of through silicon vias, the embedded interconnect layer being coupled to a first end of the plurality of through silicon vias, the bridge interconnect further including a redistribution layer coupled with a second end of the plurality of through silicon vias at the second side of the silicon substrate.

[0089] In some embodiments, the interconnect bridge is coupled with a wire layer of the organic substrate using a conductive adhesive applied to the second side of the silicon substrate.

[0090] In some embodiments, the conductive adhesive is an anisotropic conductive adhesive, wherein applying pressure to the anisotropic conductive adhesive creates an electrical connection by compression of conductive particles.

[0091] In some embodiments, the substrate of the interconnect bridge is a conductive substrate, the embedded interconnect layer having an ohmic contact with the conductive substrate.

[0092] In some embodiments, the interconnect bridge is coupled with a wire layer of the organic substrate using a conductive adhesive applied to the second side of the conductive substrate.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a substrate;

an embedded interconnect layer in a first side of the substrate, the embedded interconnect layer including a plurality of contacts; and

one or more conductive paths through the substrate, the one or more conductive paths being connected with the embedded interconnect layers.

2. The apparatus of claim 1, wherein the substrate is a silicon substrate including a plurality of through silicon vias, the embedded interconnect layer being coupled to a first end of the plurality of through silicon vias, and further comprising:

a redistribution layer coupled with a second end of the plurality of through silicon vias at the second side of the silicon substrate.

3. The apparatus of claim 2, wherein the apparatus is coupled with a wire layer of an organic substrate using a conductive adhesive applied to the second side of the silicon substrate.

4. The apparatus of claim 3, wherein the conductive adhesive is an anisotropic conductive adhesive, wherein applying pressure to the anisotropic conductive adhesive creates an electrical connection by compression of conductive particles.

5. The apparatus of claim 3, wherein the one or more conductive paths include a plurality of conductive paths from the wire layer of the organic substrate to the embedded interconnect layer through the through silicon vias.

6. The apparatus of claim 1, wherein the substrate is a conductive substrate, the embedded interconnect layer having an ohmic contact with the conductive substrate.

7. The apparatus of claim 6, wherein the apparatus is coupled with a wire layer of an organic substrate using a conductive adhesive applied to the second side of the conductive substrate.

8. The apparatus of claim 7, wherein the one of more conductive paths include a single conductive path from the wire layer of the organic substrate to the embedded interconnect layer through the conductive substrate.

9. A method comprising:

fabricating a substrate;

embedding metal and dielectric layers in a first side of the substrate, the embedded interconnect layer including a plurality of contacts; and

generating one or more conductive paths through the substrate, the one or more conductive paths being connected with the embedded interconnect layers.

10. The method of claim 9, wherein fabricating the substrate includes fabricating a silicon substrate, and further comprising:

forming a plurality of through silicon via through the silicon substrate, the embedded interconnect layer being coupled to a first end of the plurality of through silicon vias.

11. The method of claim 10, and further comprising:

processing the silicon substrate to expose the through silicon vias on a second, opposite side of the silicon substrate.

12. The method of claim 11, and further comprising:

forming a redistribution layer (RDL) coupled with a second end of the plurality of through silicon vias at the second side of the silicon substrate.

13. The method of claim 12, further comprising applying a conductive adhesive to the second side of the silicon substrate, and coupling the silicon substrate with a wire layer of an organic substrate using the conductive adhesive.

14. The method of claim 13, wherein the conductive adhesive is an anisotropic conductive adhesive, further comprising applying pressure to the anisotropic conductive adhesive to create an electrical connection by compression of conductive particles.

15. The method of claim 13, wherein generating the one or more conductive paths includes generating a plurality of conductive paths from the wire layer of the organic substrate to the embedded interconnect layer through the through silicon vias.

16. The method of claim 9, wherein fabricating the substrate includes:

bonding a conductive bridge substrate to a carrier wafer;

embedding the metal and dielectric layers in a first side of the conductive bridge substrate; and

de-bonding the conductive bridge substrate from the carrier wafer.

17. The method of claim 16, further comprising applying a conductive adhesive to a second side of the conductive bridge substrate, and coupling the silicon substrate with a wire layer of an organic substrate using the conductive adhesive.

18. The method of claim 17, wherein generating the one or more conductive paths includes generating a single conductive path from the wire layer of the organic substrate to the embedded interconnect layer through the conductive bridge substrate.

19. A package comprising:

a plurality of chips;

an organic substrate; and

an interconnect bridge coupled with the organic substrate to connect one or more of the plurality of chips, the interconnect bridge including:

a substrate,

an embedded interconnect layer in a first side of the substrate, the embedded interconnect layer including a plurality of contacts, and

one or more conductive paths through the substrate to the organic substrate, the one or more conductive paths being connected with the embedded interconnect layers.

20. The package of claim 19, wherein the substrate is a silicon substrate including a plurality of through silicon vias, the embedded interconnect layer being coupled to a first end of the plurality of through silicon vias, the bridge interconnect further including:

a redistribution layer coupled with a second end of the plurality of through silicon vias at the second side of the silicon substrate.

21. The package of claim 20, wherein the interconnect bridge is coupled with a wire layer of the organic substrate using a conductive adhesive applied to the second side of the silicon substrate.

22. The package of claim 21, wherein the conductive adhesive is an anisotropic conductive adhesive, wherein applying pressure to the anisotropic conductive adhesive creates an electrical connection by compression of conductive particles.

23. The package of claim 19, wherein the substrate of the interconnect bridge is a conductive substrate, the embedded interconnect layer having an ohmic contact with the conductive substrate.

24. The package of claim 23, wherein the interconnect bridge is coupled with a wire layer of the organic substrate using a conductive adhesive applied to the second side of the conductive substrate.

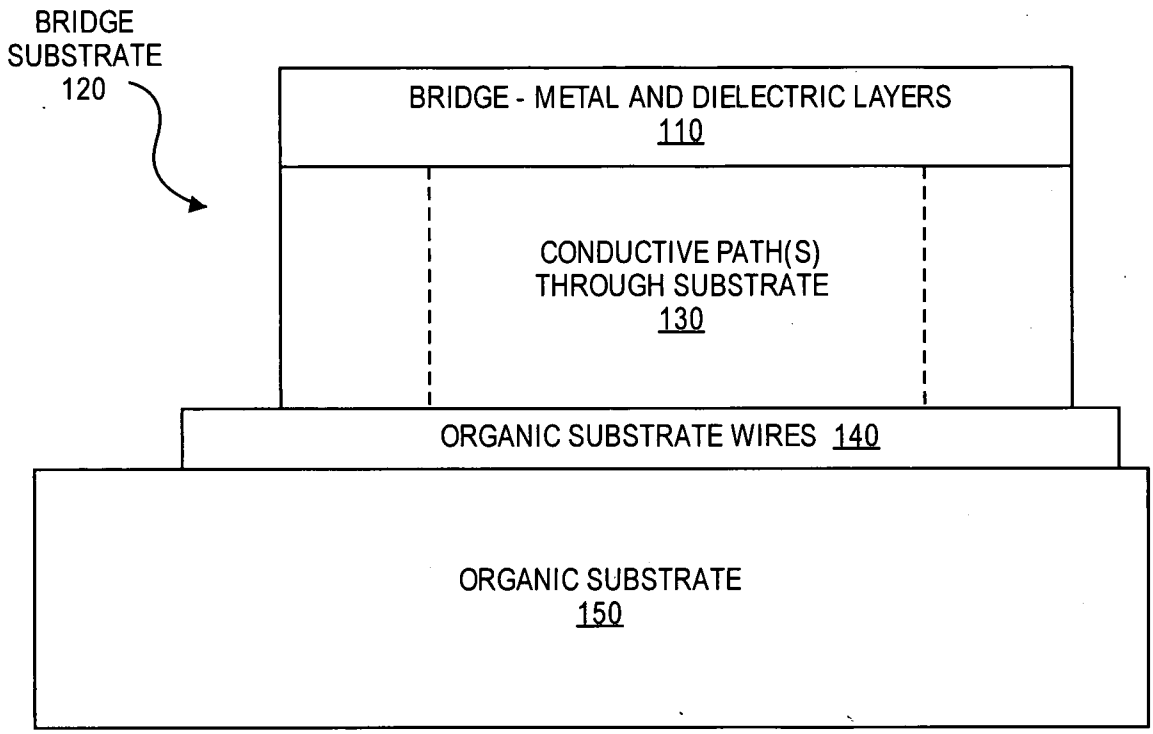
BRIDGE
SUBSTRATE
120
BRIDGE - METAL AND DIELECTRIC LAYERS
110
CONDUCTIVE PATH(S)
THROUGH SUBSTRATE
130
ORGANIC SUBSTRATE WIRES 140
ORGANIC SUBSTRATE
150

FIG. 1

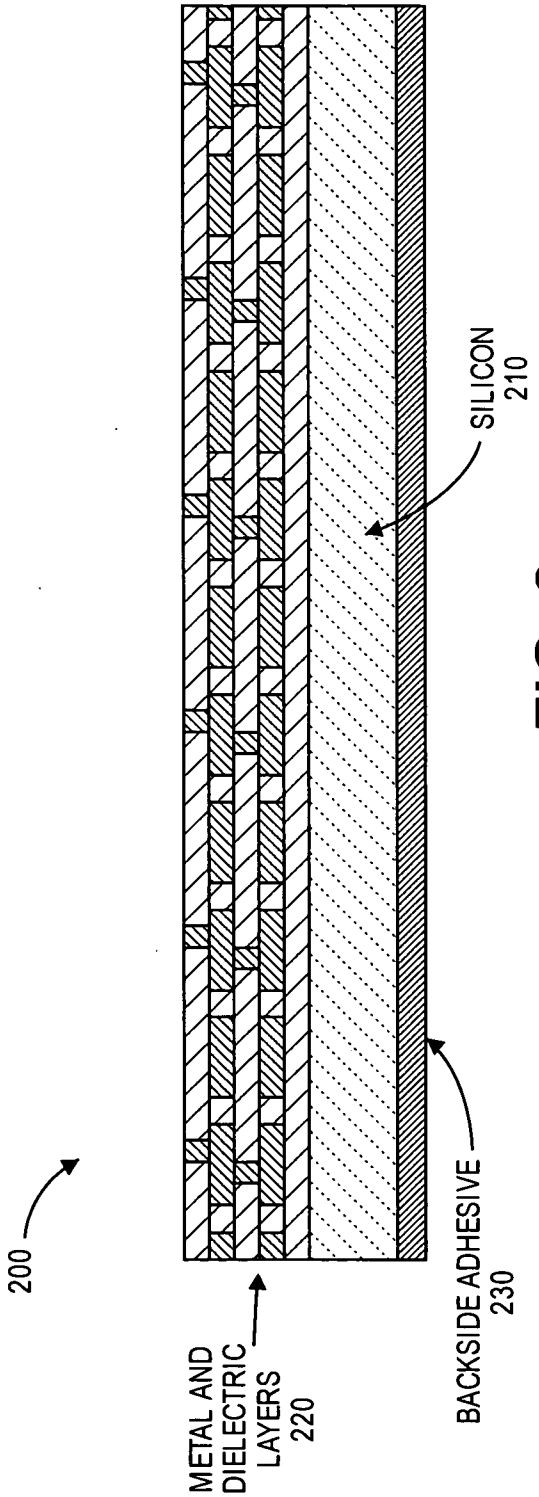
200
METAL AND DIELECTRIC LAYERS 220
SILICON 210
BACKSIDE ADHESIVE 230

FIG. 2

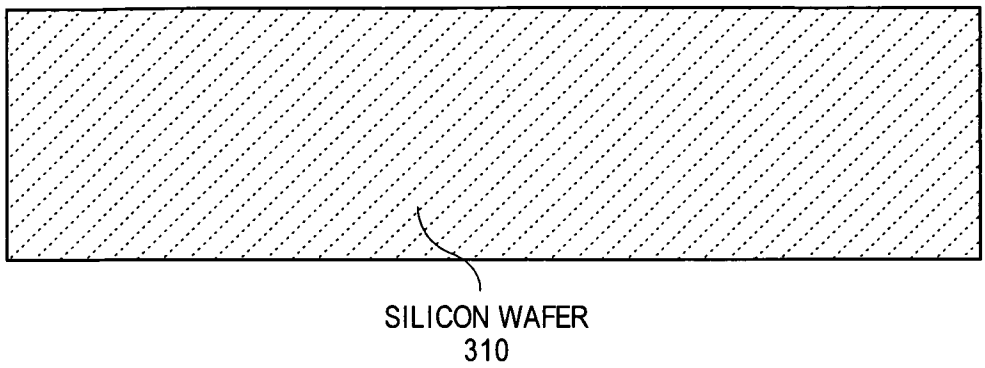

FIG. 3A

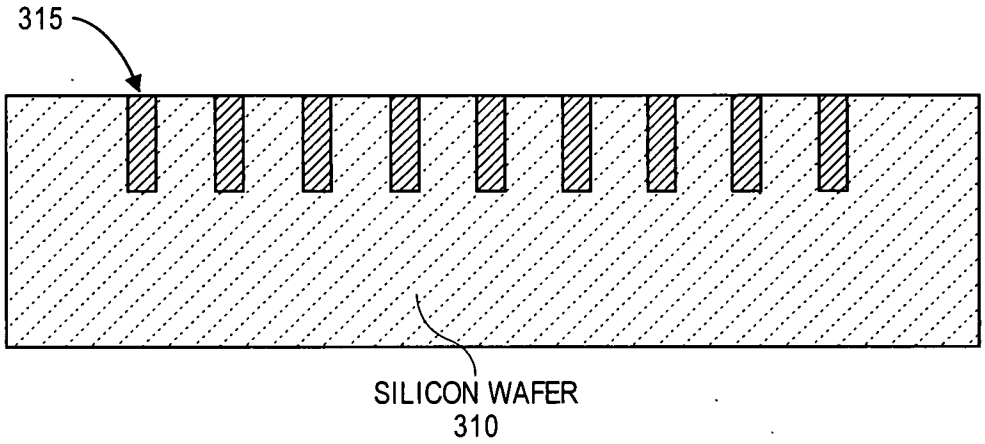

FIG. 3B

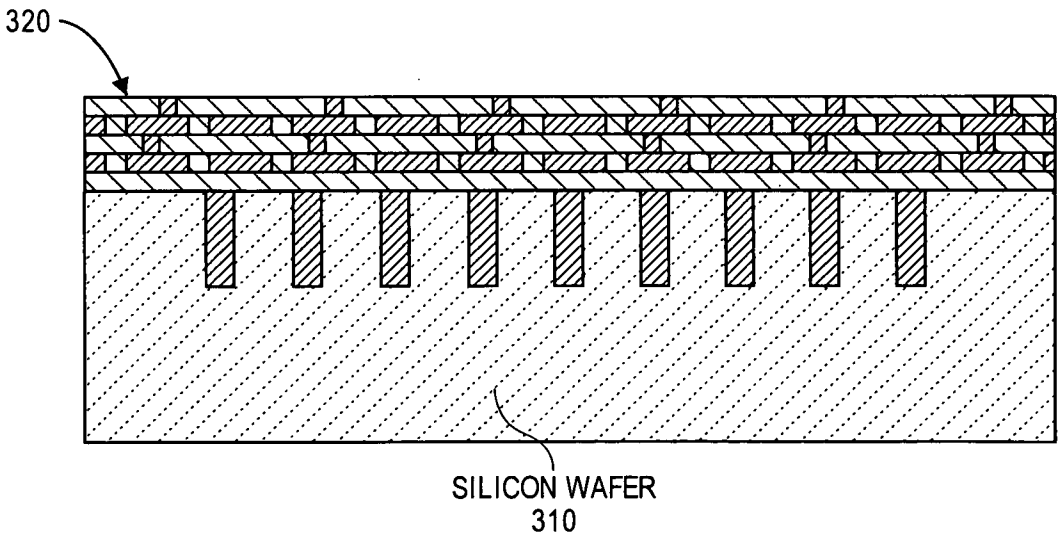

FIG. 3C

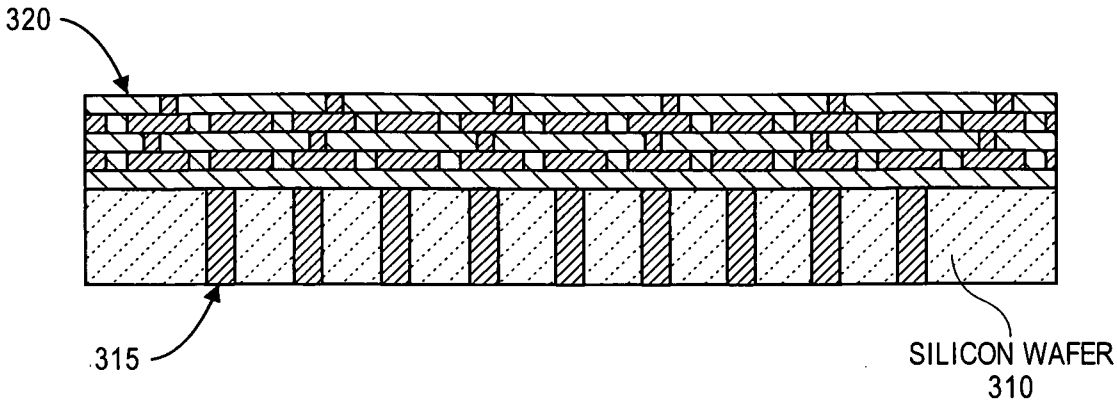

FIG. 3D

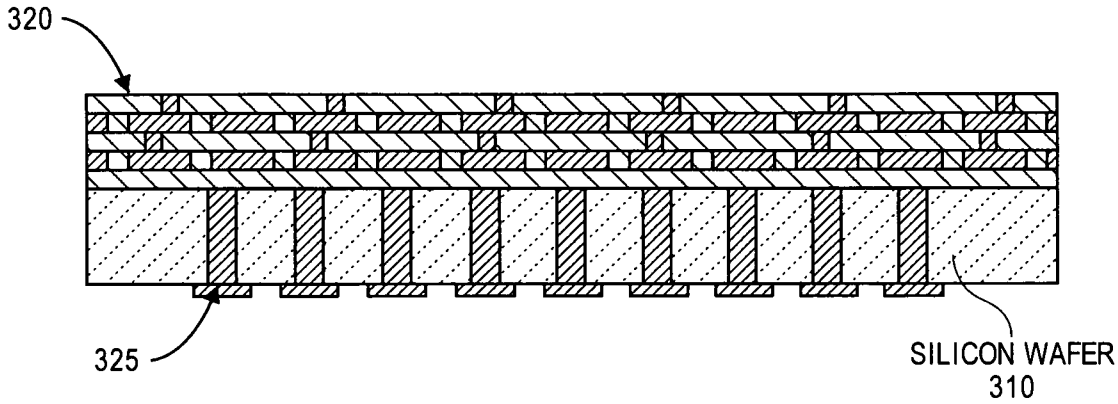

FIG. 3E

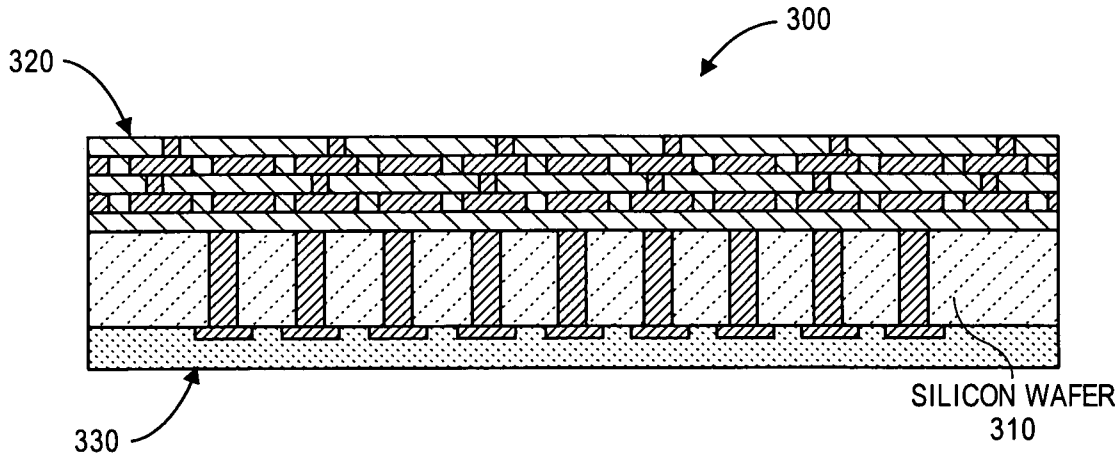

FIG. 3F

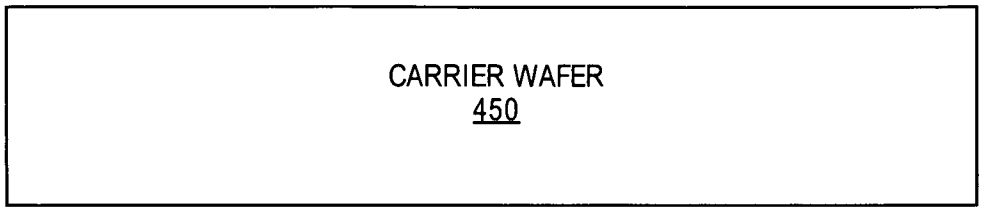

FIG. 4A

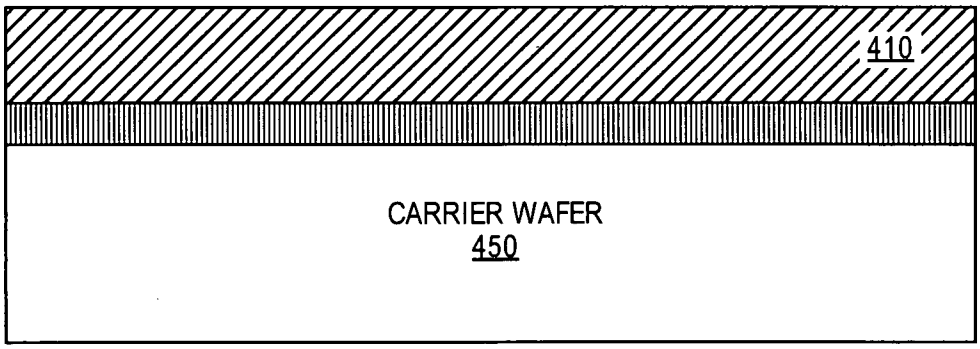

FIG. 4B

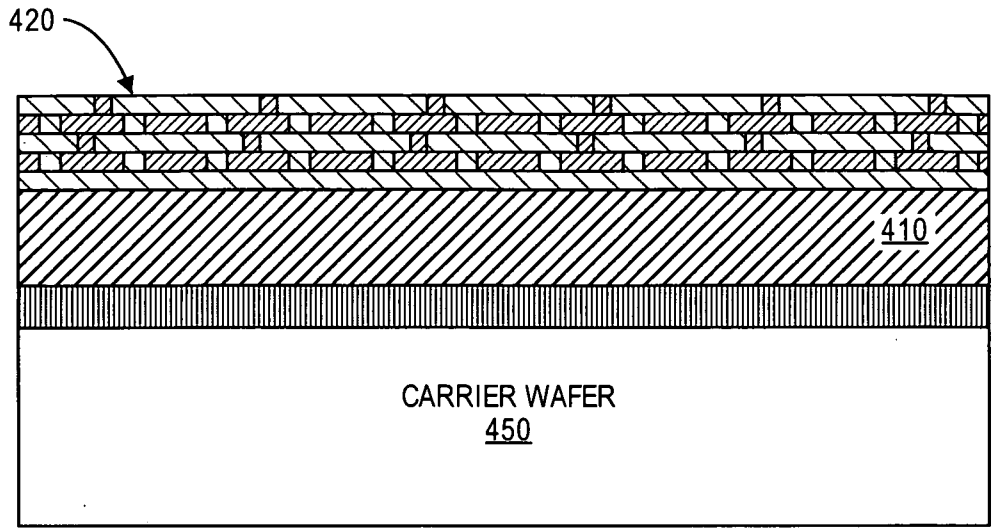

FIG. 4C

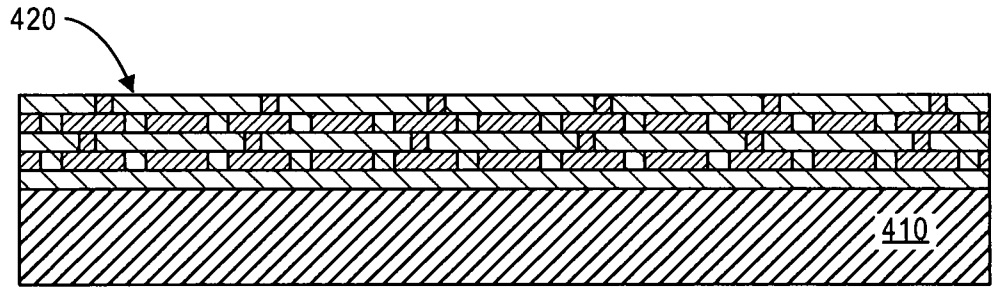

FIG. 4D

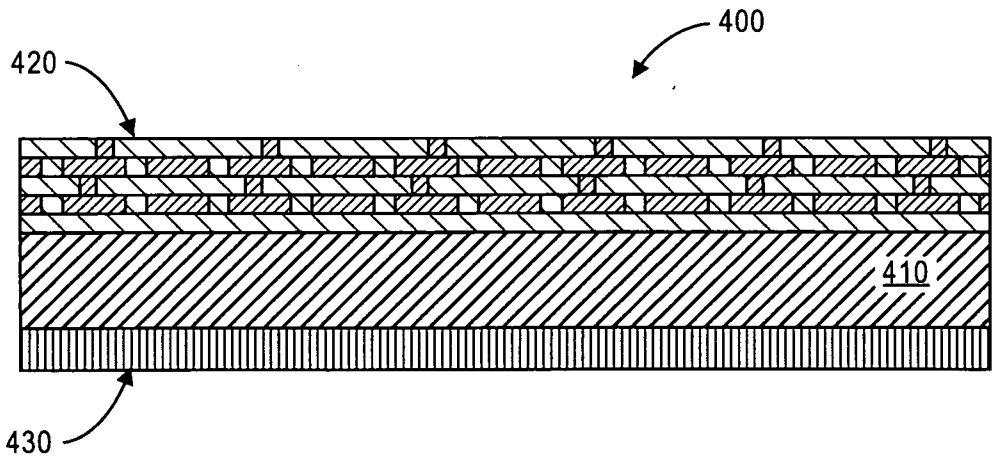

FIG. 4E

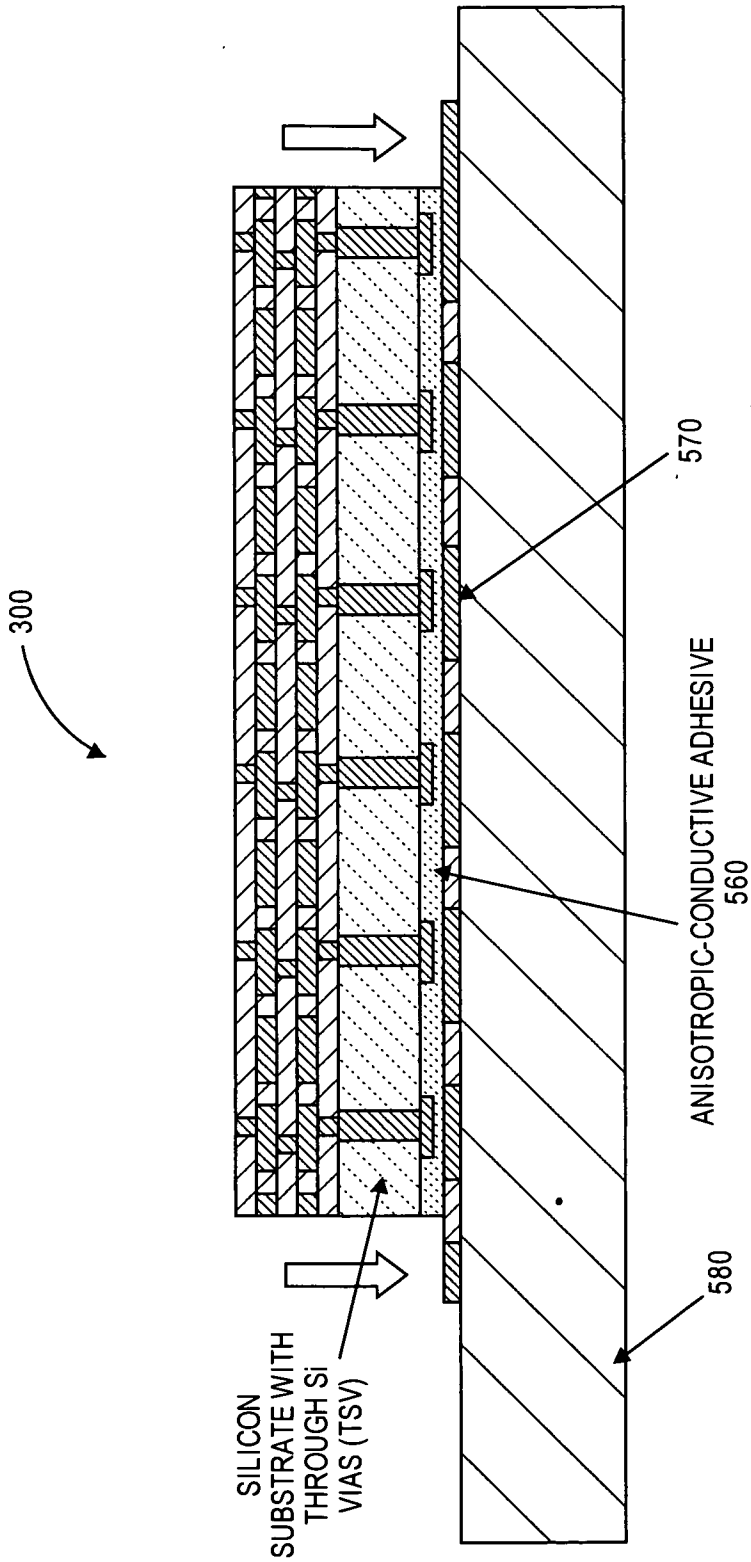
300
570
ANISOTROPIC-CONDUCTIVE ADHESIVE
560
580
SILICON SUBSTRATE WITH THROUGH Si VIAS (TSV)

FIG. 5

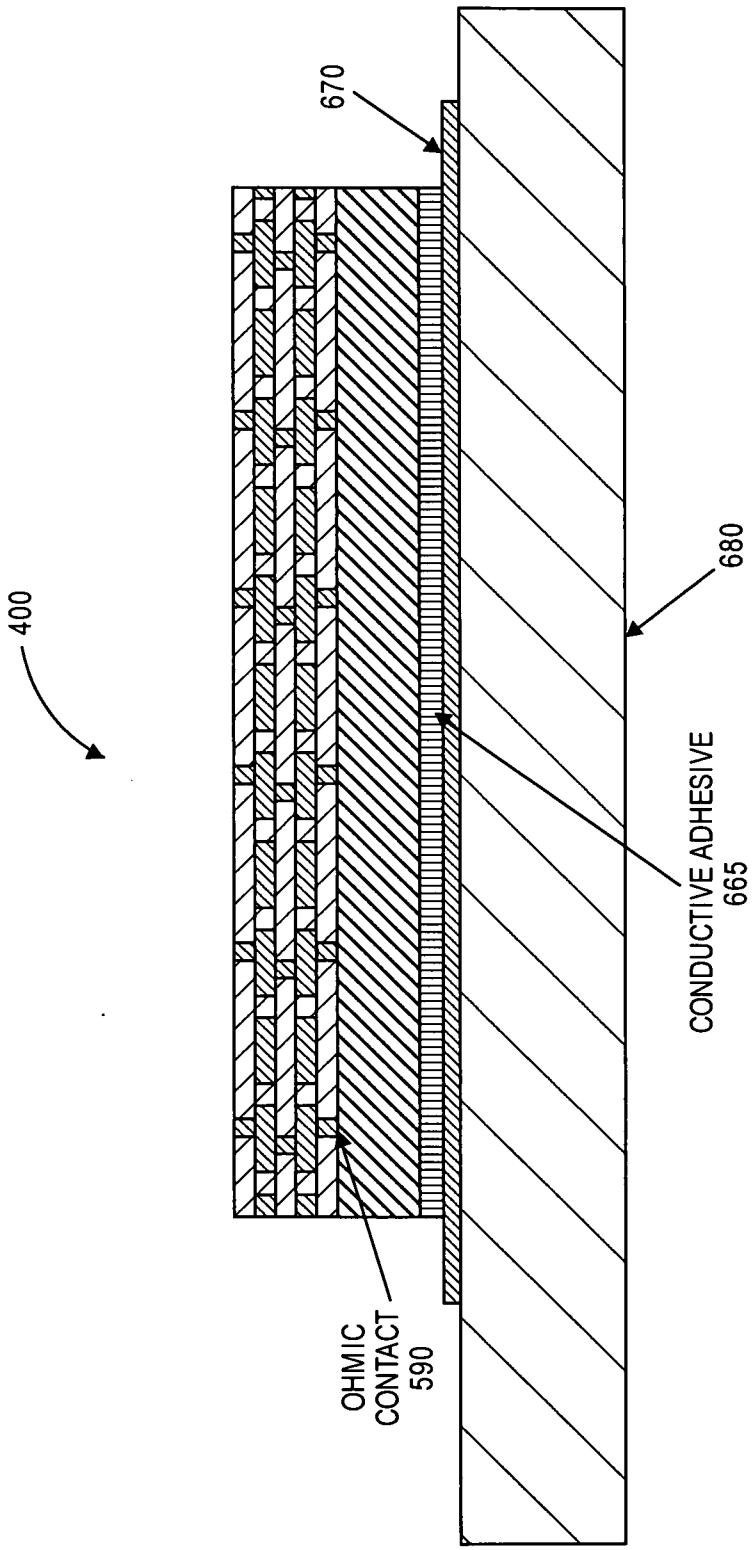

FIG. 6

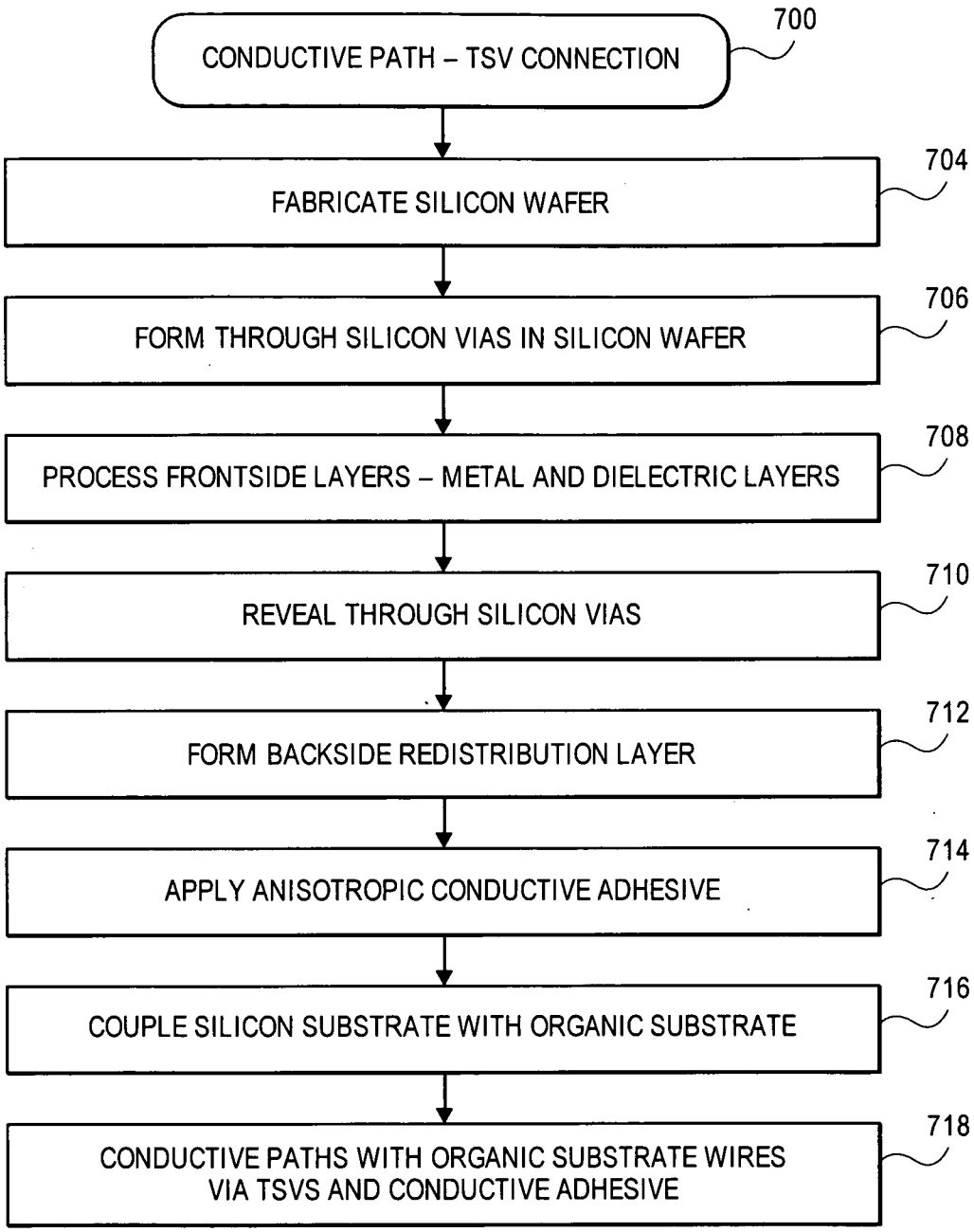
CONDUCTIVE PATH – TSV CONNECTION
700
FABRICATE SILICON WAFER
704
FORM THROUGH SILICON VIAS IN SILICON WAFER
706
PROCESS FRONTSIDE LAYERS – METAL AND DIELECTRIC LAYERS
708
REVEAL THROUGH SILICON VIAS
710
FORM BACKSIDE REDISTRIBUTION LAYER
712
APPLY ANISOTROPIC CONDUCTIVE ADHESIVE
714
COUPLE SILICON SUBSTRATE WITH ORGANIC SUBSTRATE
716
CONDUCTIVE PATHS WITH ORGANIC SUBSTRATE WIRES VIA TSVS AND CONDUCTIVE ADHESIVE
718

FIG. 7

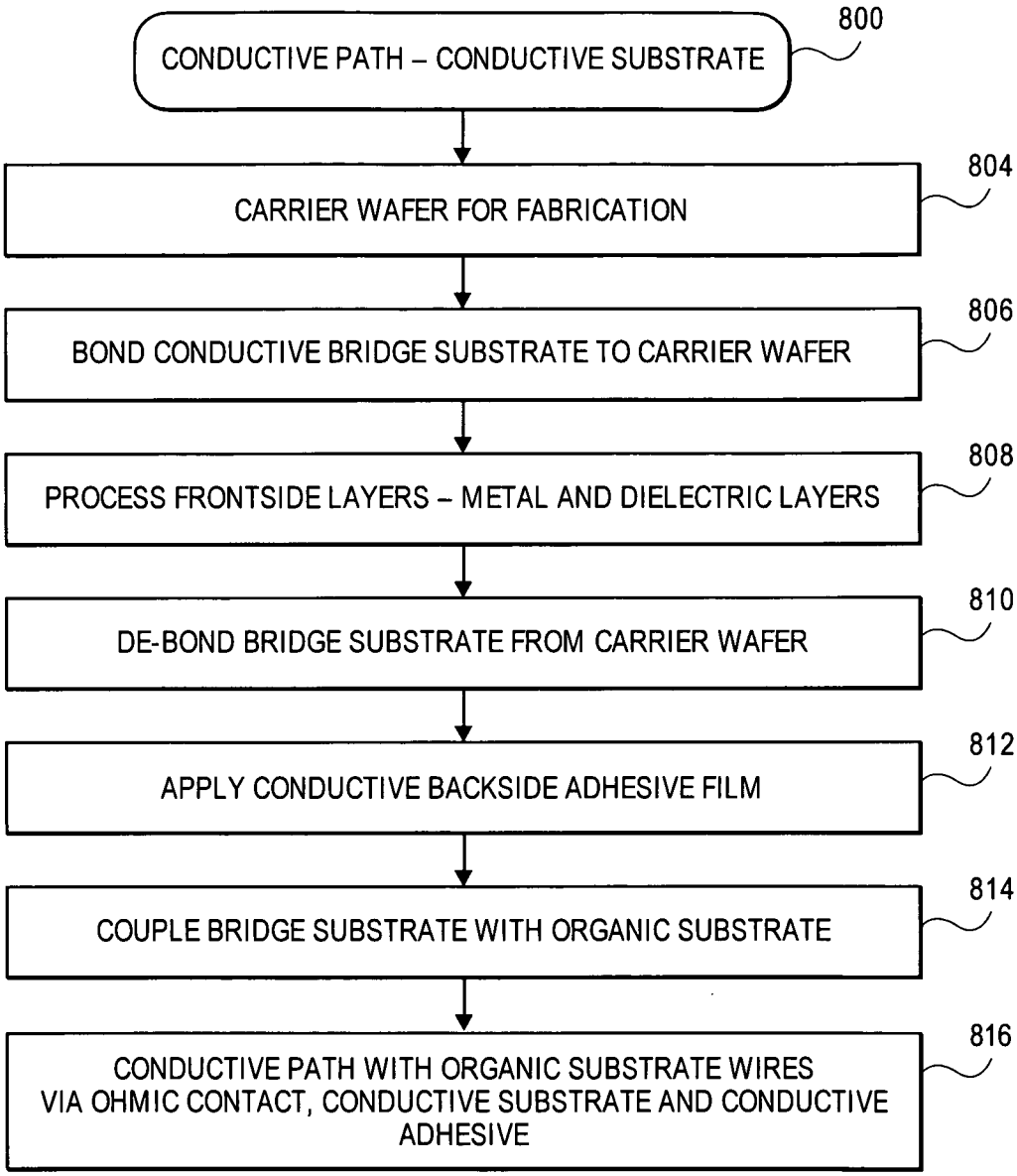
800
CONDUCTIVE PATH – CONDUCTIVE SUBSTRATE
804
CARRIER WAFER FOR FABRICATION
806
BOND CONDUCTIVE BRIDGE SUBSTRATE TO CARRIER WAFER
808
PROCESS FRONTSIDE LAYERS – METAL AND DIELECTRIC LAYERS
810
DE-BOND BRIDGE SUBSTRATE FROM CARRIER WAFER
812
APPLY CONDUCTIVE BACKSIDE ADHESIVE FILM
814
COUPLE BRIDGE SUBSTRATE WITH ORGANIC SUBSTRATE
816
CONDUCTIVE PATH WITH ORGANIC SUBSTRATE WIRES VIA OHMIC CONTACT, CONDUCTIVE SUBSTRATE AND CONDUCTIVE ADHESIVE

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000398

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/12(2006.01)i, H01L 23/48(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/12; H01L 21/22; H01L 21/50; H01L 23/48; H01L 21/762; H01L 21/66; H01L 23/522; H01L 23/538; H01L 23/495

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: bridge, interconnect, source, conductive adhesive, substrate, package

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0042643 A1 (CHEN-HUA YU et al.) 13 February 2014 See abstract, paragraphs [0016]-[0070] and figures 1-8.	1-2,9-12,19-20
Y		3-8,13-18,21-24
Y	US 8802454 B1 (ARIFUR RAHMAN et al.) 12 August 2014 See abstract, column 3, line 19 - column 4, line 44 and figures 1-1 - 3.	3-5,7-8,13-15 ,17-18,21-22,24
Y	US 2013-0154109 A1 (RAMNATH VENKATRAMAN et al.) 20 June 2013 See abstract, paragraph [0019] and figure 1.	6-8,23-24
Y	US 2013-0214423 A1 (MARIAM SADAKA) 22 August 2013 See abstract, paragraphs [0056]-[0057] and figures 8-9.	16-18
A	US 2012-0104578 A1 (HSIEN-PIN HU et al.) 03 May 2012 See abstract, paragraphs [0014]-[0021] and figure 1D.	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2016 (26.09.2016)	**26 September 2016 (26.09.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/000398

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0042643 A1	13/02/2014	CN 103579183 A	12/02/2014
		TW 201407750 A	16/02/2014
		TW I520308 B	01/02/2016
		US 8810006 B2	19/08/2014
US 8802454 B1	12/08/2014	None	
US 2013-0154109 A1	20/06/2013	WO 2013-090914 A1	20/06/2013
US 2013-0214423 A1	22/08/2013	CN 103258782 A	21/08/2013
		FR 2987494 A1	30/08/2013
		KR 10-2013-0094750 A	26/08/2013
		TW 201336000 A	01/09/2013
		US 8970045 B2	03/03/2015
US 2012-0104578 A1	03/05/2012	US 2012-0238057 A1	20/09/2012
		US 8105875 B1	31/01/2012
		US 8319349 B2	27/11/2012
		US 8759150 B2	24/06/2014