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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) Title: COPPER PILLAR ATTACH SUBSTRATE

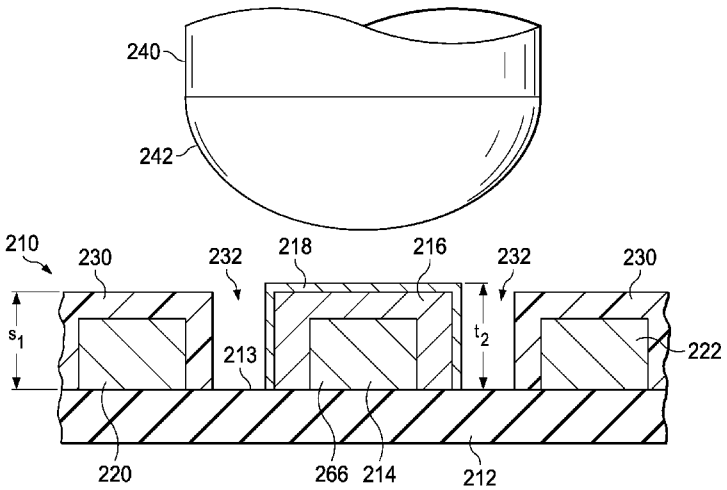

FIG. 6

(57) Abstract: An electronic assembly includes a copper pillar attach substrate (210) that has a dielectric layer (212) and a solder resist layer (230) overlying the dielectric layer (212). The solder resist layer (230) has a plurality of solder resist openings (232). A plurality of parallel traces (214, 220, 222) are formed on the dielectric layer (212). Each trace (214, 220, 222) has a first end portion (262), a second end portion (264) and an intermediate portion (266). The first and second end portions (262, 264) of each trace (214, 220, 222) are covered by the solder resist layer (230), and the intermediate portions (266) are positioned in the solder resist openings (232). Each of the intermediate portions (266) has at least one conductive coating layer (216, 218) on it and has a height measured from the dielectric layer (212) to a topmost one of the at least one conductive coating layer (216, 218) that is at least as great as the solder resist layer (230) thickness.

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COPPER PILLAR ATTACH SUBSTRATE

BACKGROUND

[0001] During the past decade flipchip technology has emerged as a popular alternative to wire bonding for interconnecting semiconductor devices such as integrated circuit (IC) dies to substrates such as printed circuit boards, carrier substrates, interposers and other dies.

[0002] "Flipchip," is also known as "controlled collapse chip connection" or its acronym, "C4." With flipchip technology, solder balls/bumps are attached to electrical contact pads on one face of a die/chip. The flipchip dies are usually processed at the wafer level, i.e., while multiple identical dies are still part of a large "wafer." Solder balls are deposited on chip pads on the top side of the wafer. The wafer is sometimes "singulated" or "diced" (cut up into separate dies) at this point to provide a number of separate flipchip dies each having solder balls on the top face surface. The chips may then be "flipped" over to connect the solder balls to matching contact pads on the top surface of a substrate such as a printed circuit board or carrier substrate on which the flipchip is mounted. Solder ball attachment is usually provided by reflow heating.

[0003] As IC dies have become more complex, the number of solder bumps/balls on flipchips have increased dramatically. Whereas in the past the solder balls were usually provided by relatively large round solder balls attached to the chip contact pads, more recently copper pillars ("CuP's") have been used in place of the solder balls. A CuP is an elongated copper post member that is attached at one end to a contact pad on the flipchip die. The CuP extends outwardly from the die in a direction perpendicular to the face of the die. Each CuP has a generally bullet or hemisphere shaped solder piece attached to its distal end. The CuP's are bonded by this solder piece to corresponding contact pads on a substrate as by reflow heating. CuP's are capable of being positioned much more densely, i.e., at a "higher pitch," than conventional solder balls/bumps. For example, a typical pitch for a flipchip solder ball array is 150μm, whereas a typical pitch for a flipchip CuP array is 40μm. One manner of facilitating connection of a substrate to a die having such high CuP density is to provide bond "traces" (also referred to as "fingers"), rather than conventional contact pads, on the substrate to which the flipchip is to be mounted. The traces are elongated contact pads

that may be positioned in close parallel relationship, traditionally without any insulating material between them.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a top isometric view of a conventional flipchip die with copper pillars.

[0005] FIG. 2 is a detailed cross-sectional view of a portion of the flipchip die of FIG. 1.

[0006] FIG. 3 is a top plan view of a portion of a conventional substrate to which a flipchip die of the type shown in FIGS. 1 and 2 may be connected.

[0007] FIG. 4 is a top plan view of a portion of another type of substrate to which a flipchip die of the type shown in FIGS. 1 and 2 may be connected.

[0008] FIG. 5 is a cross-sectional view of another substrate of the type shown in FIG. 4.

[0009] FIG. 6 is a cross-sectional elevation view of another substrate to which a flipchip die of the type shown in FIGS. 1 and 2 may be connected.

[0010] FIG. 7 is a cross-sectional elevation view of a substrate, such as shown in FIG. 6, attached to a flipchip die, such as shown in FIGS. 1 and 2.

[0011] FIG. 8 is a top plan view of a flipchip die mounted on a substrate as shown in FIG. 7, with the entire flipchip, except for cross-sectional portions of the copper pillars, cut away.

[0012] FIG. 9 is a flow chart of a method of forming a CuP attach substrate.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] An electronic assembly includes a CuP attach substrate 210 that has a dielectric layer 212 and a solder resist layer 230 overlying the dielectric layer 212. The solder resist layer 212 has a plurality of solder resist openings 232 in it. A plurality of parallel traces 214, 220, 222 are formed on the dielectric layer 212. Each trace has a first end portion 262, a second end portion 264 and an intermediate portion 266. The first and second end portions 262, 264 are covered by the solder resist layer 230. The intermediate portions 266 are positioned in the openings 232 in the solder resist layer 230. Each of the intermediate portions 264 has at least one conductive coating layer 216, 218 on it. The height of each intermediate portion 264 measured from the top surface 213 of the dielectric

layer 212 to the top of the topmost conductive coating layer 218 is at least as great as the thickness of the solder resist layer 230.

[0014] As illustrated by FIG. 1, a conventional flipchip die 10 comprises a semiconductor substrate 12 that contains internal circuitry. The substrate has a first or active face 14 and a second or inactive face 15 opposite the first face 14. An array of copper pillars 16 project from the active face surface 14 of the die 10. The copper pillar array 16 includes a number of individual copper pillars 18 which may be arranged in any desired configuration on the first face 14.

[0015] FIG. 2 illustrates a typical structure of a pair of conventional copper pillars 18 projecting from the first face 14 of the die 10. Each of the individual copper pillar 18 may comprise a generally bullet or hemisphere shaped solder tip portion 20 mounted on a generally cylindrical copper post portion 22. Each copper post portion 22 is mounted on a contact pad 24 that is formed at the top surface of the silicon substrate 12. The contact pad 24 is connected to internal circuitry (not shown) in the silicon substrate 12. The copper post portion 22 may be conventionally physically and electrically connected to the contact pad 24 as by under bump metal layer 26 in a manner well known in the art. Thus, each copper pillar 18 is electrically connected to internal circuitry in the semiconductor substrate 12 through the contact pad 24 and under bump metal layer 26. A passivation layer 17 on the top surface 14 of the die 10 encompasses each copper pillar 18.

[0016] FIG. 3 is a top plan view of a portion of a substrate 30 which is adapted to be connected to some of the copper pillars (" CuP's") 18 of the flipchip die 10. The substrate 30 may be a printed circuit board, IC package carrier board, interposer, or other type of electrical connection substrate. The substrate 30 has a top surface 32 upon which a plurality of generally parallel traces (sometimes referred to herein simply as "traces") 34, 36, 38, 40 are provided by use of conventional or other methods. The traces 34, 36, 38, 40 may be made of copper or another conductive metal. The traces may be coated with other material such as tin or silver to facilitate bonding with the solder tips of copper pillars. The traces 34, 36, 38, 40 are separated by spaces 44, 46, 48 which may all be of the same width. The traces 34, 36, 38, 40 may also be of the same width. A typical width range for the prior art traces 34, etc., is 15 μm to 20 μm. The spaces 44, 46, 48 between traces may have a typical width range of 40 μm to 80 μm. The ratio of the width of a trace to the width of the space between

them is typically about 2.5 to 4. The positions at which the solder tip portions 20 of associated CuP's 18 are connected to individual traces 34, 36, 38, 40 are illustrated by dashed circles and cross hairs at 52, 54, 56, 58. Opposite longitudinal ends of the traces 34, 36, etc., are covered, respectively, with strips 62, 64 of solder resist. Solder resist is a nonconductive material used to shield conductive pads and traces from solder or other conductive material. Solder resist is sometimes referred to in the art as "solder mask." A typical width (a direction parallel to the direction in which the traces extend) range of a solder resist strip provided over an end portion of a trace is about 70μm to 170 μm.

[0017] FIG. 4 is a top plan view of a portion of a substrate 31 which, like the substrate 30 of FIG. 3, is adapted to be connected to some of the copper pillars ("CuP's") 18 of the flipchip die 10. The structure of the substrate 31 is similar to that of substrate 30, except that a layer of solder resist completely covers the traces except for a small solder resist opening over each trace. The semiconductor substrate 31 has parallel, spaced apart traces or "traces" 35, 37, 39, 41 formed on a top surface 33 thereof. A layer of solder resist 63 covers all of the traces between opposite ends of the traces, except for small openings 51, 53, 55, 57 above an intermediate portion of each trace 35, 37, 39, 41 where a solder resist opening 51, 53, 55, 57 is provided. The openings are somewhat larger than the width of each trace and are provided in staggered relationship. The openings 51, 53, 55, 57 are also wider than the diameter of CuP's 52, 54, 56, 58,which are bonded to portions of corresponding traces that are exposed by the openings 51, 53, 55, 57.

[0018] FIG. 5 is a cross-sectional elevation view of a substrate 110 having a structure substantially identical to that of substrate 31 shown in FIG. 4. Substrate 110 has a dielectric layer 112. A first trace 114 is formed on a top surface 111 of the dielectric layer 112. The trace 114 may be a copper trace or may be formed from another suitable conductor such as gold. As shown in FIG. 5, a conductor coating 116 that is readily bondable with solder, for example tin or silver, covers the top and side surfaces of a portion of trace 114. The portion of the trace 114 to which the coating 116 is applied is positioned within the solder resist opening 132. A second trace 118 is positioned adjacent to one side of trace 112 and a third trace 122 is positioned adjacent to the other side of the first trace 112. A solder resist layer 130 covers all of the traces 114, 118, 122, except in the area of a solder resist opening above an intermediate portion of each trace, such as solder resist opening 132 positioned over an

intermediate portion 115 of first trace 114. The solder resist openings are staggered such as the solder resist openings 51, 53, 55, 57 shown in FIG. 4. Thus, in FIG. 5, there is no opening over traces 118 and 122 at a location thereon adjacent to the opening 132 over trace 114. Solder resist 130 covers both the top and side portions of traces 118 and 122 adjacent to the intermediate portion 115 of trace 114 that lies in the solder resist opening 132. The height "s_1" of the solder resist layer 130 at the opening 132 is greater than the height "t_1" measured from the substrate surface 111 to the top of the conductive coating 116 on the first trace 114. A CuP 140 having a solder tip 142 is positioned directly above trace 114 intermediate portion 115 and may be bonded to trace 114 by moving it downwardly into contact with the coating 116 and then reflowing solder tip 142 and coating 116. The bonding of the tip of CuP to a coated trace is known in the art and is thus not further described herein.

[0019] Applicant has discovered certain problems associated with flipchip die mount substrates such as described with reference to FIGS. 4 and 5 above. One problem is that the manufacturing tolerances for such substrates are very small and deviation from these tolerances may cause the flipchip/substrate assembly to fail in several different ways. For example, if the solder resist layer 130 is shifted on the dielectric layer 112 a small distance to the left from the position shown in FIG. 5, a portion of the trace 118 may become exposed and any solder 142 from the CuP 140 that may run into the solder resist opening 132 during reflow may cause traces 114 and 118 to short out. The same shift to the left may cause the portion of the opening 132 between trace 114 and trace 122 to be reduced so much that the CuP 140 will be prevented by the solder resist around trace 122 from moving freely into contacting relationship with the tip of trace 114. As the CuP 140 descends it may shave off a portion of the solder resist around trace 122 with the shaved off portion of solder resist falling onto the coating layer 116 and interfering with the bond between the solder tip 142 and the coating layer 116. Making the solder resist opening 132 too small causes a similar problem and results in solder resist residue falling onto the coating layer 116 of the trace 122 in the area of the solder resist opening 132. Also, reducing the opening size of the solder resist increases the risk of not making a good contact between the CuP tip 142 and the trace 114. To prevent such problems from arising the size of the solder resist opening 132 may be increased. However increasing the size of the solder resist opening 132 may result in a

different failure mode, so called "solder resist undercut." Undercut frequently happens when the width of the solder resist covering on adjacent Cu trace, such as 118 and 122 decreases. Optimizing the process that produces solder resist openings so that the solder resist openings are not too large and not too small is very costly. The below described structures and processes may be used to obviate problems such as described above.

[0020] FIGS. 6 is a side elevation view of a semiconductor substrate 210 having a dielectric layer 212 with a top surface 213. A first trace 214 is formed on surface 213. The trace 214 may be copper, gold or other suitable conductor. The first trace 214 has an intermediate portion 215 of its length that is positioned within a solder resist opening 232 of a solder resist layer 230. A first conductive coating layer 216 covers the intermediate portion 215 of the first trace 214. This layer 216 is formed from a conductive material such as copper with a melting temperature that is sufficiently high that it does not melt during reflow heating as further described below. A second coating 218 may be applied over the first coating 216 on the first trace 214 in the intermediate portion 215 thereof. Both coating layers 216, 218 are conductive coating layers. The first coating layer 216 may have a composition similar to the trace 214, for example both the trace and the first coating layer 216 may be copper. The first coating layer 216 in one embodiment is thicker than the second coating layer 218. The first coating layer 216 may be selected from materials that adhere well to the trace 214 and which do not melt at reflow temperatures. The second coating layer may 218 may be selected from conductor materials that adhere well to the first coating, that bond well to solder, and that melt at reflow temperatures. For example, the second layer could be tin or silver or an appropriate alloy. The coatings 216, 218 may be applied to the intermediate portion 215 after the formation of the solder resist opening 232 by conventional means. A second trace 220 is positioned parallel and adjacent to one side of the first trace 214. A third trace 222 is positioned parallel and adjacent to the other side of the first trace 214. The thickness of the second and third layers 216, 218 combined, "t_2," is greater than the height, "s_1," of the solder resist layer 230 at the opening 232. Thus, as the copper pillar 240 descends it makes first contact with the second layer 216 of the trace 214, not the solder resist layer 230, even if the copper pillar 240 is not precisely centered on the trace 214. This happens because the top of the second layer 216 is the highest surface on the substrate 210 in the vicinity of the copper pillar 240. The result is that the solder tip 242 of CuP 240 makes

contact with second layer 216 before having any opportunity to contact the solder resist layer 230. Therefore, as shown in FIG. 7, a bond 250 between coating layer 218 and the solder tip 242 is formed that is free of any debris from the solder resist layer 230, as illustrated in FIG. 7. By raising the contact surface of the trace 214 above the solder resist layer 230 another positive affect is also achieved. The solder resist opening 232 may be reduced in size with respect to the size of the CuP 240 since it is no longer necessary for the CuP 240 to fit into the solder resist opening. Thus, solder resist undercut is prevented. Also the diameters of the CuP's 240 may be increased with respect to the size of the solder resist openings. A diameter increase in the CuP makes it easier to engage each CuP with a corresponding trace. In other words, the alignment between CuP's and corresponding traces need not be as precise with the structure shown in FIGS. 6 and 7 as with the structures shown in FIGS.3-5 because each CuP may be given a wider footprint without causing other problems. For example, as shown in FIGS. 6 and 7, CuP's could be made with footprints that are wider than the corresponding solder resist openings 232 that are functionally connectable to a substrate, such as 210, that has an overall trace height t_2 (including coatings) in the corresponding solder resist opening 232 that is greater than the height s_1 of the solder resist layer 230. It will also be understood that the CuP may be given a wider footprint even if its cross-sectional shape is other than a circle, for example an oval or a rectangle or other geometric shape. Thus, defective assemblies may be reduced and product yield rates may be improved by structures such as shown and described in FIGS. 6 and 7.

[0021] FIG. 8 is a top plan view of a flipchip die and substrate assembly a type having cross-sectional configuration which may be the same as illustrated in FIGS.6 and 7. In this embodiment, the traces 214, 220, 222, etc., each have a first end 262 and a second end 264. The first ends 262 and the second ends 264 of adjacent traces, e.g. 214, 220, are staggered. As a result the first ends 262 of every other trace, e.g., 220, 222, etc., terminate at the same imaginary line AA and the first ends 264 of the other traces 214, etc., are positioned substantially inwardly of line AA. The same relationship exists with respect to the second ends 264 of the traces and the imaginary line BB. The edge of the solder resist layer 230 may lie along or outwardly of lines AA and BB. An advantage of this positioning over the prior art positioning of traces, where the traces in any array of parallel traces all begin at the same imaginary line and end at the same imaginary line, is that the total length of the traces

on the substrate 210 of FIG. 8 is substantially reduced. Also, if the inwardly positioned ends 262 or 264 of adjacent traces are terminated such that there is no overlap between adjacent traces, as shown in FIG. 8, then the possibility of a short between adjacent traces is substantially reduced. (The phrase "adjacent traces" as used herein refers to traces having adjacent axes, even when the traces themselves are of lengths that are not even partially coextensive.) As a result, the lateral distance between traces may be reduced, enabling a denser design and thus use of associated CuP flipchip dies with higher pitches. Also shorter length traces may reduce the possibility of Cu migration and certain undesirable electrical effects such as parasitic capacitance. It also enables the use of larger solder resist openings and thus enables the use of a substrate design that is easier to manufacture than those of the prior art.

[0022] FIG. 9 is a block diagram of A method of forming a copper pillar attach substrate. The method includes as shown at 302, providing a substrate with a dielectric layer. The method also includes, as shown at 304, forming a plurality of parallel traces on the dielectric layer. The method further includes, as shown at 306, applying a solder resist layer over the plurality of parallel traces and includes as shown at 308, forming openings in the solder resist layer that exposes an intermediate portion of each trace. The method further includes, as shown at 310, coating the exposed intermediate portion of each of the traces with conductive material that extends to a height above the height of the solder resist layer.

[0023] Those skilled in the art will appreciate that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An electronic assembly comprising:

a copper pillar attach substrate comprising:

a dielectric layer;

a solder resist layer overlying the dielectric layer, the solder resist layer having a plurality of openings therein and having a solder resist layer thickness; and

a plurality of parallel traces formed on the dielectric layer, each trace having a first end portion, a second end portion and an intermediate portion, the first and second end portions being covered by the solder resist layer, the intermediate portions being positioned in the openings in the solder resist layer, each of the intermediate portions having at least one conductive coating layer thereon and having a height measured from the dielectric layer to a topmost one of the at least one conductive coating layer that is at least as great as the solder resist layer thickness.

2. The assembly of claim 1, the at least one conductive coating layer comprising a first conductive coating layer and a second conductive coating layer.

3. The assembly of claim 2, the first conductive coating layer comprising copper.

4. The assembly of claim 2, the second conductive coating layer comprising tin.

5. The assembly of claim 1, the traces comprising copper.

6. The assembly of claim 1, the openings in the solder resist layer being staggered.

7. The assembly of claim 1, adjacent ones of the plurality of parallel traces being separated by a trace spacing distance, the solder resist layer openings being staggered, and further comprising a die having a plurality of copper pillars, each of the copper pillars having a tip portion connected to the intermediate portion of an associated one of the plurality of

traces; each of the copper pillars having a cross-sectional dimension measured perpendicular to the parallel traces that is greater than a dimension of an associated one of the solder resist openings measured perpendicular to the parallel traces.

8. The assembly of claim 7 the tip portion of each of the copper pillars being bonded to the at least one coating layer on the intermediate portion of an associated one of the plurality of traces.

9. The assembly of claim 8, the at least one conductive coating layer on the intermediate portion of each of the plurality of traces comprising a first coating layer and second coating layer over the first coating layer, the solder tip portion of the copper pillar being bonded to the second coating layer.

10. The assembly of claim 9, the first coating layer being thicker than the second coating layer.

11. The assembly of claim 7, the solder tip portions each having a circular cross section.

12. The assembly of claim 1 the plurality of parallel traces being positioned in an area defined by a first line perpendicular to the traces and intersecting an outermost one of the trace first end portions and a second line perpendicular to the traces and intersecting an outermost one of the trace second end portions and wherein the plurality of traces each has a length less than distance between the first line and the second line.

13. The assembly of claim 12 wherein the plurality of traces each has a length less than one half the distance between the first line and the second line.

14. The assembly of claim 12 wherein the layer of solder resist extends at least to the first line and to the second line in a region extending from at least a first one of the plurality of parallel traces to at least a last one of the plurality of parallel traces.

15. An electronic assembly comprising:

a copper pillar attach substrate comprising:

a dielectric layer;

a solder resist layer overlying the dielectric layer, the solder resist layer having a plurality of openings therein and having a solder resist layer thickness; and

a plurality of parallel traces formed on the dielectric layer, each trace having a first end portion, a second end portion and an intermediate portion, the first and second end portions being covered by the solder resist layer, the intermediate portions being positioned in the openings in the solder resist layer, the plurality of parallel traces being positioned in an area defined by a first line perpendicular to the traces and intersecting an outermost one of the trace first end portions and a second line perpendicular to the traces and intersecting an outermost one of the trace second end portions and wherein the plurality of traces each has a length less than distance between the first line and the second line.

16. The assembly of claim 15, wherein the plurality of traces each has a length less than one half the distance between the first line and the second line.

17. The assembly of claim 15, wherein the layer of solder resist extends at least to the first line and to the second line in a region extending from at least a first one of the plurality of parallel traces to at least a last one of the plurality of parallel traces.

18. A method of forming a copper pillar attach substrate, comprising:

providing a substrate with a dielectric layer;

forming a plurality of parallel traces on the dielectric layer;

applying a solder resist layer over the plurality of parallel traces,

forming openings in the solder resist layer that exposes an intermediate portion of each trace; and

coating the exposed intermediate portion of each of the traces with conductive material that extends to a height above the height of the solder resist layer.

19. The method of claim 18 wherein the forming a plurality of parallel traces on the dielectric layer comprises staggering the starting point and the ending point of parallel traces such that the lengths of adjacent traces do not overlap.

20. The method of claim 18 wherein the forming openings in the solder resist layer that exposes an intermediate portion of each trace comprises forming staggered openings.

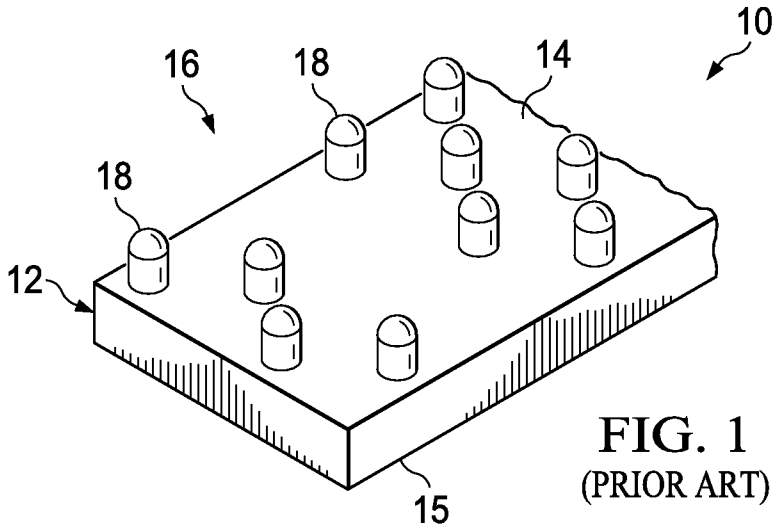


FIG. 1
(PRIOR ART)

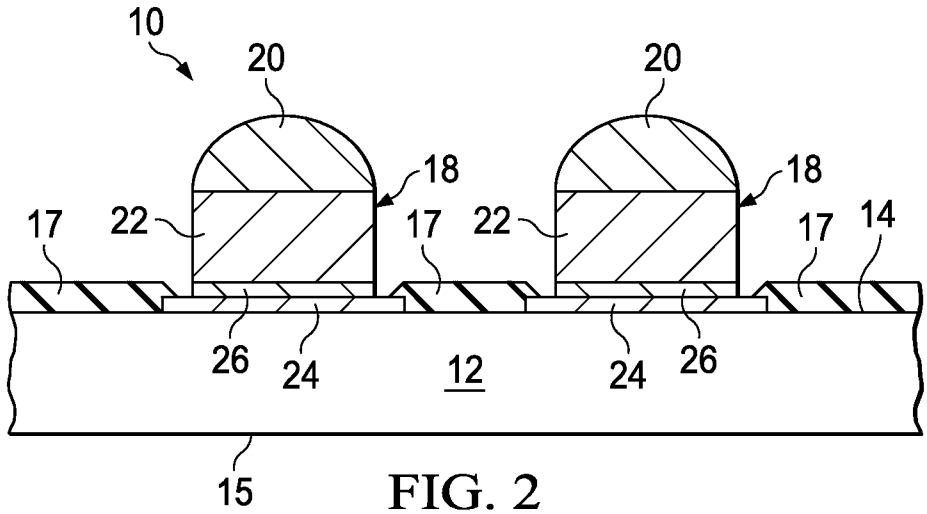


FIG. 2
(PRIOR ART)

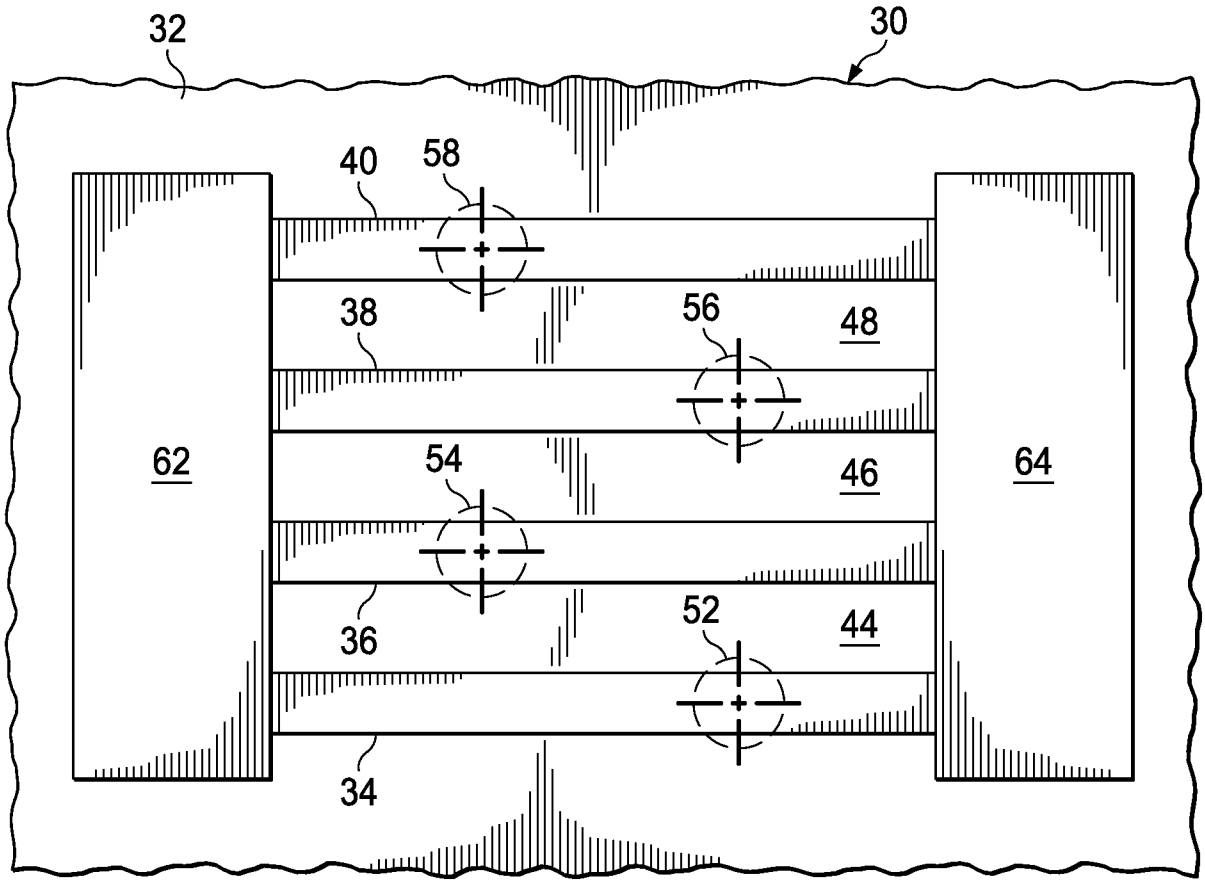


FIG. 3
(PRIOR ART)

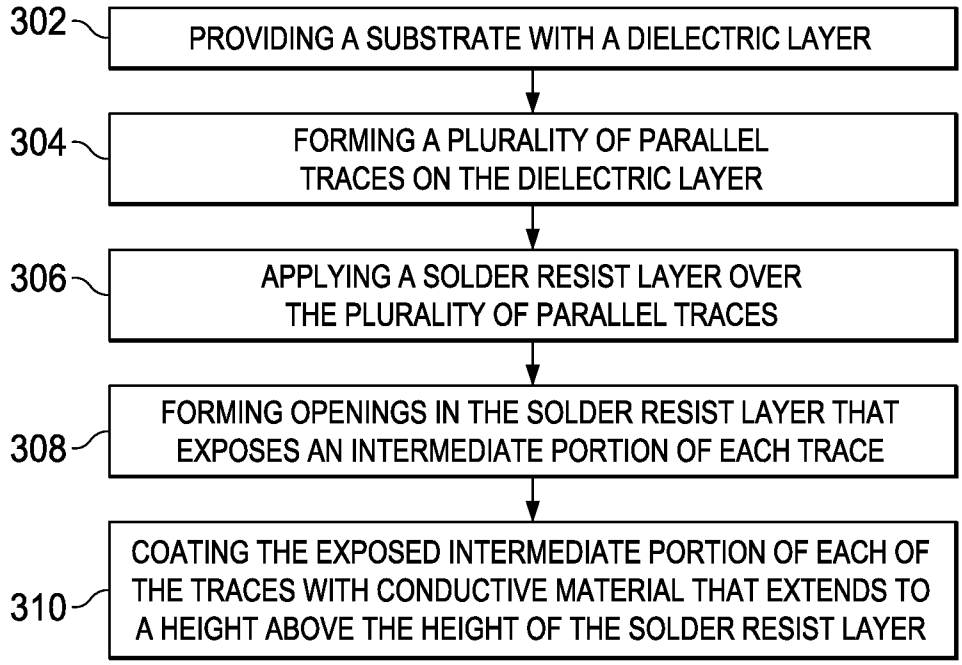


FIG. 9

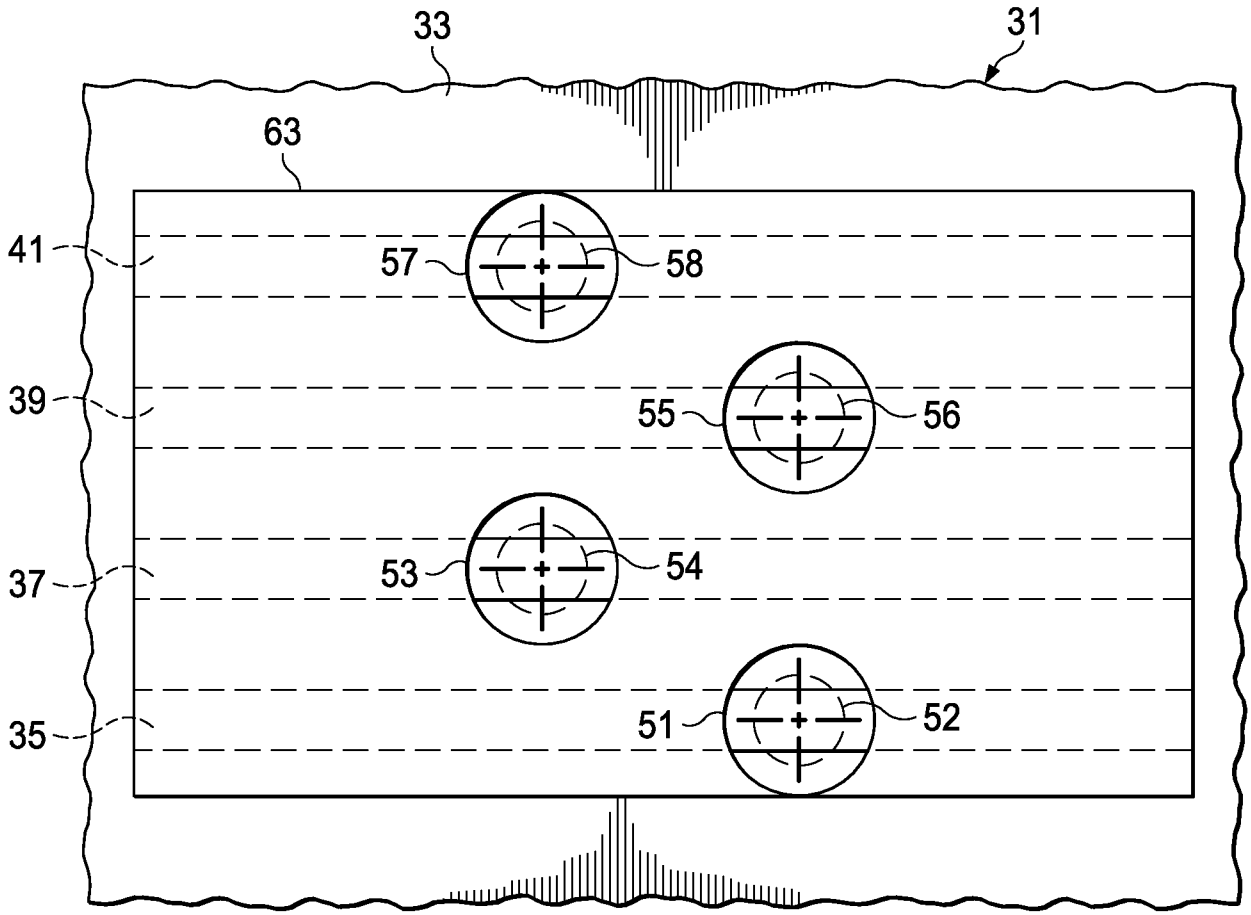


FIG. 4
(PRIOR ART)

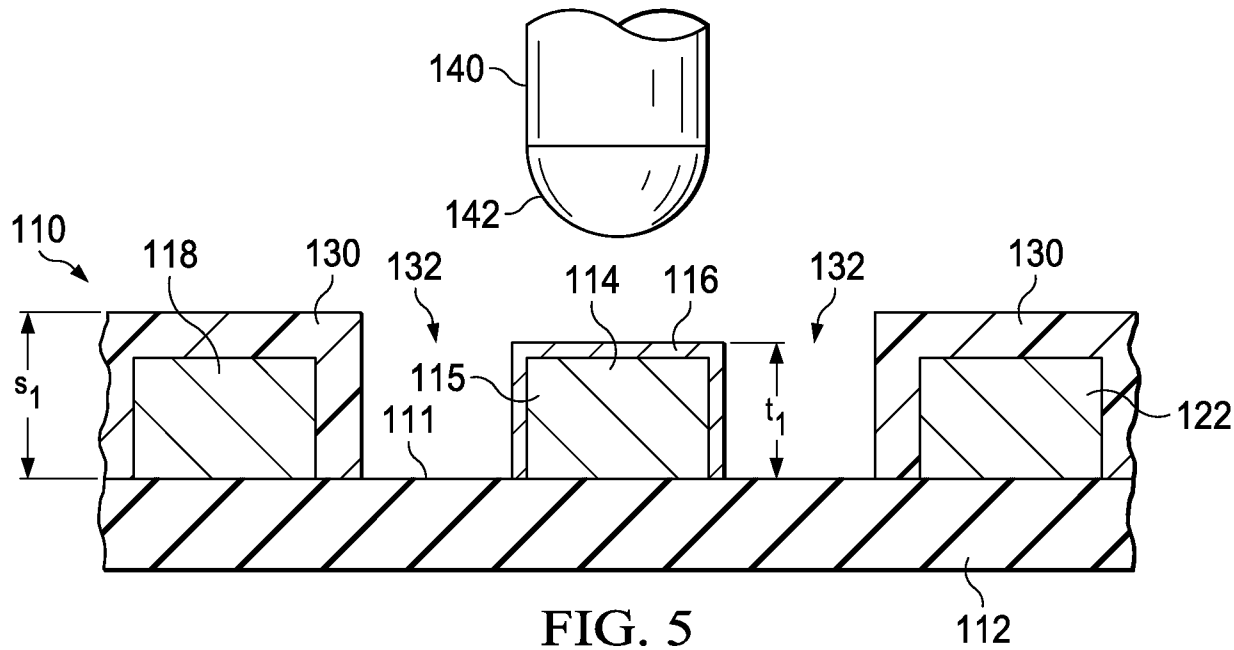
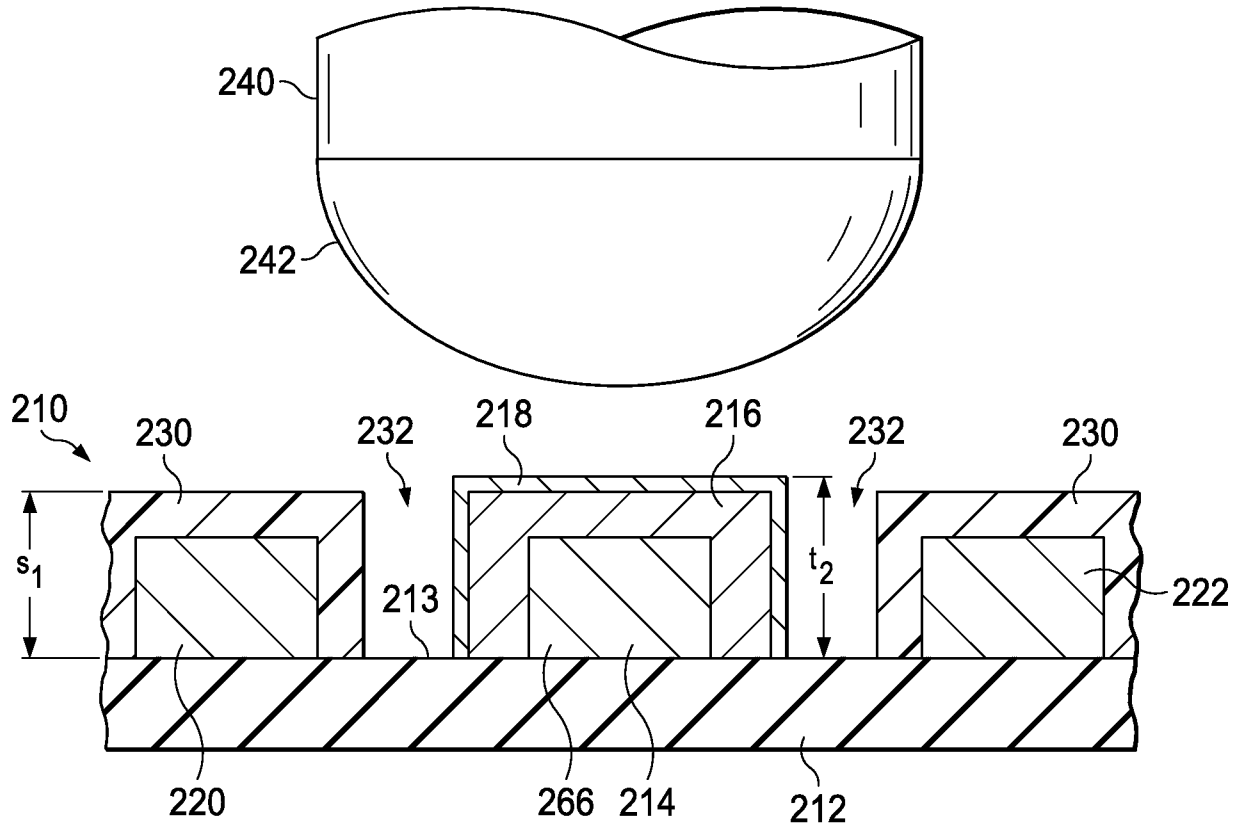


FIG. 5
(PRIOR ART)


240
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s_1
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t_2
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220
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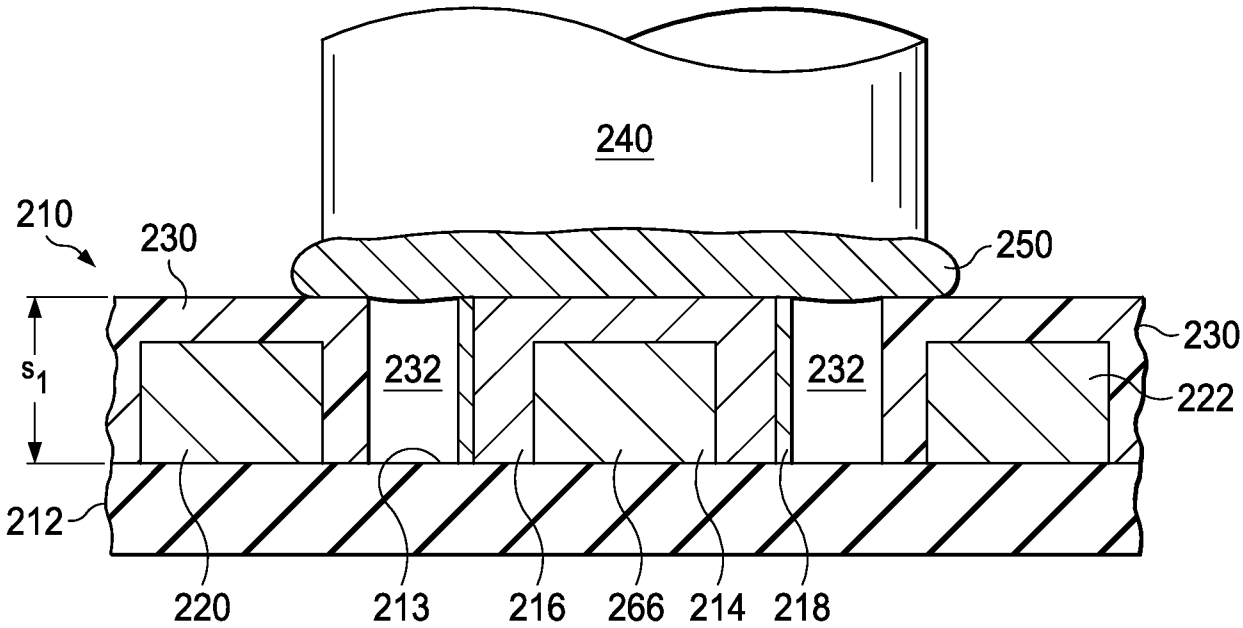
214
212

FIG. 6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s_1
232
232
230
222
212
220
213
216
266
214
218

FIG. 7

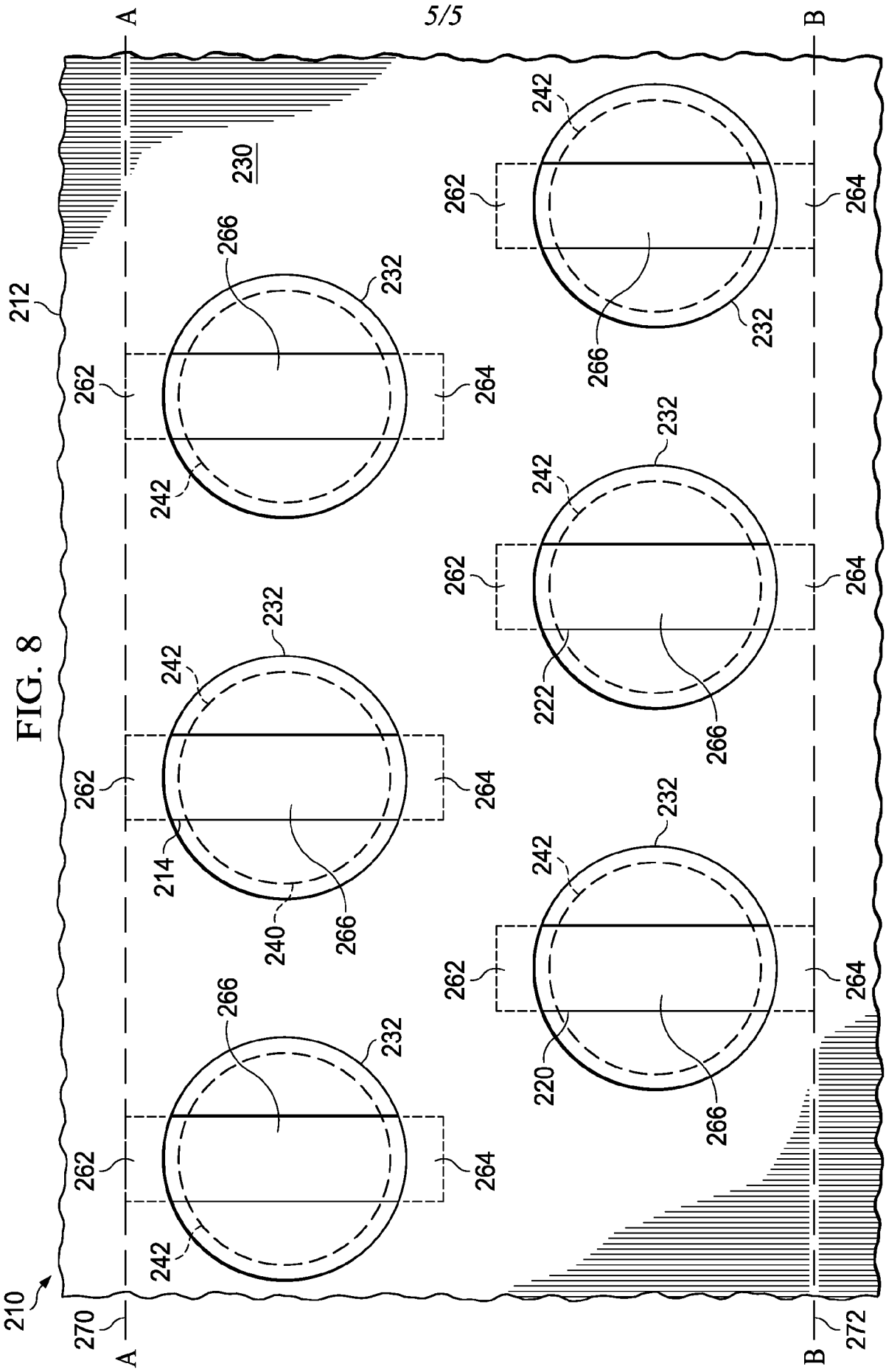

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/022334

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/52 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/02, 23/00, 23/52, 25/00, 27/01

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Fine Pitch Copper Pillar Flip Chip. Technology Solutions. Amkor Technology Rev Date: 6/10 [online]. Retrieved from the Internet: <URL: http: http://www.amkor.com/go/Copper-Pillar-Flip-Chip>, p. 1-3	15-17
Y		1-14, 18-20
Y	US 2011/0260316 A1 (STATS CHIPPAC, LTD.) 27.10.2011, par. [0045], [0048], [0052], fig. 4j, 6e	1-14, 18-20
A	US 2011/0149452 A1 (SKYWORKS SOLUTIONS, INC.) 23.06.2011	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 June 2014 (16.06.2014)	10 July 2014 (10.07.2014)
Name and mailing address of the ISA/ FIPS Russia, 123995, Moscow, G-59, GSP-5, Berezhkovskaya nab., 30-1 Facsimile No. +7 (499) 243-33-37	Authorized officer S. Grechishnikov Telephone No. 499-240-25-91

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