April 4, 1967 W. K. SONNEMANN 3,312,867

STATIC TIME-OVERCURRENT RELAYS

Filed April 26, 1963 2 Sheets-Sheet 1

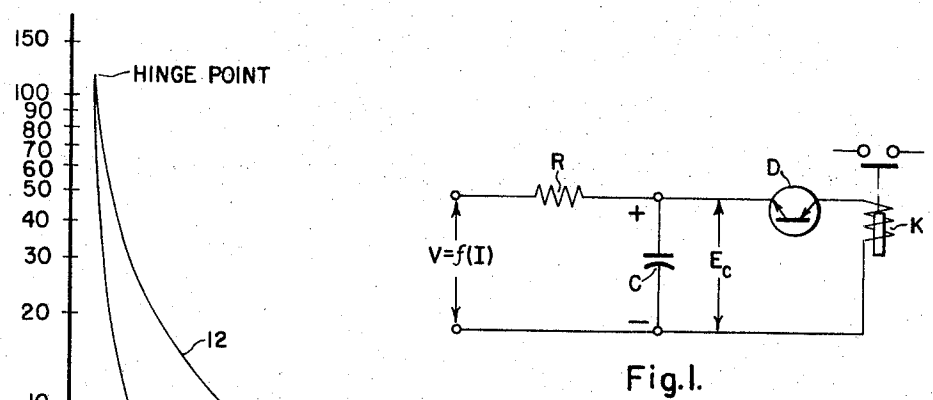


Fig.1.

Fig.2.

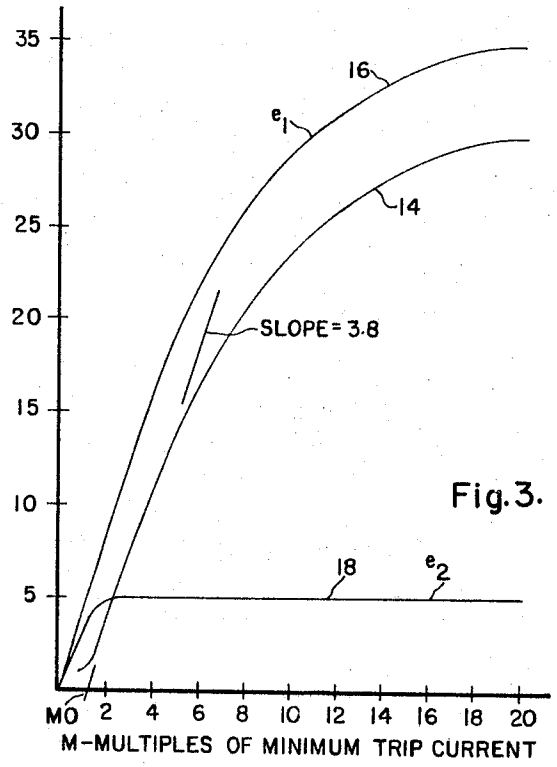


Fig.3.

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STATIC TIME-OVERCURRENT RELAYS

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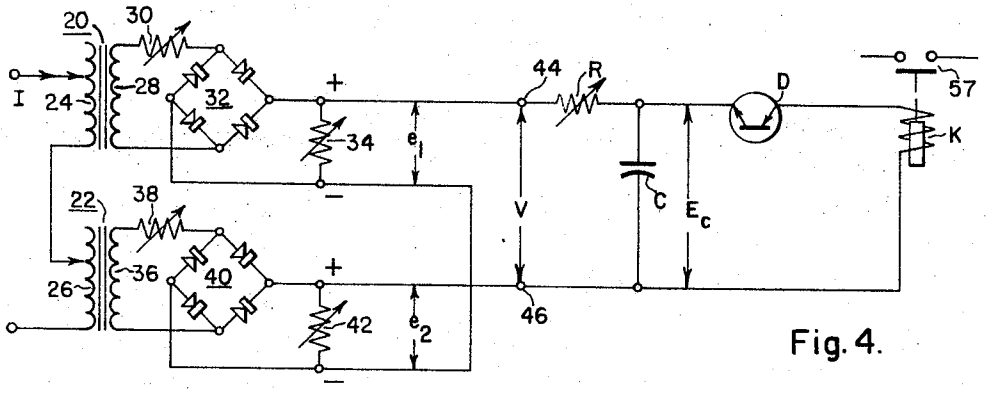


Fig. 4.

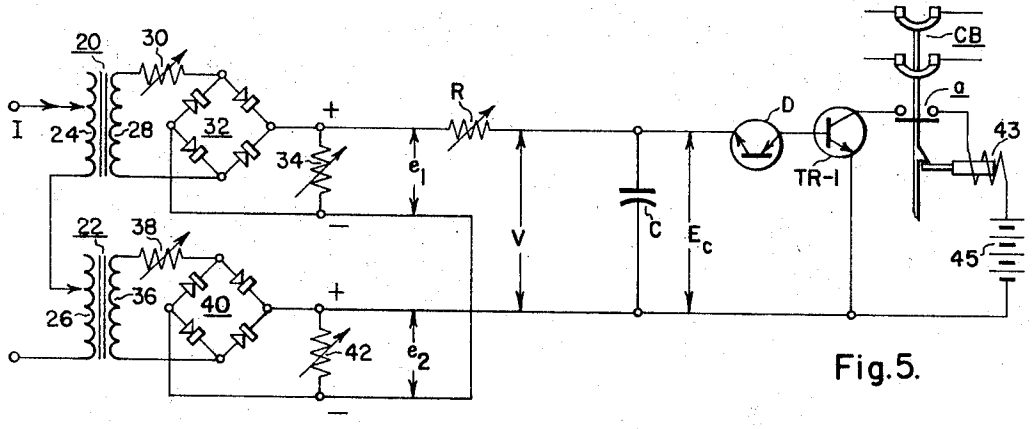


Fig. 5.

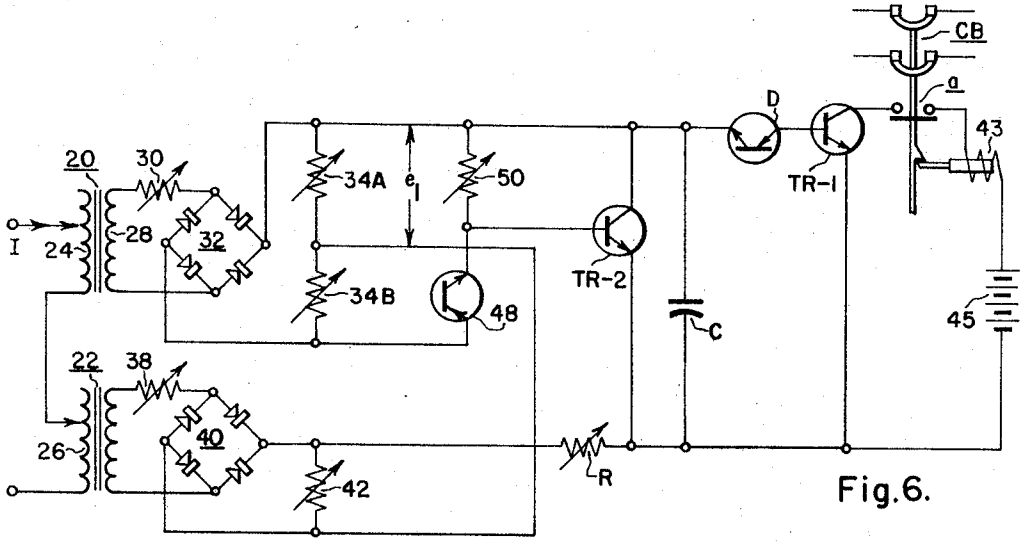


Fig. 6.

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STATIC TIME-OVERCURRENT RELAYS

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This invention relates to time delay relays which are designed to trip when an overcurrent condition persists in a circuit, the time required to trip the relay being a function of the degree of overcurrent. More particularly, the invention relates to protective relays of the type described having static components.

Relays can be actuated by various existing static circuits capable of achieving a time delay which decreases as current through a circuit increases above a lower minimum trip value; and in this respect they are somewhat similar in function to the induction disc type relay. Such circuits, however, do not have the same time-current curve as induction disc time-overcurrent relays, meaning that they cannot be substituted in power systems designed in reliance upon the time-current characteristics of the induction disc type relay.

As an overall object, the present invention provides novel time-overcurrent relay circuits employing static components.

More specifically, an object of the invention is to provide a static time-overcurrent relay having a time-current curve which closely approximates that of induction disc type relays presently in use, thereby enabling the substitution of such static relays in existing power systems.

Still another object of the invention is to provide a novel static time-overcurrent relay incorporating positive means for preventing tripping of the relay below a minimum current value, regardless of the time during which that current value persists.

In accordance with the invention, the time-current curve of an induction disc type relay is approximated by passing the current which is to be monitored through the primary windings of a pair of transformers connected in series. One of the transformers is designed to saturate at realtively high voltage and current conditions, while the other transformer is designed to saturate at low voltage and current conditions. By rectifying voltages appearing across the secondaries of the transformers and by combining the rectified voltages in opposing relationship, a single voltage is derived which, when applied across a resistance-capacitance delay network, will cause the voltage across the capacitance to reach a predetermined trip value in accordance with a time-current curve closely approximating that of the induction disc type relay. The circuit is completed by a device, such as a diode back-biased by the voltage across the capacitance, which will break down to permit the capacitance to discharge through a utilization device when the voltage across the capacitance reaches the aforesaid trip value.

The above and other objects and features of the invention will become apparent from the following detailed description taken in connection with the accompanying drawings which form a part of this specification, and in which:

FIGURE 1 is a schematic circuit diagram of a resistance-capacitance delay network which is used, in combination with other circuit elements, in providing the static time-overcurrent relay of the invention;

FIG. 2 is a graph illustrating the time-current characteristic of the network of FIG. 1 as compared with that of a conventional induction disc time-overcurrent relay;

FIG. 3 is a graph of current expressed as multiples of minimum trip time versus voltage applied to a resistance-capacitance network such as that of FIG. 1, showing the manner in which the desired voltage characteristic is obtained in accordance with the invention;

FIG. 4 is a schematic circuit diagram of one embodiment of the invention;

FIG. 5 is a schematic circuit diagram of another embodiment of the invention employing a transistor switch device; and

FIG. 6 is a schematic circuit diagram of still another embodiment of the invention employing means to prevent tripping of a relay below a minimum current value, regardless of the time duration of that current value.

Referring to FIG. 2 of the drawings, a curve **10** represents the time curve of a standard type CO–8 induction disc time overcurrent relay manufactured by the Westinghouse Electric Corporation at Newark, N.J., for the #11 time dial setting. In FIG. 2 ordinates t represent time and abscissas M represent multiples of minimum trip current. This curve includes a point represented by $M=1.3$ and $t=115.6$. I now will consider the problem of developing a comparable time curve by a static network.

Referring to FIG. 1 a conventional resistance-capacitance network is shown for obtaining time delay wherein the input voltage, $V=f(I)$, is used to charge a storage device, preferably a capacitor C, with the polarity shown. Connected across the capacitor C is a diode D in series with the energizing coil of a utilization device such as a relay K. Diode D is of the type known as a Beckman diode or a Dynistor (trademark) threshold diode of the type manufactured by Westinghouse Electric Corporation. The diode D is biased in the back direction by the voltage across capacitor C, and its characteristics are such that it resists the flow of current with an exceptionally high value of resistance until a critical threshold voltage is reached, after which it breaks down and allows current to flow with very little resistance through the energizing coil of relay K. The time delay of a circuit such as that shown in FIG. 1 is dependent upon the values of resistor R and capacitor C, as well as the applied voltage V, in logarithmic fashion. Thus,

$$t=\frac{RC}{.434}\ \text{Log}\ \frac{V}{V-1} \qquad (1)$$

If $V=M$ and the curve represented by this equation is to include the point on the curve **10** designated above by $M=1.3$ $(=V)$ and $t=115.6$, then

$$t=181.5\ \text{Log}\ \frac{V}{V-1} \qquad (2)$$

where

t=trip time
R=resistance of resistor R
C=capacitance of capacitor C
V=input voltage which may be expressed in multiples of a unit value, wherein a unit corresponds to that threshold value of the voltage E_c across the capacitor C required to fire the diode D.

Although a circuit such as that shown in FIG. 1 could be used for time-overcurrent relay applications, its time-current characteristic does not correspond to that of conventional induction disc time-overcurrent relays presently in use.

Using the Equation 2 given above, the curve for the resistance-capacitance circuit of FIG. 1 turns out to be as shown by curve **12** in FIG. 2. The point defined by $V=M=1.3$ and $t=115.6$ serves as a "hinge point" for the two curves. It is, of course, obvious that curve **12** does not fit curve **10**; and, accordingly, a time delay circuit such as that shown in FIG. 1 cannot, by itself, be used to replace an induction disc time-overcurrent relay corresponding to the curve **10**.

As was explained above, the present invention is concerned with providing means whereby a static arrangement such as that shown in FIG. 1 can be made to produce a curve which will fit curve **10** in FIG. 2. It is apparent that furnishing the voltage $V=f(I)$ from the rectified output of a single saturating transformer is not what is required. That is, the output of a saturated transformer diminishes from a fixed ratio to the primary current; whereas it can be seen from a comparison of curves **10** and **12** in FIG. 2 that the opposite is desired. In other words, the output of some desired device to furnish $V=f(I)$ should yield an increasing ratio of V to I (or M) as the current increases.

With reference to FIG. 3, curve **14** represents the voltage input to the circuit of FIG. 1 as a function of current in order to achieve a time-current characteristic approximating that of an induction disc time-overcurrent relay. Curve **14** of FIG. 3 was calculated from the data of Table I as follows:

values of current by saturating the iron of the transformer which produces the curve. Similarly, it is conceivable that a curve with an increasnig slope at lower values of current could be produced in a transformer design by working the iron at very low values of induction. However, to have the bend at the low end of the scale, corresponding to the toe of the saturation curve, come out properly to fit design specifications and at the same time bend over properly to equally exacting specifications at the high values of current is a quite impractical task.

It is, however, practical to design a transformer which will have a substantially straight-line output curve up to saturation and then bend over, as shown by curve **16** of FIG. 3. This curve has been drawn on the basis of $e_1=3.8M$ (i.e., the slope is 3.8) up to $M=5$. In accordance with the present invention, another transformer, having a V–M curve **18** as shown in FIG. 3 is provided to furnish an output which is subtracted from curve **16**, thereby achieving the desired curve **14**. The method for

TABLE I

[Establish RC at $M_{20}=20$; $V_{20}=30$ p.u.; $t_{20}=2.18$]

$$t=\frac{RC}{.434}\log\frac{V}{V-1};\quad RC=\frac{t\times.434}{\log\frac{V}{V-1}}$$

$$RC=\frac{2.18\times.434}{\log\frac{30}{29}}=65.3,\text{ whence }V=\frac{1}{1-\epsilon^{-t/65.3}}$$

(1) M	(2) t_c	(3) $t/65.3$	(4) $\epsilon^{-t/65.3}$	(5) $1-\epsilon^{-t/65.3}$	(6) V	(7) $e'_1=3.8M$	(8) e'_2	(9) e_1	(10) e_2
1.0					1.0	3.8	2.8	3.8	2.8
1.3	115.6	1.77	.1702	.8298	1.205	4.94	3.735	4.94	3.735
2	27.03	.414	.661	.339	2.95	7.6	4.65	7.6	4.65
3	11.04	.1692	.8442	.1558	6.42	11.4	4.98	11.4	4.98
4	6.64	.1017	.9035	.0965	10.37	15.2	4.83	15.37	5
5	4.91	.0752	.9275	.0725	13.80	19.0	5.2	18.8	5
6	4.07	.0623	.9395	.0605	16.54	22.8	6.26	21.54	5
8	3.27	.0501	.9511	.0489	20.45	30.4	9.95	25.45	5
12	2.62	.0401	.9608	.0392	25.5	45.6	20.1	30.5	5
16	2.32	.0355	.9652	.0348	28.75	60.8	32.05	33.75	5
20	2.18	.0334	.9671	.0329	30.0	76.0	46.0	35.00	5

With reference to the foregoing Table I, the first two columns represent data taken from the published characteristics of the type CO–8 induction disc time-overcurrent relay mentioned above with the #11 time dial setting. The current is expressed as M which is a multiple of minimum trip, and t_c, seconds to trip, is expressed in seconds. At the top of Table I, the work indicates that the voltage, V, has been arbitrarily assumed to be 30 per unit at $M=20$. Some other value could be used, but this was arbitrarily chosen. The 30 per unit means that the value of this voltage is 30 times the value for E_c from FIG. 1 which will cause the diode D to break down and actuate whatever device is to be actuated. With these assumptions, RC was calculated to be 65.3 as shown. From this, and utilizing the formula which is applicable to this type of circuit, desired values for V were calculated as shown in the sixth column of Table I. The values for V from Table I are plotted as curve **14** in FIG. 3. It is to be noted that this curve has a straight-line section where the slope, $\Delta V/\Delta M$ is 3.8, after which, at higher values of M, it exhibits something similar to the saturation characteristic of transformers. It should be noted, however, that if this straight-line section is projected downwardly, it intersects the M axis at about 1.3, indicated by M_0.

At the current value $M=1$, the voltage $V=1$. At $M=1.3$, the voltage $V=1.205$, and the slope of this change is 0.683, considerably less than the slope of 3.8 for the straight-line portion. Beyond the value of $M=5$, the calculated curve **14** for V bends over like a saturation curve. Curves can be made to bend over at higher

deriving data for transformers having the characteristic curves **16** and **18** of FIG. 3 is illustrated by columns 7, 8, 9 and 10 in Table I above. In column 7, e'_1 is tabulated as a straight-line curve all the way to $M=20$, where $e'_1=76$. The respective values of V from column 6 were subtracted from values of column 7, yielding column 8 for e'_2. It will be noted that the values of e'_2 increase in saturation curve fashion to around 5.0 volts, with a little wavering between $M=3$ and $M=5$. After this point, the e'_2 values begin to ascend with an upward sweep. This type of response is not practical either; however, up to $M=5$, with a little wobble around $M=4$, the output e'_2 looks like the output curve of a saturated transformer. Accordingly, in column 10 the values for e_2 were taken from column 8 up to 4.98 volts at $M=3$. From that point on, e_2 is presumed to remain constant at 5 volts, as shown by the table. It is practical to design a transformer yielding this sort of rectified output. With column 10 thus established, these values were added to the values for V from column 6, resulting in e_1, column 9. Column 9 is plotted as curve **16** in FIG. 3. It is practical to design a transformer having such a rectified output curve. Thus, by designing transformers having rectified output curves e_1 and e_2, FIG. 2, and taking the difference between them, curve **14** for V results with only slight inaccuracies.

A circuit illustrating the manner in which curve **14** can be derived is shown in FIG. 4. It comprises a pair of transformers **20** and **22** having their primary windings **24** and **26**, respectively, connected in series. The current I of a circuit to be monitored is passed through both of

the primary windings **24** and **26** as shown. Connected across the secondary winding **28** of transformer **20** is a variable resistor **30** and a full-wave rectifier **32**, the output of rectifier **32** appearing across variable resistor **34** and identified as e_1. In a similar manner, the secondary winding **36** of transformer **22** is connected across the series combination of a variable resistor **38** and a full-wave rectifier **40**, the output of the rectifier **40** appearing across variable resistor **42** as voltage e_2. The voltages e_1 and e_2 correspond to the curves **18** and **16**, respectively, of FIG. 3. That is, the rectified output e_1 of transformer **20** is made to agree wth curve **16** of FIG. 3; while the rectified output e_2 of transformer **22** is made to agree with curve **18** of FIG. 3. Resistors **34** and **42** are provided for calibration adjustment. Similarly, resistors **30** and **38** are shown as variable resistors for the purposes of calibration adjustment.

It will be noted that the resistors **34** and **42** are connected in series opposition with the result that the voltages e_1 and e_2 are combined in opposing relationship to produce a difference voltage shown as V in FIG. 4. Beyond points **44** and **46**, the circuit of FIG. 4 is the same as that of FIG. 1 and comprises a resistor R and a capacitor C. Across the terminals of capacitor C is a diode D of the type described in connection with FIG. 1, and the energizing coil of a trip relay K.

With the arrangement shown, the voltage V, which is the difference between e_1 and e_2, will charge capacitor C through the variable resistor R. The correct setting of the variable resistor R to use in connection with the capacitor C to obtain the desired time curve **14** of FIG. 3 is dependent somewhat upon the internal resistances of the sources behind points **44** and **46**. However, adjustment of the value of resistor R will yield time curves corresponding to different time dial settings on the present induction disc time-overcurrent relays, inasmuch as the time of operation is linear with respect to R as shown by the formulas in Table I.

When the capacitor C charges to a fixed value, E_c, the diode D breaks down and allows the capacitor to discharge through the energizing coil of trip relay K, thereby closing contacts **57** which are used in the trip circuit for a circuit breaker or the like, not shown. The diode D, as in the circuit of FIG. 1, is such that it resists the flow of current with an exceptionally high value of resistance until a critical voltage is reached, after which it breaks down and allows current to flow with very little resistance. In all of the foregoing, the breakdown value E_c is taken as one per unit. For example, in Table I, at $M=20$, $V=30$. This means that for this line of the table the voltage V is thirty times the breakdown voltage E_c, or 30 per unit.

With reference now to FIG. 5, the circuit is similar to that of FIG. 4; and, accordingly, elements in FIG. 5 which correspond to those shown in FIG. 4 are identified by like reference numerals. The diode D is used as before, but instead of a trip relay such as K in FIG. 4, transistor TR–1 is used directly in the trip circuit for the circuit breaker CB which includes trip coil **43**, battery **45** and a switch *a* which is closed when the circuit breaker is closed and open when the circuit breaker is open. The transistor TR–1 may be a silicon-controlled-rectifier of the type which, once it is "triggered off," by a discharge through the diode D presents a low restistance to the flow of current through the trip coil **43** until such time as the current is interrupted by the opening of a switch, such as the switch *a* of FIG. 5, the switch *a* being the usual *a* switch of the breaker. The arrangement shown in FIG. 5 is thus a completely static time-overcurrent relay arrangement.

From the foregoing, it is apparent that the circuits of FIGS. 4 and 5 provide means whereby a static time-overcurrent relay may be constructed to yield time curves duplicating those now existing with induction disc time-overcurrent relays. This is accomplished in accordance with the foregoing explanation by combining the rectified output of transformer **20**, which is designed to saturate at high voltage and current conditions, in opposing relationship with the rectified output of transformer **22** which is designed to saturate at low voltage and current conditions. There is, however, one disadvantage to the circuits illustrated in FIGS. 4 and 5. This is due to the fact that the capacitor C of both circuits will be partially charged by the flow of load current below the desired minimum trip value. Minimum trip occurs, of course, when E_c is just equal to the breakdown value of the diode D. The capacitor may be partially charged to this voltage by the flow of load current prior to the occurrence of a short-circuit current on the system. This, of course, is undesirable inasmuch as it would alter the time of operation.

In FIG. 6 a circuit is shown which eliminates the possibility of the capacitor being partially charged by the flow of load current prior to the occurrence of a short-circuit current on the system. Here, again, elements in FIG. 6 which correspond to those shown in FIG. 4 or 5 are identified by like reference numerals. It will be noted, however, that the resistor **34** is now replaced by serially-connected resistors **34A** and **34B**. Connected in shunt with the resistors **34A** and **34B** is a diode **48** and a variable resistor **50**. The diode **48**, like diode D, is of the Beckman type described above characterized in that it resists the flow of current with an exceptionally high value of resistance until a critical voltage is reached, after which it breaks down and allows current to flow with very little resistance. The junction of diode **48** and resistor **50** is connected to the base of transistor TR–2 connected in shunt with capacitor C.

The constants of FIG. 6 are such that the breakdown voltage of diode **48** occurs at the desired minimum trip point. That is, it occurs when the current I passing **20** and **22** reaches the minimum point at which the circuit through the primary windings **24** and **26** of transformers breaker CB should trip. Diode **48** is energized, as shown, through the resistor **50** across a voltage which is equal to the voltage e_1 multiplied by the ratio of the sum of the resistances of resistors **34A** and **34B** over the resistance of resistor **34A**.

At current values below the minimum trip, the diode **48** does not conduct. Thus, the base and the collector of transistor TR–2 are both positive with respect to the emitter. Consequently, the transistor conducts and the capacitor C is short circuited. When the current I in the primary windings **24** and **26** of transformers **20** and **22** reaches the minimum trip value, the diode **48** conducts and lowers the potential on the base of transistor TR–2, well below the potential on the emitter of the transistor TR–2. Transistor TR–2 now becomes non-conducting and the circuit functions in the same way as previously described for FIGS. 3, 4 and 5. Thus, means are provided with the circuit of FIG. 6 to keep the capacitor C from partially charging at current values lower than minimum trip.

Another advantage of the arrangement of FIG. 6 is that it provides a "quick reset" feature. For example, if the current I through the primaries of the transformers does not flow long enough at values higher than the minimum trip value to cause operation, then it is desirable for the device to reset itself. Such short duration currents occur on power systems when a fault is cleared by some other breaker; and in such cases, it is often desirable for the time-overcurrent relay to reset itself quickly. In the case of circuits shown in FIG. 6, when the current subsides below the minimum trip value, the diode **48** becomes non-conducting, which, in turn, causes transistor TR–2 to become conducting. This causes an immediate short circuit of the condenser C and removes any residual charge thereon, thereby providing for quick reset.

If a Beckman diode is used for diode **48**, the resistor **50** must be chosen such that the diode will operate on the critical part of its curve so that any slight diminution in

current would cause it to immediately shut off. This is called the "hold current" value. Although a Beckman diode is desirable for this purpose, it should be noted that a Zener diode could also be used at the same point in the circuit to accomplish the same purpose. The resistor 34B is chosen such that, with the diode 48 conducting, the potential on the base of transistor TR–2 will always be negative with respect to the potential on its emitter, even though the current from right to left through resistor R from the emitter of transistor TR–2 has reached a minimum value just prior to charging the capacitor C to the critical voltage E_c where operation occurs. This is important at relatively low current values where the time of operation of the device is quite long, such as 115.6 seconds.

Although the invention has been shown in connection with certain specific embodiments, it will be readily apparent to those skilled in the art that various changes in form and arrangement of parts may be made to suit requirements without departing from the spirit and scope of the invention.

I claim as my invention:

1. A time-overcurrent relay comprising a pair of transformers each having primary and secondary windings thereon, one of said transformers being designed to saturate at high voltage and current conditions and the other transformer being designed to saturate at low voltage and current conditions, means for passing current to be monitored through both of said primary windings, circuit means for combining electrical quantities proportional to voltages appearing across said secondary windings in opposing relationship to produce a single voltage proportional to the difference between said first-mentioned voltages, a capacitor, means for applying said single voltage across said capacitor, a utilization device, and means for discharging said capacitor through the utilization device when the voltage across said capacitor reaches a predetermined magnitude.

2. A time-overcurrent relay comprising a pair of transformers each having primary and secondary windings thereon, one of said transformers being designed to saturate at high voltage and current conditions and the other transformer being designed to saturate at low voltage and current conditions, means for passing current to be monitored through both of said primary windings, means for rectifying voltages appearing across the secondary windings of said transformers, means for combining said rectified voltages in opposing relationship to produce a single voltage proportional to the difference between said first-mentioned rectified voltages, a capacitor, means for applying said single voltage across said capacitor, a utilization device, and means for discharging said capacitor through the utilization device when the voltage across the capacitor reaches a predetermined magnitude.

3. A time-overcurrent relay comprising a pair of transformers each having primary and secondary windings thereon, one of said transformers being designed to saturate at high voltage and current conditions and the other transformer being designed to saturate at low voltage and current conditions, means for connecting said primary windings in series and for passing current to be monitored through the series combination of said primary windings, means for rectifying the voltages appearing across the secondary windings of said transformers, means for combining said rectified voltages in opposing relationship to produce a single voltage proportional to the difference between said first-mentioned voltages, a capacitor, means for applying said single voltage across said capacitor, a utilization device, and means including a unidirectional current device for connecting said capacitor to the utilization device, the unidirectional current device being of the type to block the flow of current between the capacitor and the utilization device until the voltage across the capacitor reaches a predetermined magnitude, at which point the unidirectional current device will break down and permit discharge of the capacitor through said utilization device.

4. A time-overcurrent relay comprising a pair of transformers each having primary and secondary windings thereon, one of said transformers being designed to saturate at high voltage and current conditions and the other transformer being designed to saturate at low voltage and current conditions, means for connecting said primary windings in series and for passing current to be monitored through the series combination of said primary windings, means including a first rectifier connected across one of said secondary windings, means including a second rectifier connected across the other of said secondary windings, impedance devices connected across the outputs of said rectifiers, means for connecting said impedance devices in series opposition such that a direct current voltage will appear across the series combination of said impedance devices equal to the difference between the voltages appearing across the respective impedance devices, a capacitor, means including an impedance device for applying said latter-mentioned direct current voltage across said capacitor, a utilization device, and means for discharging said capacitor through the utilization device when the voltage across the capacitor reaches a predetermined magnitude.

5. A time-overcurrent relay comprising a pair of transformers each having primary and secondary windings thereon, one of said transformers being designed to saturate at high voltage and current conditions and the other transformer being designed to saturate at low voltage and current conditions, means for connecting said primary windings in series and for passing current to be monitored through the series combination of said primary windings, means for rectifying voltages appearing across said secondary windings, means for combining said rectified voltages in opposing relationship to produce a single voltage proportional to the difference between said rectified voltages, a capacitor, means for applying said single voltage across said capacitor, a utilization device, a source of voltage of said utilization device, means including a normally cut-off semiconducting device for connecting said voltage source to said utilization device, and means for initiating conduction in said semiconducting device to connect the voltage source to said utilization device when the voltage across the capacitor reaches a predetermined magnitude.

6. In a time-overcurrent relay, the combination of a pair of transformers each having a primary and secondary winding thereon, said transformers being arranged to saturate at different levels of primary current, means for connecting said primary windings in series and for causing a current to flow through the series combination of said primary windings, circuit means for combining electrical quantities proportional to voltages appearing across said secondary windings in opposing relationship to produce a single voltage proportional to the difference between said first-mentioned voltages, a capacitor, means for applying said single voltage across said capacitor, a normally closed switch device connected across said capacitor whereby the capacitor will normally be shorted, means for opening said switch device when a predetermined minimum current flows through said primary windings, a utilization device, and means for discharging said capacitor through the utilization device when the voltage across the capacitor reaches a predetermined magnitude.

7. A time-overcurrent relay comprising a pair of transformers each having a primary and secondary winding thereon, one of said transformers being designed to saturate at high voltage and current conditions and the other transformer being designed to saturate at low voltage and current conditions, means for connecting said primary windings in series and for causing a current to flow through said primary windings, means for rectifying voltages appearing across the secondary windings of said

transformers, means for combining at least portions of said rectified voltages in opposing relationship to produce a single voltage proportional to the difference between said portions of the rectified voltages, a capacitor, means for applying said single voltage across said capacitor, a normally closed transistor switch device connected across said capacitor whereby the capacitor will be normally shorted, means for cutting off said transistor when the current through said primary windings exceeds a predetermined minimum value, a utilization device, and means for discharging said capacitor through the utilization device when the voltage across the capacitor reaches a predetermined magnitude.

8. The relay of claim 7 wherein the means for cutting off said transistor comprises the combination of an impedance element and a unidirectional current device connected in series across the rectifying means associated

with one of said secondary windings, said unidirectional current device being cut off until current through the primary windings reaches a predetermined magnitude, and a connection between the junction of said series-connected impedance element and unidirectional current device and the base of said transistor.

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