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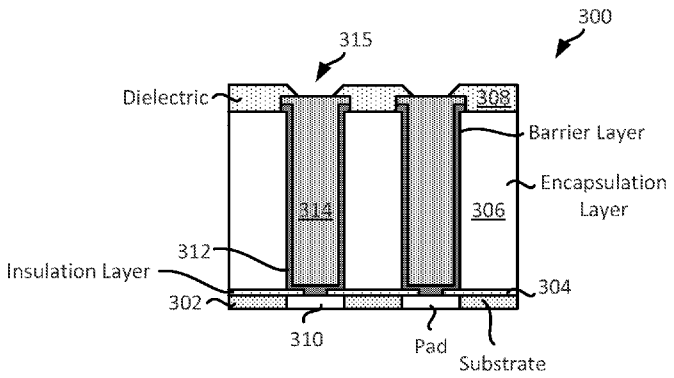


FIG. 3

(57) Abstract: Some novel features pertain to an integrated device that includes an encapsulation layer, a via structure traversing the encapsulation layer, and a pad. The via structure includes a via that includes a first side, a second side, and a third side. The via structure also includes a barrier layer surrounding at least the first side and the third side of the via. The pad is directly coupled to the barrier layer of the via structure. In some implementations, the integrated device includes a first dielectric layer coupled to a first surface of the encapsulation layer. In some implementations, the integrated device includes a substrate coupled to a first surface of the encapsulation layer. In some implementations, the integrated device includes a first die coupled to the substrate, where the encapsulation layer encapsulates the first die. In some implementations, the via includes a portion configured to operate as a pad.

WO 2015/123301 A1

INTEGRATED DEVICE COMPRISING VIA WITH SIDE BARRIER LAYER TRAVERSING ENCAPSULATION LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to U.S. Application No. 14/274,517, entitled "Integrated Device Comprising Via With Side Barrier Layer Traversing Encapsulation Layer", filed May 9, 2014 which claims priority to U.S. Provisional Application No. 61/939,523, entitled "Integrated Device Comprising Via With Side Barrier Layer Traversing Encapsulation Layer", filed February 13, 2014, which are hereby expressly incorporated by reference herein.

BACKGROUND

Field

[0002] Various features relate to an integrated device that includes a via with a side barrier layer that traverses an encapsulation layer.

Background

[0003] FIG. 1 illustrates a first package 102 being coupled to a second package 104. The first package 102 includes a first substrate 106, a first die (e.g., chip) 108, a mold 110, a first set of solder balls 116, and a first set of interconnects 118, and a third set of solder balls 126. The first substrate 106 may include traces and/or vias (both of which are not shown). The second package 104 includes a second substrate 105, a second die 107, a third die 109, a second set of solder balls 115, a first set of wire bonding 117, and a second set of wire bonding 119. The second substrate 105 may include traces and/or vias (both of which are not shown). The second package 104 is positioned above the first package 102.

[0004] The first die 108 is coupled to a first surface (e.g., top surface) of the first substrate 106 through the first set of interconnects 118. The mold 110 encapsulates the first die 108 and the first set of interconnects 118. The first set of solder balls 116 is coupled to a second surface (e.g., bottom surface) of the first substrate 106. The third set of solder balls 126 is coupled to the first surface (e.g., top surface) of the first substrate

106. The third set of solder balls 126 is surrounded by the mold 110. The first substrate 106 includes a set of traces and/or vias that may electrically connect to the first die 108 and/or the first set of solder balls 116.

[0005] The second die 107 and the third die 109 are coupled to a first surface (e.g., top surface) of the second substrate 105. The second die 107 is electrically coupled to the traces and/or vias of the second substrate 105 through the first set of wire bonding 117. The third die 109 is electrically coupled to the traces and/or vias of the second substrate 105 through the second set of wire bonding 119. The second set of solder balls 115 is coupled to a second surface (e.g., bottom surface) of the second substrate 105.

[0006] FIG. 2 illustrates a conventional package on package (PoP) integrated device. As shown in FIG. 2, the integrated device 200 includes the first package 102 and the second package 104 of FIG. 1. As shown in FIG. 2, when the first package 102 is coupled to the second package 104, the second set of solder balls 115 of the second package 104 is coupled to the third set of solder balls 126 of the first package 102.

[0007] One major drawback of the package on package (PoP) configuration shown in FIGS. 1 and 2 is that it creates an integrated device with a form factor that may be too large for the needs of mobile computing devices. That is, the PoP configuration shown in FIG. 2 may be too thick and/or have a surface area that is too large to meet the needs and/or requirements of mobile computing devices. In particular, there is a constant need to reduce the size of integrated devices, especially integrated device that are going to be implemented in mobiles devices. Moreover, the process of fabricating the PoP configuration can be complicated and costly.

[0008] Therefore, there is a need for a cost effective integrated package that has an improved form factor (e.g., smaller, narrower, thinner). Ideally, such an integrated package will provide higher density connections, as well being more cost effective (e.g., cheaper) to fabricate than current integrated packages.

SUMMARY

[0009] Various features, apparatus and methods described herein provide an integrated device that includes a via with a side barrier layer that traverses an encapsulation layer.

[0010] A first example provides an integrated device that includes an encapsulation layer, a via structure traversing the encapsulation layer, and a pad. The via structure includes a via that includes a first side, a second side, and a third side. The via structure

also includes a barrier layer surrounding at least the first side and the third side of the via. The pad is directly coupled to the barrier layer of the via structure.

[0011] According to an aspect, the integrated device includes a first dielectric layer coupled to a first surface of the encapsulation layer. In some implementations, the integrated device includes a second dielectric layer coupled to a second surface of the encapsulation layer.

[0012] According to one aspect, the integrated device includes a substrate coupled to a first surface of the encapsulation layer. In some implementations, the integrated device includes a first die coupled to the substrate, where the encapsulation layer encapsulates the first die. In some implementations, the via structure further comprises a fill.

[0013] According to an aspect, the via includes a seed layer.

[0014] According to one aspect, the via includes a portion configured to operate as a pad.

[0015] According to an aspect, the integrated device includes one of at least an interposer, a package device, and/or a package-on-package (PoP) device.

[0016] According to one aspect, the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

[0017] A second example provides an apparatus that includes an encapsulation layer, a via structure traversing the encapsulation layer, and a pad. The via structure includes a via that includes a first side, a second side, and a third side. The via structure includes a barrier means surrounding at least the first side and the third side of the via. The pad is directly coupled to the barrier layer of the via structure.

[0018] According to an aspect, the apparatus includes a first dielectric layer coupled to a first surface of the encapsulation layer. In some implementations, the apparatus includes a second dielectric layer coupled to a second surface of the encapsulation layer.

[0019] According to one aspect, the apparatus includes a substrate coupled to a first surface of the encapsulation layer. In some implementations, the apparatus a first die coupled to the substrate, where the encapsulation layer encapsulates the first die.

[0020] According to an aspect, the via structure includes a fill means.

[0021] According to one aspect, the via includes a seed layer.

[0022] According to an aspect, the via includes a portion configured to operate as a pad.

[0023] According to one aspect, the apparatus includes one of at least an interposer, a package device, and/or a package-on-package (PoP) device.

[0024] According to an aspect, the apparatus is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

[0025] A third example provides a method for fabricating an integrated device. The method forms a pad on a substrate. The method forms an encapsulation layer on the substrate. The method forms a via structure in the encapsulation layer, where forming the via structure includes (1) forming a barrier layer in the encapsulation layer, and (2) forming a via on the barrier layer, the via comprising a first side, a second side, and a third side, the via is formed on the barrier layer such that the barrier layer surrounds at least the first side and the third side of the via, where the barrier layer is directly coupled to the pad.

[0026] According to an aspect, the method forms a first dielectric layer on a first surface of the encapsulation layer.

[0027] According to one aspect, the method forms a second dielectric layer on a second surface of the encapsulation layer.

[0028] According to an aspect, the method removes at least a portion of the substrate.

[0029] According to one aspect, the method couples a first die to the substrate, where forming the encapsulation layer comprising encapsulating the first die with the encapsulation layer.

[0030] According to an aspect, forming the via structure includes forming a fill.

[0031] According to one aspect, forming the via includes forming a seed layer on the barrier layer.

[0032] According to an aspect, forming the via includes forming a portion a via as a pad.

[0033] According to one aspect, the integrated device comprises one of at least an interposer, a package device, and/or a package-on-package (PoP) device.

[0034] According to an aspect, the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a

communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

DRAWINGS

[0035] Various features, nature and advantages may become apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

[0036] FIG. 1 illustrates a profile view of a first package being coupled to a second package.

[0037] FIG. 2 illustrates a conventional package-on-package (PoP) device.

[0038] FIG. 3 illustrates an example of a through encapsulation via (TEV) that includes a side barrier layer.

[0039] FIG. 4 illustrates an example of an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0040] FIG. 5 (comprising FIGS. 5A, 5B, and 5C) illustrates an exemplary sequence for providing / manufacturing an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0041] FIG. 6 illustrates an example of an interposer that includes a through encapsulation via (TEV) with a side barrier layer.

[0042] FIG. 7 (comprising FIGS. 7A, 7B, and 7C) illustrates an exemplary sequence for providing / manufacturing an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0043] FIG. 8 illustrates an example of a through encapsulation via (TEV) that includes a side barrier layer and fill.

[0044] FIG. 9 illustrates an example of an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0045] FIG. 10 (comprising FIGS. 10A, 10B, and 10C) illustrates an exemplary sequence for providing / manufacturing an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0046] FIG. 11 illustrates an example of an interposer that includes a through encapsulation via (TEV) with a side barrier layer and a fill.

[0047] FIG. 12 (comprising FIGS. 12A, 12B, and 12C) illustrates an exemplary sequence for providing / manufacturing an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0048] FIG. 13 illustrates an exemplary a flow diagram of a method for providing / manufacturing an integrated device that includes a through encapsulation via (TEV) with a side barrier layer.

[0049] FIG. 14 illustrates various electronic devices that may integrate an integrated device, a semiconductor device, a die, an integrated circuit and/or PCB described herein.

DETAILED DESCRIPTION

[0050] In the following description, specific details are given to provide a thorough understanding of the various aspects of the disclosure. However, it will be understood by one of ordinary skill in the art that the aspects may be practiced without these specific details. For example, circuits may be shown in block diagrams in order to avoid obscuring the aspects in unnecessary detail. In other instances, well-known circuits, structures and techniques may not be shown in detail in order not to obscure the aspects of the disclosure.

Overview

[0051] Some novel features pertain to an integrated device (e.g., integrated package, interposer) that includes an encapsulation layer, a via structure traversing the encapsulation layer, and a pad. The via structure includes a via that includes a first side, a second side, and a third side. The via structure also includes a barrier layer surrounding at least the first side and the third side of the via. The pad is directly coupled to the barrier layer of the via structure. In some implementations, the via structure also includes a fill (e.g., polymer fill). In some implementations, the integrated device includes a first dielectric layer coupled to a first surface of the encapsulation layer. In some implementations, the integrated device includes a second dielectric layer coupled to a second surface of the encapsulation layer. In some implementations, the integrated device includes a substrate coupled to a first surface of the encapsulation layer. In some implementations, the integrated device includes a first die coupled to the substrate, where the encapsulation layer encapsulates the first die. In some implementations, the substrate includes a set of through substrate vias (TSVs). In some implementations, the via includes a seed layer. In some implementations, the via includes a portion configured to operate as a pad.

Exemplary Integrated Device That Includes Via With Side Barrier Layer Traversing an Encapsulation Layer

[0052] FIG. 3 illustrates an example of a set of through encapsulation vias (TEVs) that may be implemented in an integrated device (e.g., integrated package device, package-on-package (PoP) device, interposer).

[0053] Specifically, FIG. 3 illustrates a substrate 302, an insulation layer 304, a encapsulation layer 306, and a dielectric layer 308. FIG. 3 also illustrates a first pad 310, a first barrier layer 312, a through encapsulation via (TEV) 314, and a cavity 315. The first pad 310 is located in the substrate 302. Different implementations may use different materials for the substrate 302 (e.g., silicon, glass, ceramic, organic). In some implementations, the substrate 302 is a wafer level substrate.

[0054] The first pad 310 is a metal material (e.g., aluminum). The insulation layer 304 is coupled to a first surface (e.g., top surface) of the substrate 302. In some implementations, the insulation layer 304 is a passivation layer. In some implementations, the insulation layer 304 is a dielectric. In some implementations, the insulation layer 304 covers at least partially the first pad 310. Different implementations may use different materials for the insulation layer 304 (e.g., different dielectric materials). In some implementations, the insulation layer 304 is a silicon nitrade (SiN) layer.

[0055] In some implementations, the encapsulation layer 306 is coupled to the insulation layer 304. For example, a first surface (e.g., bottom surface) of the encapsulation layer 306 is coupled to a second surface (e.g., top surface) of the insulation layer 304. Different implementations may use different materials for the encapsulation layer 306. In some implementations, the encapsulation layer 306 is a film layer. In some implementations, the encapsulation layer 306 is made of a material that has a photo-patternable property. In some implementations, the encapsulation layer 306 is made of a material that can be removed (e.g., etched) through a photo etching process. In some implementations, a photo-etching process on the encapsulation layer 306 ensures that other component of the package does not get damaged when the a cavity is formed (e.g., created) in the encapsulation layer 306 in the process of forming a TEV. For example, in some implementations, the use of a photo-etching process on the encapsulation layer 306 that is photo-patternable ensures that the pad 310 does not get damaged, which would be the case if a laser where used to create a cavity in the encapsulation layer 306. For instances, when a laser process is used to create the cavity

in the encapsulation layer over a pad (e.g., pad 310), the laser will damage and/or destroy the pad (e.g., pad 310), which would prevent the TEV from properly coupling to the interconnects in the substrate.

[0056] The first barrier layer 312 and the TEV 314 are located in the encapsulation layer 306. The TEV 314 is a metal layer (e.g., copper) that traverses the encapsulation layer 306. In some implementations, the TEV 314 includes a seed layer. In such instances, the TEV 314 includes a metal layer (e.g., copper layer) and a seed layer. In some implementations, the seed layer is between the metal layer of the TEV 314 and the barrier layer 312. The TEV 314 has a first side (e.g., bottom side), a second side (e.g., top side), and a third side (e.g., vertical side). In some implementations, the third side of the TEV 314 may be the walls of the TEV 314. In some implementations, the TEV 314 may have a non-horizontal side. For example, the TEV 314 may have a non-perpendicular or non-horizontal side (e.g., diagonal side).

[0057] As shown in FIG. 3, the first barrier layer 312 is coupled to the TEV 314. In particular, the TEV 314 is surrounded in the encapsulation layer 306 by the first barrier layer 312. The first barrier layer 312 is coupled to the first side of the TEV 314 and the third side (e.g., vertical side) of the TEV 314. Thus, as shown in FIG. 3, in some implementations, the TEV 314 is not in direct contact (e.g., free of direct contact) with the encapsulation layer 306. Different implementations may use different materials for the first barrier layer 312. In some implementations, the first barrier layer 312 is one of at least titanium (Ti), TiN, and/or TiW. However, the first barrier layer 312 may be other materials and is not limited to the materials listed.

[0058] The first barrier layer 312 is coupled to the first pad 310. In some implementations, the first barrier layer 312 is at least partially surrounded by the insulation layer 304.

[0059] The dielectric layer 308 is coupled to the encapsulation layer 306. In some implementations, the first surface (e.g., bottom surface) of the dielectric layer 308 is coupled to the second surface (e.g., top surface) of the encapsulation layer 306. In some implementations, a second surface (e.g., top surface) of the dielectric layer 308 may be aligned with the top surface of the TEV 314. In some implementations, the dielectric layer 308 may include a cavity 315 that opens the dielectric layer 308 and exposes part of the top surface of the TEV 314.

[0060] As shown in FIG. 3, the TEV 314 is configured in such a way that the TEV 314 is both a via and a pad. In some implementations, the combination of the via and

the pad may be referred to as a via structure. In some implementations, the via structure includes the TEV 314 and the first barrier layer 312. In some implementations, the TEV 314 has a T-shape. In some implementations, the first barrier layer 312 has a U-shape.

[0061] The via structure that includes the first barrier layer 312 and the TEV 314, as shown in FIG. 3, may be implemented in different integrated devices. In some implementations, the via structure may be implemented in an integrated package device (e.g., package-on-package (PoP) device).

[0062] FIG. 3 illustrates that the first pad 310 is embedded in the substrate 302. However, in some implementations, the first pad 310 is located on the surface of the substrate 302.

[0063] FIG. 4 illustrates an integrated package device 400 that includes a set of via structures 401. In some implementations, the via structures 401 may be the via structure shown in FIG. 3, and/or any novel via structure described and illustrated in the present disclosure.

[0064] As shown in FIG. 4, the integrated package device 400 includes a substrate 402, a first die 404, a second die 406, a first set of interconnects 414, a second set of interconnects 416, an encapsulation layer 418, a first dielectric layer 420, a second dielectric layer 422, a set of through substrate vias (TSVs) 424, a third set of interconnects 426, a set of solder balls 428, and a first pad 430. In some implementations, the substrate 402 may include a set of interconnects (e.g., traces, vias), which are not shown for the purpose of clarity. The set of interconnects may be coupled to one or more pads (e.g., pad 430) and/or the third set of interconnects 426.

[0065] The first die 404 is coupled the substrate 402 through the first set of interconnects 414 (e.g., first bump, first pillar interconnect, first solder). The second die 406 is coupled the substrate 402 through the second set of interconnects 416 (e.g., second bump, second pillar interconnect, second solder). The encapsulation layer 418 covers the first and second dies 404 and 406.

[0066] The set of via structures 401 traverses the encapsulation layer 418 and is coupled to the substrate 402. In some implementations, the set of via structures 401 is coupled to at least the first pad 430. In some implementations, the first pad 430 is coupled to at least one of the set of TSVs 424. At least one of the TSV from the set of TSVs 424 may be coupled to the third set of interconnects 426. At least one interconnect from the third set of interconnects 426 may be coupled to a solder ball from the set of solder balls 428.

[0067] In some implementations, a dielectric layer 409 is coupled (e.g., formed) on the first surface of the substrate 402. In some implementations, the dielectric layer 409 is similar and/or the same as the insulation layer 304. In some implementations, the encapsulation layer 418 is coupled to the dielectric layer 409.

[0068] One of the via structures 401 includes at least a first barrier layer 403 (e.g., first barrier layer 312) and a through encapsulation via (TEV) 405 (e.g., TEV 314). The first barrier layer 403 and the TEV 405 are located in the encapsulation layer 418. The TEV 405 is a metal layer (e.g., copper) that traverses the encapsulation layer 418. In some implementations, the TEV 405 includes a seed layer. In such instances, the TEV 405 includes a metal layer (e.g., copper layer) and a seed layer. In some implementations, the seed layer is between the metal layer of the TEV 405 and the barrier layer 403. The TEV 405 has a first side (e.g., bottom side), a second side (e.g., top side), and a third side (e.g., vertical side). In some implementations, the third side of the TEV 405 may be the walls of the TEV 405. In some implementations, the vertical side of the TEV 405 is perpendicular to the top and/or bottom surfaces of the encapsulation layer 418.

[0069] The first barrier layer 403 is coupled to the TEV 405. In particular, the TEV 405 is surrounded in the encapsulation layer 418 by the first barrier layer 403. The first barrier layer 403 is coupled to the first side of the TEV 405 and the third side (e.g., vertical side) of the TEV 405. Thus, as shown in FIG. 4, in some implementations, the TEV 405 is not in direct contact (e.g., free of direct contact) with the encapsulation layer 418.

[0070] FIG. 4 illustrates that the first pad 430 is embedded in the substrate 402. However, in some implementations, the first pad 430 is located on the surface of the substrate 402. Although not show in FIG. 4 for the purpose of clarity, the first pad 430 is coupled to an interconnect (e.g., a via, trace) in the substrate 402.

[0071] In some implementations, the integrated device 400 is a package (e.g., integrated package) from a package-on-package (PoP) integrated device. As such, in some implementations, another integrated device (e.g., another package) may be coupled to the integrated device 400. For example, another integrated device comprising a substrate and an interconnect (e.g., solder ball) may be coupled to the top portion of the integrated device 400. In such instances, the interconnect (e.g., solder ball) may be coupled to the via structure 401 of the integrated device 400.

Exemplary Sequence for Providing / Fabricating an Integrated Device That Includes Via With Side Barrier Layer Traversing an Encapsulation Layer

[0072] In some implementations, providing an integrated device (e.g., integrated package) that includes a via structure, includes several processes. FIG. 5 (which comprises FIGS. 5A-5C) illustrates an exemplary sequence for providing an integrated device. In some implementations, the sequence of FIGS. 5A-5C may be used to provide / manufacture the integrated device of FIGS. 3 and/or 4, and/or other integrated devices described in the present disclose.

[0073] It should also be noted that the sequence of FIGS. 5A-5C may be used to provide / manufacture integrated devices that also include circuit elements. It should further be noted that the sequence of FIGS. 5A-5C may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device.

[0074] In some implementations, the process of FIGS. 5A-5C illustrates a novel process that provides an integrated device with high density interconnects.

[0075] As shown in stage 1 of FIG. 5A, a substrate 502 is provided (e.g., fabricated). In some implementations, the substrate 502 is a wafer. Different implementations may use different materials for the substrate (e.g., silicon substrate, glass substrate, ceramic substrate, organic substrate). The substrate 502 includes a set of through substrate vias (TSVs) 504 and a set of pads 505. In some implementations, the substrate 502 may also include other interconnects (e.g., traces). The set of pads 505 is located on a first surface (e.g., top surface) of the substrate 502. In some implementations, the set of pads 505 is embedded in the first surface of the substrate 502. In some implementations, a dielectric layer 503 is coupled (e.g., formed) on the first surface of the substrate 502. In some implementations, the dielectric layer 503 is similar and/or the same as the insulation layer 304. The dielectric layer 503 may include one or more openings and/or cavities above one or more pads 505 and/or one or more set of TSVs 504. In some implementations, the substrate 502 may include a set of interconnects (e.g., traces, vias), which are not shown for the purpose of clarity. The set of interconnects may be coupled to one or more pads (e.g., pad 505).

[0076] At stage 2, a first die 506 and a second die 508 are coupled to the substrate 502. The first die 506 is coupled to the substrate 502 through a first set of interconnects 516 (e.g., first pillar, first solder). In some implementations, at least one of the first set of interconnects is electrically coupled to at least one TSV from the set of TSVs 504. The second die 508 is coupled to the substrate 502 through a second set of interconnects

518 (e.g., first pillar, first solder). In some implementations, at least one of the second set of interconnects 518 is electrically coupled to at least one TSV from the set of TSVs 504.

[0077] At stage 3, an encapsulation layer 520 is provided (e.g., formed) on the substrate 502 and/or the dielectric layer 503 on the substrate 502. The encapsulation layer 520 encapsulates the first die 506 and the second die 508. In some implementations, the encapsulation layer 520 may be coupled directly to the substrate 502. Different implementations may use different materials for the encapsulation layer 520. In some implementations, the encapsulation layer 520 is a film layer. In some implementations, the encapsulation layer 520 is made of a material that has a photo-patternable property.

[0078] At stage 4, at least one cavity 525 is formed in the encapsulation layer 520. In some implementations, the cavity 525 is formed (e.g., created) over a pad (e.g., pad 505). In some implementations, the cavity 525 is formed by using a photo etching process (e.g., photolithography process).

[0079] At stage 5, a barrier layer 530 is provided (e.g., formed, deposited). In some implementations, a plating process is used to form the barrier layer 530. The barrier layer 530 may cover the inside walls of the cavity 525, at least part of the pad 505, and/or the first surface of the encapsulation layer 520. Different implementations may use different materials for the barrier layer 530. In some implementations, the barrier layer 530 is one of at least titanium (Ti), (TiN), Aluminium Copper (AlCu), tinanium copper alloy (TiCu) and/or titanium tungsten copper alloy (TiWCu). However, different implementations may use different materials. As such, the material for the barrier layer 530 should not be limited to the materials listed above.

[0080] A seed layer 532 is also provided (e.g., formed, deposited) on the barrier layer 530. In some implementations, a plating process is used to form the seed layer 532 on the barrier layer 530. Different implementations may use different materials for the seed layer 532. In some implementations, the seed layer 532 is a metal layer.

[0081] At stage 6, a photo resist layer 534 is provided (e.g., formed, deposited) on the seed layer 532. In some implementations, providing the photo resist layer 534 includes providing the photo resist layer 534 and selectively removing some portions of the photo resist layer 534.

[0082] At stage 7, a metal layer 536 is provided (e.g., formed, deposited) on the seed layer 532. In some implementations, the metal layer 536 is provided on the seed

layer 532 that is not covered by the photo resist layer 534. In some implementations, a lithography and plating process is used to provide the metal layer 536 on the seed layer 532. In some implementations, the metal layer 536 and the seed layer 532 are the same material. Thus, in some implementations, the metal layer 536 may include the seed layer 532.

[0083] At stage 8, the photo resist layer 534, the seed layer 532, and the barrier layer 530 are selectively removed (e.g., etched). In some implementations, the photo resist layer 534, the seed layer 532, and the barrier layer 530 are removed concurrently. In some implementations, the photo resist layer 534, the seed layer 532, and the barrier layer 530 are removed sequentially. As shown at stage 8, a via structure 538 is fabricated after the photo resist layer 534, the seed layer 532, and the barrier layer 530 are selectively removed. In some implementations, the via structure 538 is one of the via structures described in FIGS. 3-4.

[0084] At stage 9, a dielectric layer 540 is optionally provided (e.g., formed) on a second surface of the encapsulation layer 520. In some implementations, a surface of the dielectric layer 540 is aligned with the surface of the via structure 538. In some implementations, the dielectric layer 540 may cover the via structure 538 and a cavity may be formed over a portion of the via structure 538.

[0085] At stage 10, another dielectric layer 550 is optionally provided (e.g., formed) on the second surface (e.g., bottom surface) of the substrate 502. In addition, a set of interconnects 552 are also provided on / in the dielectric layer 550. In some implementations, the set of interconnects 552 includes at least one of a redistribution layer and/or an under bump metallization (UBM) layer. In some implementations, at least one interconnect from the set of interconnects 552 is electrically coupled to at least one TSV from the set of TSVs 504.

[0086] At stage 11, a set of solder ball 554 is coupled to the set of interconnects 552. In some implementations, after stage 10, an integrated device 560 is fabricated that includes an encapsulation layer and a via structure that includes a side barrier layer.

Exemplary Integrated Device That Includes Via With Side Barrier Layer Traversing an Encapsulation Layer

[0087] FIG. 6 illustrates an integrated package device that includes a set of via structures 610. Specifically, FIG. 6 illustrates an example of an interposer 600 that includes a set of via structures 610. In some implementations, the via structures 610

may be the via structure shown in FIG. 3, and/or any novel via structure described and illustrated in the present disclosure.

[0088] As shown in FIG. 6, the interposer 600 includes an encapsulation layer 602, a first dielectric layer 604, a substrate 606, a first pad 608, and the set of via structures 610. The first dielectric layer 604 is coupled to a first surface (e.g., top surface) of the encapsulation layer 602. The substrate 606 is coupled to a second surface (e.g., bottom surface) of the encapsulation layer 602. In some implementations, a second dielectric layer (e.g., encapsulation layer 304) may be positioned between the substrate 606 and the second surface of the encapsulation layer 602.

[0089] The set of via structures 610 traverses the encapsulation layer 602. In some implementations, the set of via structures 610 is coupled to at least the first pad 608. One of the via structures 610 includes at least a barrier layer 612 and a through encapsulation via (TEV) 614. The barrier layer 612 and the TEV 614 are located in the encapsulation layer 602. In some implementations, the barrier layer 612 is coupled to (e.g., is in direct contact with) the pad 608. The TEV 614 is a metal layer (e.g., copper) that traverses the encapsulation layer 602. In some implementations, the TEV 614 includes a seed layer. In such instances, the TEV 614 includes a metal layer (e.g., copper layer) and a seed layer. In some implementations, the seed layer is between the metal layer of the TEV 614 and the barrier layer 612. The TEV 614 has a first side (e.g., bottom side), a second side (e.g., top side), and a third side (e.g., vertical side). In some implementations, the third side of the TEV 614 may be the walls of the TEV 614. In some implementations, the vertical side of the TEV 614 is perpendicular to the top and/or bottom surfaces of the encapsulation layer 602.

[0090] The barrier layer 612 is coupled to the TEV 614. In particular, the TEV 614 is surrounded in the encapsulation layer 602 by the barrier layer 612. The barrier layer 612 is coupled to the first side of the TEV 614 and the vertical side of the TEV 614. Thus, as shown in FIG. 6, in some implementations, the TEV 614 is not in direct contact (e.g., free of direct contact) with the encapsulation layer 602.

Exemplary Sequence for Providing / Fabricating an Integrated Device That Includes Via With Side Barrier Layer Traversing an Encapsulation Layer

[0091] In some implementations, an integrated device may include an interposer. In some implementations, providing an integrated device (e.g., integrated package) that includes a via structure several processes. FIG. 7 (which includes FIGS. 7A-7C)

illustrates an exemplary sequence for providing an integrated device. In some implementations, the sequence of FIGS. 7A-7C may be used to provide / manufacture the integrated device of FIGS. 3, 4 and/or 6, and/or other integrated devices described in the present disclose.

[0092] It should further be noted that the sequence of FIGS. 7A-7C may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device.

[0093] In some implementations, the process of FIGS. 7A-7C illustrates a novel process that provides an integrated device (e.g., interposer) with high density interconnects.

[0094] As shown in stage 1 of FIG. 7A, a carrier 702 is provided (e.g., fabricated). In some implementations, the carrier 702 is one of at least a substrate and/or wafer. Different implementations may use different materials for the carrier (e.g., silicon substrate, glass substrate, ceramic substrate, organic substrate). The carrier 702 includes a set of pads 705. In some implementations, the carrier 702 may also include other interconnects (e.g., traces). The set of pads 705 is embedded in a first surface (e.g., top surface) of the carrier 702. In some implementations, the set of pads 705 is located on the first surface (e.g., top surface) of the carrier 702. In some implementations, a dielectric layer 703 is coupled (e.g., formed) on the first surface of the substrate 704. In some implementations, the dielectric layer is similar and/or the same as the insulation layer 304.

[0095] At stage 2, an encapsulation layer 720 is provided (e.g., formed) on the carrier 702 and/or the dielectric layer 703 on the carrier 702. In some implementations, the encapsulation layer 720 encapsulates the pads 705. In some implementations, the encapsulation layer 720 may be coupled directly to the carrier 702. Different implementations may use different materials for the encapsulation layer 720. In some implementations, the encapsulation layer 720 is a film layer. In some implementations, the encapsulation layer 720 is made of a material that has a photo-patternable property. In some implementations, the encapsulation layer 720 is made of a material that can be removed (e.g., etched) through a photo etching process.

[0096] At stage 3, at least one cavity 725 is formed in the encapsulation layer 720. In some implementations, the cavity 725 is formed (e.g., created) over a pad (e.g., pad 705). In some implementations, the cavity 725 is formed by using a photo etching process (e.g., photolithography process).

[0097] At stage 4, a barrier layer 730 is provided (e.g., formed, deposited). In some implementations, a plating process is used to form the barrier layer 730. The barrier layer 730 may cover the inside walls of the cavity 725, at least part of the pad 705, and/or the first surface of the encapsulation layer 720. Different implementations may use different materials for the barrier layer 730. Different implementations may use different materials for the barrier layer 730. In some implementations, the barrier layer 730 is one of at least titanium (Ti), (TiN), Aluminium Copper (AlCu), tinanium copper alloy (TiCu) and/or titanium tungsten copper alloy (TiWCu).

[0098] A seed layer 732 is also provided (e.g., formed, deposited) on the barrier layer 730. In some implementations, a plating process is used to form the seed layer 732 on the barrier layer 730. Different implementations may use different materials for the seed layer 732. In some implementations, the seed layer 732 is a metal layer.

[0099] At stage 5, a photo resist layer 734 is provided (e.g., formed, deposited) on the seed layer 732. In some implementations, providing the photo resist layer 734 includes providing the photo resist layer 734 and selectively removing some portions of the photo resist layer 734.

[00100] At stage 6, a metal layer 736 is provided (e.g., formed, deposited) on the seed layer 732. In some implementations, the metal layer 736 is provided on the seed layer 732 that is not covered by the photo resist layer 734. In some implementations, a lithography and plating process is used to provide the metal layer 736 on the seed layer 732. In some implementations, the metal layer 736 and the seed layer 732 are the same material. Thus, in some implementations, the metal layer 736 may include the seed layer 732.

[00101] At stage 7, the photo resist layer 734, the seed layer 732, and the barrier layer 730 are selectively removed (e.g., etched). In some implementations, the photo resist layer 734, the seed layer 732, and the barrier layer 730 are removed concurrently. the photo resist layer 734, the seed layer 732, and the barrier layer 730 are removed sequentially. As shown at stage 7, a via structure 738 is fabricated after the photo resist layer 734, the seed layer 732, and the barrier layer 730 are selectively removed. In some implementations, the via structure 738 is one of the via structures described in FIGS. 3-4.

[00102] At stage 8, a dielectric layer 740 is optionally provided (e.g., formed) on a second surface of the encapsulation layer 720. In some implementations, a surface of the dielectric layer 740 is aligned with the surface of the via structure 738. In some

implementations, the dielectric layer 740 may cover the via structure 738 and a cavity may be formed over a portion of the via structure 738.

[00103] At stage 8, at least a portion of the carrier 702 is removed (e.g., polish, grinded, etched). In some implementations, the carrier 702 is removed until a surface of the carrier 702 is aligned with a surface of the pad 705. In some implementations, after stage 9, an integrated device 760 is fabricated that includes an encapsulation layer and a via structure that includes a side barrier layer.

Exemplary Integrated Device That Includes Via With Side Barrier Layer And Fill Traversing an Encapsulation Layer

[00104] FIG. 8 illustrates an example of a set of through encapsulation vias (TEVs) that may be implemented in an integrated device (e.g., integrated package device, package-on-package (PoP) device, interposer).

[00105] Specifically, FIG. 8 illustrates a substrate 802, an insulation layer 804, a encapsulation layer 806, and a dielectric layer 808. FIG. 8 also illustrates a first pad 810, a first barrier layer 812, a through encapsulation via (TEV) 814, a fill 816, and a cavity 817. The first pad 810 is located in the substrate 802. Different implementations may use different materials for the substrate 802 (e.g., silicon, glass, ceramic, organic). In some implementations, the substrate 802 is a wafer level substrate.

[00106] The first pad 810 is a metal material (e.g., aluminum). The insulation layer 804 is coupled to a first surface (e.g., top surface) of the substrate 802. In some implementations, the insulation layer 804 is a passivation layer. In some implementations, the insulation layer 304 is a dielectric. In some implementations, the insulation layer 804 covers at least partially the first pad 810. Different implementations may use different materials for the insulation layer 804 (e.g., different dielectric materials). In some implementations, the insulation layer 804 is a silicon nitrade (SiN) layer.

[00107] In some implementations, the encapsulation layer 806 is coupled to the insulation layer 804. For example, a first surface (e.g., bottom surface) of the encapsulation layer 806 is coupled to a second surface (e.g., top surface) of the insulation layer 804. Different implementations may use different materials for the encapsulation layer 806. In some implementations, the encapsulation layer 806 is a film layer. In some implementations, the encapsulation layer 806 is made of a material that has a photo-patternable property. In some implementations, the encapsulation layer 806

is made of a material that can be removed (e.g., etched) through a photo etching process. In some implementations, a photo-etching process on the encapsulation layer 806 ensures that other component of the package does not get damaged when the a cavity is formed (e.g., created) in the encapsulation layer 806 in the process of forming a TEV. For example, in some implementations, the use of a photo-etching process on the encapsulation layer 806 that is photo-patternable ensures that the pad 810 does not get damaged, which would be the case if a laser where used to create a cavity in the encapsulation layer 806. For instances, when a laser process is used to create the cavity in the encapsulation layer over a pad (e.g., pad 810), the laser will damage and/or destroy the pad (e.g., pad 810), which would prevent the TEV from properly coupling to the interconnects in the substrate.

[00108] The first barrier layer 812, the TEV 814 and the fill 816 are located in the encapsulation layer 806. The TEV 814 is a metal layer (e.g., copper) that traverses the encapsulation layer 806. In some implementations, the TEV 814 includes a seed layer. In such instances, the TEV 814 includes a metal layer (e.g., copper layer) and a seed layer. In some implementations, the seed layer is between the metal layer of the TEV 814 and the barrier layer 812. The TEV 814 has a first side (e.g., bottom side), a second side (e.g., top side), and a third side (e.g., vertical side). In some implementations, the third side of the TEV 814 may be the walls of the TEV 814. In some implementations, the TEV 814 may have a non-horizontal side. For example, the TEV 814 may have a non-perpendicular or non-horizontal side (e.g., diagonal side). Different implementations may use different materials for the fill 816. For example, the fill 816 may include a polymer fill. In some implementations, the fill 816 provides structure stability for the via structure.

[00109] FIG. 8 illustrates that the TEV 814 conforms to the shape of the barrier layer 812. In this example, the barrier layer 812 has a U shaped cross-section. Similarly, the TEV 814 has a U shaped cross-section. FIG. 8 also illustrates that the fill 816 is coupled to the TEV 814. In particular, the fill 816 is surrounded by the TEV 814. The first barrier layer 812 is coupled to the TEV 814. In particular, the TEV 814 is surrounded in the encapsulation layer 806 by the first barrier layer 812. The first barrier layer 812 is coupled to the first side of the TEV 814 and the third side (e.g., vertical side) of the TEV 814. Thus, as shown in FIG. 8, in some implementations, the TEV 814 is not in direct contact (e.g., free of direct contact) with the encapsulation layer 806. Different implementations may use different materials for the first barrier layer 812. In some

implementations, the first barrier layer 812 is one of at least titanium (Ti), TiN, and/or TiW. However, the first barrier layer 812 may be other materials and is not limited to the materials listed.

[00110] The first barrier layer 812 is coupled to the first pad 810. In some implementations, the first barrier layer 812 is at least partially surrounded by the insulation layer 804.

[00111] The dielectric layer 808 is coupled to the encapsulation layer 806. In some implementations, the first surface (e.g., bottom surface) of the dielectric layer 808 is coupled to the second surface (e.g., top surface) of the encapsulation layer 806. In some implementations, the dielectric layer 808 may include a cavity 817 that opens the dielectric layer 808 and exposes part of the top surface of the TEV 814. As shown in FIG. 8, the cavity 817 exposes the wing portion (e.g., horizontal portion) of the TEV 814.

[00112] As shown in FIG. 8, the TEV 814 is configured in such a way that the TEV is both a via and a pad. In some implementations, the combination of the via and the pad may be referred to as a via structure. In some implementations, the via structure includes the TEV 814 and the first barrier layer 812.

[00113] The via structure that includes the first barrier layer 812 and the TEV 814, as shown in FIG. 8, may be implemented in different integrated devices. In some implementations, the via structure may be implemented in an integrated package device (e.g., package-on-package (PoP) device).

[00114] FIG. 8 illustrates that the first pad 810 is embedded in the substrate 802. However, in some implementations, the first pad 810 is located on the surface of the substrate 802.

[00115] FIG. 9 illustrates an integrated package device 900 that includes a set of via structures 901. In some implementations, via structures 901 may be the via structure shown in FIG. 8, and/or any novel via structure described and illustrated in the present disclosure.

[00116] As shown in FIG. 9, the integrated package device 900 includes a substrate 902, a first die 904, a second die 906, a dielectric layer 909, a first set of interconnects 914, a second set of interconnects 916, an encapsulation layer 918, a first dielectric layer 920, a second dielectric layer 922, a set of through substrate vias (TSVs) 924, a third set of interconnects 926, a set of solder balls 928, and a first pad 930. In some implementations, the substrate 902 may include a set of interconnects (e.g., traces, vias),

which are not shown for the purpose of clarity. The set of interconnects may be coupled to one or more pads (e.g., pad 930) and/or the third set of interconnects 926.

[00117] The first die 904 is coupled the substrate 902 through the first set of interconnects 914 (e.g., first pillar, first solder). The second die 906 is coupled the substrate 902 through the second set of interconnects 916 (e.g., second pillar, second solder). The encapsulation layer 918 covers the first and second dies 904 and 906.

[00118] The set of via structures 901 traverses the encapsulation layer 918 and is coupled to the substrate 902. In some implementations, the set of via structures 901 is coupled to at least the first pad 930. In some implementations, the first pad 930 is coupled to at least one of the set of TSVs 924. At least one of the TSV from the set of TSVs 924 may be coupled to the third set of interconnects 926. At least one interconnect from the third set of interconnects 926 may be coupled to a solder ball from the set of solder balls 928.

[00119] In some implementations, a dielectric layer 909 is coupled (e.g., formed) on the first surface of the substrate 902. In some implementations, the dielectric layer 909 is similar and/or the same as the insulation layer 804. In some implementations, the encapsulation layer 918 is coupled to the dielectric layer 909.

[00120] One of the via structures 901 includes at least a first barrier layer 903 (e.g., first barrier layer 812), a through encapsulation via (TEV) 905 (e.g., TEV 814) and a fill 907. The first barrier layer 903, the TEV 905, and the fill 907 are located in the encapsulation layer 918. The TEV 905 is a metal layer (e.g., copper) that traverses the encapsulation layer 918. In some implementations, the TEV 905 includes a seed layer. In such instances, the TEV 905 includes a metal layer (e.g., copper layer) and a seed layer. In some implementations, the seed layer is between the metal layer of the TEV 905 and the barrier layer 903. The TEV 905 has a first side (e.g., bottom side), a second side (e.g., top side), and a third side (e.g., vertical side). In some implementations, the third side of the TEV 905 may be the walls of the TEV 905. In some implementations, the vertical side of the TEV 905 is perpendicular to the top and/or bottom surfaces of the encapsulation layer 918. Different implementations may use different materials for the fill 907. For example, the fill 907 may include a polymer fill. In some implementations, the fill 907 provides structural stability for the via structure 901.

[00121] The first barrier layer 903 is coupled to the TEV 905. In particular, the TEV 905 is surrounded in the encapsulation layer 918 by the first barrier layer 903. The first barrier layer 903 is coupled to the first side of the TEV 905 and the third side (e.g.,

vertical side) of the TEV 905. Thus, as shown in FIG. 9, in some implementations, the TEV 905 is not in direct contact (e.g., free of direct contact) with the encapsulation layer 918. In some implementations, the TEV 905 conforms to the shape of the first barrier layer 903. The fill 907 is surrounded by the TEV 905.

[00122] FIG. 9 illustrates that the first pad 930 is embedded in the substrate 902. However, in some implementations, the first pad 930 is located on the surface of the substrate 902. Although not show in FIG. 9 for the purpose of clarity, the first pad 930 is coupled to an interconnect (e.g., a via, trace) in the substrate 902.

[00123] In some implementations, the integrated device 900 is a package (e.g., integrated package) from a package-on-package (PoP) integrated device. As such, in some implementations, another integrated device (e.g., another package) may be coupled to the integrated device 900. For example, another integrated device comprising a substrate and an interconnect (e.g., solder ball) may be coupled to the top portion of the integrated device 900. In such instances, the interconnect (e.g., solder ball) may be coupled to the via structure 901 of the integrated device 900.

Exemplary Sequence for Providing / Fabricating an Integrated Device That Includes Via With Side Barrier Layer And Fill Traversing an Encapsulation Layer

[00124] In some implementations, providing an integrated device (e.g., integrated package) that includes a via structure several processes. FIG. 10 (which includes FIGS. 10A-10C) illustrates an exemplary sequence for providing an integrated device. In some implementations, the sequence of FIGS. 10A-10C may be used to provide / manufacture the integrated device of FIGS. 8 and/or 9, and/or other integrated devices described in the present disclose.

[00125] It should also be noted that the sequence of FIGS. 10A-10C may be used to provide / manufacture integrated devices that also include circuit elements. It should further be noted that the sequence of FIGS. 10A-10C may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device.

[00126] In some implementations, the process of FIGS. 10A-10C illustrates a novel process that provides an integrated device with high density interconnects.

[00127] As shown in stage 1 of FIG. 10A, a substrate 1002 is provided (e.g., fabricated). In some implementations, the substrate 1002 is a wafer. Different implementations may use different materials for the substrate (e.g., silicon substrate, glass substrate, ceramic substrate, organic substrate). The substrate 1002 includes a set

of through substrate vias (TSVs) 1004 and a set of pads 1005. In some implementations, the substrate 1002 may also include other interconnects (e.g., traces). The set of pads 1005 is embedded in a first surface (e.g., top surface) of the substrate 1002. In some implementations, the set of pads 1005 is located on the first surface (e.g., top surface) of the substrate 1002. In some implementations, a dielectric layer 1003 is coupled (e.g., formed) on the first surface of the substrate 1002. In some implementations, the dielectric layer 1003 is similar and/or the same as the insulation layer 304. The dielectric layer 1003 may include one or more openings and/or cavities above one or more pads 1005 and/or one or more set of TSVs 1004. In some implementations, the substrate 1002 may include a set of interconnects (e.g., traces, vias), which are not shown for the purpose of clarity. The set of interconnects may be coupled to one or more pads (e.g., pad 1005).

[00128] At stage 2, a first die 1006 and a second die 1008 are coupled to the substrate 1002. The first die 1006 is coupled to the substrate 1002 through a first set of interconnects 1016 (e.g., first pillar, first solder). In some implementations, at least one of the first set of interconnects is electrically coupled to at least one TSV from the set of TSVs 1004. The second die 1008 is coupled to the substrate 1002 through a second set of interconnects 1018 (e.g., first pillar, first solder). In some implementations, at least one of the second set of interconnects 1018 is electrically coupled to at least one TSV from the set of TSVs 1004.

[00129] At stage 3, an encapsulation layer 1020 is provided (e.g., formed) on the substrate 1002 and/or the dielectric layer 1003 on the substrate 1002. The encapsulation layer 1020 encapsulates the first die 1006 and the second die 1008. In some implementations, the encapsulation layer 1020 may be coupled directly to the substrate 1002. Different implementations may use different materials for the encapsulation layer 1020. In some implementations, the encapsulation layer 1020 is a film layer. In some implementations, the encapsulation layer 1020 is made of a material that has a photo-patternable property.

[00130] At stage 4, at least one cavity 1025 is formed in the encapsulation layer 1020. In some implementations, the cavity 1025 is formed (e.g., created) over a pad (e.g., pad 1005). In some implementations, the cavity 1025 is formed by using a photo etching process (e.g., photolithography process).

[00131] At stage 5, a barrier layer 1030 is provided (e.g., formed, deposited). In some implementations, a plating process is used to form the barrier layer 1030. The barrier

layer 1030 may cover the inside walls of the cavity 1025, at least part of the pad 1005, and/or the first surface of the encapsulation layer 1020. Different implementations may use different materials for the barrier layer 1030. In some implementations, the barrier layer 1030 is one of at least titanium (Ti), (TiN), Aluminium Copper (AlCu), tinanium copper alloy (TiCu) and/or titanium tungsten copper alloy (TiWCu). However, different implementations may use different materials. As such, the material for the barrier layer 1030 should not be limited to the materials listed above.

[00132] A seed layer 1032 is also provided (e.g., formed, deposited) on the barrier layer 1030. In some implementations, a plating process is used to form the seed layer 1032 on the barrier layer 1030. Different implementations may use different materials for the seed layer 1032. In some implementations, the seed layer 1032 is a metal layer.

[00133] At stage 6, a photo resist layer 1034 is provided (e.g., formed, deposited) on the seed layer 1032. In some implementations, providing the photo resist layer 1034 includes providing the photo resist layer 1034 and selectively removing some portions of the photo resist layer 1034.

[00134] At stage 7, a metal layer 1036 is provided (e.g., formed, deposited) on the seed layer 1032. In some implementations, the metal layer 1036 is provided on the seed layer 1032 that is not covered by the photo resist layer 1034. In some implementations, a lithography and plating process is used to provide the metal layer 1036 on the seed layer 1032. In some implementations, the metal layer 1036 and the seed layer 1032 are the same material. Thus, in some implementations, the metal layer 1036 may include the seed layer 1032. As shown in stage 7, the metal layer 1036 is provided on the seed layer 1032 such that it conforms (e.g., contours) with the barrier layer 1030. Stage 7 also illustrates that the metal layer 1036 does not completely fill the cavity 1025, leaving behind a cavity 1037.

[00135] At stage 8, a fill 1039 is provided in the cavity 1037. Different implementations may provide different materials for the fill 1039. For example, the fill 1039 may includes a polymer fill. In some implementations, the fill 1039 is configured to provide structural stability for a via structure.

[00136] At stage 9, the photo resist layer 1034, the seed layer 1032, and the barrier layer 1030 are selectively removed (e.g., etched). In some implementations, the photo resist layer 1034, the seed layer 1032, and the barrier layer 1030 are removed concurrently. In some implementations, the photo resist layer 1034, the seed layer 1032, and the barrier layer 1030 are removed sequentially. As shown at stage 9, a via structure

1038 is fabricated after the photo resist layer 1034, the seed layer 1032, and the barrier layer 1030 are selectively removed. In some implementations, the via structure 1038 is one of the via structures described in FIGS. 8-9.

[00137] At stage 10, a dielectric layer 1040 is optionally provided (e.g., formed) on a second surface of the encapsulation layer 1020. In some implementations, a surface of the dielectric layer 1040 is aligned with the surface of the via structure 1038. In some implementations, the dielectric layer 1040 may cover the via structure 1038 and a cavity may be formed over a portion of the via structure 1038.

[00138] At stage 11, another dielectric layer 1050 is optionally provided (e.g., formed) on the second surface (e.g., bottom surface) of the substrate 1002. In addition, a set of interconnects 1052 are also provided on / in the dielectric layer 1050. In some implementations, the set of interconnects 1052 includes at least one of a redistribution layer and/or an under bump metallization (UBM) layer. In some implementations, at least one interconnect from the set of interconnects 1052 is electrically coupled to at least one TSV from the set of TSVs 1004.

[00139] At stage 12, a set of solder ball 1054 is coupled to the set of interconnects 1052. In some implementations, after stage 10, an integrated device 1060 is fabricated that includes an encapsulation layer and a via structure that includes a side barrier layer.

Exemplary Integrated Device That Includes Via With Side Barrier Layer And Fill Traversing an Encapsulation Layer

[00140] FIG. 11 illustrates an integrated package device that includes a set of via structures 1110. Specifically, FIG. 11 illustrates an example of an interposer 1100 that includes a set of via structures 1110. In some implementations, the via structures 1110 may be the via structure shown in FIG. 8, and/or any novel via structure described and illustrated in the present disclosure.

[00141] As shown in FIG. 11, the interposer 1100 includes an encapsulation layer 1102, a first dielectric layer 1104, a substrate 1106, a first pad 1108, and a set of via structures 1110. The first dielectric layer 1104 is coupled to a first surface (e.g., top surface) of the encapsulation layer 1102. The substrate 1106 is coupled to a second surface (e.g., bottom surface) of the encapsulation layer 1102. In some implementations, a second dielectric layer (e.g., encapsulation layer 304) may be positioned between the substrate 1106 and the second surface of the encapsulation layer 1102.

[00142] The set of via structures 1110 traverses the encapsulation layer 1102. In some implementations, the set of via structures 1110 is coupled to at least the first pad 1108. One of the via structures 1110 includes at least a barrier layer 1112, a through encapsulation via (TEV) 1114 and a fill 1116. The barrier layer 1112, the TEV 1114, and the fill 1116 are located in the encapsulation layer 1102. In some implementations, the barrier layer 1112 is coupled to (e.g., is in direct contact with) the pad 1108. The TEV 1114 is a metal layer (e.g., copper) that traverses the encapsulation layer 1102. In some implementations, the TEV 1114 includes a seed layer. In such instances, the TEV 1114 includes a metal layer (e.g., copper layer) and a seed layer. In some implementations, the seed layer is between the metal layer of the TEV 1114 and the barrier layer 1112. The TEV 1114 has a first side (e.g., bottom side), a second side (e.g., top side), and a third side (e.g., vertical side). In some implementations, the third side of the TEV 1114 may be the walls of the TEV 1114. In some implementations, the TEV 1114 may have a non-horizontal side. For example, the TEV 1114 may have a non-perpendicular or non-horizontal side (e.g., diagonal side). Different implementations may use different materials for the fill 1116. For example, the fill 1116 may include a polymer fill. In some implementations, the fill 1116 provides structure stability for the via structure.

[00143] FIG. 11 illustrates that the TEV 1114 conforms to the shape of the barrier layer 1112. In this example, the barrier layer 1112 has a U shaped cross-section. Similarly, the TEV 1114 has a U shaped cross-section. FIG. 11 also illustrates that the fill 1116 is coupled to the TEV 1114. In particular, the fill 1116 is surrounded by the TEV 1114. The first barrier layer 1112 is coupled to the TEV 1114. In particular, the TEV 1114 is surrounded in the encapsulation layer 1102 by the first barrier layer 1112. The first barrier layer 1112 is coupled to the first side of the TEV 1114 and the third side (e.g., vertical side) of the TEV 1114. Thus, as shown in FIG. 11, in some implementations, the TEV 1114 is not in direct contact (e.g., free of direct contact) with the encapsulation layer 1102. Different implementations may use different materials for the first barrier layer 1112. In some implementations, the first barrier layer 1112 is one of at least titanium (Ti), TiN, and/or TiW. However, the first barrier layer 1112 may be other materials and is not limited to the materials listed.

Exemplary Sequence for Providing / Fabricating an Integrated Device That Includes Via With Side Barrier Layer And Fill Traversing an Encapsulation Layer

[00144] In some implementations, an integrated device may include an interposer. In some implementations, providing an integrated device (e.g., integrated package) that includes a via structure several processes. FIG. 12 (which includes FIGS. 12A-12C) illustrates an exemplary sequence for providing an integrated device. In some implementations, the sequence of FIGS. 12A-12C may be used to provide / manufacture the integrated device of FIGS. 8, 9 and/or 11, and/or other integrated devices described in the present disclose.

[00145] It should further be noted that the sequence of FIGS. 12A-12C may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device.

[00146] In some implementations, the process of FIGS. 12A-12C illustrates a novel process that provides an integrated device (e.g., interposer) with high density interconnects.

[00147] As shown in stage 1 of FIG. 12A, a carrier 1202 is provided (e.g., fabricated). In some implementations, the carrier 1202 is one of at least a substrate and/or wafer. Different implementations may use different materials for the carrier (e.g., silicon substrate, glass substrate, ceramic substrate, organic substrate). The carrier 1202 includes a set of pads 1205. In some implementations, the carrier 1202 may also include other interconnects (e.g., traces). The set of pads 1205 is embedded in a first surface (e.g., top surface) of the carrier 1202. In some implementations, the set of pads 1205 is located on the first surface (e.g., top surface) of the carrier 1202. In some implementations, a dielectric layer 1203 is coupled (e.g., formed) on the first surface of the substrate 1204. In some implementations, the dielectric layer is similar and/or the same as the insulation layer 304.

[00148] At stage 2, an encapsulation layer 1220 is provided (e.g., formed) on the carrier 1202 and/or the dielectric layer 1203 on the carrier 1202. In some implementations, the encapsulation layer 1220 encapsulates the pads 1205. In some implementations, the encapsulation layer 1220 may be coupled directly to the carrier 1202. Different implementations may use different materials for the encapsulation layer 1220. In some implementations, the encapsulation layer 1220 is a film layer. In some implementations, the encapsulation layer 1220 is made of a material that has a photo-patternable property. In some implementations, the encapsulation layer 1220 is made of a material that can be removed (e.g., etched) through a photo etching process.

[00149] At stage 3, at least one cavity 1225 is formed in the encapsulation layer 1220. In some implementations, the cavity 1225 is formed (e.g., created) over a pad (e.g., pad 1205). In some implementations, the cavity 1225 is formed by using a photo etching process (e.g., photolithography process).

[00150] At stage 4, a barrier layer 1230 is provided (e.g., formed, deposited). In some implementations, a plating process is used to form the barrier layer 1230. The barrier layer 1230 may cover the inside walls of the cavity 1225, at least part of the pad 1205, and/or the first surface of the encapsulation layer 1220. Different implementations may use different materials for the barrier layer 1230. Different implementations may use different materials for the barrier layer 1230. In some implementations, the barrier layer 1230 is one of at least titanium (Ti), (TiN), Aluminium Copper (AlCu), tinanium copper alloy (TiCu) and/or titanium tungsten copper alloy (TiWCu).

[00151] A seed layer 1232 is also provided (e.g., formed, deposited) on the barrier layer 1230. In some implementations, a plating process is used to form the seed layer 1232 on the barrier layer 1230. Different implementations may use different materials for the seed layer 1232. In some implementations, the seed layer 1232 is a metal layer.

[00152] At stage 5, a photo resist layer 1234 is provided (e.g., formed, deposited) on the seed layer 1232. In some implementations, providing the photo resist layer 1234 includes providing the photo resist layer 1234 and selectively removing some portions of the photo resist layer 1234.

[00153] At stage 6, a metal layer 1236 is provided (e.g., formed, deposited) on the seed layer 1232. In some implementations, the metal layer 1236 is provided on the seed layer 1232 that is not covered by the photo resist layer 1234. In some implementations, a lithography and plating process is used to provide the metal layer 1236 on the seed layer 1232. In some implementations, the metal layer 1236 and the seed layer 1232 are the same material. Thus, in some implementations, the metal layer 1236 may include the seed layer 1232.

[00154] As shown in stage 6, the metal layer 1236 is provided on the seed layer 1232 such that it conforms (e.g., contours) with the barrier layer 1230. Stage 6 also illustrates that the metal layer 1236 does not completely fill the cavity 1225, leaving behind a cavity 1237.

[00155] At stage 7, a fill 1239 is provided in the cavity 1237. Different implementations may provide different materials for the fill 1239. For example, the fill

1239 may includes a polymer fill. In some implementations, the fill 1239 is configured to provide structural stability for a via structure.

[00156] At stage 8, the photo resist layer 1234, the seed layer 1232, and the barrier layer 1230 are selectively removed (e.g., etched). In some implementations, the photo resist layer 1234, the seed layer 1232, and the barrier layer 1230 are removed concurrently. the photo resist layer 1234, the seed layer 1232, and the barrier layer 1230 are removed sequentially. As shown at stage 12, a via structure 1238 is fabricated after the photo resist layer 1234, the seed layer 1232, and the barrier layer 1230 are selectively removed. In some implementations, the via structure 1238 is one of the via structures described in FIGS. 8-9.

[00157] At stage 9, a dielectric layer 1240 is optionally provided (e.g., formed) on a second surface of the encapsulation layer 1220. In some implementations, a surface of the dielectric layer 1240 is aligned with the surface of the via structure 1238. In some implementations, the dielectric layer 1240 may cover the via structure 1238 and a cavity may be formed over a portion of the via structure 1238.

[00158] At stage 10, at least a portion of the carrier 1202 is removed (e.g., polish, grinded, etched). In some implementations, the carrier 1202 is removed until a surface of the carrier 1202 is aligned with a surface of the pad 1205. In some implementations, after stage 10, an integrated device 1260 is fabricated that includes an encapsulation layer and a via structure that includes a side barrier layer.

Exemplary Method for Providing / Fabricating an Integrated Device That Includes Via With Side Barrier Layer Traversing an Encapsulation Layer

[00159] In some implementations, providing an integrated device (e.g., integrated package) that includes a via structure several processes. FIG. 13 illustrates a method for providing an integrated device. In some implementations, the method of FIG. 13 may be used to provide / manufacture the integrated device of FIGS. 3, 4, 8 and/or 9, and/or other integrated devices described in the present disclose.

[00160] It should also be noted that the method of FIG. 13 may be used to provide / manufacture integrated devices that also include circuit elements. It should further be noted that the method of FIG. 13 may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device.

[00161] In some implementations, the process of FIG. 13 illustrates a novel process that provides an integrated device with high density interconnects.

[00162] The method provides (at 1305) a substrate. In some implementations, providing a substrate may include form and/or fabricating a substrate (e.g., substrate 502). In some implementations, the substrate is a wafer. Different implementations may use different materials for the substrate (e.g., silicon substrate, glass substrate, ceramic substrate, organic substrate). The substrate may include a set of through substrate vias (TSVs) and a set of pads. In some implementations, the substrate may also include other interconnects (e.g., traces). In some implementations, the set of pads is located on a first surface (e.g., top surface) of the substrate. In some implementations, the set of pads is embedded in the first surface of the substrate. In some implementations, the substrate may include a dielectric layer that is coupled (e.g., formed) on the first surface of the substrate.

[00163] The method further provides (at 1310) at least one die to the substrate. In some implementations, providing at least one die includes coupling a first die and a second die to the substrate. In some implementations, the first die is coupled to the substrate through a first set of interconnects (e.g., first pillar, first solder).

[00164] The method also provides (at 1315) an encapsulation layer. In some implementations, providing the encapsulation layer includes forming an encapsulation layer on the substrate and/or the dielectric layer on the substrate. In some implementations, the encapsulation layer encapsulates the first die. Different implementations may use different materials for the encapsulation layer. In some implementations, the encapsulation layer is a film layer. In some implementations, the encapsulation layer is made of a material that has a photo-patternable property.

[00165] The method then provides (at 1320) at least one via with a barrier layer in the encapsulation layer. In some implementations, providing at least one via with a barrier layer includes forming a cavity in the encapsulation layer and providing at least one metal layer in the cavity. In some implementations, the cavity is formed (e.g., created) over a pad. In some implementations, the cavity is formed by using a photo etching process (e.g., photolithography process).

[00166] In some implementations, providing at least one metal layer includes providing (e.g., forming) a barrier layer in the cavity. In some implementations, a plating process is used to form the barrier layer. The barrier layer may cover the inside walls of the cavity, at least part of the pad, and/or the first surface of the encapsulation layer. Different implementations may use different materials for the barrier layer. In some implementations, the barrier layer is one of at least titanium (Ti), (TiN),

Aluminium Copper (AlCu), tinanium copper alloy (TiCu) and/or titanium tungsten copper alloy (TiWCu). However, different implementations may use different materials. As such, the material for the barrier layer should not be limited to the materials listed above.

[00167] In some implementations, providing at least one metal layer further includes providing (e.g., forming, depositing) a seed layer on the barrier layer. In some implementations, a plating process is used to form the seed layer on the barrier layer. Different implementations may use different materials for the seed layer.

[00168] In some implementations, providing a via with a barrier layer also includes providing (e.g., forming, depositing) a photo resist layer on the seed layer. In some implementations, providing the photo resist layer includes providing the photo resist layer 534 and selectively removing some portions of the photo resist layer.

[00169] The method then provides a metal layer on the seed layer. In some implementations, the metal layer is provided on the seed layer that is not covered by the photo resist layer. In some implementations, a lithography and plating process is used to provide the metal layer on the seed layer. In some implementations, the metal layer and the seed layer are the same material. Thus, in some implementations, the metal layer may include the seed layer.

[00170] The method may then selectively remove the photo resist layer, the seed layer, and the barrier layer are selectively removed (e.g., etched). In some implementations, the photo resist layer, the seed layer, and the barrier layer are removed concurrently. In some implementations, the photo resist layer, the seed layer, and the barrier layer are removed sequentially.

[00171] In some implementations, a dielectric layer may optionally be provided (e.g., formed) on a second surface of the encapsulation layer. In some implementations, another dielectric layer may optionally be provided (e.g., formed) on the second surface (e.g., bottom surface) of the substrate. In addition, a set of interconnects may also be provided on / in the dielectric layer.

Exemplary Electronic Devices

[00172] FIG. 14 illustrates various electronic devices that may be integrated with any of the aforementioned integrated device, semiconductor device, integrated circuit, die, interposer or package. For example, a mobile telephone 1402, a laptop computer 1404, and a fixed location terminal 1406 may include an integrated device1400 as described

herein. The integrated device 1400 may be, for example, any of the integrated circuits, dies, interposer, or packages described herein. The devices 1402, 1404, 1406 illustrated in FIG. 14 are merely exemplary. Other electronic devices may also feature the integrated device 1400 including, but not limited to, mobile devices, hand-held personal communication systems (PCS) units, portable data units such as personal digital assistants, GPS enabled devices, navigation devices, set top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, communications devices, smartphones, tablet computers or any other device that stores or retrieves data or computer instructions, or any combination thereof.

[00173] One or more of the components, steps, features, and/or functions illustrated in FIGS. 3, 4, 5A-5C, 6, 7A-7C, 8, 9, 10A-10C, 11, 12A-12C, 13 and/or 14 may be rearranged and/or combined into a single component, step, feature or function or embodied in several components, steps, or functions. Additional elements, components, steps, and/or functions may also be added without departing from the disclosure. It should also be noted that FIGS. 3, 4, 5A-5C, 6, 7A-7C, 8, 9, 10A-10C, 11, 12A-12C, 13 and/or 14 and its corresponding description in the present disclosure is not limited to dies and/or ICs. In some implementations, FIGS. 3, 4, 5A-5C, 6, 7A-7C, 8, 9, 10A-10C, 11, 12A-12C, 13 and/or 14 and its corresponding description may be used to manufacture, create, provide, and/or produce integrated devices. In some an integrated device may include a die package, an integrated circuit (IC), a wafer, a semiconductor device, and/or an interposer.

[00174] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any implementation or aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects of the disclosure. Likewise, the term "aspects" does not require that all aspects of the disclosure include the discussed feature, advantage or mode of operation. The term "coupled" is used herein to refer to the direct or indirect coupling between two objects. For example, if object A physically touches object B, and object B touches object C, then objects A and C may still be considered coupled to one another—even if they do not directly physically touch each other.

[00175] Also, it is noted that the embodiments may be described as a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the

operations may be re-arranged. A process is terminated when its operations are completed.

[00176] The various features of the disclosure described herein can be implemented in different systems without departing from the disclosure. It should be noted that the foregoing aspects of the disclosure are merely examples and are not to be construed as limiting the disclosure. The description of the aspects of the present disclosure is intended to be illustrative, and not to limit the scope of the claims. As such, the present teachings can be readily applied to other types of apparatuses and many alternatives, modifications, and variations will be apparent to those skilled in the art.

CLAIMS

WHAT IS CLAIMED IS:

1. An integrated device comprising:

an encapsulation layer;

a via structure traversing the encapsulation layer, wherein the via structure comprises:

a via comprising a first side, a second side, and a third side; and

a barrier layer surrounding at least the first side and the third side of the via; and

a pad directly coupled to the barrier layer of the via structure.

2. The integrated device of claim 1, further comprising a first dielectric layer coupled to a first surface of the encapsulation layer.

3. The integrated device of claim 2, further comprising a second dielectric layer coupled to a second surface of the encapsulation layer.

4. The integrated device of claim 1, further comprising a substrate coupled to a first surface of the encapsulation layer.

5. The integrated device of claim 4, further comprising a first die coupled to the substrate, wherein the encapsulation layer encapsulates the first die.

6. The integrated device of claim 4, wherein the via structure further comprises a fill.

7. The integrated device of claim 1, wherein the via comprises a seed layer.

8. The integrated device of claim 1, wherein the via comprises a portion configured to operate as a pad.

9. The integrated device of claim 1, wherein the integrated device comprises one of at least an interposer, a package device, and/or a package-on-package (PoP) device.

10. The integrated device of claim 1, wherein the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

11. An apparatus comprising:

an encapsulation layer;

a via structure traversing the encapsulation layer, wherein the via structure comprises:

a via comprising a first side, a second side, and a third side; and

a barrier means surrounding at least the first side and the third side of the via; and

a pad directly coupled to the barrier means of the via structure.

12. The apparatus of claim 11, further comprising a first dielectric layer coupled to a first surface of the encapsulation layer.

13. The apparatus of claim 12, further comprising a second dielectric layer coupled to a second surface of the encapsulation layer.

14. The apparatus of claim 11, further comprising a substrate coupled to a first surface of the encapsulation layer.

15. The apparatus of claim 14, further comprising a first die coupled to the substrate, wherein the encapsulation layer encapsulates the first die.

16. The apparatus of claim 11, wherein the via structure further comprises a fill means.

17. The apparatus of claim 11, wherein the via comprises a seed layer.

18. The apparatus of claim 11, wherein the via comprises a portion configured to operate as a pad.

19. The apparatus of claim 11, wherein the apparatus comprises one of at least an interposer, a package device, and/or a package-on-package (PoP) device.

20. The apparatus of claim 11, wherein the apparatus is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

21. A method for fabricating an integrated device, comprising:

forming a pad on a substrate;

forming an encapsulation layer on the substrate; and

forming a via structure in the encapsulation layer, wherein forming the via structure comprises:

forming a barrier layer in the encapsulation layer; and

forming a via on the barrier layer, the via comprising a first side, a second side, and a third side, the via is formed on the barrier layer such that the barrier layer surrounds at least the first side and the third side of the via, wherein the barrier layer is directly coupled to the pad.

22. The method of claim 21, further comprising forming a first dielectric layer on a first surface of the encapsulation layer.

23. The method of claim 22, further comprising forming a second dielectric layer on a second surface of the encapsulation layer.

24. The method of claim 21, further comprising removing at least a portion of the substrate.

25. The method of claim 21, further comprising coupling a first die to the substrate, wherein forming the encapsulation layer comprising encapsulating the first die with the encapsulation layer.

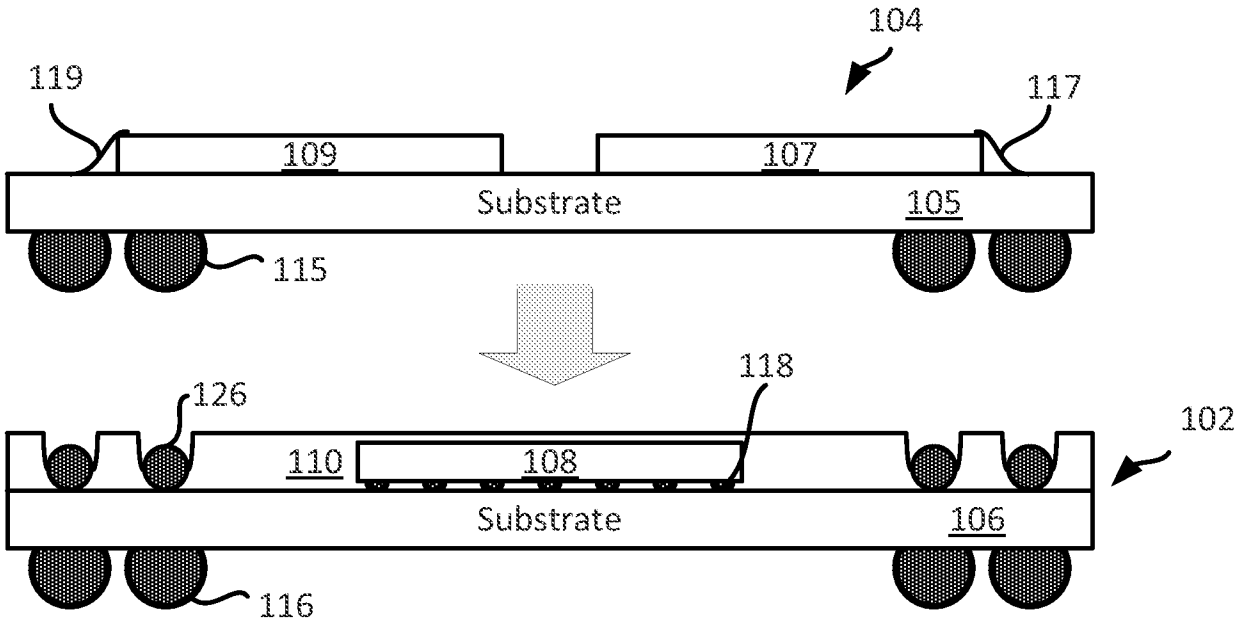
26. The method of claim 21, wherein forming the via structure further comprises forming a fill.

27. The method of claim 21, wherein forming the via comprises forming a seed layer on the barrier layer.

28. The method of claim 21, wherein forming the via comprises forming a portion a via as a pad.

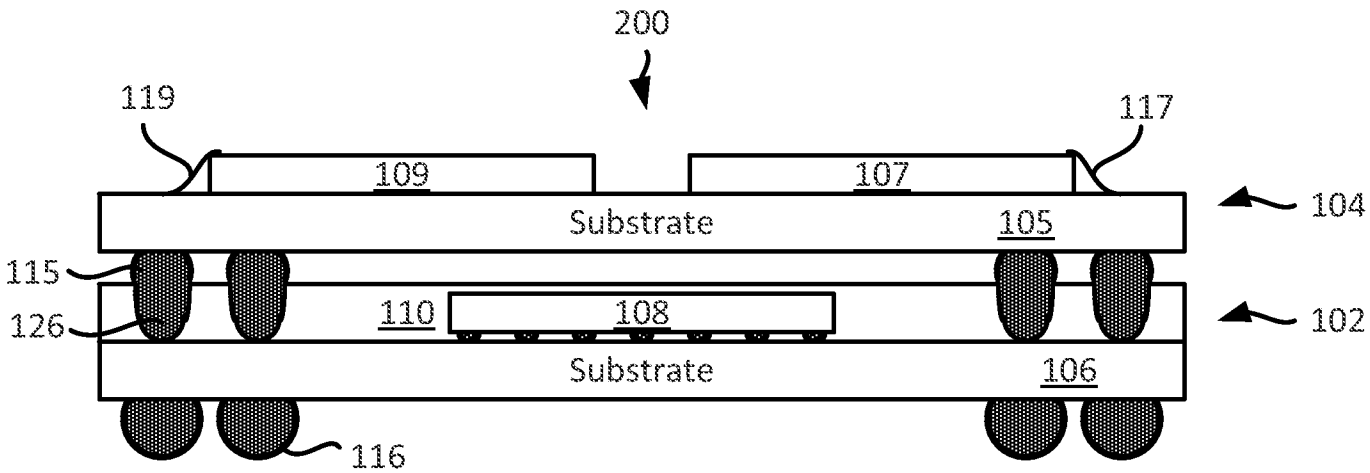
29. The method of claim 21, wherein the integrated device comprises one of at least an interposer, a package device, and/or a package-on-package (PoP) device.

30. The method of claim 21, wherein the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.



PRIOR ART

FIG. 1



PRIOR ART

FIG. 2

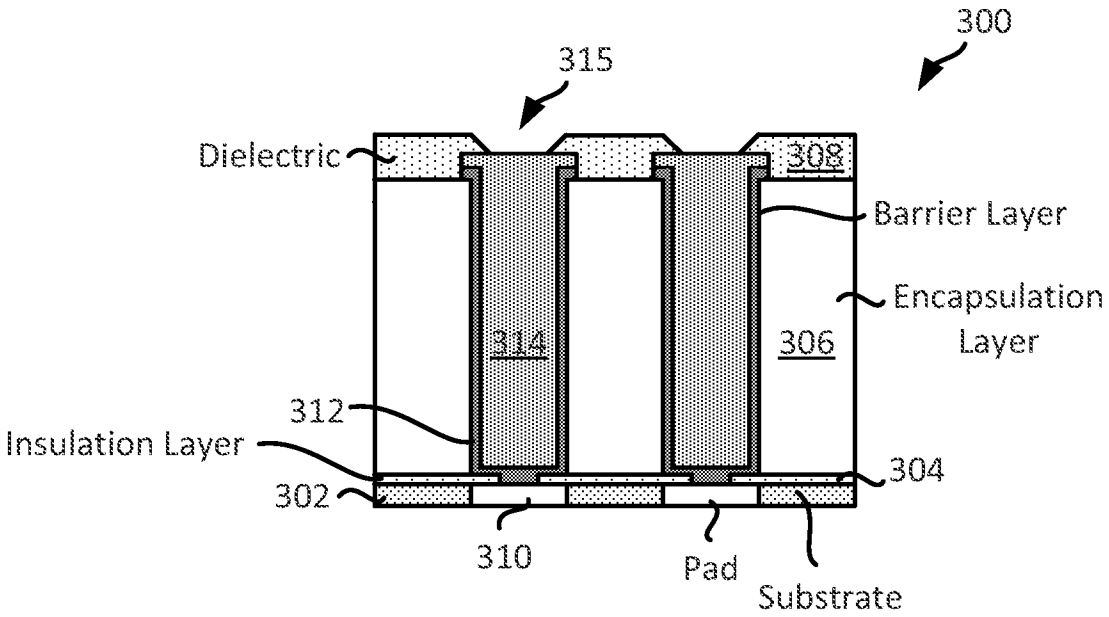

300
315
Dielectric
308
Barrier Layer
Encapsulation Layer
314
306
312
Insulation Layer
304
302
310
Pad
Substrate

FIG. 3

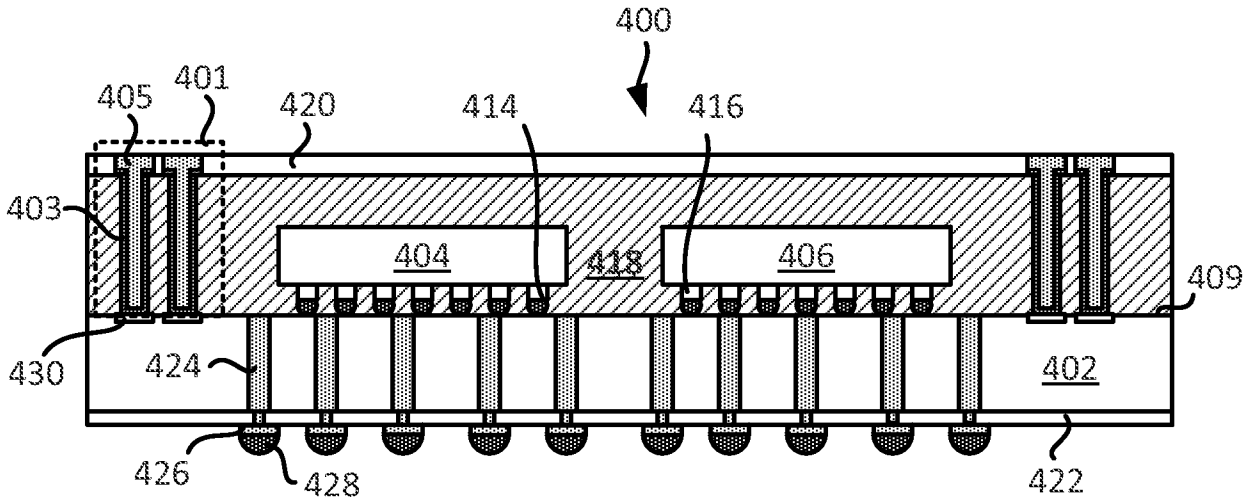

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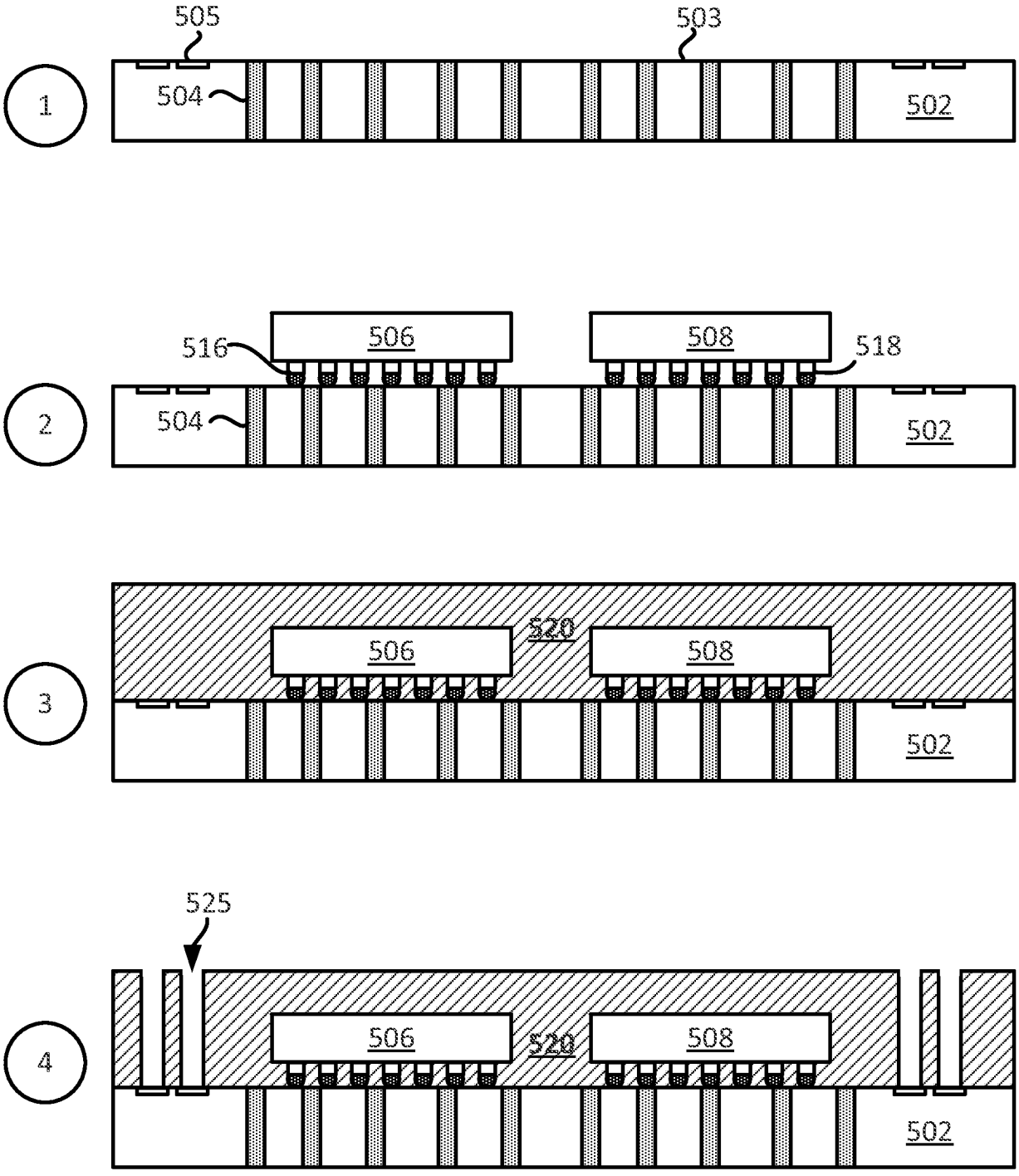
FIG. 4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503
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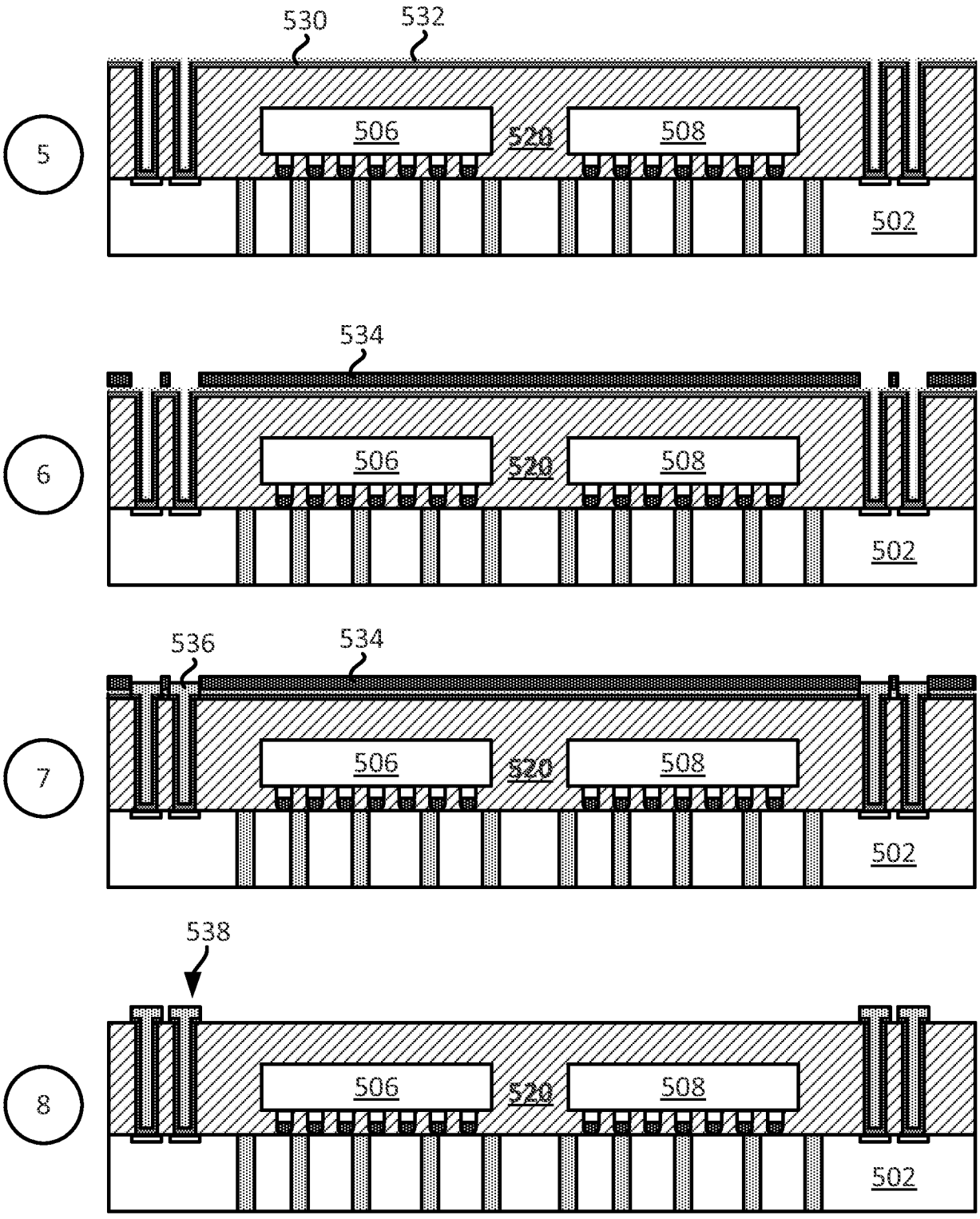
502

FIG. 5A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502
8
538
506
520
508
502

FIG. 5B

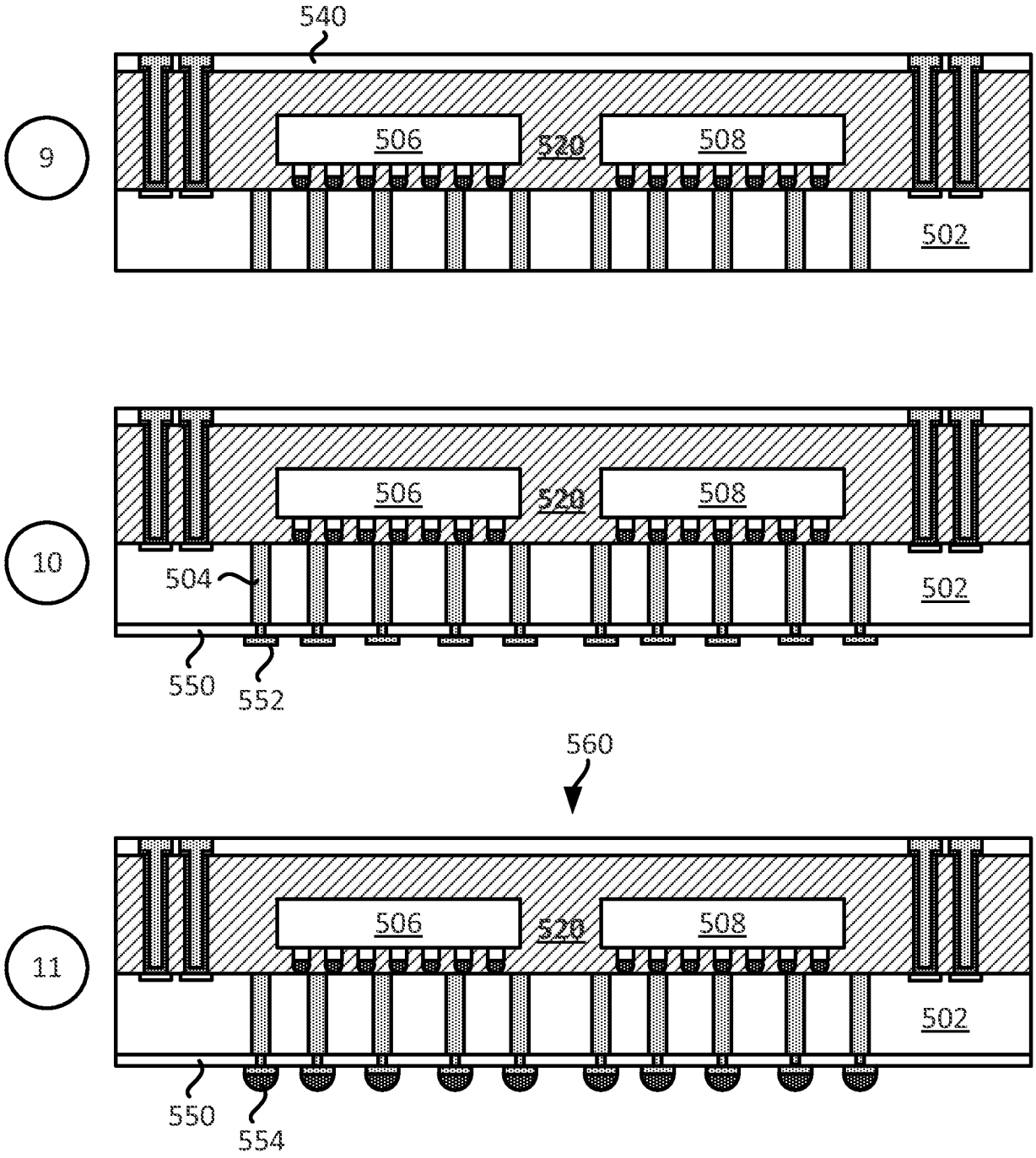


FIG. 5C

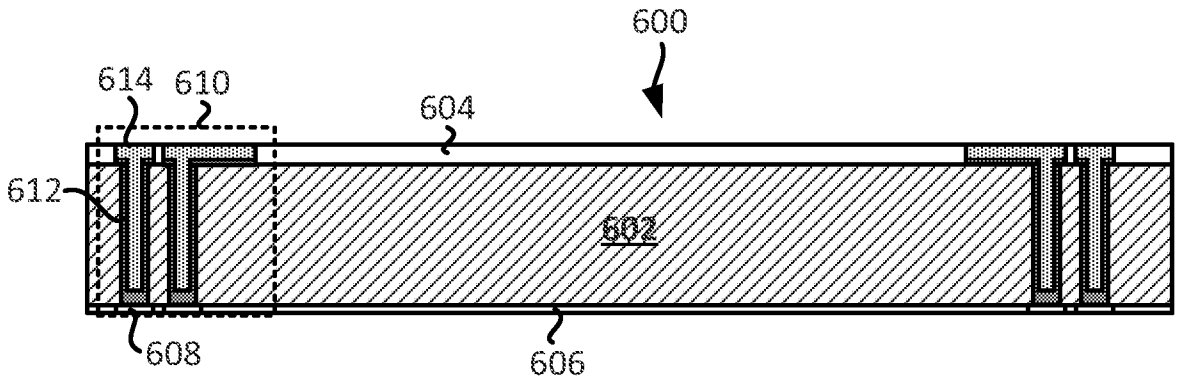


FIG. 6

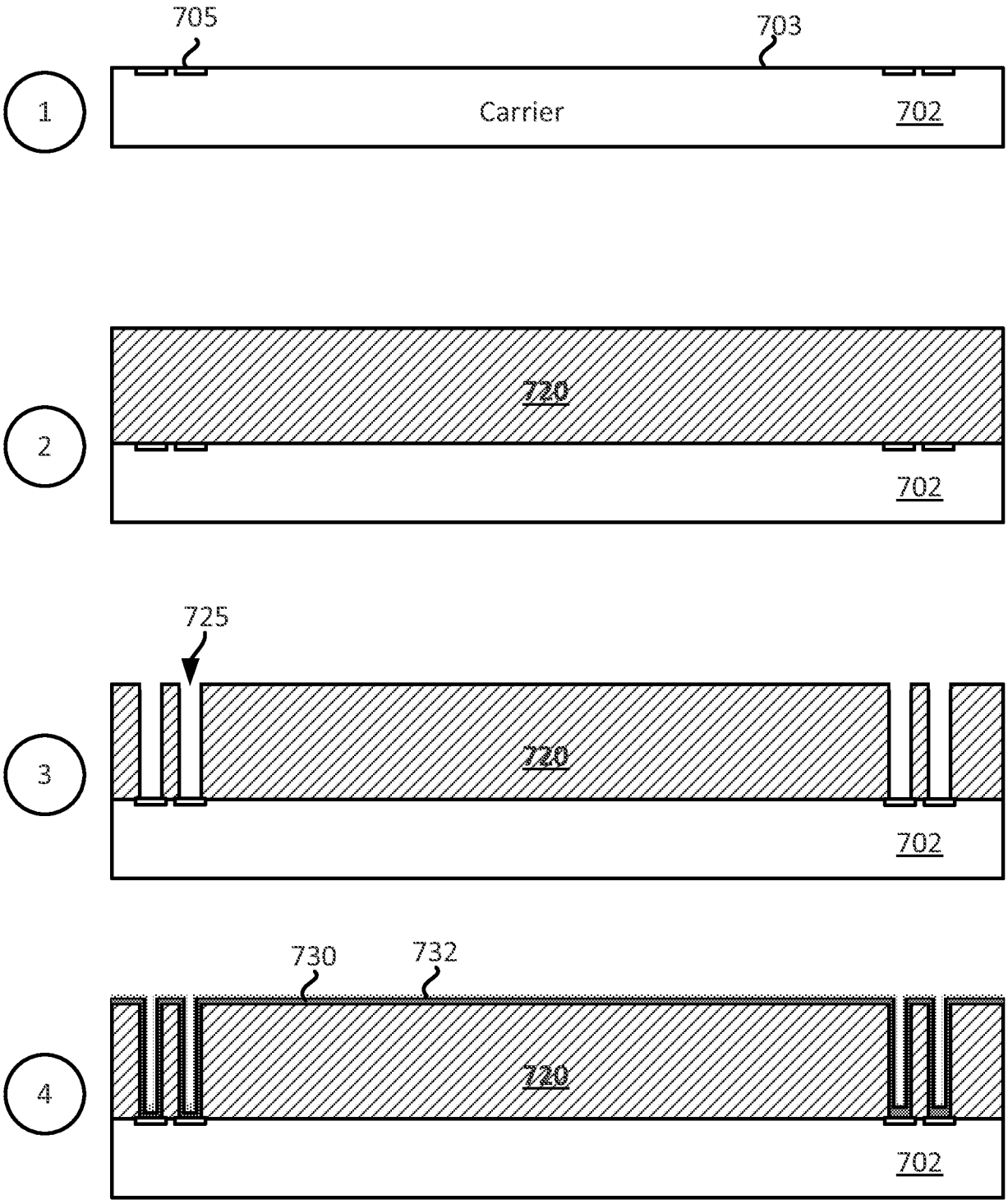


FIG. 7A

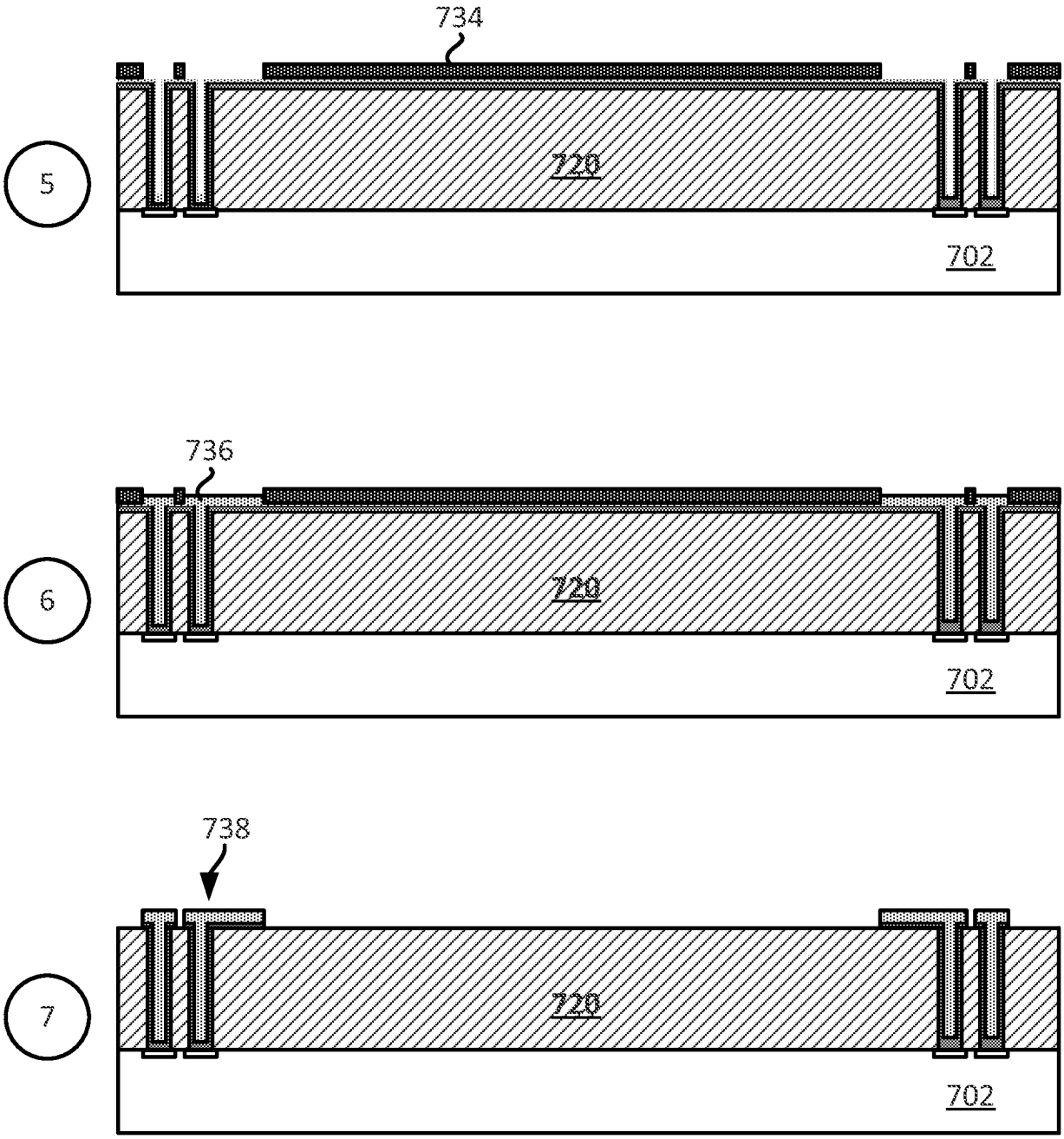


FIG. 7B

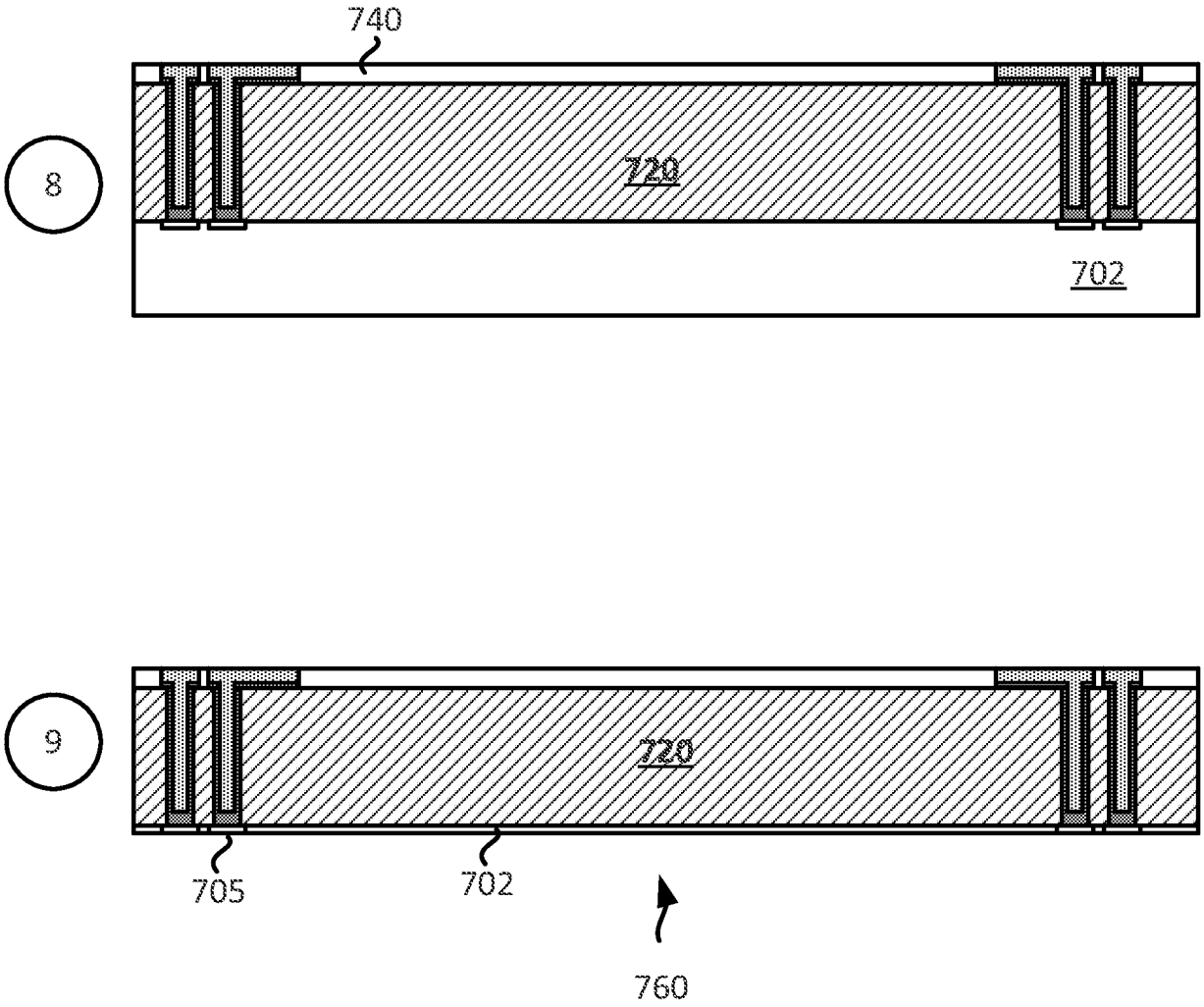


FIG. 7C

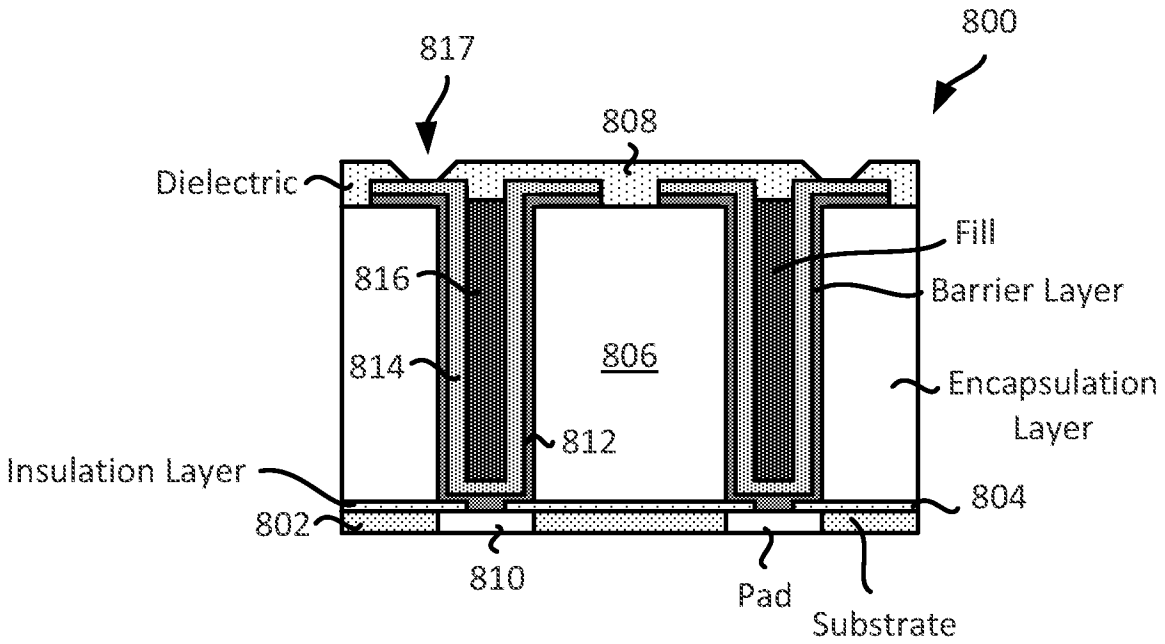
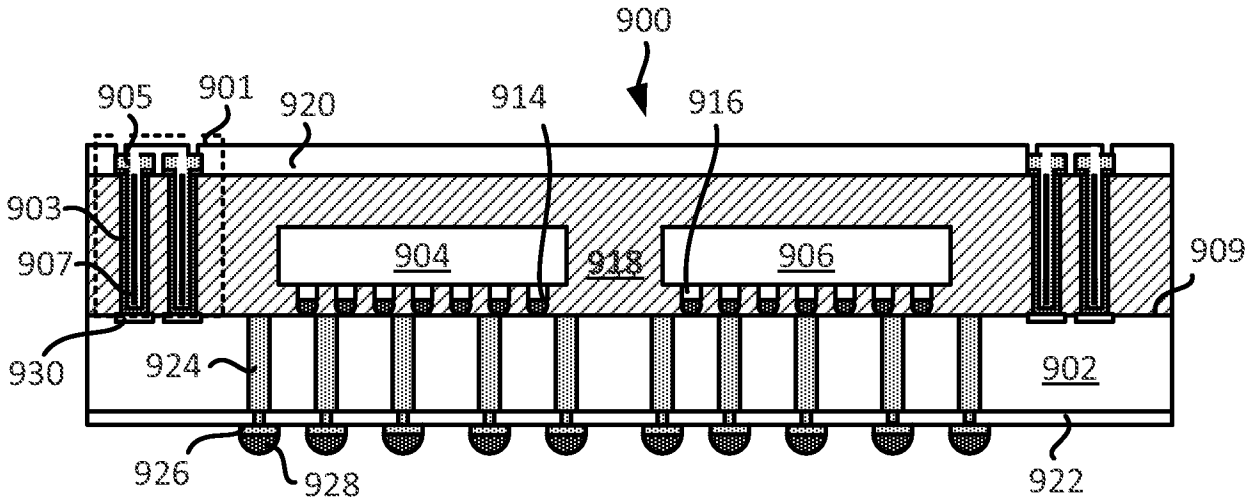

800
817
808
Dielectric
Fill
816
Barrier Layer
806
814
Encapsulation Layer
812
Insulation Layer
804
802
810
Pad
Substrate

FIG. 8


900
905
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903
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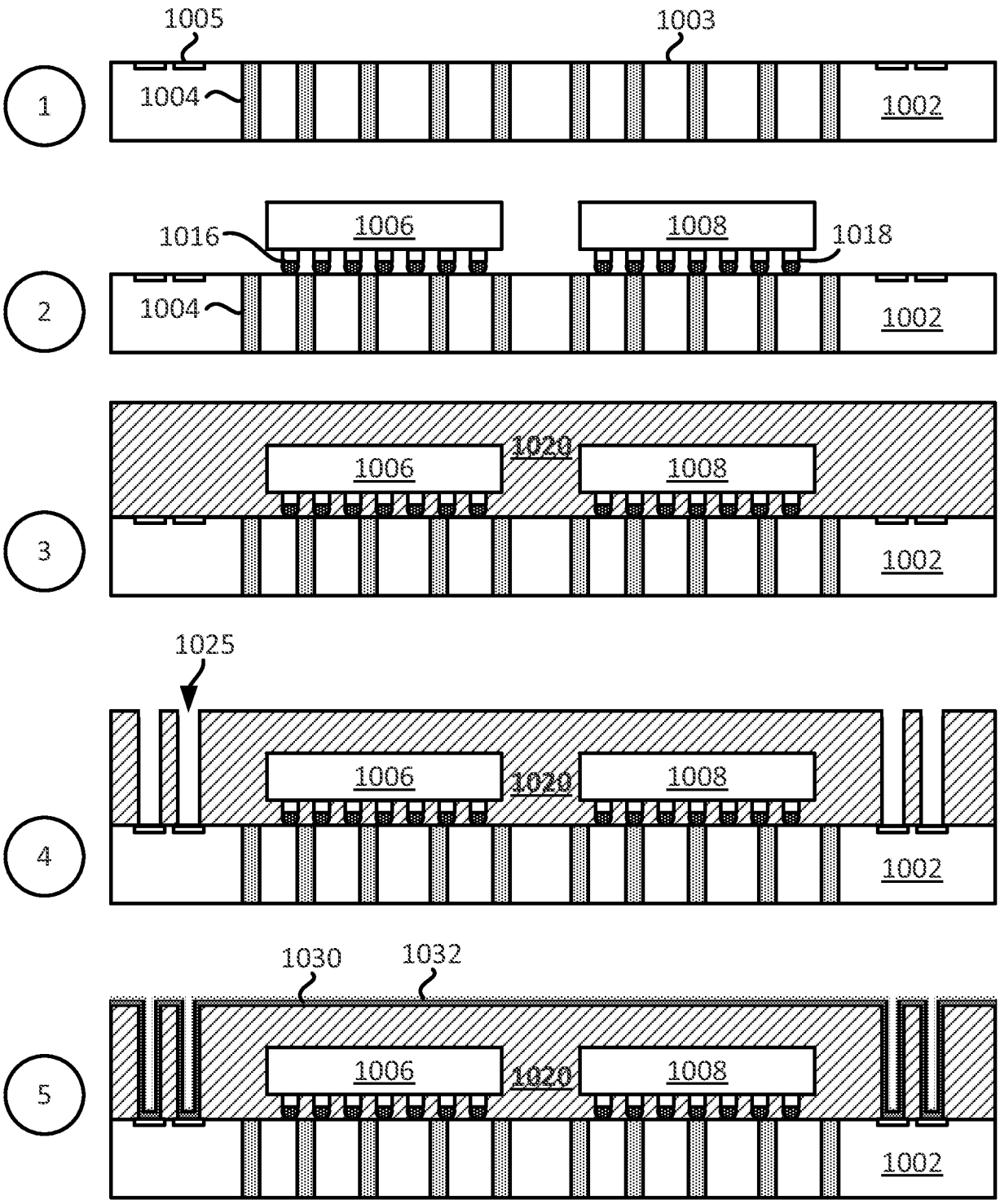
FIG. 9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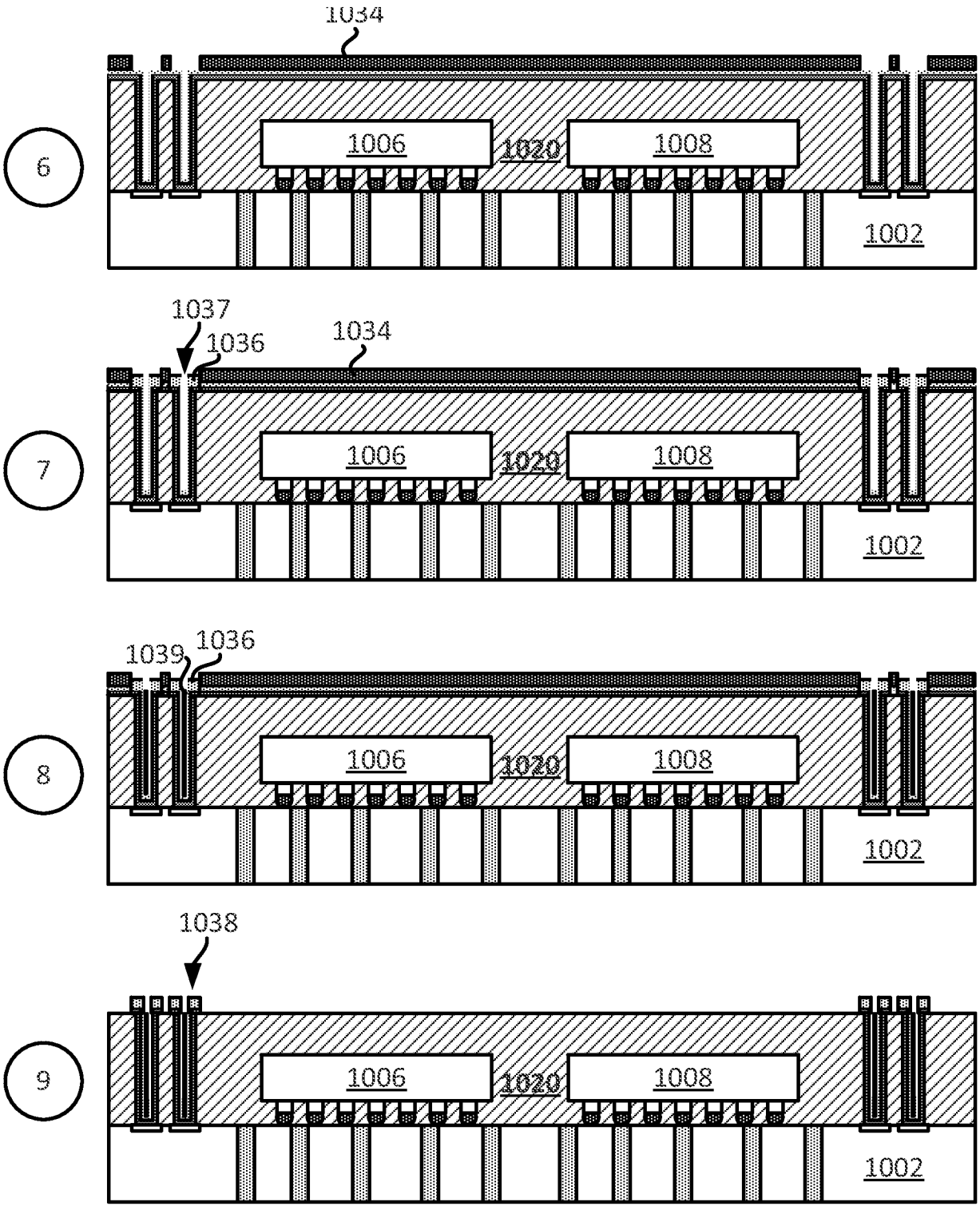
1020
1008
1002
5
1030
1032
1006
1020
1008
1002

FIG. 10A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1006
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1034
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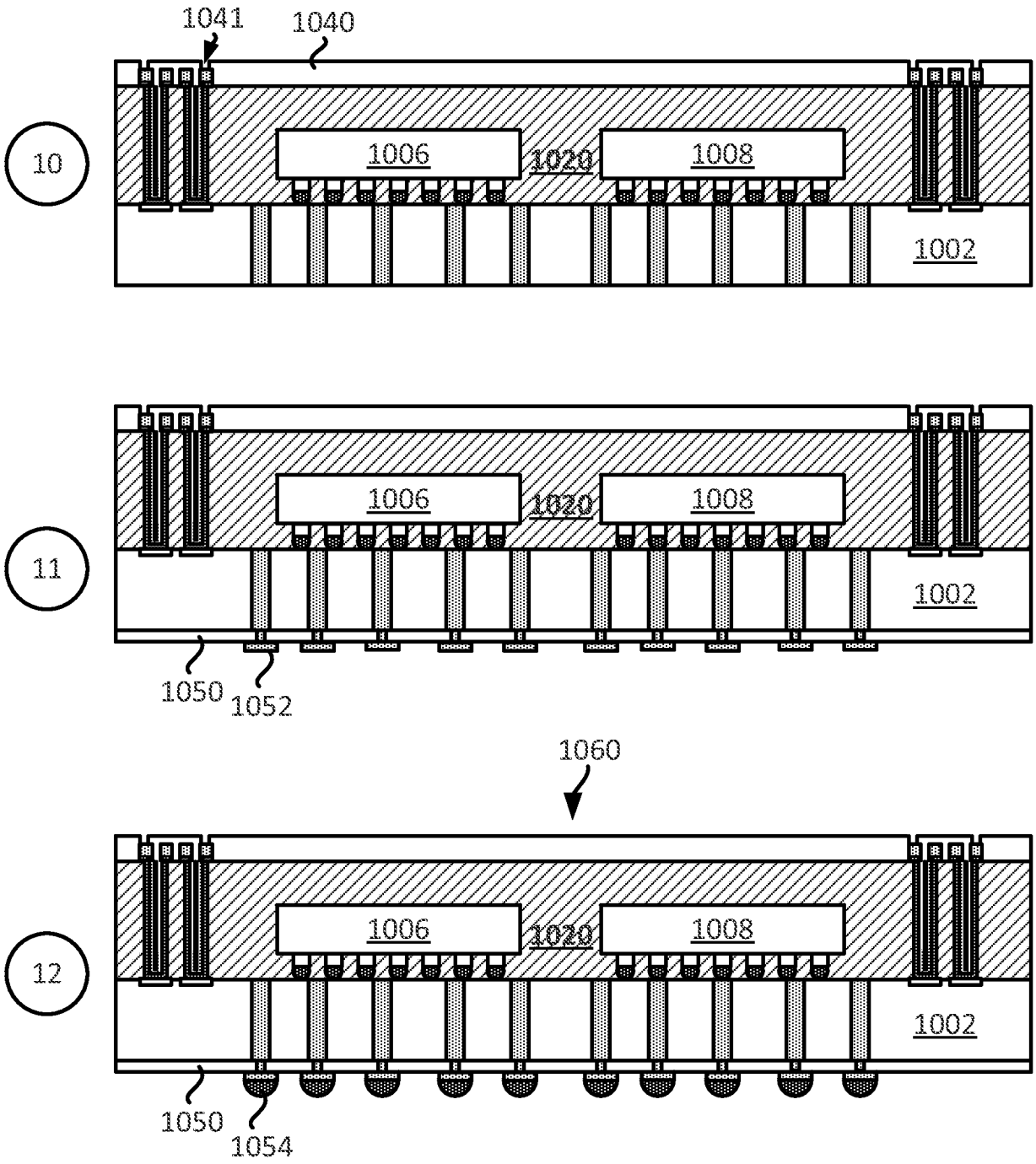
1020
1008
1002
9
1038
1006
1020
1008
1002

FIG. 10B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1008
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1006
1020
1008
1002
1050
1054

FIG. 10C

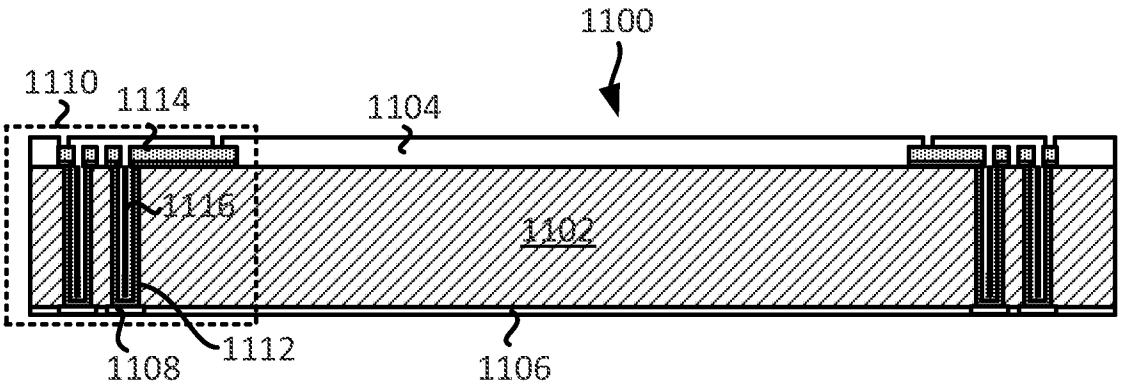
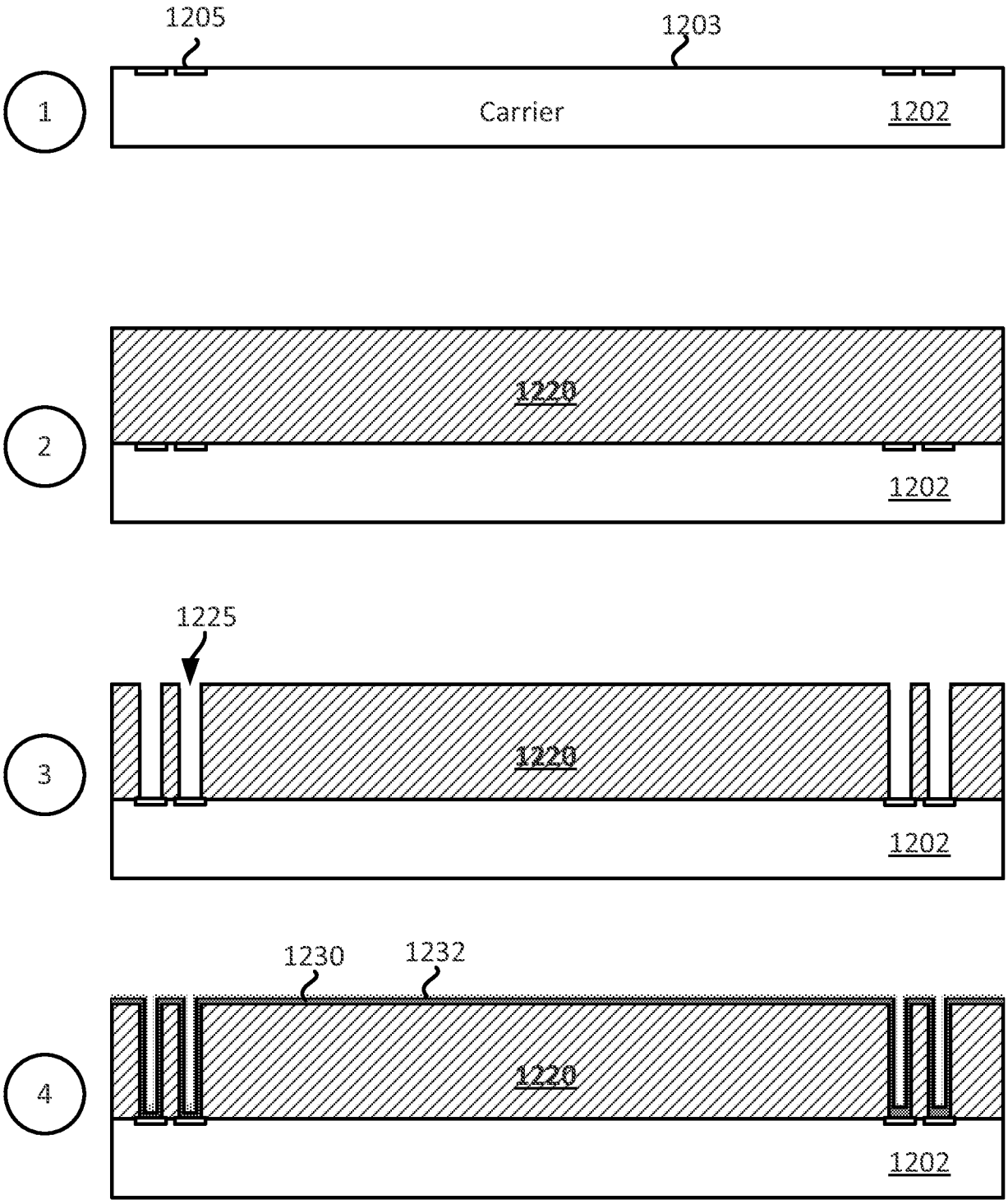


FIG. 11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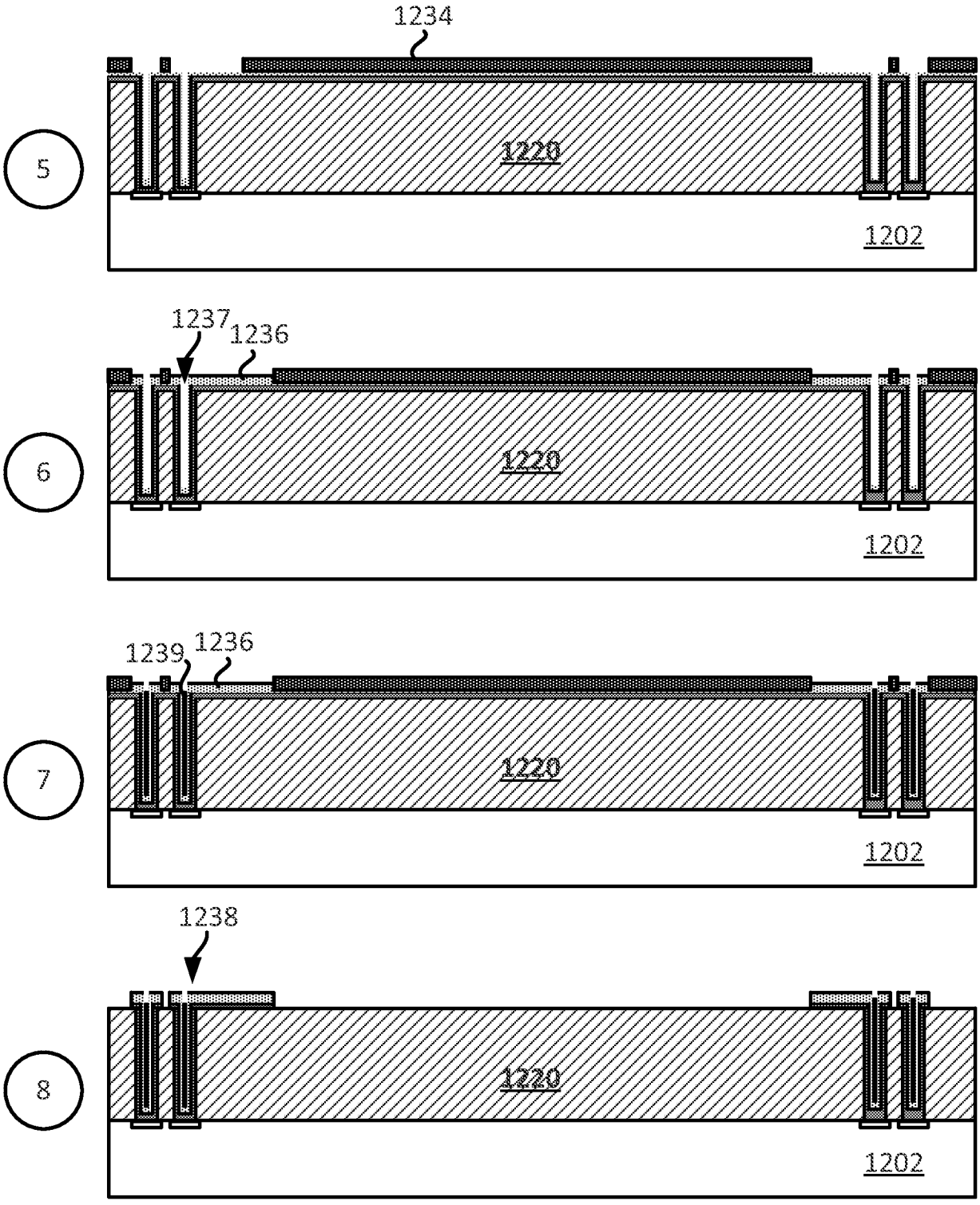
1203
1
Carrier
1202
1220
2
1202
1225
1220
3
1202
1230
1232
1220
4
1202

FIG. 12A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1236
1220
1202
6
1239
1236
1220
1202
7
1238
1220
1202
8

FIG. 12B

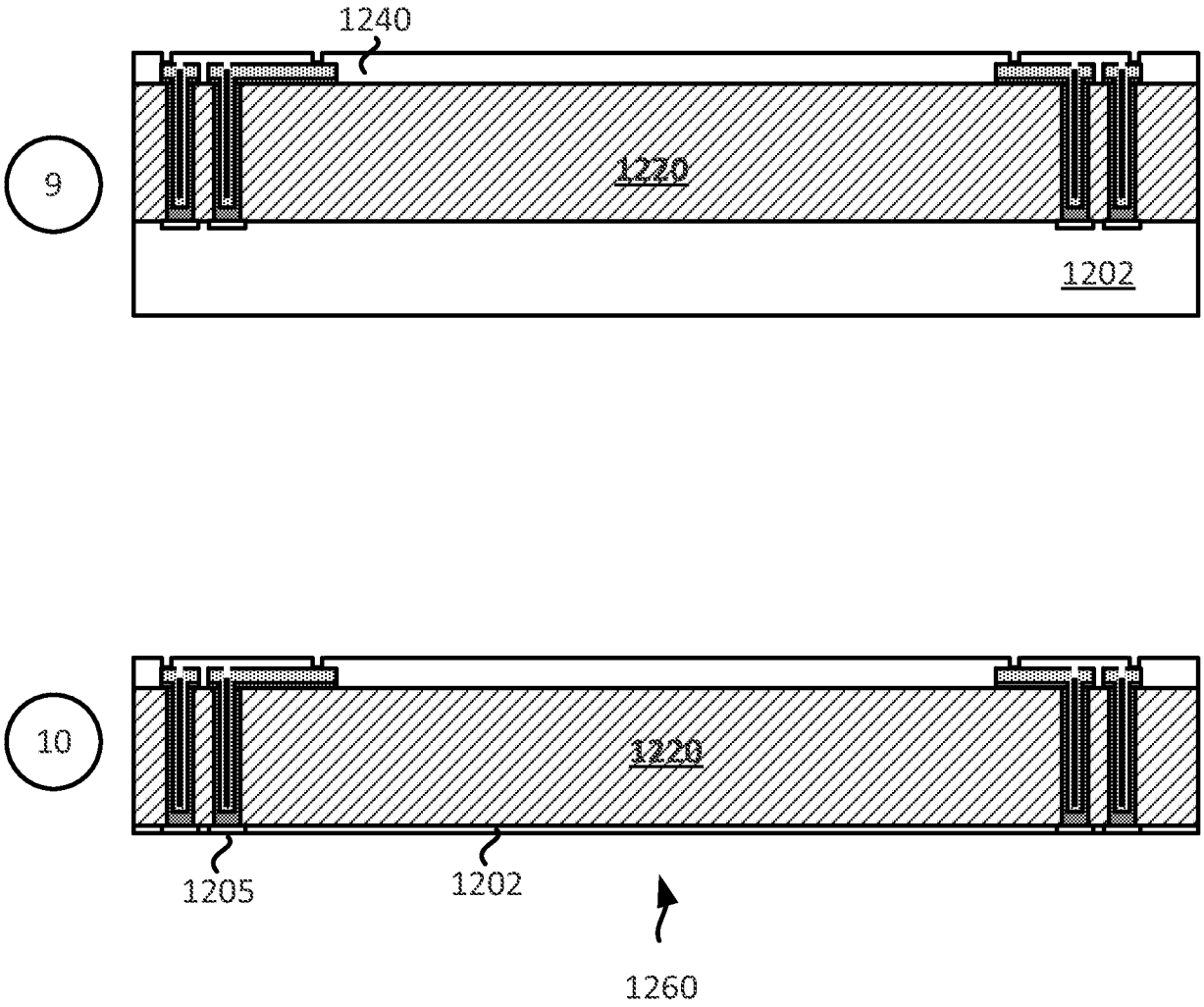

FIG. 12C

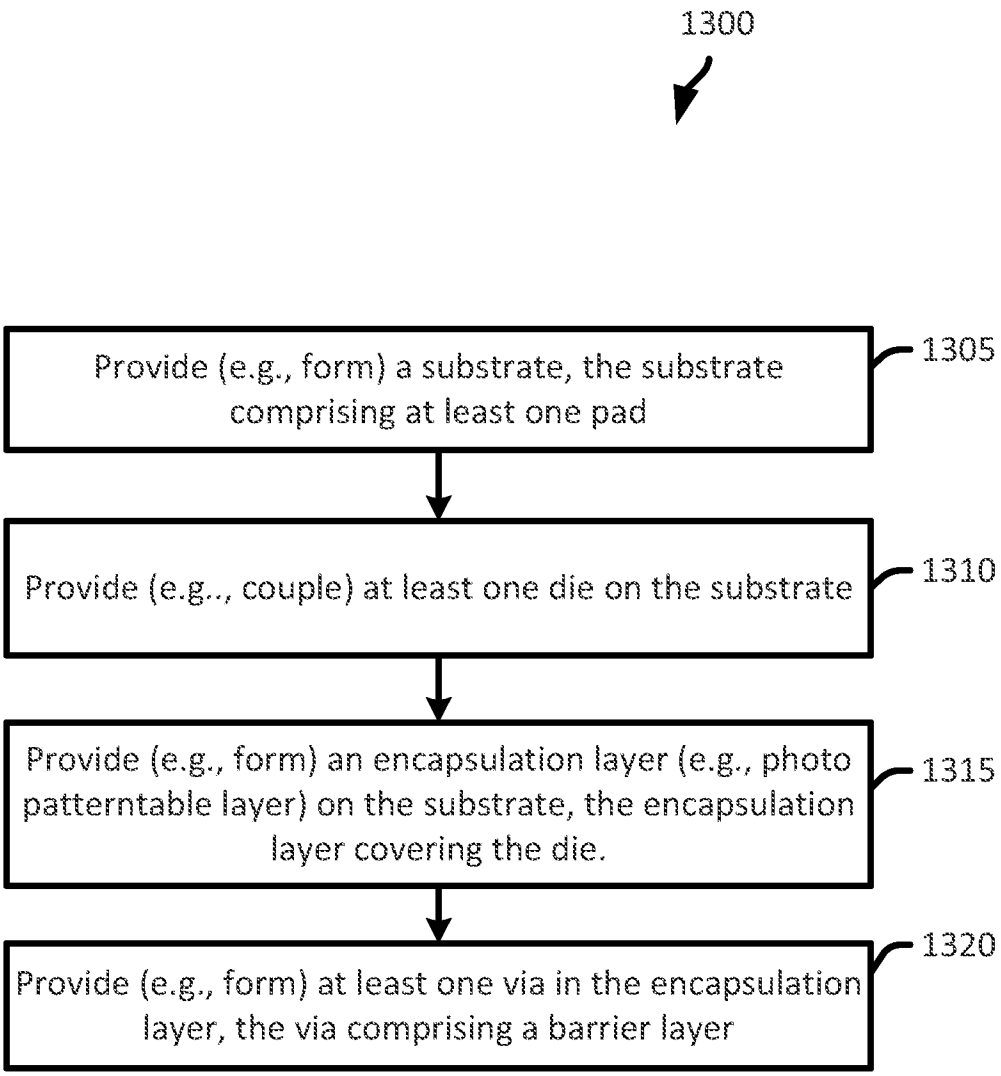
1300
Provide (e.g., form) a substrate, the substrate comprising at least one pad
1305
Provide (e.g.., couple) at least one die on the substrate
1310
Provide (e.g., form) an encapsulation layer (e.g., photo patterntable layer) on the substrate, the encapsulation layer covering the die.
1315
Provide (e.g., form) at least one via in the encapsulation layer, the via comprising a barrier layer
1320

FIG. 13

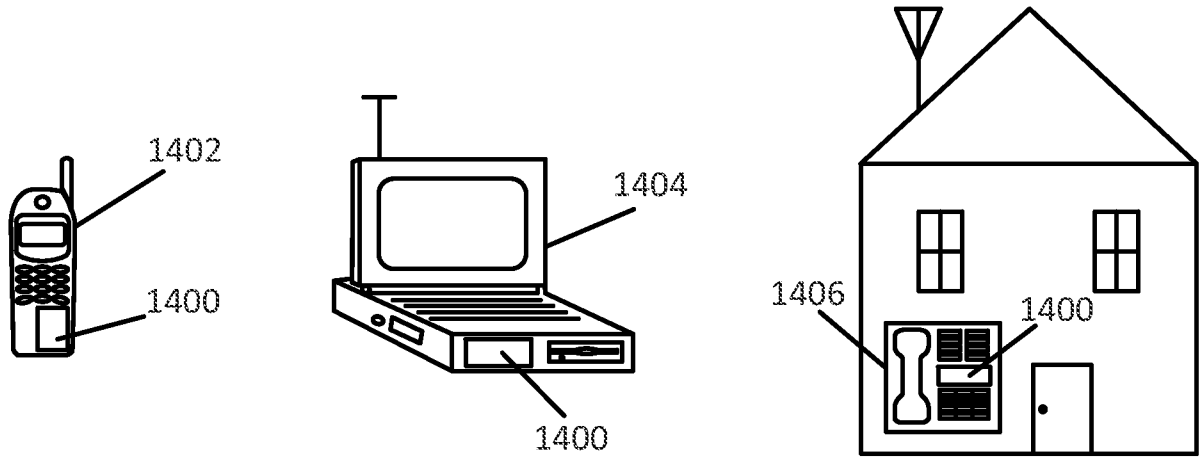

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/015421

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/498 H01L25/10
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/168944 A1 (GAN KAH WEE [MY] ET AL) 5 July 2012 (2012-07-05) paragraphs [0066], [0067]; figure 4B -----	1-3, 5-13, 15-23, 25-30
X	US 2013/341786 A1 (HSU CHUN-LEI [TW] ET AL) 26 December 2013 (2013-12-26) paragraph [0047]; figure 8 -----	1,4,11, 14,21,24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 April 2015	08/05/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kästner, Martin

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/015421

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012168944 A1	05-07-2012	NONE	
US 2013341786 A1	26-12-2013	CN 103515362 A	15-01-2014
		KR 20140000608 A	03-01-2014
		TW 201401482 A	01-01-2014
		US 2013341786 A1	26-12-2013