

- [54] **ELECTRICAL FUEL CONTROL SYSTEM
FOR INTERNAL COMBUSTION ENGINES**
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- [73] Assignee: **Nippondenso Co., Ltd.**, Kariya,
Japan
- [*] Notice: The portion of the term of this
patent subsequent to June 11, 1991,
has been disclaimed.

- [22] Filed: Feb. 20, 1974

- [21] Appl. No.: 444,170

Related U.S. Application Data

- [63] Continuation-in-part of Ser. No. 327,603, Jan. 26, 1973, Pat. No. 3,816,717, which is a continuation of Ser. No. 126,830, March 22, 1971, abandoned.

[30] **Foreign Application Priority Data**

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Apr. 10, 1970	Japan.....	45-30951
Apr. 15, 1970	Japan.....	45-32103
Apr. 15, 1970	Japan.....	45-32106
Apr. 22, 1970	Japan.....	45-34606

- [52] **U.S. Cl.**..... 235/150.21; 132/32 EA; 235/150.1;
235/150.53; 235/164
- [51] **Int. Cl.**². **F02D 5/00**; F02D 37/02; G05B 15/02
- [58] **Field of Search**..... 235/150.21, 150.1, 164,
235/151; 123/32 EA

[56]

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Primary Examiner—Felix D. Gruber

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57]

ABSTRACT

An electrical control system with a plurality of sensors, shifted code setting circuits, selecting means, adders, memories and a command signal generator causing output signals of the sensors to be respectively binary-coded, shifted by the shifted code setting circuits and selected in accordance with the output signals of the sensor corresponding thereto in the manner previously programmed, for developing respective output signals which are added in a time-sharing manner controlled by the command signal generator to obtain an engine control signal to secure the optimum engine condition.

11 Claims, 45 Drawing Figures

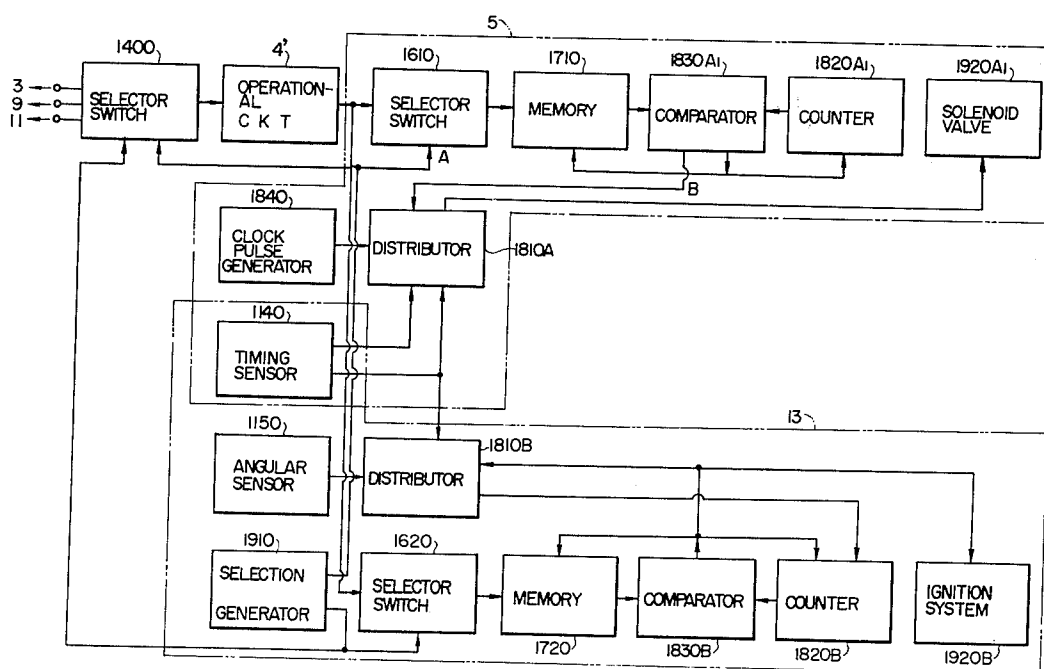


FIG. 1

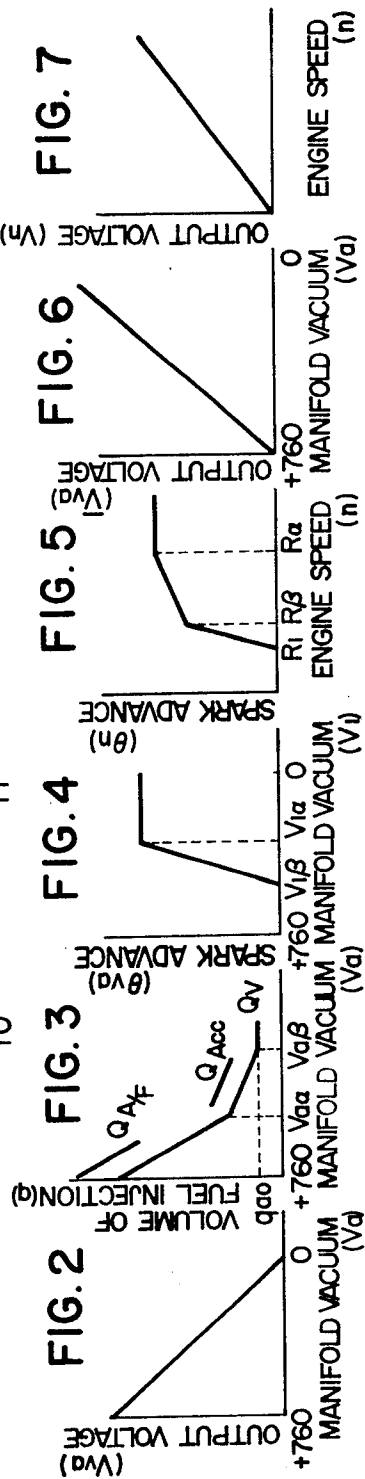
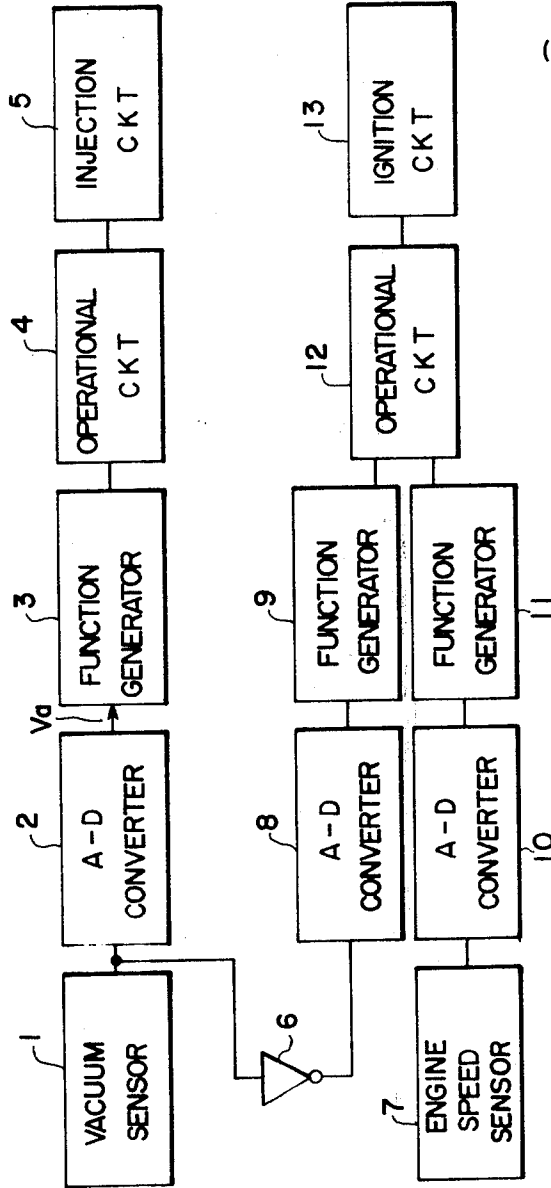


FIG. 8

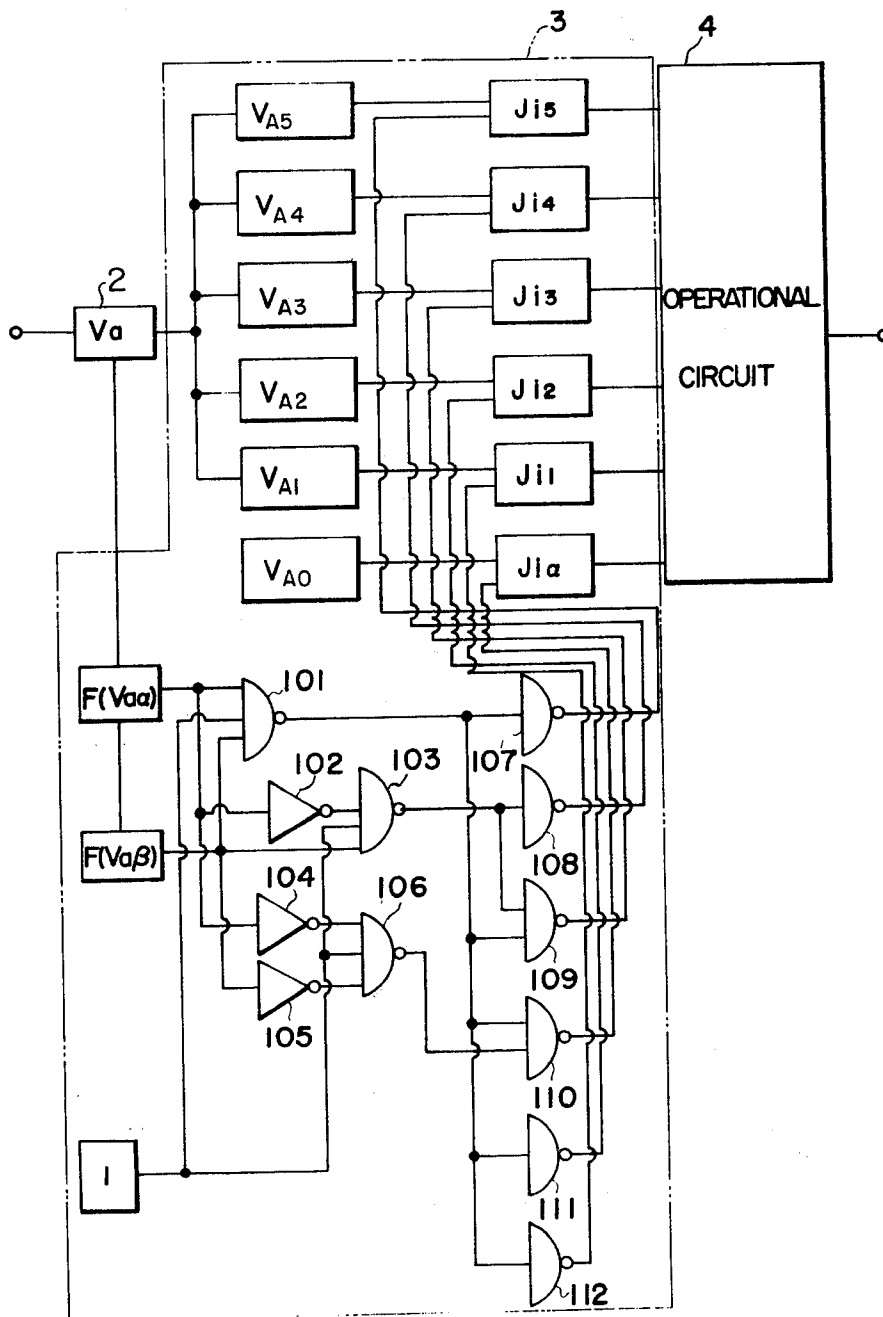


FIG. 9

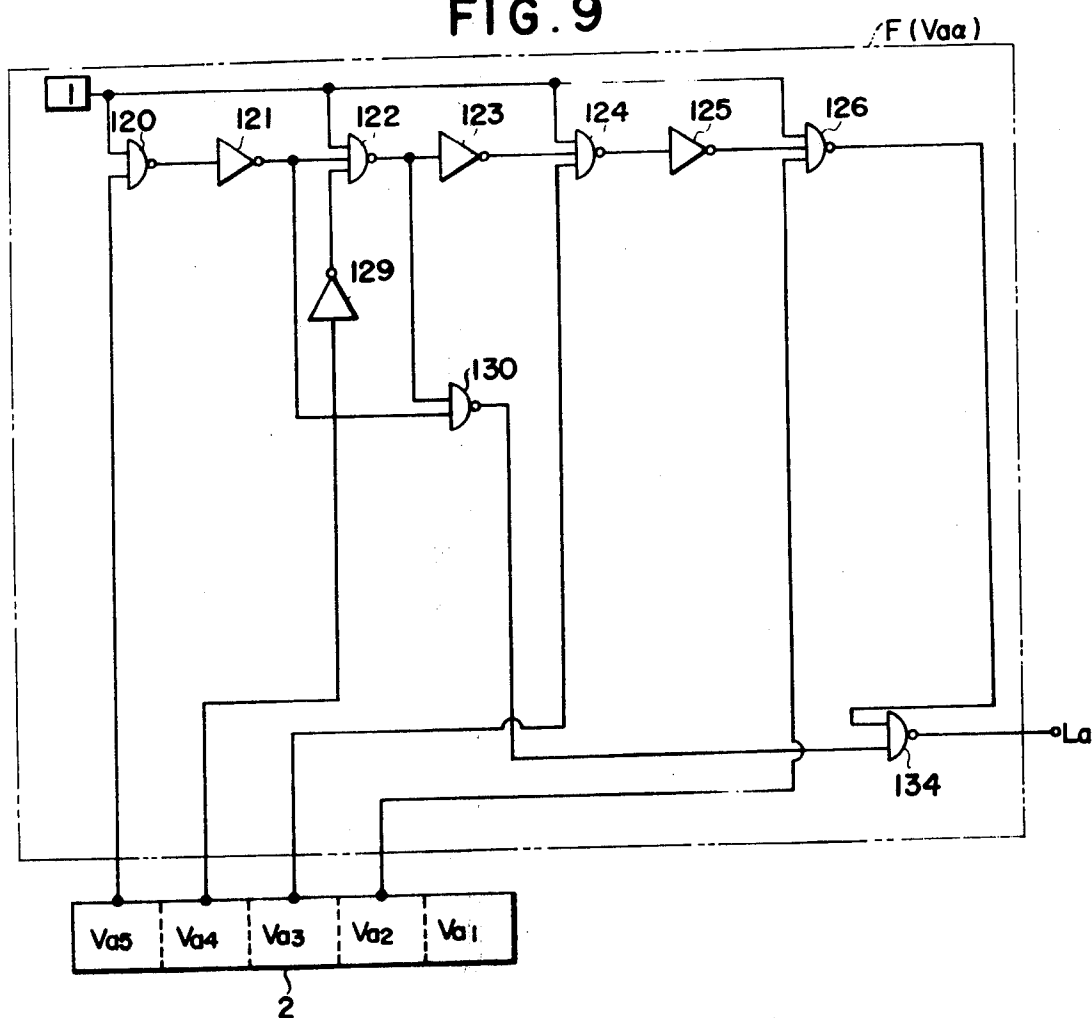


FIG. 10

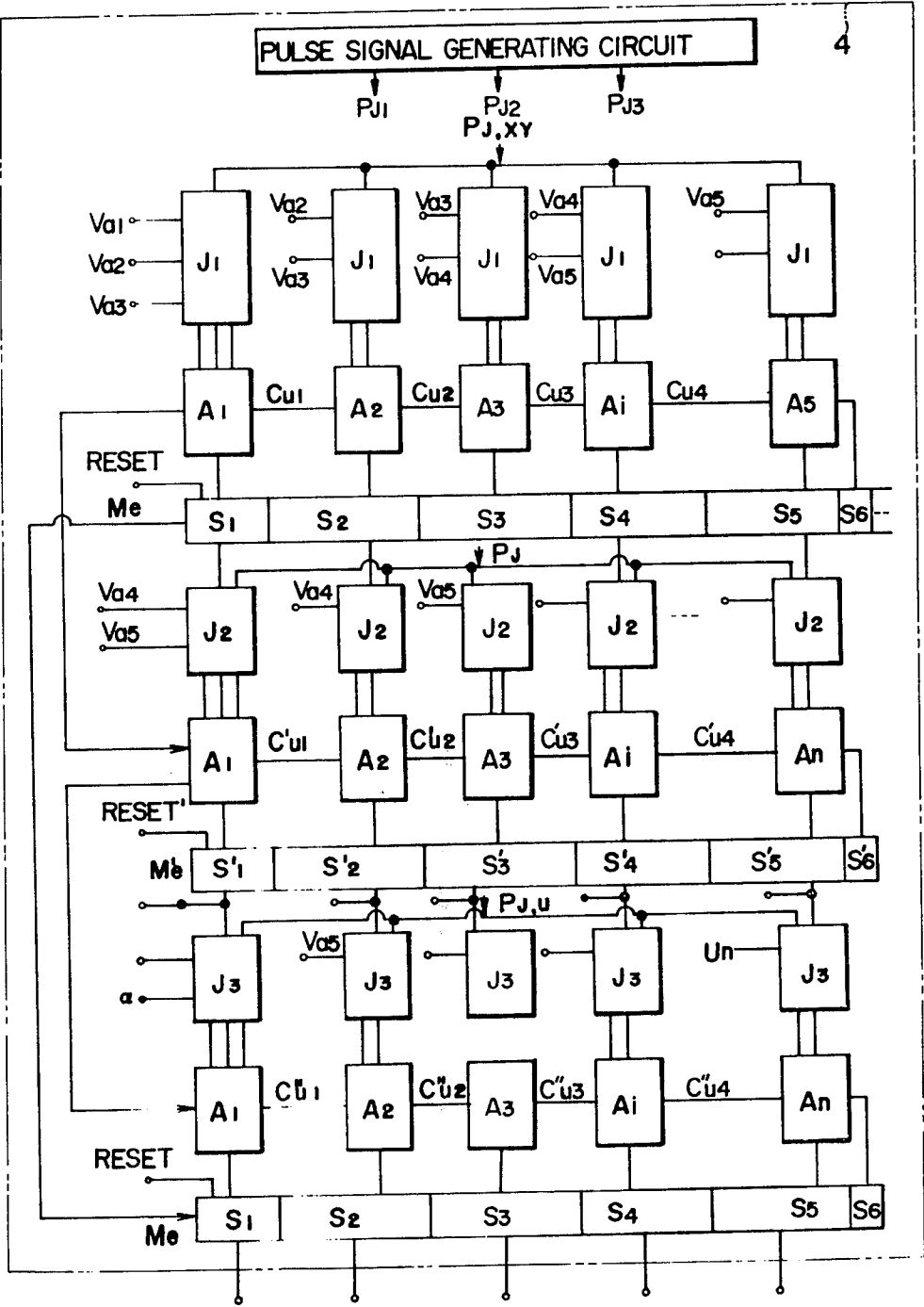


FIG. 11

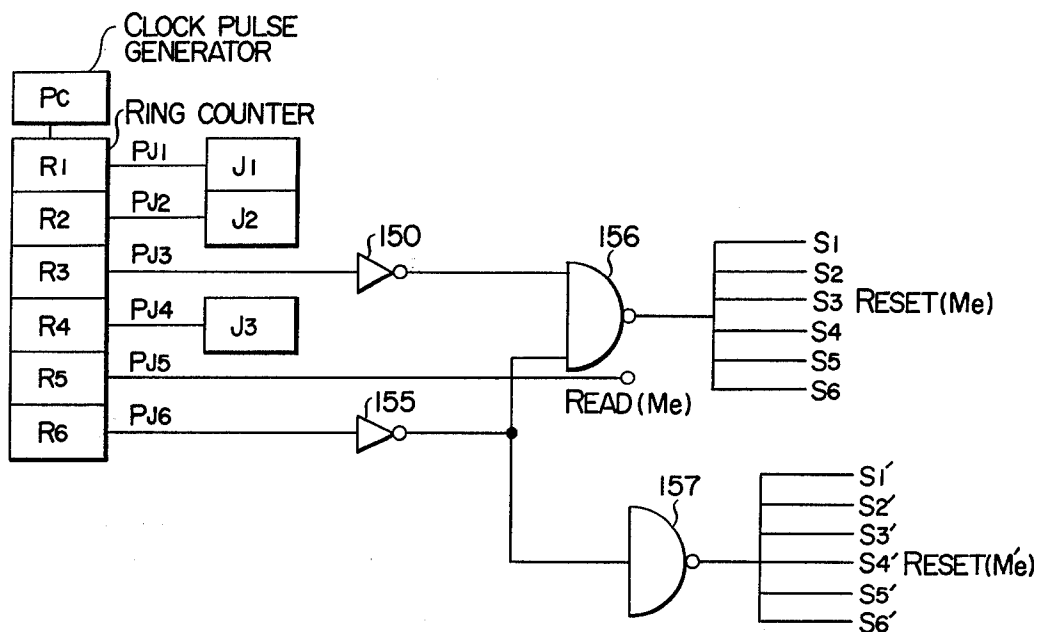


FIG. 12

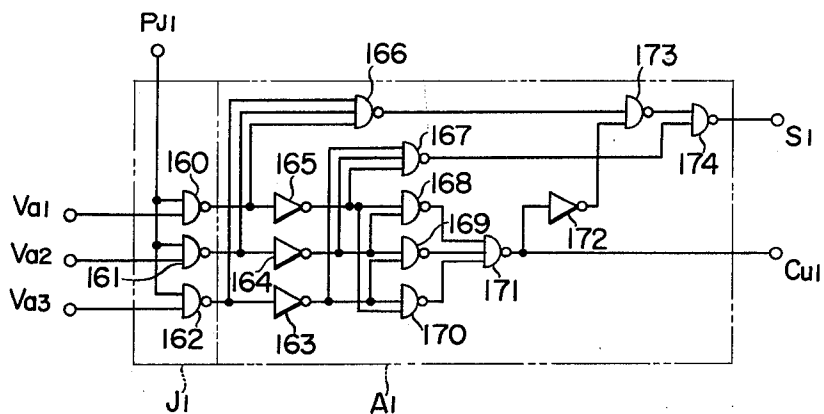


FIG. 13

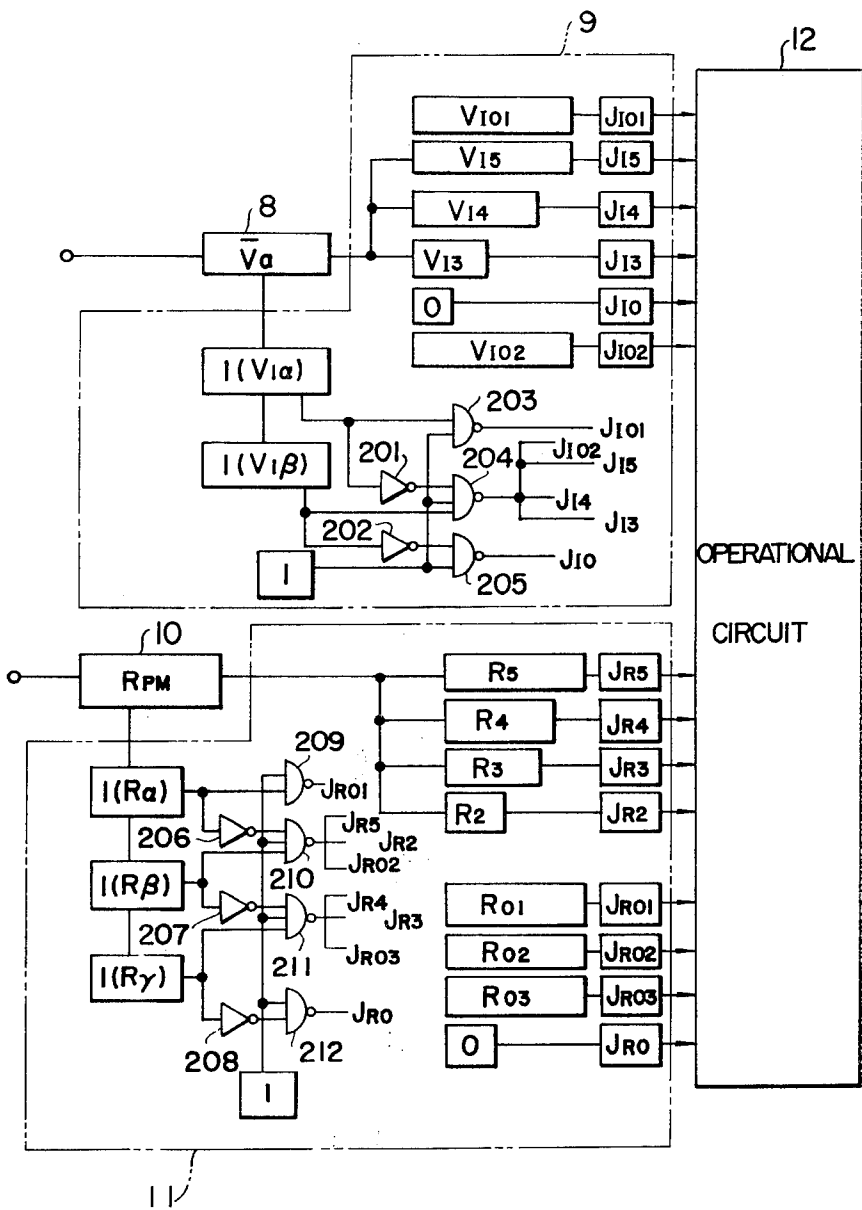


FIG. 14

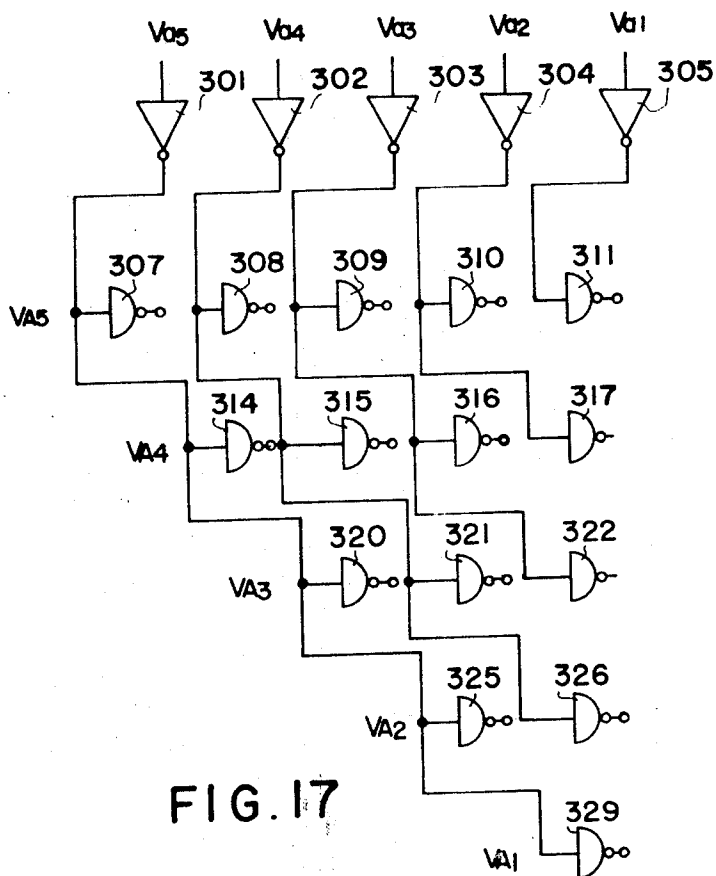


FIG. 17

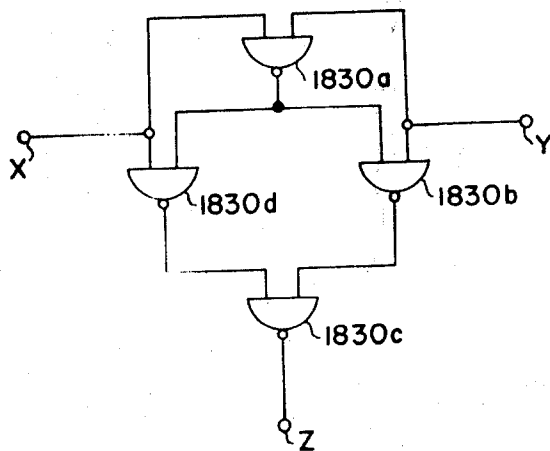


FIG. 15

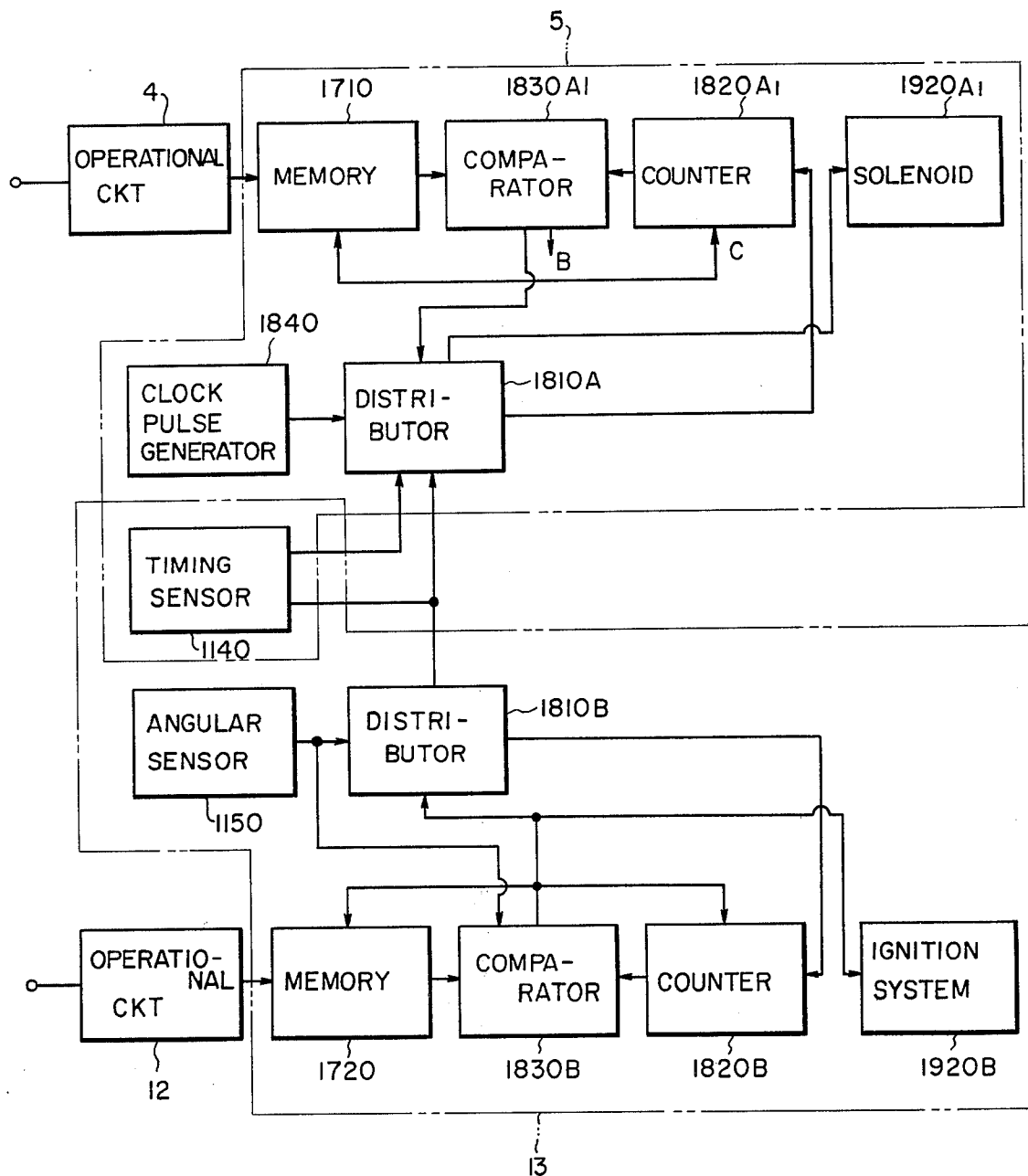


FIG. 16

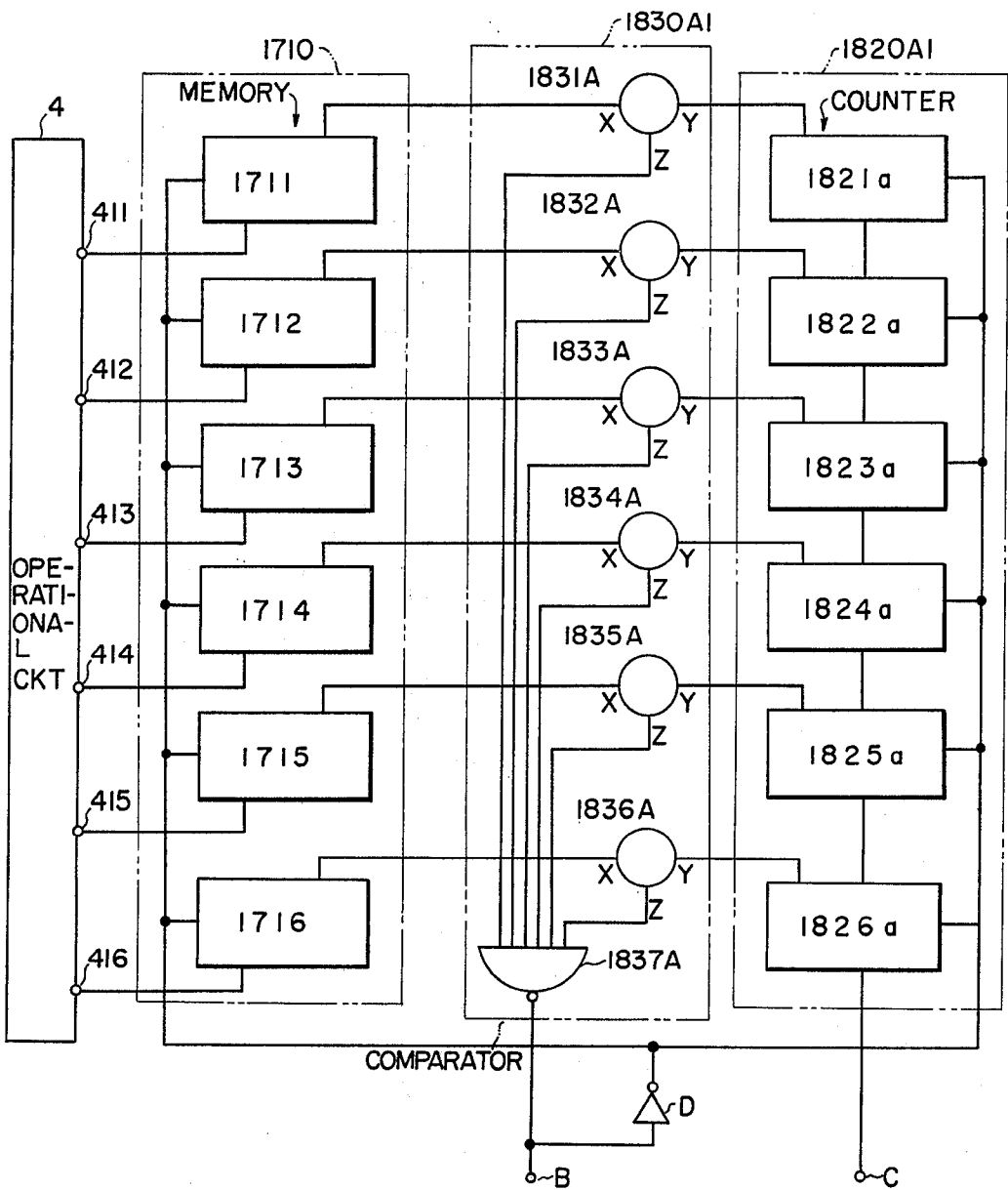


FIG. 18

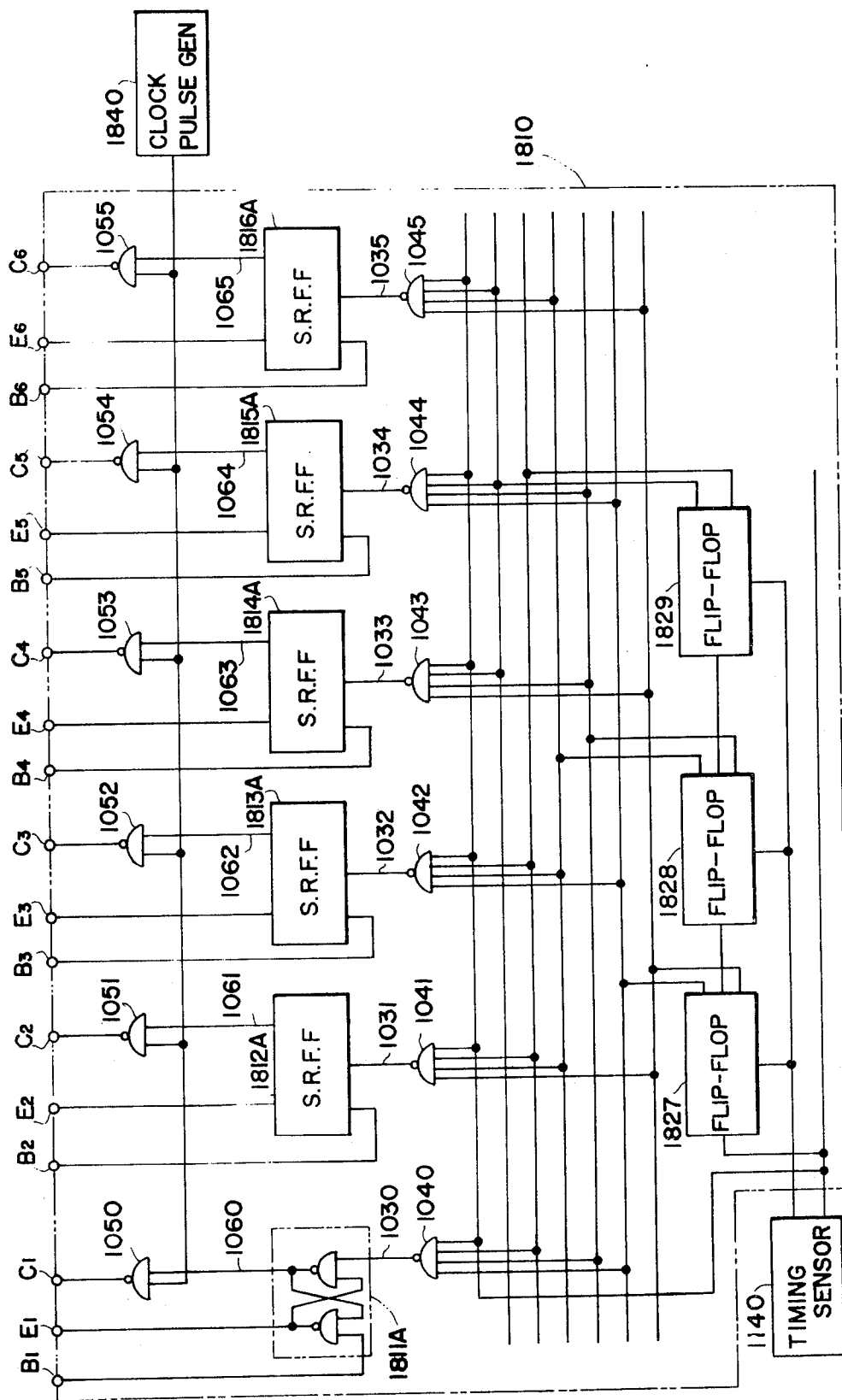


FIG. 19

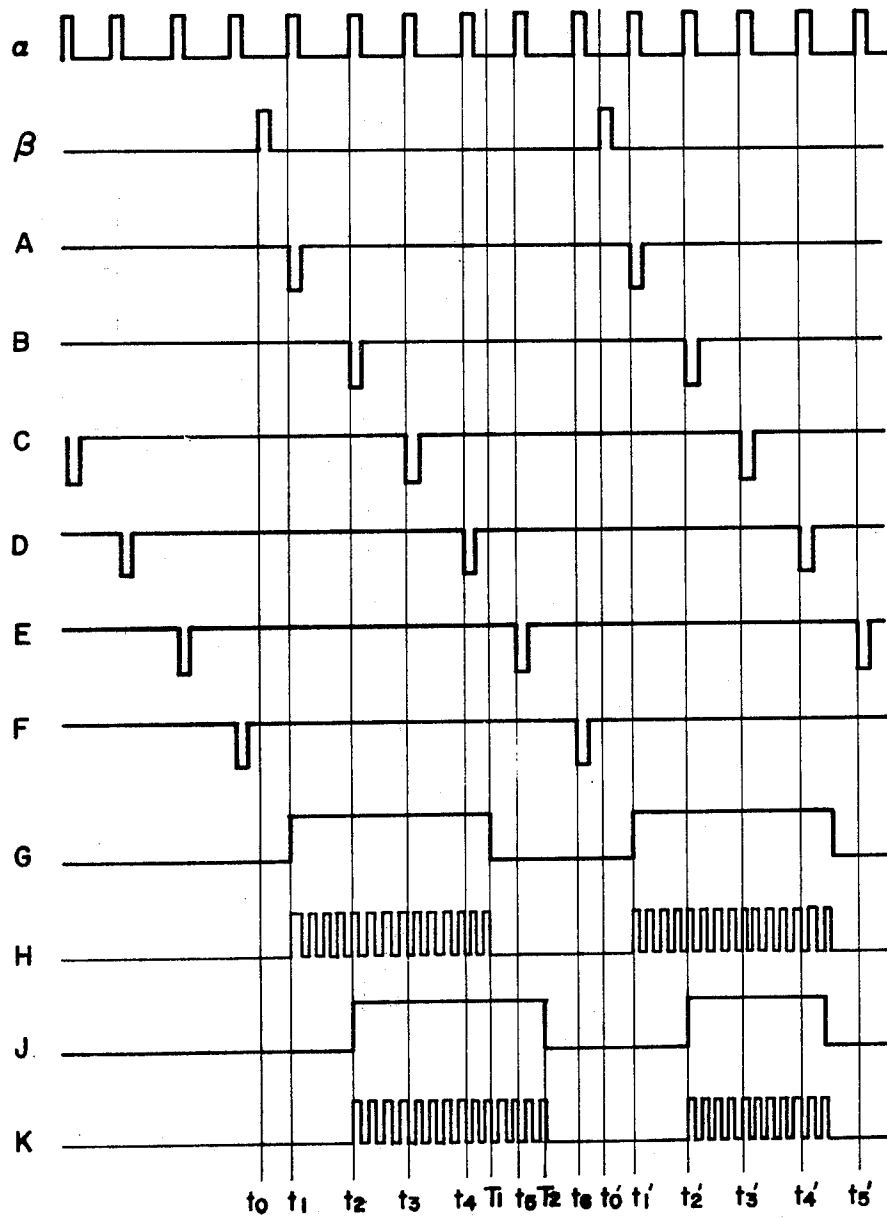


FIG. 20

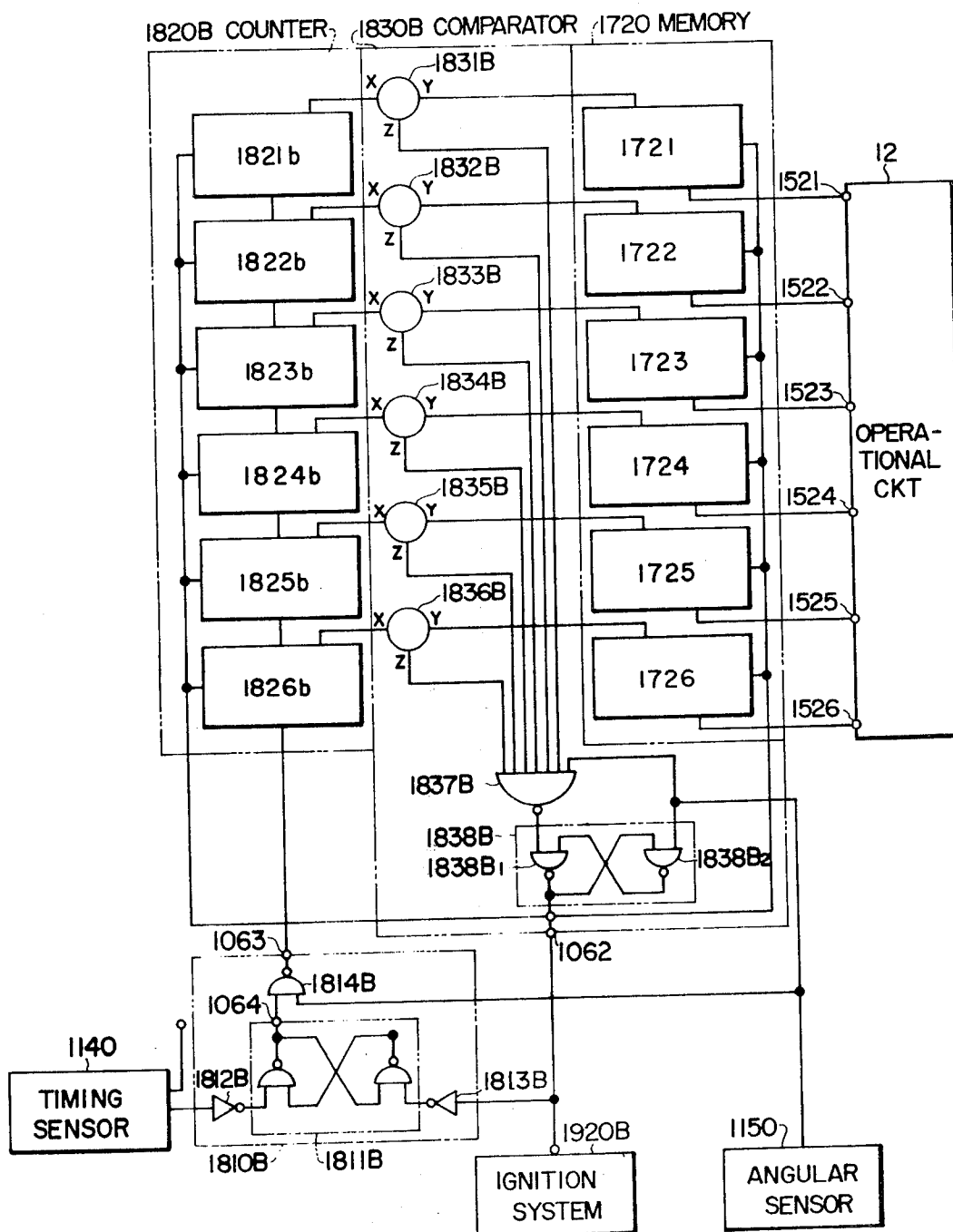


FIG. 21

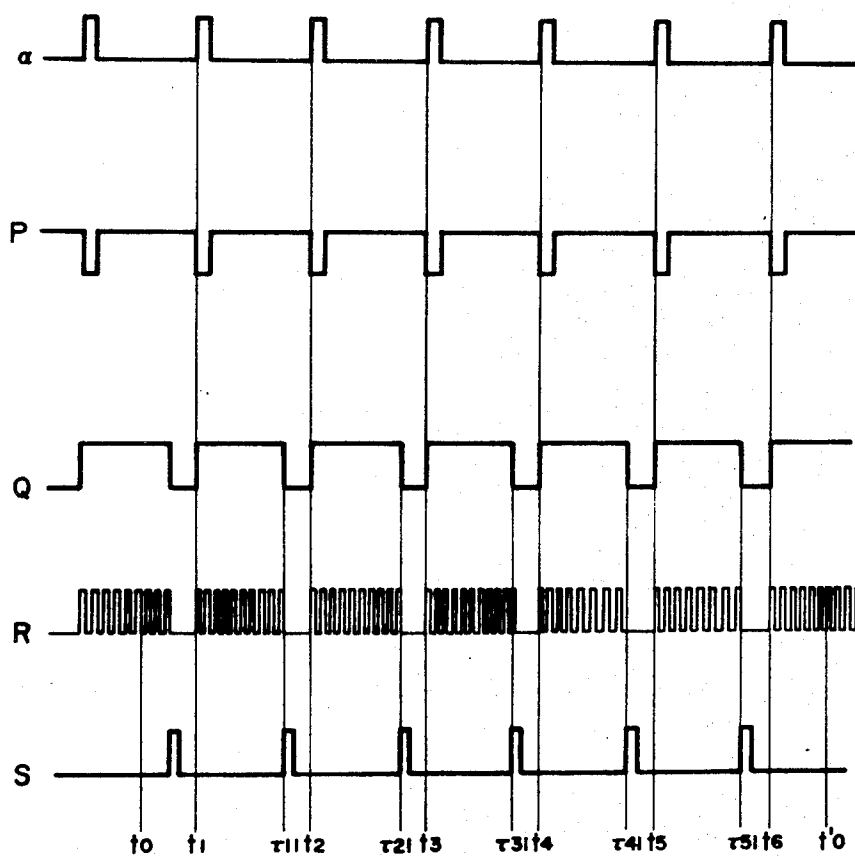


FIG. 22

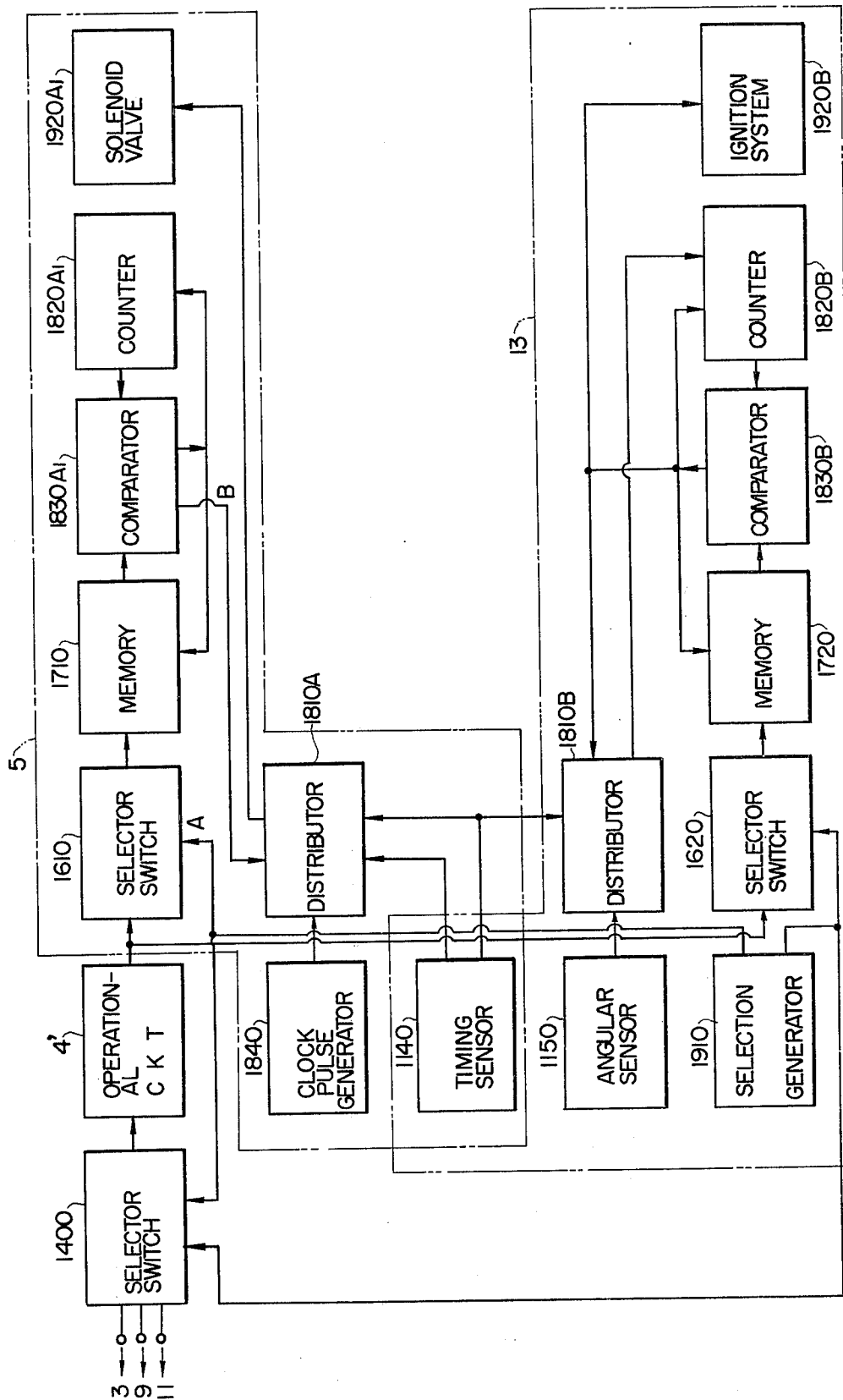


FIG. 23

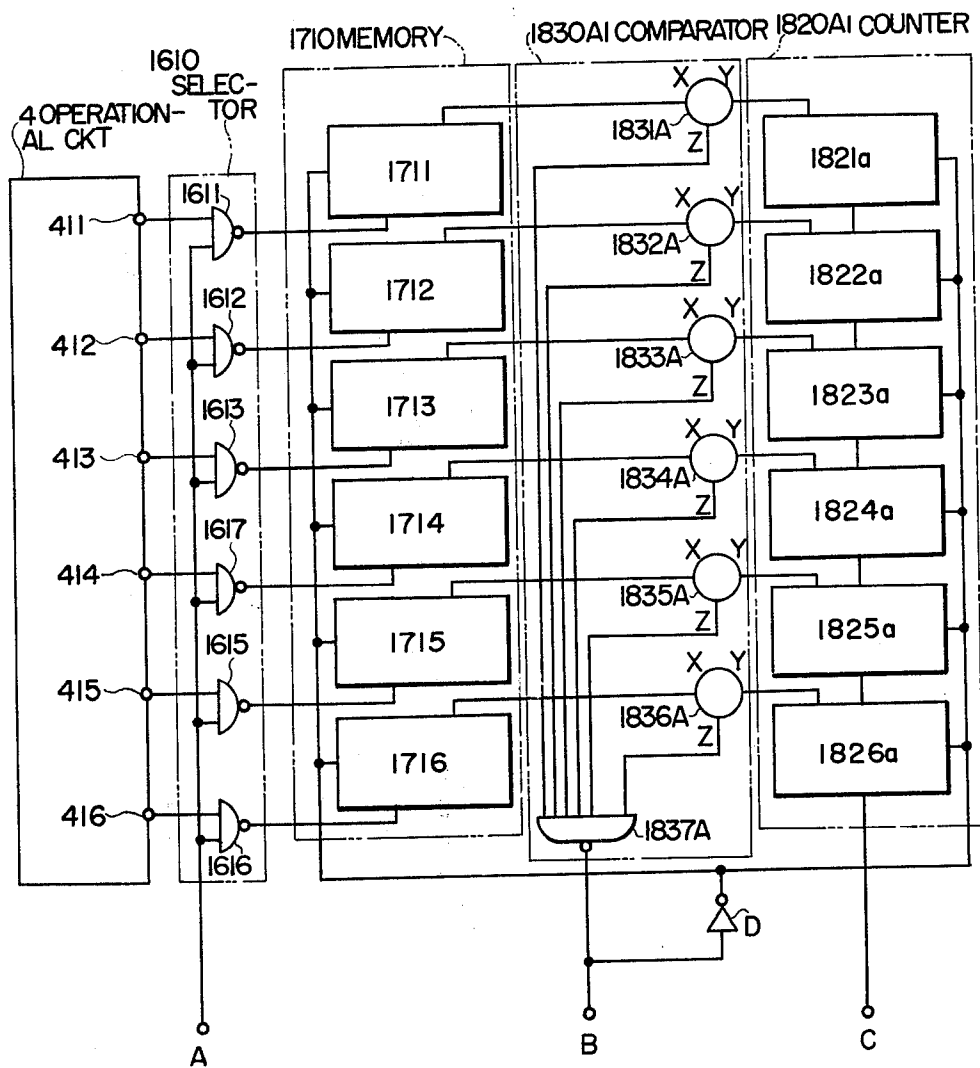


FIG. 24

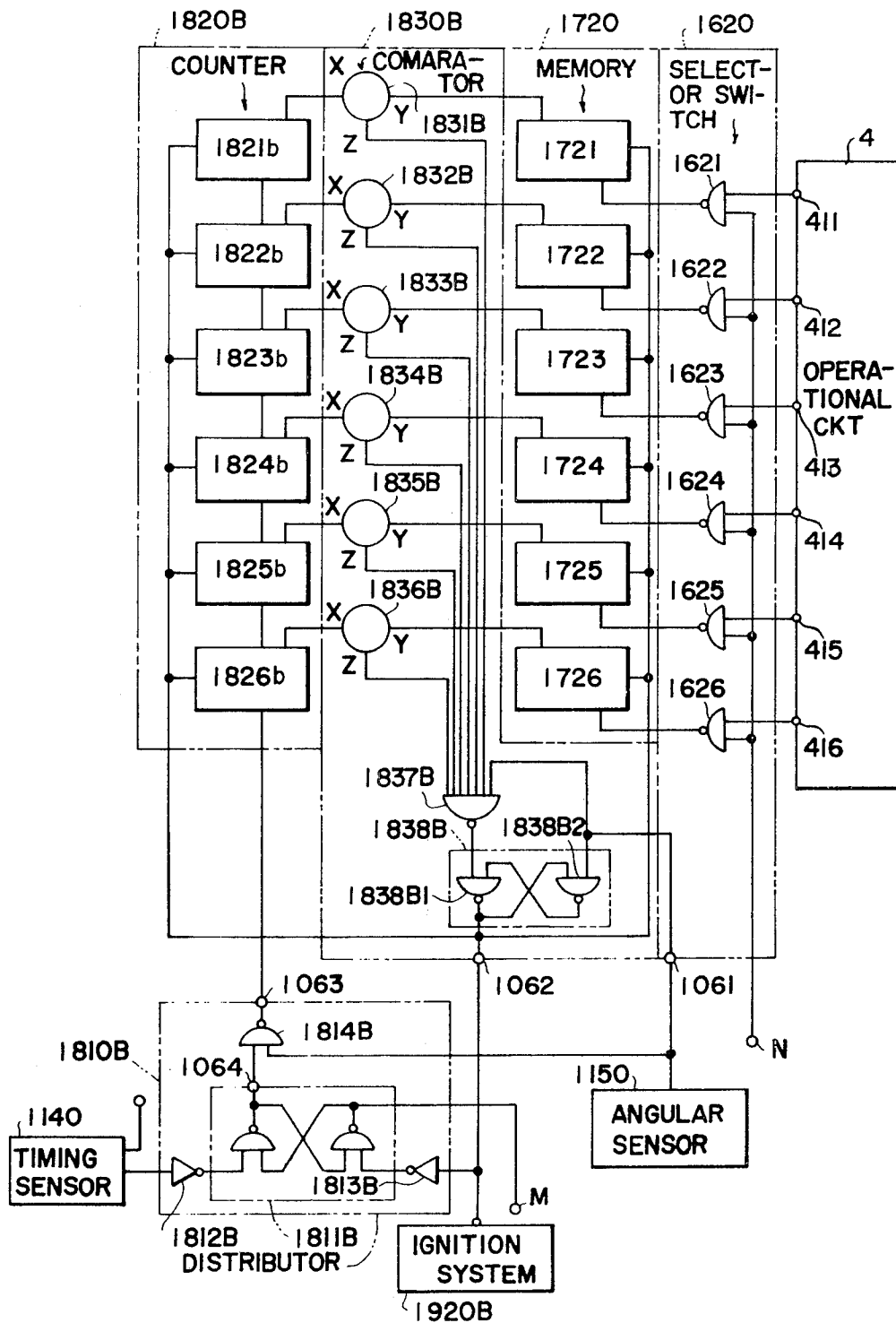


FIG. 26

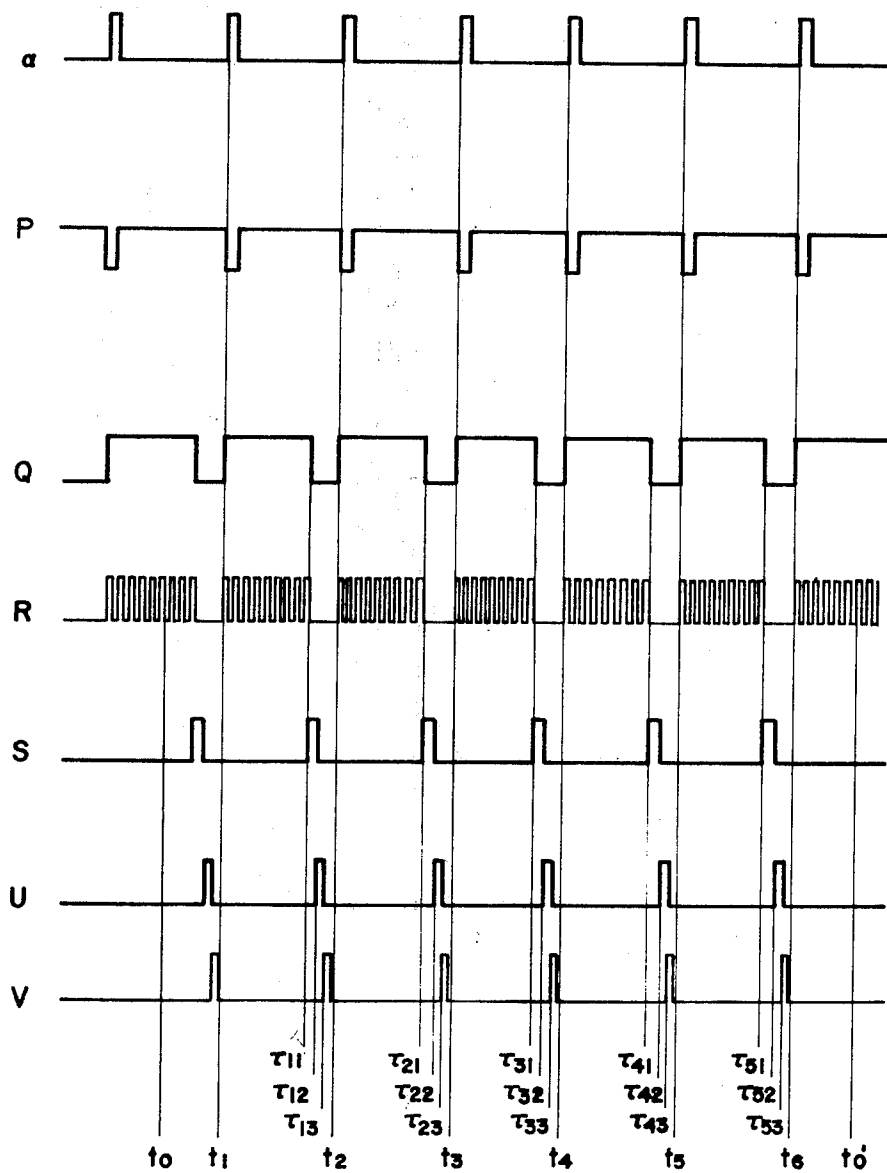


FIG. 27

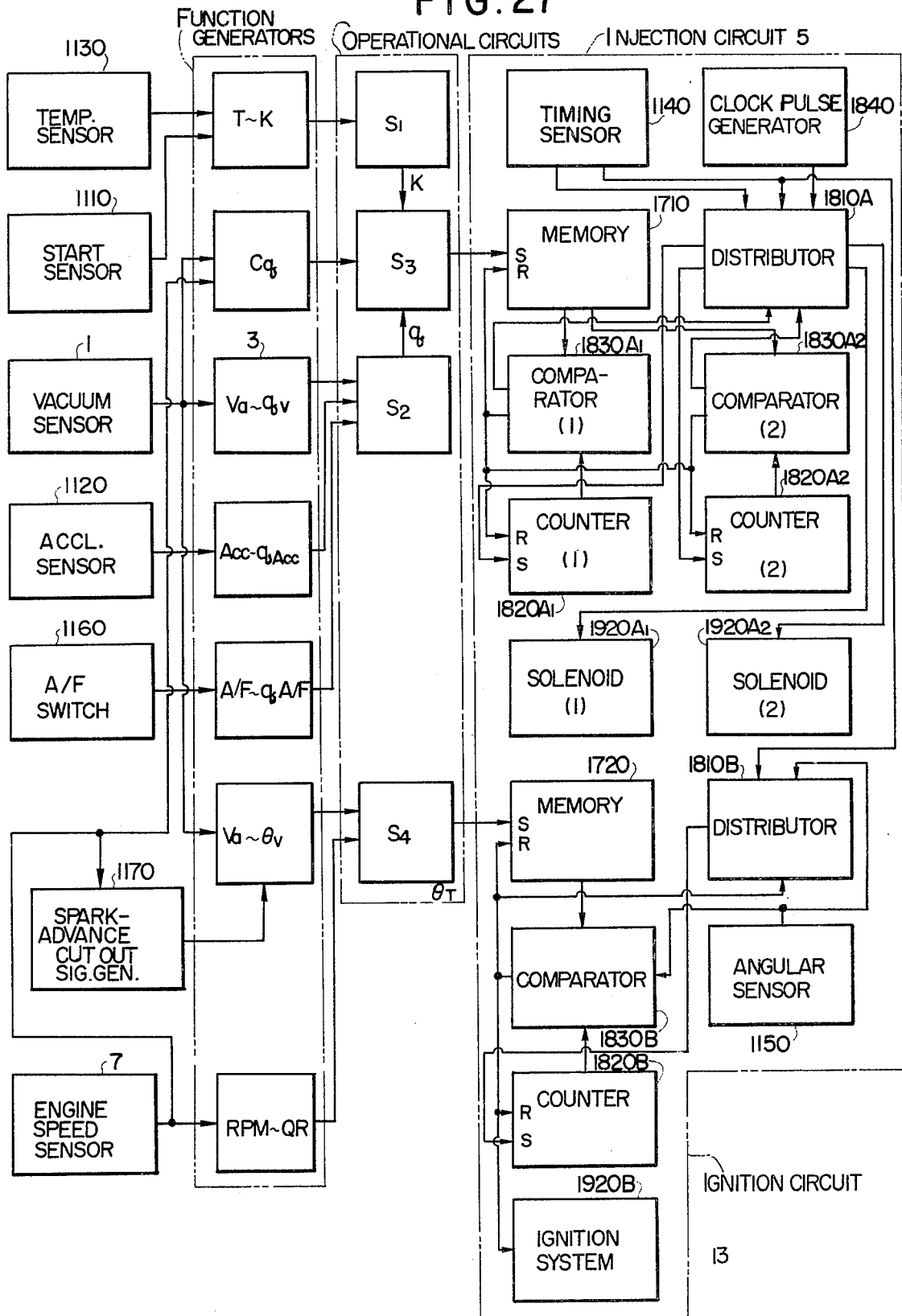


FIG. 28

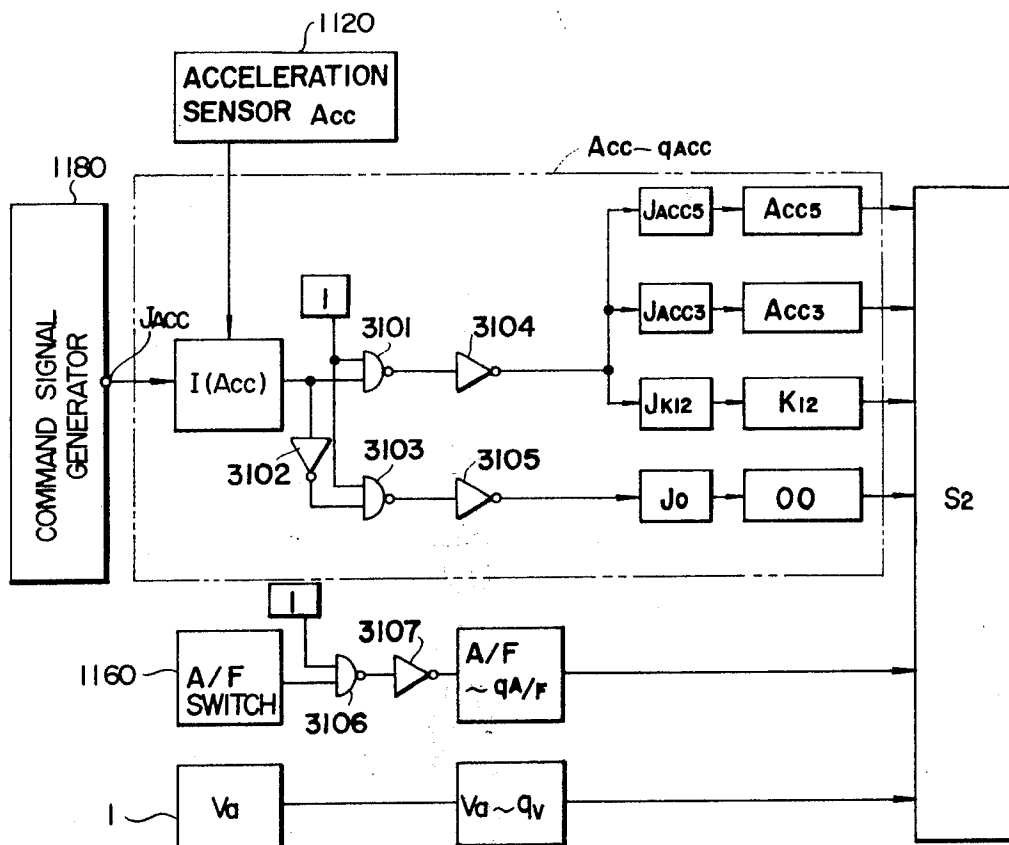


FIG. 29

FIG. 30

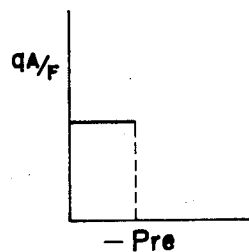
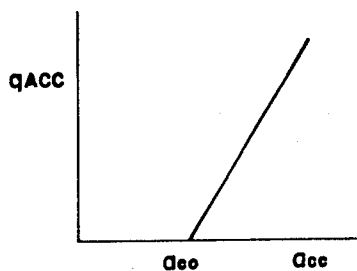


FIG. 31

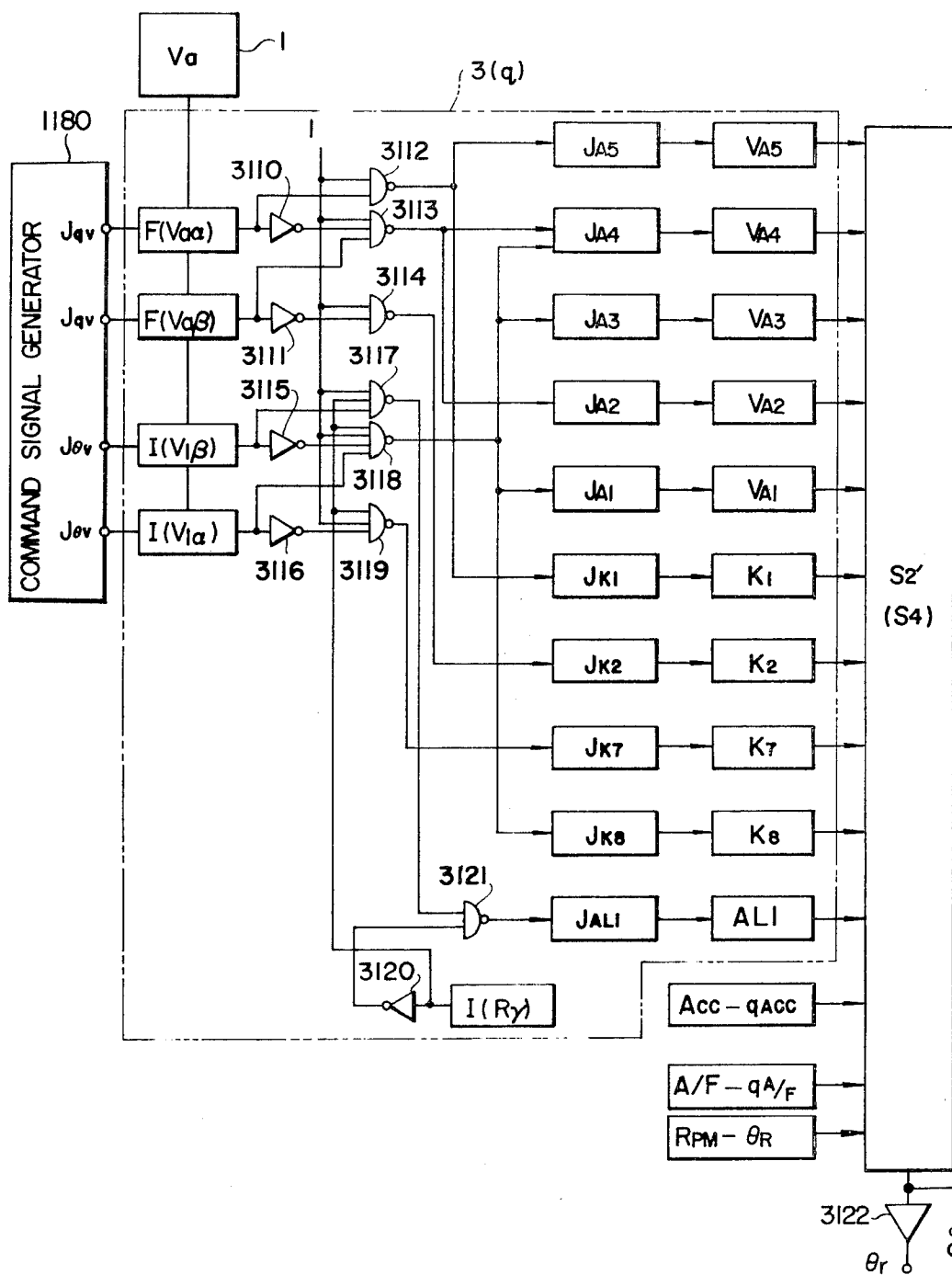


FIG. 33

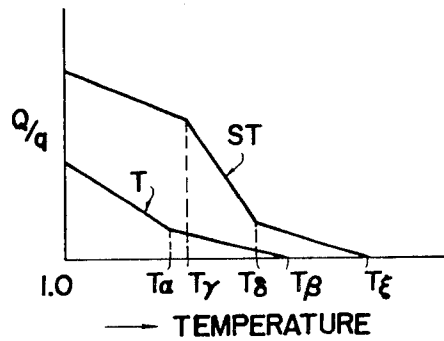
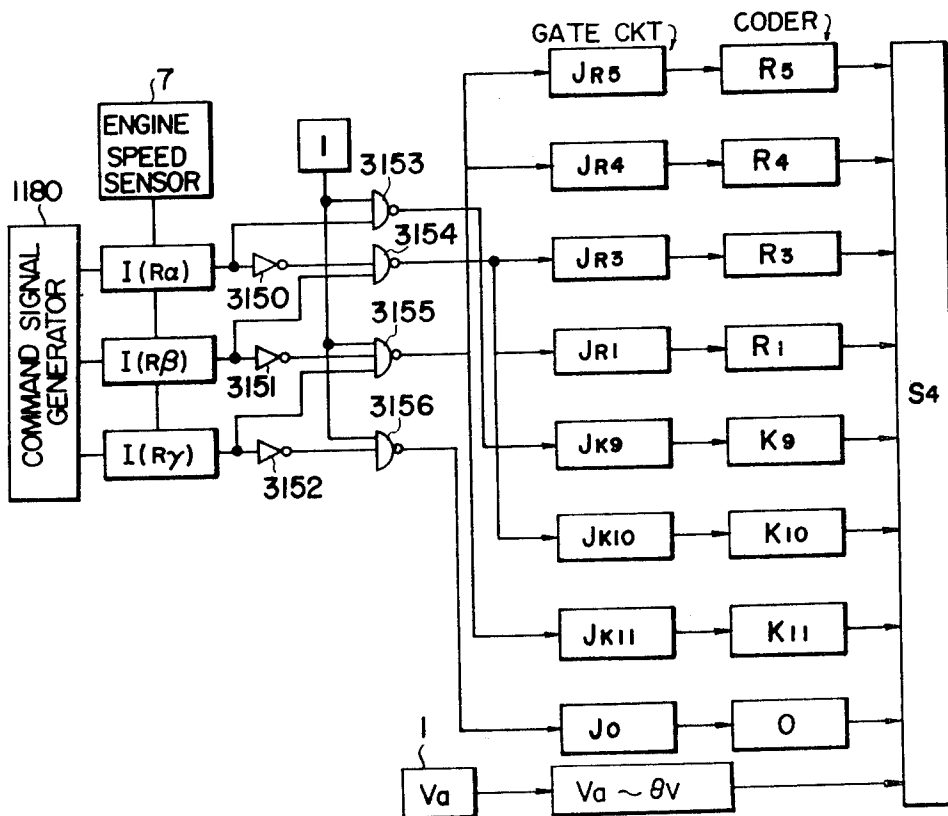


FIG. 34



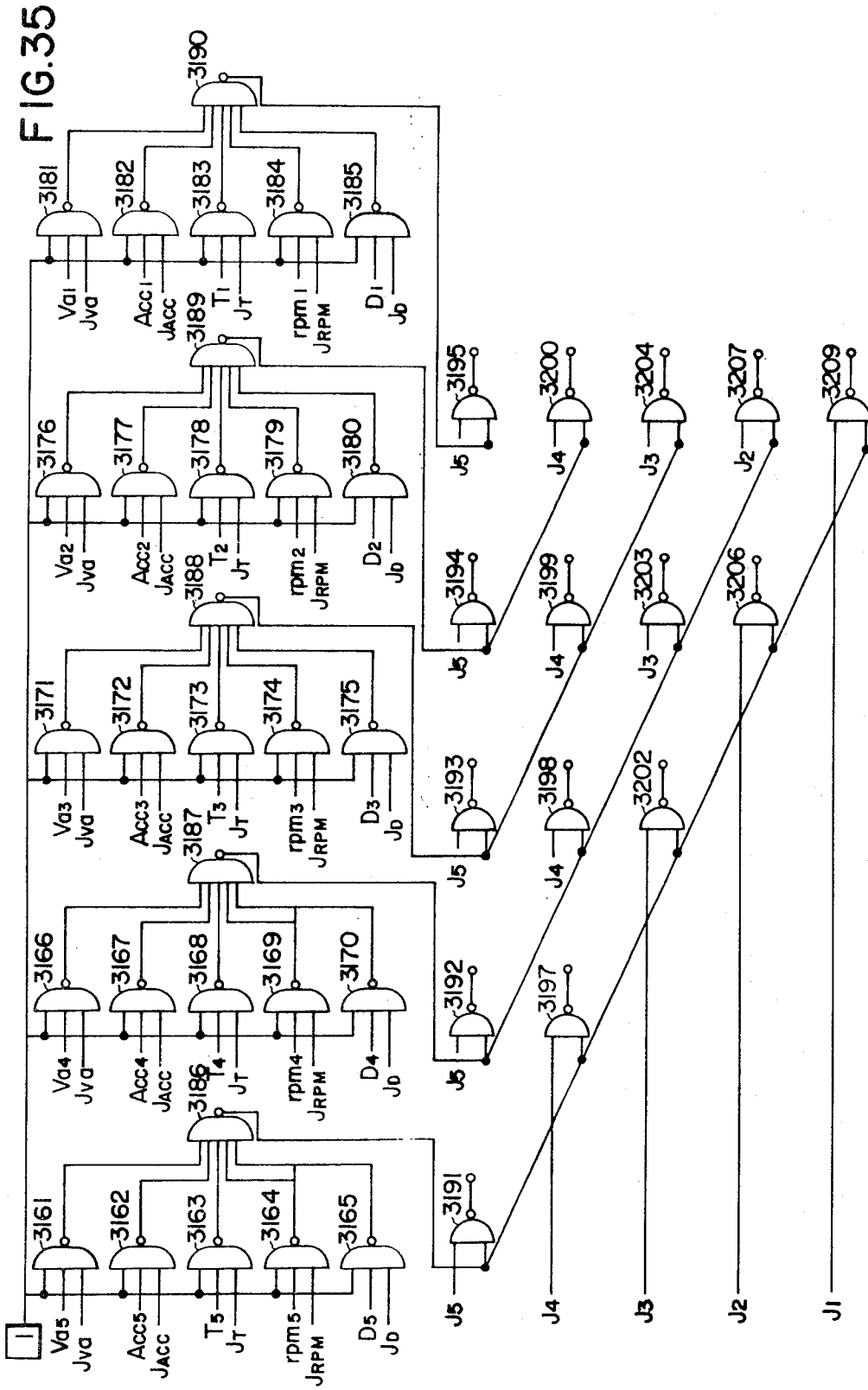


FIG. 36

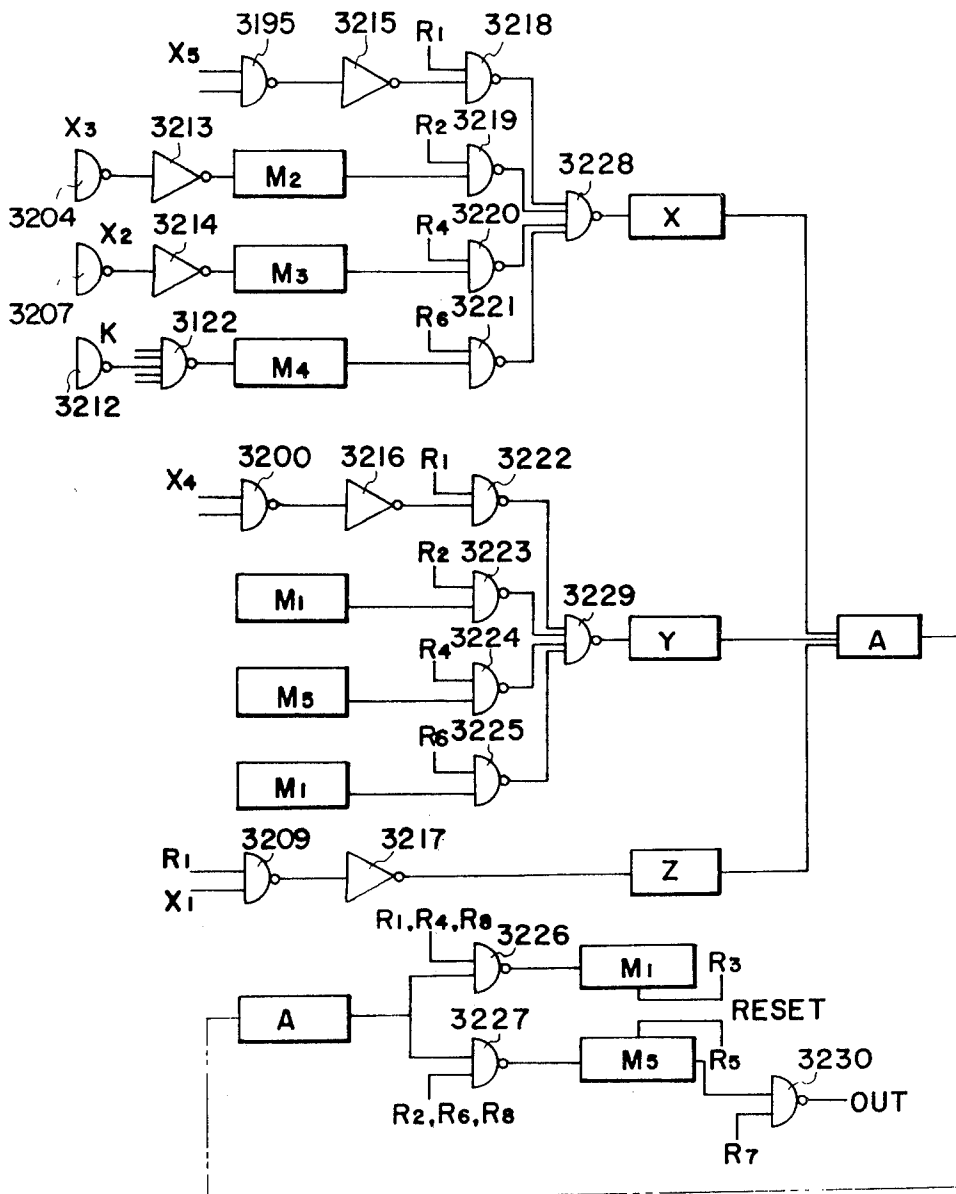


FIG. 37

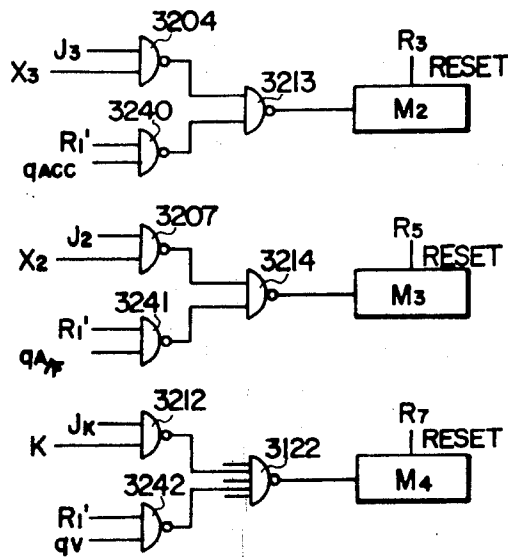


FIG. 38

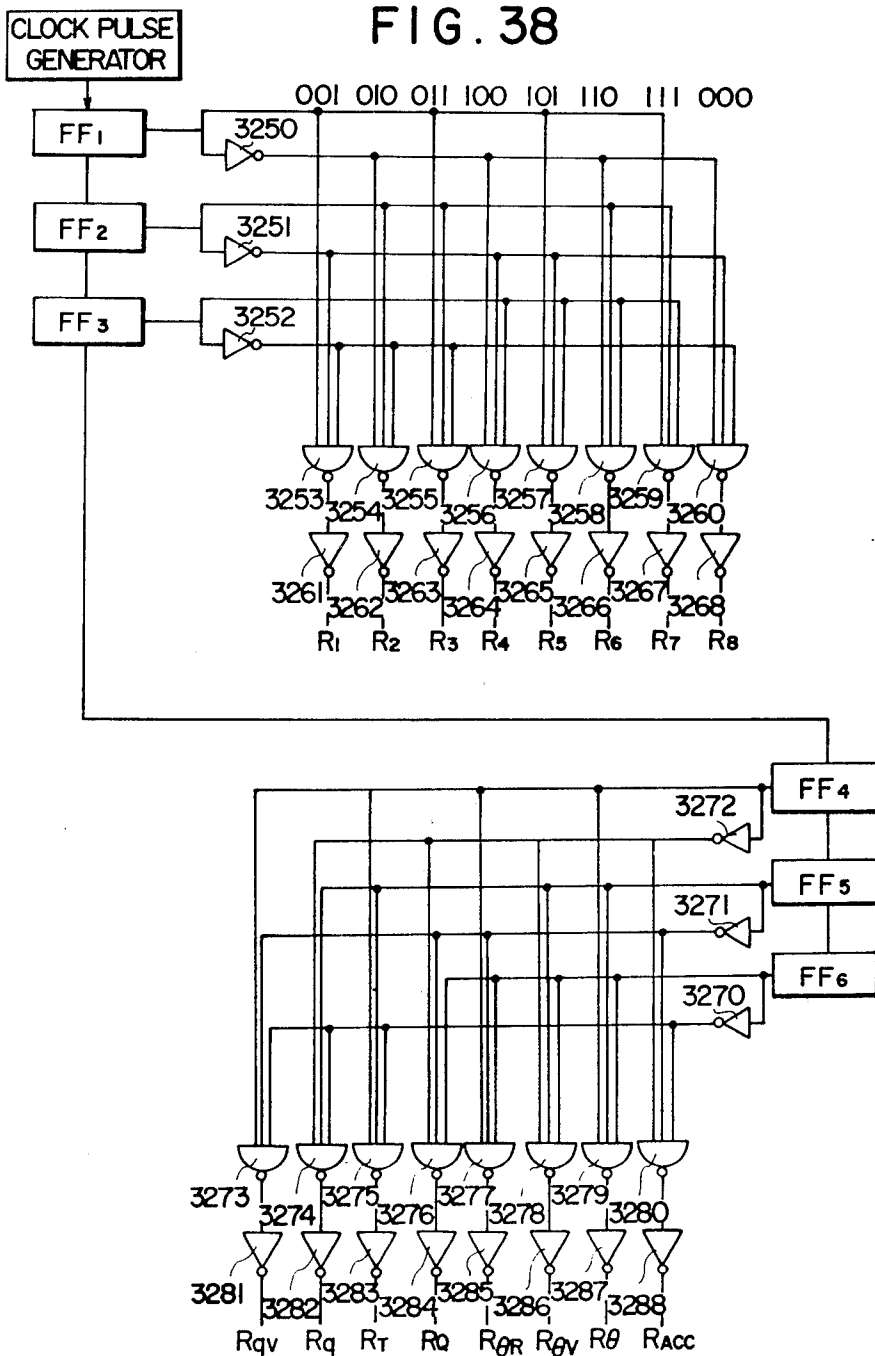


FIG. 39

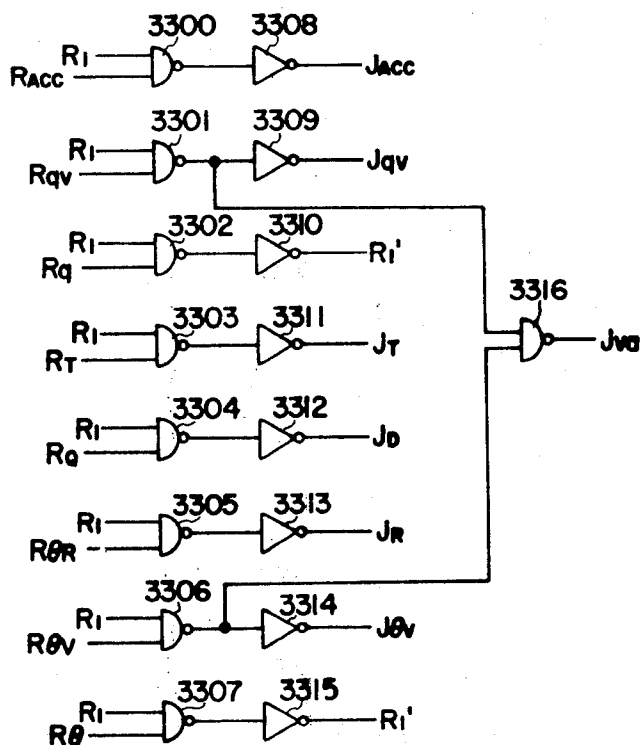


FIG. 40

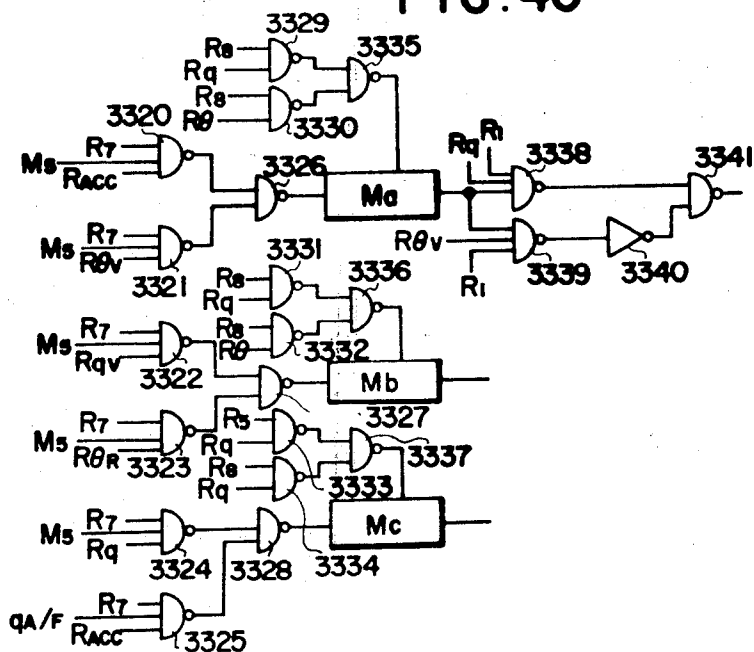


FIG. 41

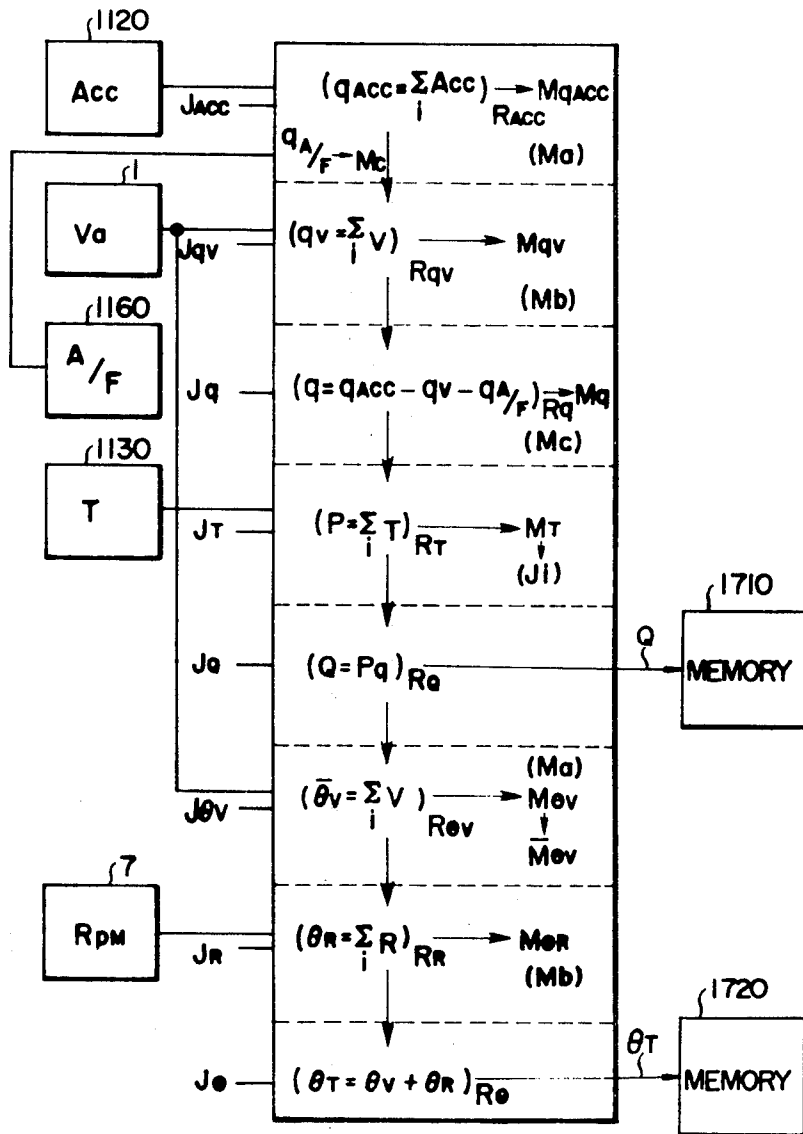


FIG. 42

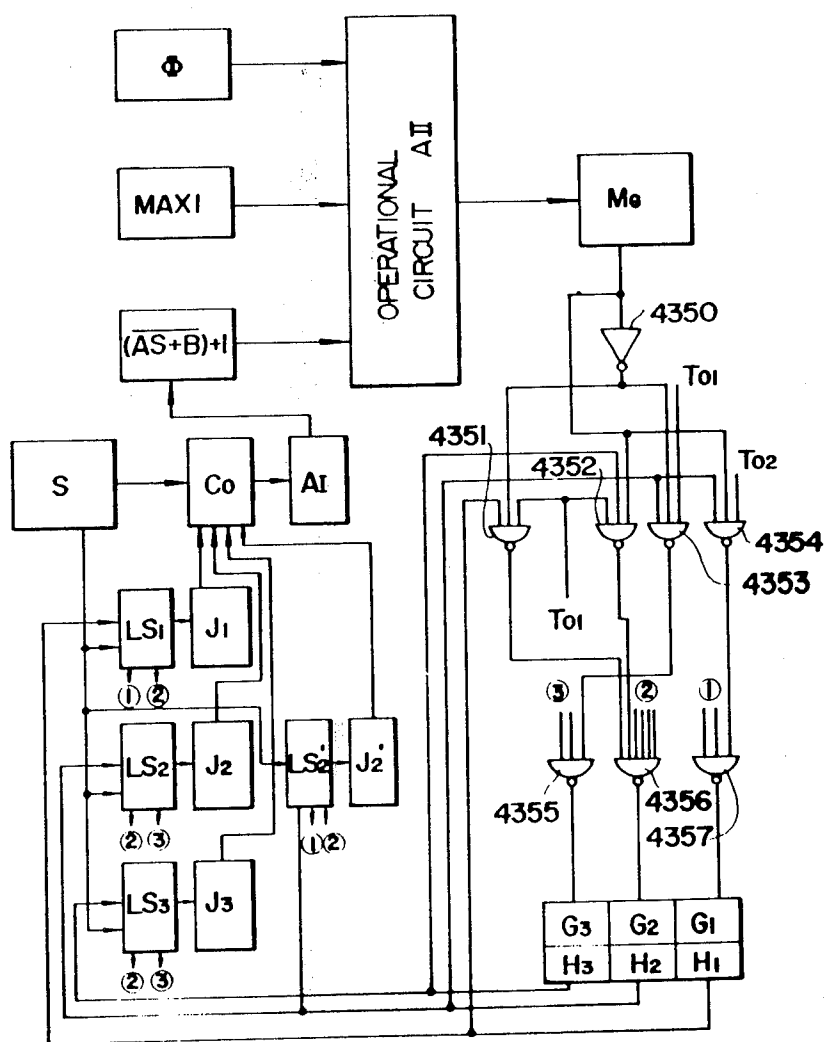


FIG. 25

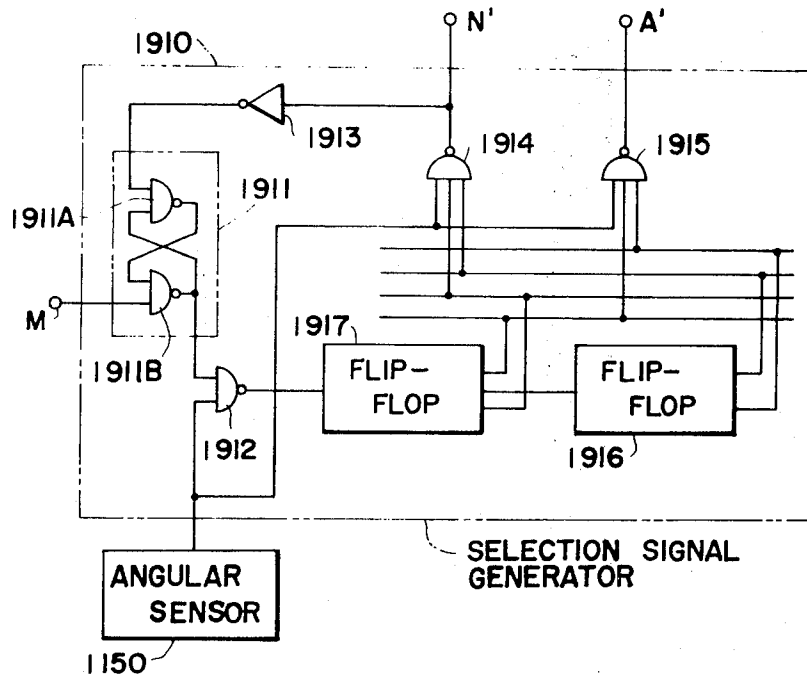


FIG. 43

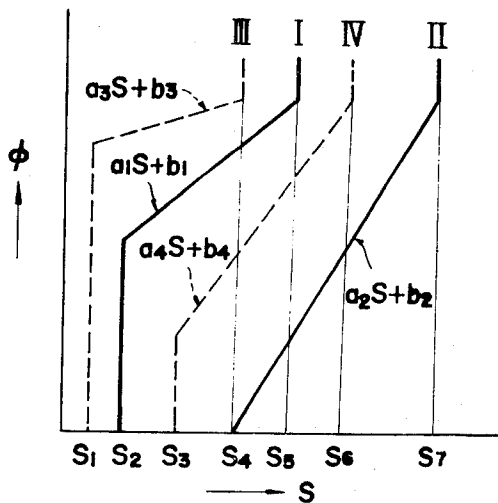


FIG. 44

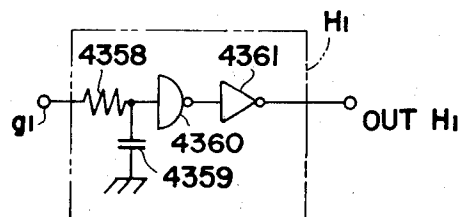
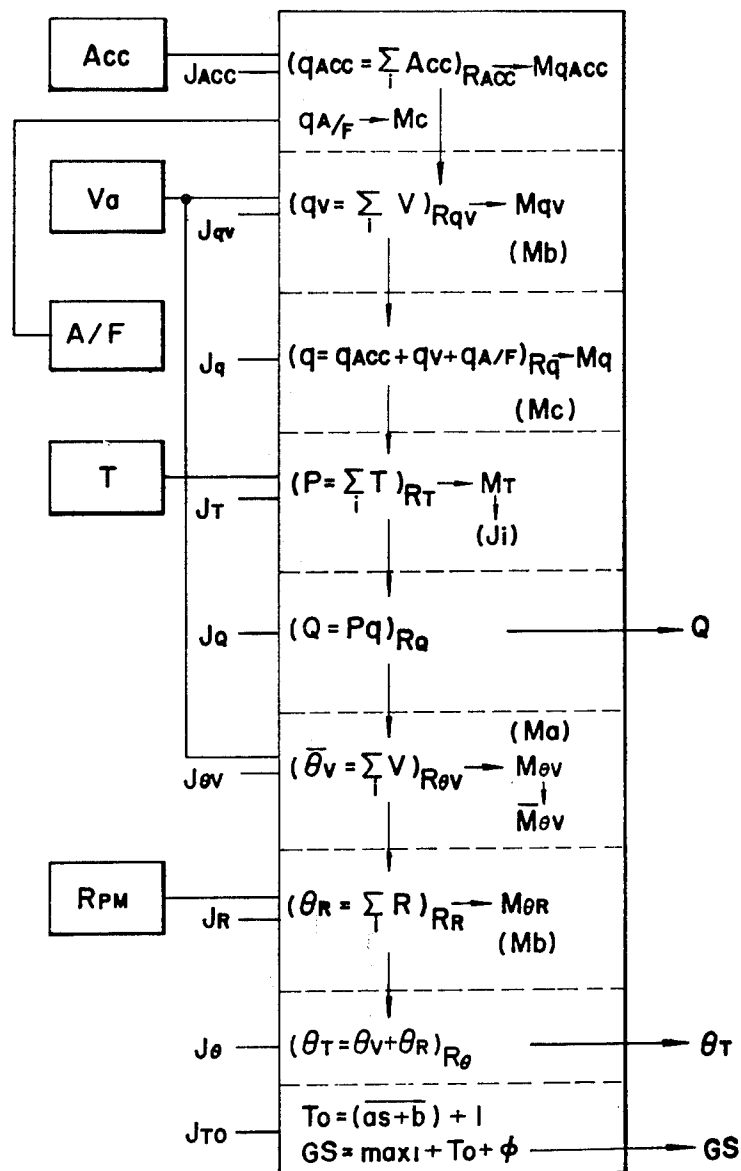


FIG. 45



ELECTRICAL FUEL CONTROL SYSTEM FOR INTERNAL COMBUSTION ENGINES

CROSS-REFERENCES TO RELATED APPLICATIONS

This is a continuation-in-part application of Patent application Ser. No. 327,603 filed Jan. 26, 1973 (now U.S. Pat. No. 3,816,717 issued June 11, 1974) which is a continuation application under Rule 60 of Patent application Ser. No. 126,830 filed Mar. 22, 1971 and now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electrical fuel control system for internal combustion engines and more particularly to a fuel control system wherein various data representing the operating conditions of an internal combustion engine are processed in a digital form to control the fuel supply to the engine.

2. Description of the Prior Art

In the conventional electrical fuel control systems for internal combustion engines, when determining the amount of fuel injection, the degree of spark advance and so on for controlling the combustion, the parameters such as the intake manifold vacuum, speed, temperature and the angle of rotation of the engine were detected by means of a vacuum sensor and the like, and the analog signals corresponding to the detected parameters were processed in their analog form to determine the amount of fuel injection, the degree of spark advance and so on.

However, with these conventional systems employing analog quantities to represent such parameters, the circuit required for determining the quantity of fuel to be injected, the correct spark timing etc., could not be uniform or standardized and a large number of linear amplifiers were necessary. Thus, these conventional systems have a drawback in that if it is desired to incorporate integrated circuits, such systems are extremely disadvantageous for this purpose, since strong consideration must be given to the generation of heat in the circuits and the rating of various resistors and transistors used must be precisely determined. There is another drawback in that since the methods of computation used are entirely of an analog nature, not only the amount of fuel injection and the spark timing may be easily caused to change by the variation of the power supply voltage and the variation of the ambient temperature, but also a malfunction may be caused by any disturbing noise. There is a further drawback in that since the conventional systems require a large number of linear amplifiers as previously described and moreover these linear amplifiers are of different characteristics, not only the systems tend to be complicated in construction, but they also tend to be costly.

SUMMARY OF THE INVENTION

The principal object of the present invention is therefore to provide a novel fuel control system for internal combustion engines, wherein in order to solve the previously mentioned deficiencies of the prior art, operations such as addition, multiplication and division are performed with digital techniques on those input signals which correspond to the various parameters of an engine to determine the quantity of fuel to be injected

and the spark timing, whereby the standardization of the construction of the digital operational circuits is achieved to provide a fuel control system which is not only simple and economical in construction, but also well adapted for incorporating integrated circuits and at the same time unsusceptible to any malfunctions due to the variations in the power supply voltage and ambient temperature as well as disturbing noises.

Another object of the present invention is the elimination of those deficiencies which may occur if the digital quantities are processed step-wise in the abovementioned digital computations. That is, it is the elimination of the drawback in that a complicated wiring circuit must be provided with respect to all the combinations involved in the characteristics of an engine, and that such complicated wiring must be repeated for all the different kinds of engines, particularly when the required characteristics of engines installed in automobiles differ depending on the purposes, capacities, etc. of the engines.

According to the present invention, therefore, the above-mentioned object is achieved by means of a computing method in which the amount of fuel injection and the spark timing are determined by subjecting all the information obtained from various sensors to digital computations including multiplication, division and addition, so that particularly any variation in the required engine characteristic can be met with a simple change of the design, while on the other hand the information from every sensor is utilized as far as possible for various characteristic correcting purposes and moreover, the construction of those converters for calculating the volume of injection and the spark timing is standardized so that the similar procedures may be followed both in the process of computing the volume of injection and in the process of determining the spark timing, while the converters which could be substituted by a single common converter are combined into such a single converter in view of the fact that the abovementioned computations could be satisfactorily performed at different times, thereby achieving a reduction in the number of circuit component parts and hence an improved reliability and a reduction in cost.

The fuel control system according to the present invention comprises sensors for detecting the parameters of an internal combustion engine and converting these parameters into analogical electric signals, analog to digital converters for converting the output signals of the sensors into digital signals, function generators for performing computations on the digital signals from the analog to digital converters to produce fuel control signals that suit the characteristics of the engine, and means for receiving the fuel control signals to control and fuel supply to the engine.

Those effects which are attributable to the present invention may be set forth as follows:

1. Since all the data handled in the operational circuits are coded as binary codes, computations can be performed in a stabilized manner against variations of the power supply voltage and other external conditions such as the ambient temperature. In other words, computations in these circuits can be performed with absolute accuracy provided that there is no disturbance large enough to interfere with the "on" and "off" signals in the circuits. As a counter measure against such disturbance, a well-known integrated circuit fuel supply may be employed to design a computing circuit

which operates with a considerable degree of accuracy.

2. Since the function generators for establishing the characteristics of an internal combustion engine generally include similar circuits, a large number of the same elements may be employed to construct these function generators and this permits a reduction of cost by mass production and a standardization of the fabricating operations.

3. When it is necessary to modify the design characteristics for different uses and types of engines, the characteristics may be modified by varying the patterns of addition.

4. Any characteristics of the fuel injection quantity and the spark advance can be attained, no matter what forms, the characteristic curves may take. Particularly, with those latest engines which require characteristics of complicated forms, the present invention is especially useful. Moreover, discontinuous characteristics can even be attained.

5. The accuracy of characteristics can be improved without making any specific provision in the operational circuits, simply by increasing the number of digits contained in any code. Thus, as far as the accuracy of characteristics is concerned, all energies can be devoted to the manufacture of the system of the present invention, solely bearing in mind the accuracy of the sensors incorporated. This means that the system of the present invention is especially useful when used with engines, particularly automobile engines which are run under considerably varying operating conditions.

6. Since the sensors incorporated are common to the fuel injection system and the spark advance system, the system of the present invention is very advantageous from the aspect of cost, and at the same time it can be made smaller and compact and simpler in construction.

7. Since all the computations can be performed on a time-sharing basis, only a single set of operational circuits function generators can be effectively utilized is required. This permits a reduction in the number of component parts with a resultant decrease in cost and the failure ratio. This reduced failure ratio lends itself to prevent an engine from stopping its rotation.

8. The inputs to the operational circuits which relate to the operating conditions of an engine, such as, the engine speed, temperature and intake manifold vacuum would change very slowly as compared with the computing speed in the operational circuits, and therefore the required computations can be performed satisfactorily according to the time-sharing system mentioned above. With this time-sharing system, the construction of the system of the invention can be made simpler.

9. Since all the information relating to the operating conditions of an engine are handled in coded form and since, with the use of a simple adapter, it is possible to externally observe the outputs of various sensors relating to the engine parameter, the fuel quantity being delivered to the engine, the degree of engine spark advance as well as the values of correction and characteristics under computation and the digital indication of these data in their numerical values are also possible, and the effectiveness of the present invention regarding engine inspection and the checking of engines under repair and during manufacturing processes is immense.

10. Since the amount of fuel injection it controlled by digitally correcting an input code corresponding to the engine temperature, it is possible to increase the accu-

racy of the correction even more by reducing the amount of fuel represented by the minimum digit of the input code and correcting the input code by an integer multiple of the minimum digit.

11. While the result obtained from a multiplication may contain a very large number of digits if the multiplication is carried out exactly, the value represented by some least significant digits of the result is very small as compared with that represented by the most significant digit of the result, and thus the least significant part of the result is practically negligible. This permits the shifting to the right of such a computational value so as to ignore any unwanted least significant digits and in this way no long series of unwanted least significant digits will be contained in the number. Moreover, the accuracy of computations can hardly be affected by this shifting. The correction of the input code is performed by producing a plurality of binary codes obtainable by successively shifting the input code to the right one place each shift and ignoring the minimum significant digit of each shifted binary code. Thus, the corrected input code remains as having the same number of places as that of the original binary code and represents approximately a multiple of the number represented by the original binary code without undesirably reducing accuracy of the correction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1 through 14 relate to a first embodiment of the present invention, in which:

FIG. 1 is a block diagram showing schematically the general construction of the first embodiment.

FIG. 2 is a diagram showing the output voltage characteristic of an engine intake manifold vacuum sensor.

FIG. 3 is a diagram showing the required fuel injection quantity characteristic of an engine.

FIG. 4 is a diagram showing the required vacuum advance characteristic of an engine.

FIG. 5 is a diagram showing the required centrifugal advance characteristic of an engine.

FIG. 6 is a diagram showing the characteristic of the engine with the output of the intake manifold vacuum sensor being inverted.

FIG. 7 is a diagram showing the output voltage characteristic of an engine speed sensor.

FIG. 8 is a block diagram of a function generator for establishing the fuel injection quantity characteristic.

FIG. 9 is an electrical wiring diagram of a discriminator.

FIG. 10 is a block diagram of an operational circuit.

FIG. 11 is a block diagram of the pulse signal generating circuit.

FIG. 12 is an electrical wiring diagram showing a part of the adder and the connecting circuits.

FIG. 13 is a block diagram of a function generator for establishing the spark advance characteristic.

FIG. 14 is an electrical wiring diagram of a coder for determining the engine intake manifold vacuum.

FIG. 15 is a block diagram showing the fuel injection distribution circuit portion and the ignition distribution circuit portion.

FIG. 16 is a detailed block diagram of the fuel injection distribution circuit portion.

FIG. 17 is an electrical wiring diagram showing the constituent elements of a comparator.

FIG. 18 is an electrical wiring diagram of the distributor.

FIG. 19 is a waveform diagram showing the voltage waveforms which appear at various portions of the distributor shown in FIG. 18.

FIG. 20 is an electrical wiring diagram of the ignition circuit portion.

FIG. 21 is a waveform diagram showing the voltage waveforms which appear at the various portions of the ignition distribution circuit.

FIG. 22 is a block diagram showing the fuel injection distribution circuit portion and the ignition distribution circuit portion of the second embodiment.

FIG. 23 is a detailed block diagram of the fuel injection distribution circuit portion.

FIG. 24 is an electrical wiring diagram of the ignition circuit.

FIG. 25 is an electrical wiring diagram of a selection signal generator.

FIG. 26 is a waveform diagram showing the voltage waveforms which appear at various portions of the ignition distribution circuit and a selector circuit, respectively.

FIG. 27 is a block diagram showing schematically the general construction of the third embodiment.

FIG. 28 is a block diagram showing the arrangement for determining the increased fuel quantity for acceleration and the air-fuel ratio setting in accordance with the signal input corresponding to the engine throttle valve opening speed and the engine throttle valve position, respectively.

FIG. 29 is a characteristic diagram showing the additional fuel quantity required for the engine for acceleration.

FIG. 30 is a characteristic diagram showing the increased fuel quantity for the air-fuel ratio setting required for the engine.

FIG. 31 is a block diagram showing a function generator arrangement for determining the amount of fuel injection and the degree of vacuum advance according to the engine intake manifold vacuum.

FIG. 32 is a block diagram showing a function generator arrangement for determining the additional fuel quantity needed for the starting and warming-up operations of the engine, respectively.

FIG. 33 is a characteristic diagram showing the additional fuel quantity requirements of the engine for starting and warming-up operation thereof.

FIG. 34 is a block diagram showing a function generator arrangement for determining the degree of centrifugal spark advance required for the engine.

FIG. 35 is a schematic diagram of a coder for the input codes from the engine.

FIG. 36 is a schematic diagram showing the connections between the codes and the adder.

FIG. 37 is a schematic diagram showing the operational circuit comprising the codes and memory circuits.

FIG. 38 is a schematic diagram of a part of an operation command signal generator.

FIG. 39 is a schematic diagram of another part of command signal generator.

FIG. 40 is a schematic diagram showing the interconnections between the operational circuits and the memory circuits.

FIG. 41 is a block diagram for explaining the sequence in which the amount of fuel injection and the spark advance required for the engine are to be determined.

FIG. 42 is a block diagram showing an arrangement for generating gear shifting commands for an automatic transmission.

FIG. 43 is a characteristic diagram showing the gear shifting requirement of the automatic transmission.

FIG. 44 is an electrical wiring diagram of a delay circuit.

FIG. 45 is a block diagram for explaining the sequence in which the amount of fuel injection and the degree of spark advance for the engine and the gear shifting of the automatic transmission are determined.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1:

In FIG. 1 illustrating a block diagram of the system according to a first embodiment of the present invention, numeral 1 designates a sensor (hereinafter referred to as a vacuum sensor) which is mounted on the engine to convert the engine intake manifold vacuum into a voltage. Numeral 2 designates an A - D converter for converting the output voltage of the vacuum sensor 1 into a binary code. Numeral 3 designates a function generator which receives the output of the A - D converter 2 to compute the amount of fuel injection in terms of binary codes; 4 an operational circuit for adding the computational results which represent fuel injection duration. Numeral 5 designates an injection circuit which injects a fuel into the engine in response to the output signal of the operational circuit 4. Numeral 6 designates an inverter which inverts the output of the vacuum sensor 1; 7 a sensor (hereinafter referred to as an engine speed sensor) which produces a voltage proportional to the engine rpm. Numeral 8 designates an analog to digital (A - D) converter for converting the output of the inverter 6 into a binary code, 9 a function generator for converting the output value of the A - D converter 8 into a spark advance. Numeral 10 designates an A - D converter which converts the output voltage of the engine speed sensor 7 which is proportional to the engine rpm into a binary code; 11 a function generator which converts the output value of the A - D converter 10 into a spark advance. Numeral 12 designates an operational circuit which forms the sum of the spark advance signal from the function generator 9 representing the vacuum advance and the spark advance signal from the function generator 11 representing the rotational spark advance; 13 an ignition circuit which ignites according to the total spark advance determined by the operational circuit 12.

The vacuum sensor 1 detects the vacuum developed in engine intake manifold as the engine rotates and it then converts the detected vacuum into an output voltage. The values of this output voltage will be as shown in FIG. 2, for example. In FIG. 2, the abscissa represents the intake manifold vacuum V_a whose value is +760 mHg, i.e., the atmospheric pressure at the origin of the coordinate and the pressure at that point on the horizontal axis which is designated as O, representing a vacuum. The ordinate represents the output voltage V_v of the vacuum sensor 1 whose value is 0 volt at the coordinate origin and it increases in potential as the ordinate lengthens upward. This voltage is converted into a binary code in the A - D converter 2 and the signal in this binary form is then applied to the function generator 3 which performs a computation to obtain the relationship between the intake manifold vacuum V_a

and the amount of fuel injection as shown in FIG. 3. In the characteristic shown in FIG. 3, the curve is broken at two points $V_{a\alpha}$ and $V_{a\beta}$ of the intake manifold vacuum V_a . A method by which this characteristic is obtained will be explained later. Then, the output signals produced by the computation in the function generator 3 are added and converted into a code corresponding to the fuel injection quantity q , whereupon a fuel whose amount of injection is determined according to this code is injected into the engine cylinders by means of the injection circuit 5.

On the other hand, the spark advance according to the engine intake manifold vacuum will vary as shown in FIG. 4. In this figure, the abscissa represents the intake manifold vacuum V_a and the ordinate represents the vacuum advance θ_{va} . This required engine spark advance characteristic has a tendency inversely corresponding to that of the required fuel injection quantity characteristic mentioned above. Thus, the inverter 6 is provided to reverse the output characteristic of the vacuum sensor 1, the inverter 6 produces an output as shown in FIG. 6. In FIG. 6, the abscissa represents the intake manifold vacuum V_a and the ordinate represents the output voltage $\bar{V}_{va}$ of the inverter 6. In this connection, the inversion of the output characteristic of the vacuum sensor 1 may be effected in an alternative manner in which the output signal of the vacuum sensor 1 is first converted into a binary code and then the complement of this binary code is formed. The output of the inverter 6 is converted by the A - D converter 8 into a binary code which is in turn converted into another binary code representing the amount of spark advance corresponding to the required spark advance characteristic of the engine. On the other hand, the output characteristic of the engine speed sensor 7 for detecting the speed of the engine is shown in FIG. 7 and the output of the sensor 7 is converted into a definite amount of spark advance corresponding to the required spark advance characteristic of the engine. This rotational spark advance characteristic required for the engine is shown in FIG. 5. In FIG. 5, the abscissa represents the engine speed n and the ordinate represents the rotational spark advance θ_n . The binary codes thus obtained are first converted into the corresponding amounts of vacuum advance and rotational advance, respectively, and the sum of the two spark advances is then formed in the operational circuit 12. The total amount of spark advance thus obtained is applied to the ignition circuit 13 which in turn effects the required ignition according to the degree of spark advance as determined by this total amount of spark advance. A readout circuit is included in the injection circuit 5 and the ignition circuit 13, respectively, and in the injection circuit 5 the fuel quantity q delivered is read out by a clock pulse of a definite time duration, since the fuel quantity q is determined by the duration of the injection. On the other hand, with the ignition circuit 13 the read operation is effected by the clock pulses having a time duration corresponding to the unit angle of the engine.

The manner in which the above described characteristics are computed will now be explained. To start with, a block diagram of an arrangement for computing the amount of fuel injection according to the intake manifold vacuum is illustrated in FIG. 8. In this figure, V_a denotes an input representing the engine intake manifold vacuum converted into a signal in the binary

code; and a block labelled V_a indicates a circuit for producing the signal V_a , i.e. the A - D converter. Other blocks shown in this and other figures, as described hereinafter, indicate respective circuits in the same manner. $F(V_{a\alpha})$ a first discriminator for determining whether the input V_a is greater or smaller than the value of the intake manifold vacuum at the point $V_{a\alpha}$ in FIG. 3; $F(V_{a\beta})$ a second discriminator for similarly determining whether the input V_a is greater or smaller than the intake manifold vacuum at the point $V_{a\beta}$ in FIG. 3. Numeral 101 designates a logical element for producing a L signal when V_a is greater than both $V_{a\alpha}$ and $V_{a\beta}$; 102 an inverter; 103 a logical element for producing a L signal when it finds that $V_{a\beta} < V_a < V_{a\alpha}$; 104 and 105 inverters; 106 a logical element for producing a L signal when it is found that $V_a < V_{a\beta}$. Designated V_{A5} is a five-place binary code input which represents the value of V_a as it is. V_{A4} designates the value of V_a which is shifted one place to the right so that the least significant digit is lost, thus changing the five-place binary number to a four-place binary number; V_{A3} the value of V_{A4} shifted one place to the right to produce a three-place binary number; V_{A2} the value of V_{A3} shifted one place to the right to produce a two-place binary number; V_{A1} the value of V_{A2} shifted one place to the right to produce a single-place binary number. V_{A0} designates a preset definite numerical value. Designated as J_{i5} is a connecting circuit for coupling the five-place V_{A5} to the adder 4, and J_{i4} , J_{i3} , J_{i2} , J_{i1} and J_{i0} designate circuits for respectively coupling the values of the four-place V_{A4} , the three place V_{A3} , the two-place V_{A2} , the single place V_{A1} and V_{A0} to the operational circuit 4. Numeral 107 designates a logical element which indicates that J_{i5} is to be coupled to the adder 4. Similarly, numerals 108, 109, 111, 112 and 110 designate logical elements for respectively indicating that J_{i4} , J_{i3} , J_{i1} and J_{i2} are to be coupled to the operational circuit 4.

With the arrangement described above, the operation will now be explained. To begin with, as the binary code input V_a is introduced, all of V_{A5} , V_{A4} , V_{A3} , V_{A2} , V_{A1} and V_{A0} are set up. Simultaneously, the value of V_a is compared with that of $V_{a\alpha}$ in the discriminator $F(V_{a\alpha})$ to determine whether the former is greater or smaller than the latter. Now, if the value of V_a is smaller than that of $V_{a\alpha}$, it is further compared with $V_{a\beta}$ in the second discriminator $F(V_{a\beta})$. If the result of the comparison indicates that the value of V_a is larger than $V_{a\alpha}$, then the conditions $V_a > V_{a\alpha}$ and $V_a > V_{a\beta}$ exist and hence $F(V_{a\alpha}) = F(V_{a\beta}) = 1$, so that the logical element 101 produces an L signal. When this happens, each of the logical elements 107, 109, 110, 111 and 112 connected to the output of the logical element 101 produces an H output, so that V_{A5} , V_{A3} , V_{A2} , V_{A1} and V_{A0} are now ready for connection to the adder 4. In other words, J_{i5} , J_{i3} , J_{i2} , J_{i1} and J_{i0} are now placed in condition for connection to the adder 4. Commands for coupling the J_{i5} , J_{i3} , J_{i2} , J_{i1} and J_{i0} to the adder 4 are issued by way of a separate circuit. Consequently, when the condition $V_a > V_{a\alpha}$ is met, the fuel quantity delivered is given as $q = V_{A5} + V_{A3} + V_{A2} + V_{A1} + V_{A0}$ and this value is applied to the injection circuit 5. Similarly, when there is the condition $V_{a\beta} < V_a < V_{a\alpha}$, the fuel quantity delivered is given as $q = V_{A4} + V_{A3}$, and when $V_a < V_{a\beta}$, $q = V_{A0}$. Since V_a is the five-place binary number, there exists the relation $V_{A5} \approx 2 V_{A4} \approx 4 V_{A3}$. Thus, the value of q is the fuel

quantity delivered from a combination of selected ones of the value of V_{A5} , V_{A4} , V_{A3} , V_{A2} , and V_{A1} . For example, if selected only V_{A5} or V_{A4} or V_{A3} , the value of q becomes roughly $1.0 V_a$, $0.5 V_a$ or $0.25 V_a$, respectively. If selected a combination of V_{A5} and V_{A3} or V_{A5} , V_{A4} and V_{A3} , or V_{A4} and V_{A3} , the value becomes $1.25 V_a$, $1.75 V_a$ or $0.5 V_a$, respectively. Other various values of q may be obtained by changing the combination. The value of V_{a0} may also be added to each of these values to obtain the value of q .

The operation described above will now be explained in detail with reference to an actual circuit. The circuit construction of the first and second discriminators $F(V_a \alpha)$ and $F(V_a \beta)$ will be as shown in FIG. 9. In this figure, numerals 120, 122, 124 and 126 designate NAND elements which decide whether the signal in each of the positions 2^4 through 2^1 is H or L. Numerals 121, 123 and 125 designate inverters which invert the signal from L to H and vice versa; 130, a logical element which performs the operation of comparison on the respective digits to give an indication of agreement or disagreement; 129 an inverter; 134, a NAND element. With this construction, the operation of the discriminators will be explained with reference to the first discriminator $F(V_a \alpha)$. The preset value of $V_a \alpha$ in this circuit is represented in the binary code as 10110 and the comparison operation is performed in the following manner to find whether V_a is greater than this preset value. Now, a H signal is applied to one of the input terminals of the NAND elements 120, 122, 124 and 126, respectively, and the five-place signal V_{a5} of the signal at the top is applied to the other input terminal of the NAND element 120. Then, if V_{a5} is H (1), the NAND element 120 produces an L output signal. The output of the NAND element 120 is inverted by way of the inverter 121, so that the output of the inverter 121 is H. Next, if V_{a4} which is four-place signal of V_a is H (1), the output of the inverter 129 is L and hence the output of the NAND element 122 is H. In this case, the output of the NAND element 130 is L and it is thus established that the value of V_a is greater than that of $V_a \alpha$, that is, the comparison $V_a > 10110$ exists. This output of the NAND element 130 is then applied to one of the input terminals of the NAND element 134 so that an H signal is produced at its output terminal L_a . In other words, the comparison $V_a > V_a \alpha$ is established. Similarly, the operation of comparison is performed on the three-place number and the two-place number, respectively, so that if $V_a > V_a \alpha$, and L signal is introduced at either one of the input terminals of the NAND element 134 which in turn produces an H signal at its output terminal L_a . As to the single-place code, there is the condition $V_a > V_a \alpha$ if $V_{a1} = 1$ and $V_a = V_a \alpha$ if $V_{a1} = 0$ and thus the discriminator may be dispensed with for V_{a1} if the value at the break point in FIG. 3 is chosen so that $V_a \geq V_a \alpha$. Therefore, the circuit is prearranged so that if the value of V_a agrees with respect to the four most significant bits 1011 of the preset binary number 10110 in the first discriminator $F(V_a \alpha)$, then the condition $V_a \geq V_a \alpha$ is present. It is also prearranged so that the comparison on the most significant bit is performed by comparing the output of the NAND element 120 with an H to make a discrimination between H and L, while the comparison operation on the lower order bits is performed only when there is found no agreement thereabout, since the existence of agreement on any higher order bit is indicated

by the H output of the corresponding inverter. The identical circuit as used with the first discriminator $F(V_a \alpha)$ may be constructed for the second discriminator $F(V_a \beta)$. In other words, what is needed is simply to construct a circuit identical with that of the first discriminator excepting that it employs a different binary number in place of the preset number 10110 of the first discriminator $F(V_a \alpha)$. In the second discriminator $F(V_a \beta)$, it is also possible to eliminate the comparison operation on the least significant bit, if it is prearranged in the manner described above that the condition $V_a \leq V_a \alpha, \beta$ is met when the comparison of the least significant bit produces an H.

Next, the manner in which the sum of any given numbers is formed in the operational circuit 4 of FIG. 8 will be explained with reference to FIG. 10. The digits to be added are designated as V_{a1} , V_{a2} , V_{a3} , V_{a4} , V_{a5} which are components of V_{A5} , V_{A4} , V_{A3} , V_{A2} , ... and V_{A0} , respectively and α . The added suffixes 1, 2, ..., 6 indicate the number of places from the least significant position. Designated as A are adders; J_1 , J_2 and J_3 , connecting circuits; S and S' memories for storing the sum of numbers, which are generally designated as memory groups Me and Me', respectively. Designated as Reset and Reset' are reset terminals which clear the memory groups Me and Me'. In these adders, three digits can be added simultaneously and so three addition signals V_{a1} , V_{a2} and V_{a3} will be coupled to the input terminals of the connecting circuit J_1 . In the adder A_1 , it is possible that an addition performed produces a carry so that the adder A_2 for the next lowest order bit adds three digits comprising two variables V_{a2} and V_{a3} and a carry C_{a1} . Similarly, the operation of addition is performed on all of the n binary digits. This addition is performed simultaneously from the lowest order bit to the highest order bit by means of a pulse signal P_{J1} . The sum for each digital position is stored in the corresponding memory in the memory group Me. The application of the next signal P_{J2} causes the addition of the sum of the lowest digits V_{a4} and V_{a5} and the partial sum stored in the S_1 , and similarly, V_{a4} and the partial sum stored in the memory S_2 , so that the results obtained are stored in the memories S'_1 and S'_2 respectively. Then, a reset pulse is applied to the reset terminal to clear the memories in the memory group Me. Whereupon, another pulse P_{J4} is applied so that the sum of the lowest order digit α , the partial sum stored in the memory S'_1 , and similarly, V_{a5} and the partial sum stored in the memory S'_2 are added. The results of this operation are stored in the memories S_1 and S_2 respectively. Similarly, the addition is repeated with the resulting partial sum being stored alternately in the memory groups Me and Me', respectively. Then, the result finally remaining in the memories S or the memories S' represents the sum total whose value constitutes the very value that indicates the duration of injection.

Referring now to FIG. 11, there is shown the construction of a pulse signal generating circuit for generating the pulses P_{J1} , P_{J2} , P_{J4} , and reset pulses to be applied to Me and Me'. In FIG. 11, reference character P_c designates a clock pulse generator for producing clock pulses comprising a continuous train of short duration pulses; R_1 , R_2 , ..., R_6 ring counters; P_{J1} , P_{J2} , P_{J3} , P_{J4} , P_5 and P_6 output pulses of the ring counters R_1 , R_2 , ..., R_6 ; J_1 , J_2 , and J_3 connecting circuits for coupling to adders those circuits in each of which the vacuum output V_a is substituted by V_{A5} , V_{A4} , ..., V_{A1} ; 156 a NAND

element for resetting the memory group Me; 157 a NAND element for resetting the memory group Me'. S₁, S₂, . . . , S₆ designate reset terminals adapted to be connected to the memory blocks of the memory group Me corresponding to the respective digit positions. In the first place, upon the completion of a first addition the sum in the adder A is entered into the memory group Me and the result of a second addition is entered into the memory group Me', and thus it is necessary to reset the memory group Me before the operation of a third addition is performed. Thereafter, for every subsequent addition either the memory group Me or the memory group Me' must be alternately reset. It is also a necessary that ultimately the final result of the addition is read out and both the memory groups Me and Me' are reset to prepare for the next series of computations. The sequence of this process will now be explained. In the first place, clock pulses P_C having a period of a definite time are applied to the ring counters R₁, R₂, . . . , R₆. Upon the application of the first clock pulse, the ring counter R₁ is set and it produces an output pulse P_{J1} at its output terminal so that the connecting circuit J₁ is coupled to the adder. Actually, one connecting circuit is provided for each digit position of V_{a5}, V_{a4}, . . . , V_{a0}. Accordingly, if

$$\sum_{i=0}^5 V_{ai}$$

at the time that the ring counter R₁ produces its output signal P_{J1} upon application of the first clock pulse, the connection circuits J₁, J₂ and J₃ connected respectively to the digit positions V_{a1} to V_{a5} of V_{a5}, the digit positions V_{a1} to V_{a4} of V_{a4} and the least significant digit position of V_{a3}, is coupled to the adder A. This represents the connecting circuit J₁ shown in FIG. 11. When another one of the clock pulses P_C is applied, the ring counter R₁ is restored to its original state and the ring counter R₂ produces an output signal P_{J2} at its output terminal, thereby coupling the connecting circuit J₂ to the adder. In this state, similarly the respective memories S₁ through S₆ in the memory group Me, the two most significant digit positions of V_{a3} and the least significant digit position of V_{a2} and a digit V_{a1} i.e. V_{a4} and V_{a3} and V_{a4} are coupled to the adder. This represents the connecting circuit J₂. As a further one of the clock pulses is applied, the ring counter R₂ is returned to its initial state and the ring counter R₃ produces an output signal P_{J3} at its output terminal so that, after being inverted in the inverter 150, this output signal P_{J3} is applied to the input of the NAND element 150 which in turn produces a reset pulse at its output. This reset pulse clears the memories S₁, S₂, . . . , S₆ in the memory group Me. Similarly, a subsequent application of the clock pulse causes the ring counter R₄ to produce an output signal P_{J4} at its output so that in like manner an addition is performed. Then, the memory group Me is eventually read out upon application of a succeeding one of the clock pulses. Whereupon, the ring counter R₆ is caused by another succeeding clock pulse to produce an output signal P₆ at its output so that the memory groups Me and Me' are reset to prepare for the next series of computations.

Referring now to FIG. 12, there is shown an embodiment of the adders described above. In this figure, reference character P_{J1} designates a signal for command-

ing the connection to the adder A₁, V_{a1}, V_{a2} and V_{a3} the least significant digits of V_{a1}, V_{a2} and V_{a3} to be added. Numeral 160, 161 and 162 designate NAND elements for coupling V_{a1}, V_{a2} and V_{a3} to the adder; 163; 164 and 165 inverters; 166; 167, 168, 169, 170, 171, 173 and 174 adding NAND elements; 172 an inverter; S₁ an L or H signal retained in the least significant digit position, C_{ut} a carry signal. When the signal P_{J1} is applied to the NAND elements 160, 161 and 162, V_{a1}, V_{a2} and V_{a3} are coupled to the adder. If any one of the signals of V_{a1}, V_{a2} and V_{a3} is in the H state, the NAND element 171 produces a carry signal H and this carry signal appears at a terminal C_{u1}. NAND element 167 produces C signal if and V_{a3} are all H signals and it put the memory S₁ in the H state. The NAND element 166 produces H signal if at least one of V_{a1}, V_{a2} and V_{a3} is an H signal. When two of V_{a1}, V_{a2} and V_{a3} are H signals, the NAND element 173 produces an H signal at a terminal S. Further, the NAND element 174 produces H signal if any one of V_{a1}, V_{a2} and V_{a3} is an H signal or if all three are H signals, respectively, and it then instructs the memory S₁ in the memory group Me to store H. As for the next least significant digit position, a circuit which operates similarly but has the signal C_{u1} in place of V_{a3} is constructed according to FIG. 10. In like manner, the adder A may be constructed for each of the higher order digit positions including the highest order digit position.

While the arrangement for computing the volume of fuel injection according to the engine intake manifold vacuum has been described, the spark timing can also be computed in exactly like manner. FIG. 13 illustrates a block diagram of a function generator arrangement required for this purpose. In FIG. 13, letter $\bar{V}_a$ designates a binary code representing the inverted intake manifold vacuum; I(V_{1α}) and I(V_{1β}) discriminators for determining whether the value of $\bar{V}_a$ is greater or smaller than the values at the points V_{1α} and V_{1β}, respectively; V₁₀₁ and V₁₀₂ constant setting elements; V₁₅, V₁₄ and V₁₃ code signals representing the value of $\bar{V}_a$ shifted to the right to produce five-place, four-place and three-place numbers, respectively; 0 a zero setting; J₁₀₁, J₁₅, J₁₄, J₁₃, J₁₀ and J₁₀₂ circuits for coupling V₁₀₁, V₁₅, V₁₄, V₁₃, V₁₀ and V₁₀₂ to an adder; 201 and 202 inverters; 203, 204 and 205 NAND elements for determining the region in which the intake manifold vacuum code lies. Letters J₁₀₁, J₁₀₂, J₁₅, J₁₄, J₁₃ and J₁₀ which are added at the output terminals of the NAND elements 203, 204 and 205 indicate that these NAND elements are connected to respective ends of the connecting circuits J₁₀₁, J₁₀₂, . . . , J₁₀. Designated as RPM is a binary code representing the engine speed; I(R_α), I(R_β) and I(R_γ) discriminators for determining whether the value of RPM is greater or smaller than the values of engine speed at the break points; 206, 207 and 208 are inverters; 208, 209, 210, 211 and 212 NAND elements which receive the output of the discriminators to determine the region in which the input RPM lies; R₅, R₄, R₃ and R₂ set values obtained by shifting to the right of the input RPM; R₀₁, R₀₂ and R₀₃ constants set independent of the input RPM; 0 a zero setting. Designated as J_{R5}, J_{R4}, . . . , J_{R0} are connecting circuits and letters J_{R01}, . . . , J_{R0} added at the outputs of the NAND elements 209, 210, 211 and 212 represent respective ends of the inputs of the like referenced connecting circuits.

With the arrangement described above, the operation will now be explained. In the vacuum advance

characteristic diagram of FIG. 4, the curve of the input $\bar{V}_a$ are broken at the points $V_{I\alpha}$ and $V_{I\beta}$. Then, the discriminators $I(V_{I\alpha})$ and $I(V_{I\beta})$ determine whether the value of $\bar{V}_a$ is greater or smaller than the values at the points $V_{I\alpha}$ and $V_{I\beta}$. Further, the NAND elements 203, 204 and 205 detect whether the value of $\bar{V}_a$ lies in the region $\bar{V}_a < V_{I\beta}$, $\bar{V}_{I\beta} < \bar{V}_a < V_{I\alpha}$ or $\bar{V}_a < V_{I\alpha}$. The amount of vacuum advance is determined according to these three regions on the graph, as follows:

If $\bar{V}_a < V_{I\beta}$, then the amount of vacuum advance $\theta_v = 0$. If $V_{I\beta} < \bar{V}_a < V_{I\alpha}$, then $\theta_v = V_{I5} + V_{I4} + V_{I3} + V_{I02}$. If $\bar{V}_a > V_{I\alpha}$, then $\theta_v = V_{I01}$.

These are the connections provided by the connecting circuits so that the results of the addition performed in the operational circuit 12 produce the curve as shown in FIG. 4. Similarly, the region in which the input RPM lies with respect to the break points R_α , R_β and R_γ of the engine speed spark advance curve is determined by the discriminators $I(R_\alpha)$, $I(R_\beta)$ and $I(R_\gamma)$ as well R 207 and 208 and the NAND elements 209, 210, 211 212, as

If $RPM < R_\gamma$, then the amount of rotational advance $\theta_R = 0$.

If $R_\gamma < RPM < R_\beta$, then $\theta_R = R_4 + R_3 + R_{03}$.

If $R_\beta < RPM < R_\alpha$, then $\theta_R = R_5 + R_2 + R_{02}$.

If $R_\alpha < RPM$, then $\theta_R = R_{01}$.

From the foregoing, the characteristic curve shown in FIG. 5 results. Then, an addition $\theta_v + \theta_R$ is performed to ultimately determine the amount θ of the total spark advance.

FIG. 14 illustrates a coder in which the input code corresponding to the engine intake manifold vacuum is shifted to the left or right to produce binary codes having varying number of digits.

Referring to FIG. 14, designated as V_{a1} is the first-place digit, i.e., the least significant digit of the five-place digital input corresponding to the engine intake manifold vacuum; V_{a2} , V_{a3} , ..., V_{a5} higher order digits of the same five-place input, respectively; 301 through 306 input inverters; V_{A5} a coder for producing a five-place code; V_{A4} , V_{A3} , V_{A2} , V_{A1} coders for producing the four-place through single-place codes having as many digits as indicated by their respective suffixes; 307 a NAND element for setting up the five-place digit or the most significant digit of the five-place code to be produced by the coder V_{A5} ; 308, 309, 310 and 311 NAND elements for setting up the corresponding digits of the five-place code in the coder V_{A5} ; 314, 315, ..., 317 similar NAND elements for the four-place number coder; 320 through 322 similar NAND elements for the five-place number coder V_{A3} ; 325 and 326 similar NAND elements for the two-place number coder V_{A2} ; 329 similar NAND elements for the single-place number coder V_{A1} ; In operation, the input codes V_{a5} through V_{a1} are supplied to the five-place number coder V_{A5} such that the largest input code V_{a5} is set up in the highest order NAND element 307. In like manner, the input code V_{a4} is set up in the NAND element 308, V_{a3} in the NAND element 309, V_{a2} in the NAND element 310, V_{a1} in the NAND element 311. Similarly, the input codes are supplied to the four-place number coder V_{A4} such that the input codes are set up in the like significance NAND elements as indicated by the suffixes of the input codes, while the input codes supplied to the three-place number coder V_{A3} are shifted one place to the right and then set up, thus shifting out

the least significant digits. In like manner, the input codes are set up in the two-place number coder V_{A2} through the single-place number coder V_{A1} each thereof shifting out the corresponding number of least significant digits of the input codes. Accordingly, there is the relation $V_{A5} \approx 2 V_{A4} \approx 4 V_{A3} \approx 8 V_{A2} \approx 16 V_{A1}$.

Next, the construction of the fuel injection circuit 5 and the ignition circuits 13 will be explained with reference to FIG. 15. In this figure, numeral 1710 designates the injection memory; 1720 the ignition memory. Numeral 1830A, designates a comparator which deenergizes the solenoid valve 1920A and erase the content stored in the injection memory 1710 when the duration of fuel injection attains or equals the stored content of the injection memory 1710. Numeral 1820A, designates the injection counter provided for the first cylinder, for example; 1810A and 1810B the injection distributor and the ignition distributor, respectively. Numeral 1840 designates the clock pulse generator; 1920A, the solenoid valve provided for the first cylinder, for example; 1920B the ignition system, 1140 the timing sensor, 1150 the angular sensor.

The construction of the fuel injection distribution circuit 1810A will now be explained in further detail with reference to FIG. 16. In this figure, numeral 4 designates the first operational circuit as previously explained; 411 to 416 output terminals for the output binary code signals of the first operational circuit 4. Numeral 1710 designates the injection memory; 1711 to 1716 flip-flops adapted to be set by the corresponding output binary code signals produced at the output terminals 411 through 416. Numeral 1830A, designates the comparator which comprises component elements 1831A through 1836A, so that when the signal inputs introduced at the two input terminals X and Y of the respective elements 1831A through 1836A are all at a high (H) or low (L) level simultaneously, each of the component elements 1831A through 1836A produces a signal voltage of low level L at the output terminal Z, while a NAND element 1837A produces a signal voltage of L level at an output terminal B when an H level signal voltage appears at all the output terminals Z of the component elements 1831A through 1836A. Numeral 1820A, designates the injection counter for counting the number of clock pulses applied to its input terminal C; 1821a through 1826a flip-flops constituting the counter 1820A. Designated as D is an inverter which inverts the output signal of the comparator 1830A, so that the content of the injection memory 1710 and the count of the injection counter 1820A, are erased when the signal level at the output terminal of the comparator 1830A, is low (L).

Referring to FIG. 17, there is shown the construction of one of the elements constituting the comparator 1830A. In this figure, numerals 1830a, 1830b, 1830c and 1830d designate NAND elements each thereof having two input terminals, X and Y input terminals; Z an output terminal. With this construction, the truth table of this element is given as follows:

X	Y	Z
L	L	L
L	H	H
H	L	H
H	H	L

where X = X terminal, Y = Y terminal, Z = Z terminal, H = H level, L = L level.

The operation of the fuel injection circuit 5 as described with reference to FIG. 15 to will now be explained. In the first place, the binary code signals produced at the output terminals 411 through 416 of the first operational circuit 4 are stored in the flip-flops 1711 through 1716 which are constituent elements of the injection memory 1710. When the clock pulse oscillator 1840 applies clock pulses to the input terminal C of the injection counter 1820A₁, the flip-flops 1821a through 1826a of the counter 1820A₁ are set in succession to count the input clock pulses in binary member. Then, when the binary code signal at the single output terminals Y of the flip-flops 1820a through 1826a in the injection counter 1820A₁ differs altogether from the binary code signal at the single output terminals X of the flip-flops 1711 through 1716 in the injection memory 1710, the output terminal B of the comparator 1830A₁ is at a low level (L), whereby with the high level (H) signal pulse inverted by the inverter D, the flip-flops 1821a through 1826a in the injection counter 1820A₁ and the flip-flops 1711 through 1716 in the injection memory 1710 are reset to clear the contents stored therein and at the same time the injection distributor 1810A is rendered inactive with the output pulse signal from the output terminal B and the clock pulses are no longer applied to the input terminal C.

While only the one injection counter 1820A₁ has been described, the other injection counter for the second cylinder and the remaining injection counters (not shown) are identical in operation with the injection counter 1820A₁, that is, the time that these counters are triggered to start action is determined by the injection distributor 1810A and the counters are caused to stop counting by means of an injection comparator provided for each counter, when the count of the respective counters attains the content stored in any corresponding memory.

Next, the construction and operation of the injection distributor 1810A mentioned above will be explained with reference to FIGS. 18 and 19. In FIG. 18, numeral 1140 designates the timing sensor having two output terminals one of which produces as many pulse signals as there are cylinders in the engine, for example, six pulse signals if the engine has six cylinders and the other output terminal produces one pulse signal for every six pulse signals produced from said one output terminal. Numeral 1840 designates the clock pulse oscillator for producing pulse signals having a predetermined frequency. Numerals 1811A, 1812A, 1813A, 1814A, 1815A and 1816A designate set/reset flip-flops (hereinafter simple referred to as S.R.F.F) each of which changes from one state to the other upon application of a first signal voltage to one input terminal and which is brought back to the state that existed just before the application of the first signal upon the application of a second signal voltage to the other input terminal; 1040, 1041, 1042, 1043, 1044 and 1045 NAND elements each thereof having four input terminals so that the signal level at the output terminal is L only when the signal levels at the four input terminals are all H. Numerals 1030, 1031, 1032, 1033, 1034 and 1035 designate the output terminals of the NAND elements 1040 through 1045, respectively. Numerals 1827, 1828 and 1829 designate flip-flops which are set with the pulse signals from the one output terminal of the timing sensor 1140 and which are reset with the pulse signal from the other output terminal of the timing sensor

1140. Designated as B₁, B₂, B₃, B₄, B₅ and B₆ are input terminals for resetting the S.R.F.F. 1811A to 1816A respectively when the output signals of the six injection comparators which are not shown are at a low level (L). Numerals 1050, 1051, 1052, 1053, 1054 and 1055 designate NAND elements each thereof having two input terminals so that clock pulses are applied to the one input terminals and the signals produced at the single output terminals of the S.R.F.F 1811A to 1816A respectively are applied to the other input terminals, whereby clock pulses are generated at the output terminals at the predetermined times as determined by the timing signals from the timing sensor 1140 for the predetermined duration. Designated as C₁, C₂, C₃, C₄, C₅ and C₆ are coupling terminals for connecting to the input terminals of the six injection counters which are not shown, and E₁, E₂, E₃, E₄, E₅ and E₆ are coupling terminals for connecting to the six solenoid valves which are not shown. Numerals 1060, 1061, 1062, 1063, 1064 and 1065 designate the output terminals of the S.R.F.F 1811A, 1812A, 1813A, 1814A, 1815A and 1816A, respectively.

With the construction described above, the operation of the injection distributor 1810A will now be explained with reference to FIG. 19. In this figure, letter α is the pulse voltage waveform produced at the one output terminal of the timing sensor 1140, β is the pulse voltage waveform produced at the other output terminal of the timing sensor 1140. Designated as A is the voltage waveform at the output terminal 1030 of the four-input NAND element 1040; B the voltage waveform at the output terminal 1031; C the voltage waveform at the output terminal 1032; D the voltage waveform at the output terminal 1033; E the voltage waveform at the output terminal 1034; F the voltage waveform at 1035. G is the voltage waveform produced at the single output terminal 1060 of the S.R.F.F 1811A when this flip-flop is set by the signal voltage waveform produced at the output terminal 1030 of the four-input NAND element 1040; H the signal voltage waveform generated at the output terminal C₁ by the application of the signal voltage produced at the output terminal 1060 and the clock pulse signal of the clock pulse oscillator 1840 to the NAND element 1050. J is the voltage waveform produced at the single output terminal 1061 of the S.R.F.F 1812A when this flip-flop is set by the signal voltage which is produced at the output terminal 1031 of the four-input NAND element 1041 by virtue of the output signal pulse from the timing sensor 1140; K the voltage waveform produced at the output terminal C₂ of the NAND element 1051 by the application of the signal voltage produced at the output terminal 1061 and the clock pulse signal of the clock pulse oscillator 1840 to the NAND element 1051. In like manner, the waveforms (not shown) which are similar with the signal voltage waveforms G and H are produced at the single output terminals 1062, 1063, 1064 and 1065 of the S.R.F.F 1813A, 1814A, 1815A and 1816A, respectively. The clock pulse signal voltages (not shown) similar to the waveforms H and K are also produced at the output terminals C₃, C₄, C₅ and C₆. In operation, the signal voltage β is first produced at time t_0 at the one output terminal of the timing sensor 1140, so that the flip-flops 1827, 1828 and 1829 are reset. Then, at time t_1 the signal voltage α is produced at the other output terminal of the timing sensor 1140 and this signal voltage α sets the

flip-flop 1827. This results in the voltage waveform at the output terminal 1030 of the four-input NAND element 1040 which is shown as A in FIG. 19. Then, at time t_2 the voltage waveform at the output terminal 1031 of the four-input NAND element 1041 falls as shown in FIG. 19-B. At time t_3 , the voltage waveform at the output terminal 1032 of the four-input terminal NAND element 1042 also falls as shown in FIG. 19-C, and similarly the voltage waveforms at the output terminals 1033, 1034 and 1035 vary at times t_4 , t_5 and t_6 as shown in FIGS. 19-D, 19-E and 19-F, respectively. At time t'_0 , the flip-flops 1827, 1828 and 1829 which have been set from time t_1 to t_6 are reset. Thereafter, at times t'_1 , t'_2 , t'_3 , t'_4 and t'_5 , the output voltages at the output terminals 1030 to 1035 vary as shown in FIGS. 19-A, 19-B, 19-C, 19-D, 19-E and 19-F. As with the output terminals C_1 and C_2 , clock pulses equivalent to those shown in FIGS. 19-H and 19-K appear at the output terminals C_3 through C_6 , that is, for the output terminal C_3 at time t_2 , C_4 at time t_4 , C_5 at time t_5 and C_6 at time t_6 . Then, when the clock pulses as shown in FIG. 19-H appear at the output terminal C_1 , the counter counts these clock pulses so that when its count in binary number attains the binary number stored in the memory (which is not shown), that is, at time T_1 , the output signal level of the comparator changes to L. This low level signal is in turn applied to the input terminal B_1 of the S.R.F.F. 1811A, whereupon the S.R.F.F. 1811A is reset and the signal voltage at the output terminal 1060 extinguishes at time T_1 and hence the clock pulse signal at the output terminal C_1 also extinguishes at time T_1 . In this case, the voltage at the output terminal E_1 disappears at time t_1 and it then reappears at time T_1 . Thus, if the output voltage at the output terminal E_1 is inverted, that is, if it is applied to a solenoid valve by way of an inverter circuit, the time interval between time t_1 and time T_1 will be the time during which the solenoid valve for the cylinder I is energized. In other words, the volume of fuel injection is determined by the binary digital signal code stored in the injection memory. Then, at time t_2 the counter for the cylinder II starts to count the clock pulses in the like manner as described above and the counter continues to count until the count becomes equal to the content of the corresponding memory, that is, up to time T_2 at which the counter stops its counting operation. Thus, the solenoid valve mounted on the cylinder II injects fuel from time t_2 to time T_2 . In like manner, the injection counters for the cylinders III, IV, V and VI start to count the clock pulses at times t_3 , t_4 , t_5 and t_6 respectively and at the same time the corresponding solenoid valves are energized to start fuel injection. Then, when the binary counts of these injection counters attain the values stored in the corresponding injection memories, the fuel injection stops. This process is repeated for the cylinders I through VI in sequence and the respective injection memories are cleared whenever the fuel injection stops, that is, the levels at the output terminals of the corresponding comparators change to L. However, as will be explained later, each time an ignition signal for producing an ignition spark to any cylinder is generated, the corresponding ignition memory is caused to restore and then a restore operation is also performed on the corresponding injection memory. Thus, no inconvenience can arise.

Next, the construction and operation of the ignition circuit 13 will be explained. Referring to FIG. 20, nu-

meral 1520 designates the second operational circuit for producing an output binary code signal corresponding to the amount of spark advance; 1820B the ignition counter for counting the pulse signals from the angular sensor 1150; 1821b through 1826b flip-flops constituting the ignition counter 1820B. Numeral 1720 designates the ignition memory for storing the output binary code signal produced at the output terminals 1521 through 1526 of the second operational circuit 1520; 1721 through 1726 flip-flops constituting the memory 1720. Numeral 1830B designates the comparator designed so that as the count of the ignition counter 1820B is found to be equal to the stored content of the ignition memory 1720, it produces an output signal to stop the counting operation of the ignition counter 1820B and at the same time it resets the counter 1820B and clears the stored content of the ignition memory 1720; 1831B through 1836B elements constituting the comparator 1830B and arranged to give their output signals when both the flip-flops 1721 through 1726 of the ignition memory 1720 and the flip-flops 1821b through 1826b of the ignition counter 1820B are at the same level. Numeral 1837B designates a seven-input NAND element adapted to produce an output signal only when all the constituent elements 1831B through 1836B of the comparator 1830B produce output signals and the signal level of the angular sensor 1150 changes to H. Numeral 1838B designates a S.R.F.F. so designed that it is set to produce an output signal at its single output terminal when the output signal of the seven-input NAND element 1837B is applied to one of the two input terminals and thereafter it is reset to reset the output voltage at the said single output terminal only when the signal pulse from the angular sensor 1150 is applied to the other input terminal of the S.R.F.F. 1838B; 1838B₁ and 1838B₂ two-input NAND elements constituting the S.R.F.F. 1838B. Numeral 1150 designates the angular sensor which produces angular signals correlated with the rotational speed of the rotating shaft of an engine, that is, it produces a preset number of pulses for every rotation of the rotating shaft. Numeral 1140 designates the timing sensor for producing pulse signals correlated with the rotation of the engine shaft; 1810B the ignition distributor so designed that it is actuated as the output signal of the timing sensor 1140 is applied to one of its input terminals, it supplies to the ignition counter 1820B the signal pulses applied to the other input terminal from the angular sensor 1150, and then it is rendered inactive by the output signal of the comparator 1830B to stop the application of the angular signal pulses to the ignition counter 1820B; 1811B a S.R.F.F. constituting the ignition distributor 1810B; 1812B and 1813B inverters for inverting the signal level at the output terminal with respect to that at the input terminal; 1814B a two-input NAND element which conducts when the signal level at the single output terminal of the S.R.F.F. changes to H, thereby applying the angular signal pulses to the counter 1820B. Numeral 1920B designates the ignition system for having an ignition spark produced by a spark plug (not shown) when the comparator 1830B produces an output signal; 1062 an output terminal of the comparator 1830B; 1063 an output terminal of the distributor 1810B; 1064 an output terminal of the S.R.F.F. 1811B.

Next, the operation of the ignition distribution circuit illustrated in FIG. 20 will be explained with reference

to FIG. 21. In this figure, designated as α is the same output voltage waveform of the timing sensor 1140 shown in FIG. 19; P the output voltage waveform of the inverter 1812B by which the S.R.F.F. 1811B is set to produce at its output terminal 1064 the signal voltage which is designated as Q. Letter R designates the output signal voltage waveform at the output terminal 1063 of the distributor 1810B; S the signal voltage waveform at the output terminal 1062 of the comparator 1830B. At time t_1 , the output signal α of the timing sensor 1140 sets the S.R.F.F. to produce the signal voltage Q at its output terminal 1064. This produces the angular signal pulse voltage such as the waveform R at the output terminal of the two-input NAND element 1814B, i.e., the output terminal 1063 of the distributor 1810B. When this happens, the ignition counter 1820B counts the angular signals so that when the count of the ignition counter 1820B attains the same value as the stored content of the ignition memory 1720 at a later time τ_{11} , the signal voltage S is produced at the output terminal 1062 of the comparator 1830B. Thus, at time τ_{11} the ignition system 1920B is actuated to have ignition sparks produced by the spark plugs. At the same time, the signal voltage at the output terminal 1062 resets both the flip-flops 1721 through 1726 of the ignition memory 1720 and the flip-flops 1821b through 1826b of the ignition counter 1820B, while this signal voltage S is applied, after being inverted by the inverter 1813B, to the S.R.F.F. 1811B so that this S.R.F.F. 1811B is simultaneously reset to terminate the signal voltage at the output terminal 1064 as shown by the waveform Q. This terminates the angular signal pulses at the output terminal 1063. This process of operation is repeated at later times $t_2, t_3, \dots, t_6$ to keep the engine operating. While the ignition sparks occur at the time τ_{11} which is delayed by the time from t_1 to τ_{11} with respect to the time t_1 , this time τ_{11} is an earlier time than the time t_2 . In other words, the "retard" with respect to the time t_1 for the output signal pulse from the timing sensor 1140 is an "advance" with respect to the time t_2 . Thus, in distributing the high voltage surge produced by the ignition system 1920B to the spark plugs, it can be arranged to have the spark occur with a "positive" spark advance so that by arranging to compute the delay time (spark retard) of the time from t_1 to τ_{11} , it is possible to compute the lead time (spark advance) of the time from t_2 to τ_{11} .

In the operation described above, the injection memory 1710 is cleared each time the injection is completed, that is, at times $T_1, T_2, \dots$. Therefore, while the content of the injection memory 1710 is zero thereafter, the injection counter 1820A is already counting at times $t_1, t_2, \dots, t_6$, so that the content of the injection memory 1710 and the count of the injection counter 1820A are not equal to each other. Thus, even if the stored content of the injection memory 1710 is erased while the injection counter 1820A is counting, there is no danger that the clearing of the memory 1710 immediately causes the injection counter 1820A to stop its counting operation, thereby stopping the injection of fuel.

Embodiment 2:

Referring to FIG. 22, there is shown the construction of the fuel injection circuit and the ignition circuit of a second embodiment. In FIG. 22 where those parts which bear the like reference numerals as used in FIG.

15 designate like component parts, numerals 1610 and 1620 designate selector switches, and 1910 a selection signal generator. In this embodiment the operational circuit 4 is connected to all the function generators 3, 9 and 11, as explained with reference to FIG. 1, through a selector switch 1400. The selector switch 1400 is actuated by said selection signal generator 1910 in synchronism with the selecting action of the selector switches 1610 and 1620 to transmit the binary coded output signals of the function generators 3, 9 and 11 to the operational circuit 4.

The construction of the fuel injection distribution circuit of the second embodiment is almost the same as that shown in FIG. 16 except for the selector circuit 1610. In FIG. 23 wherein the like reference numerals as used in FIG. 16 designate the like component parts, letter A designates an input terminal for receiving the selection signal from the selection signal generator 1910. Numerals 2611 through 2616 NAND elements constituting the selector switch 1610.

The operation of the injection counter 1820A₁, comparator 1830A₁, memory 1710 and selector switch 1610 as employed in the injection distribution circuit shown in FIG. 23 will now be explained. In the first place, when a signal pulse voltage is applied from the selection signal generator 1910 to the input terminal A of the selector switch 1610, this operates the selector switch 1610 so that the binary coded signal produced by the operational circuit 4 is written by way of the NAND elements 1611 through 1616 of the selector switch 1610 into the corresponding flip-flops 1711 through 1716 which are constituting elements of the injection memory 1710. Whereupon, the signal pulse voltage applied to the input terminal A of the selector switch 1610 is turned off so that the connection between the operational circuit 4 and the injection memory 1710 is interrupted. Then, as the clock pulses are applied at the input terminal C of the injection counter 1820A₁ from the clock pulse oscillator 1840, the flip-flops 1821 through 1826 of the counter 1820A₁ are set in succession thereby counting the applied clock pulses in a binary number system. In this situation, when the binary coded signal appearing at the single output terminals of the respective flip-flops 1821 through 1826 of the injection counter 1820A₁ differ altogether from the binary coded signal appearing at the single output terminals of the flip-flops 1711 through 1716 constituting the injection memory 1710, the output signal at the output terminal B of the comparator 1830A₁ changes to L so that the injection counter 1820A₁ and the injection memory 1710 are reset with the signal pulse inverted by the inverter D, thereby erasing the count of the counted and the content of the memory, respectively. Concurrently, the distributor 1810A (shown in FIG. 18) stops the operation so that the clock pulse signals are no longer applied at the input terminal C of the injection counter 1820A₁. While the injection counter 1820A₁ has been described by way of an example, the operation of the injection counter 1820A₂ and other counters (not shown) for other engine cylinders is identical with the above described operation of the injection counter 1820A₁, that is, the time of operation is set by the distributor 1810A, and when a comparator provided for each counter finds the count of the counter to be equal to the content of the corresponding injection memory, the counter stops its operation.

Next, the construction of the injection circuit which is almost same as that shown in FIG. 20 except for the selection switch 1620 will be explained with reference to FIG. 24. In FIG. 24, like reference numerals as used in FIG. 20 designate the like component parts. The selector switch 1620 is adapted so that when there is a high level (H) at one its input terminals, it conducts with the resultant conduction among the remaining plurality of input terminals and its plurality of output terminals, and numerals 1621 through 1626 designate two-input NAND elements. Designated as M is an output terminal of the distributor 1810B which is inverted to H when the output signal voltage appears at the output terminal 1062 of the comparator 1830B; N an input terminal of the selector switch 1620.

Next, the construction of the selection signal generator 1910 will be explained with reference to FIG. 25. In this figure, numeral 1911 designates a S.R.F.F. which is set to produce a signal voltage when a signal voltage is applied at one input terminal and which is reset to produce a signal voltage at the other output terminal when another signal voltage is applied later at the other input terminal; 1911A and 1911B two-input NAND elements constituting the S.R.F.F. 1911. Numeral 1912 designates a NAND element; 1913 an inverter; 1914 and 1915 three-input NAND elements for distributing the angular pulse signals; 1916 and 1917 flip-flops for counting the angular pulse signals. Designated at N' is an output terminal for supplying a selection signal to the input terminal N of the selector switch 1620; A' an output terminal for supplying a selection signal to the input terminal A (FIG. 23) of the selector switch 1610; M an input terminal of the S.R.F.F. 1911 connected to the output terminal of the ignition distributor 1810B which produces a signal voltage concurrent with the occurrence of an ignition spark upon the application of the signal voltage to the ignition system by the comparator 1830B.

Next, the operation of the ignition memory 1720; comparator 1830B, ignition distributor 1810, ignition counter 1820B and selection signal generator 1910 which are constructed as described above will be explained with reference to FIG. 26. In FIG. 26, designated as α is the timing pulse voltage waveforms produced at the output terminal of the timing sensor 1140; P the output voltage waveform of the inverter 1812B which sets the S.R.F.F. 1811B to produce at its output terminal 1064 the signal voltage designated as Q; R the output signal voltage waveform at the output terminal 1063 of the distributor 1810B; S the signal voltage waveform at the output terminal 1062 of the comparator 1830B; U the selection signal voltage waveform produced at the output terminal N' of the selection signal generator 1910; V the selection signal voltage waveform appearing at the output terminal A' of the selection signal generator 1910. Now at the time t_1 , the output signal α of the timing sensor 1140 sets the S.R.F.F. 1811B to produce the signal voltage Q at its output terminal 1064. This causes the angular pulse signal voltage as shown in FIG. 26-R to appear at the output terminal of the two-input NAND element 1814B, that is, at the output terminal of the ignition distributor 1810B. Whereupon, the flip-flops 1821b through 1826b of the ignition counter 2820B count the angular pulse signals, so that when the count of the ignition counter 1820B attains the value of the content of the ignition memory 1720 at a later time τ_{11} , the signal volt-

age S appears at the output terminal 1062 of the comparator 1830. Consequently, at time τ_{11} , the ignition system 1920B is actuated to cause the spark plug to produce an ignition spark. Concurrently, the signal voltage S at the output terminal 1062 resets the flip-flops 1721 through 1726 of the ignition memory 1720 and the flip-flops 1821b through 1826b of the ignition counter 1820B so as to erase the content of the memory 2720 and the count of the counter 1820B, and at the same time the signal voltage S is inverted by the inverter 1813B which is then applied to the S.R.F.F. 1811B so that this S.R.F.F. 1811B is reset to terminate the signal voltage at the output terminal 1064 as shown by the waveform Q, thereby terminating the angular pulse signal at the output terminal 1063. Concurrently, the signal voltage S sets the S.R.F.F. 1911 of the selection signal generator 1910 to initiate the counting of the angular pulse signals by the flip-flops 1916 and 1917, whereby at time τ_{12} the selection signal U appears at the output terminal N' and then at time τ_{13} the selection signal V appears at the output terminal A'. Here, the signal voltage U is applied at the input terminal N of the selector switch 1620 and the signal voltage V is applied at the input terminal A of the selector switch 1610 and thus, while the contents of the ignition memory 1720 and the injection memory 1710 are respectively erased at time τ_{11} and at time T_1 (FIG. 19) at which the fuel injection stops, at time τ_{12} the ignition memory 1720 newly stores a further binary codes signal and at time τ_{13} the injection memory 1710 newly stores a further binary coded signal. This process is repeated thereafter at times $t_2, t_3, \dots, t_6$, thereby maintaining the continued operation of the engine. In this connection, while the ignition spark occurs at time τ_{11} which is delayed by the time from τ_{11} to t_1 with respect to the time t_1 , this time τ_{11} is earlier than the time t_2 . In other words, the "retard" with respect to the time t_1 of the output timing pulse signal of the timing sensor 1140 is the "advance" with respect to the time t_2 . Thus, in distributing the high voltage surge produced by the ignition system 1920B to the spark plug, it can be arranged to have the spark occur with a "positive" spark advance so that by computing the delay time (spark retard) of from τ_{11} to t_1 , it is possible to compute the lead time (spark advance) of from t_2 to τ_{11} .

In the operation described hereinbefore, the injection memory 2710 is erased each time the injection is completed, that is, at times $T_1, T_2, \dots, T_6$. Thus, as previously explained, the content of the injection memory 1710 remains at zero until such times as $\tau_{13}, \tau_{23}, \dots$. However, the injection counters 1820A₁ and 1820A₂ (another counter not shown) are already set to count at the times t_1 and t_2 and therefore the content of the injection memory 1710 and the counts of the injection counters 1820A₁ and 1820A₂ are unequal. As above-mentioned, it should be apparent that even if the injection memory 1710 is erased while the injection counters 1820A₁ and 1820A₂ are operating, this clearing of the memory 1710 would not cause the injection counters 1820A₁ and 1820A₂ to stop their counting operation to stop the fuel injection.

It is now evident from the foregoing that the system of the present embodiment is advantageous over the system of the first embodiment in that since it incorporates a selection circuit for selectively coupling the first and second output digital signals of an operational circuit to the succeeding stage and the circuit for supply-

ing selection command signals to the selection circuit, both the fuel injection system and the ignition system can be combined in a very rational manner by virtue of the so-called time sharing system realized by these operational and selection circuits.

Embodiment 3:

The general construction and operation of the system of a third embodiment of the invention will be explained with reference to FIG. 27. In this figure, designated as 1130 is a temperature sensor for detecting the temperature of an engine, which comprises a thermistor for measuring the temperature of the engine oil, cooling water or the like, a constant voltage source which supplies a constant voltage to the thermistor and an A - D converter for detecting and converting the voltage across the thermistor into a digital signal. 1110 designates a start sensor for detecting the start of the engine to produce an H or L signal, that is, a sensor which detects, for example, the voltage across the starting terminal of the engine starting motor switch, i.e., the key switch, or an engine speed lower than a predetermined value to thereby produce an H or L signal. 1 designates a vacuum sensor which comprises, for example, a transducer for converting the engine intake manifold vacuum into a DC voltage as described hereinbefore and an A - D converter for converting the output voltage of the transducer into a digital quantity. Designated as 1120 is an acceleration sensor for producing an output proportional to the opening speed of the engine throttle valve; the acceleration sensor may comprise a generator which produces a voltage proportional to the opening speed of the engine throttle valve, a time constant circuit operable in response to the output voltage of the generator and an A - D converter, wherein the output voltage of the generator is applied to the time constant circuit where the voltage proportional to the output voltage of the generator is converted into a damped waveform decreasing with a predetermined time constant and the A - D conversion is performed according to this waveform to obtain a digital output corresponding to the opening speed of the throttle.

1160 designates a switch which varies the air-fuel ratio so that in order to obtain the maximum amount of power from the engine, the mixture is richer when the engine throttle valve is almost fully opened than when the throttle openings are other than full-throttle. The switch may comprise two chambers one of which is opened to the atmosphere and the other communicates with the intake manifold to admit the intake manifold thereinto, a diaphragm displaceable by the difference in pressure between the two chambers and a switch which operates in response to the movement of the diaphragm, whereby the switch may be closed or opened to produce an H or L signal. Numeral 7 designates an engine speed sensor for detecting the engine speed in terms of a digital quantity, which may comprise a generator as described in preceding embodiments and an A - D converter for converting the detected maximum voltage into a digital quantity. Alternately, the engine speed sensor may comprise an integrating circuit which integrates a voltage waveform synchronized with the rotation of the engine and having a constant magnitude and a constant pulse width so as to produce a DC voltage proportional to the number of

pulses per unit time, and a circuit which effects the A - D conversion of this DC voltage.

These are the sensors for obtaining those numerical values which are necessary to control the fuel injection and the ignition timing of an engine. In addition, some other sensors are required for the computation of the fuel injection and the ignition timing requirements of the engine. Such sensors include an injection start sensor for initiating the fuel injection, a rotational angle sensor 1150 which detects the angle of rotation of the engine crankshaft to determine the ignition timing, and a clock pulse generator 1840 for generating clock pulses on the basis of the minimum duration of the injection.

Next, explanation will be made of those function generators in FIG. 27 which are incorporated in the system of the present embodiment. Designated as T - K is a function generator which receives the output signals of the temperature sensor 1130' and the start sensor 1110 to determine a pattern in a manner that will be explained later, so that how much quantity of fuel as determined according to the intake manifold vacuum and other conditions may be increased to suit the temperature of the engine at the start thereof will be calculated according to this pattern. Letter C_q designates a fuel cutoff signal generator, $V_a - qv$ a function generator which designated as 3 in the preceding embodiments and receives the output signal of the vacuum sensor V_a to convert the amount of the engine intake manifold into the rate of fuel flow required for the engine; $A_{cc} qA_{cc}$ a function generator which receives the output signal of the acceleration sensor 1120 to increase the volume of injection; $A/F - qA/F$ a function generator for determining the amount of fuel to be increased to change the air-fuel ratio according to the output signal of the switch 1160, and whether the volume of fuel injection should be increased by a predetermined amount is determined by this function generator. Letter S_1 designates an operational circuit into which the numerical value contained in the function generator T - K is transferred; S_2 an operational circuit for forming the sum of the output signals of the function generators $V_a - qv$, $A_{cc} qA_{cc}$ and $A/F - qA/F$; S_3 an operational circuit which adds the output signal of the operational circuit S_2 according to the output signal pattern of the operational circuit S_1 , and the output value of the operational circuit S_3 ultimately determines the volume of injection. 1710 designates a memory circuit into which the output signal value of the operational circuit S_3 is transferred for storage; 1810A a distributor, 1820A₁ and 1820A₂ counter circuits 1830A₁ and 1830A₂ comparators which constitute read circuits for reading out the content of the memory circuit 1710 according to the output signals of the timing sensor 1140 and the clock pulse oscillator 1840; 1920A₁ and 1920A₂ injection circuits each having an electromagnetically operated injection valve mounted on the engine, so that the volume of each injection is determined by the time during which the solenoid coil of the injection valve is energized, that is, the time that the injection valve remains open.

It is to be noted here that the system of the present embodiment is applied to a six-cylinder engine and that the injection circuits 1920A₁ and 1920A₂ and their read circuits such as 1820A₁, 1820A₂, 1830A₁ and 1830A₂ are provided for two of the six cylinders, and thus the corresponding injection circuits and their read

circuits (not shown) are similarly provided for the remaining four cylinders. In the case of a multiple-cylinder engine wherein the injection of fuel into the respective cylinders is performed at different times, it is possible to arrange so that only the injection circuits are provided in like number and each of the read circuits of a smaller number serves on a plurality of injection circuits to effect the required injection. $V_a - \theta_i$ is a function generator which converts the output of the vacuum sensor V_a into θ_i ; 1170 a spark advance cutout signal generator which prevents the occurrence of any spark advance by the engine intake manifold vacuum when the engine speed is lower than a predetermined engine rpm; $RPM - \theta_R$ a function generator referred to in the preceding embodiments for converting the output signal of the engine speed sensor RPM into the amount of spark advance required; S_4 an operational circuit for forming the sum of the amount of vacuum advance impressed from the function generator $V_a - \theta_i$ and the amount of rotational advance impressed from the function generator $RPM - \theta_R$, the output of the operational circuit S_4 representing the total amount of spark advance required; 1720 a memory circuit into which the output of the adder S_4 representing the total advance required is introduced for storage; 1810B a distributor, 1820B a counter, 1830B a comparator, respectively, for reading out the content of the memory circuit 1720 in accordance with the output signal of the angular sensor 1150 and the timing sensor 1140; 1920B an ignition system which effects the ignition of the engine upon completion of a read operation by the ignition read circuit.

With the arrangement described above, the output signal of the acceleration sensor 1120 is first converted in the function generator $A_{cc} - qA_{cc}$ into a signal representing the amount of fuel to be increased for acceleration and simultaneously whether the fuel quantity should be increased to change the air-fuel ratio is determined in the function generator $A/F - qA/F$ according to the output signal of the A/F switch 1160. The acceleration increment signal qA_{cc} produced in the function generator $A_{cc} - qA_{cc}$ is temporarily stored. Then, upon receipt of the output signal from the vacuum sensor V_a , the function generator $V_a - qv$ produces the fuel injection signal qv corresponding to the intake manifold vacuum, so that this signal is added to the previously produced acceleration increment signal qA_{cc} and the air-fuel ratio change signal qA/F from the function generator $A/F - qA/F$ in the operational circuit S_2 to compute the steady state fuel injection quantity q . That is, the steady state fuel injection quantity $q = qv + qA_{cc} + qA/F$ is stored. Whereupon, depending on whether the engine is at start and whether the engine is warming up, the function generators $T - K$ is brought into action, thus transferring its pattern K into the operational circuit S_1 . When this happens, the preliminary stored value of the fuel injection quantity q is added to the value of the pattern K in the operational circuit S_3 to determine the ultimate total fuel injection quantity Q which is in turn stored in the memory circuit 1710. Then, the output signal of the vacuum sensor 1 is applied to the function generator $V_a - \theta_i$, so that the function generators computes and stores the spark advance θ_i corresponding to the intake manifold vacuum. On the other hand, upon receipt of the output signal of the engine speed sensor 7, the function generator $RPM - \theta_R$ computes and stores the spark advance θ_R corre-

sponding to the engine speed, so that this spark advance θ_R is added to the spark advance θ_i in the operational circuit S_4 to produce the final total spark advance $\theta_T = \theta_i + \theta_R$ which is in turn stored in the memory circuit 1720.

In the foregoing explanation, all the computations are performed in binary codes. The function generator for computation employed in this embodiment will now be explained with reference to FIGS. 28 et seq. FIG. 28 illustrates a block diagram of a function generator for producing the acceleration increment signal qA_{cc} and the air-fuel ratio change signal qA/F ; FIG. 29 a diagram showing the required acceleration increment qA_{cc} of the engine corresponding to the output signal a_{cc} of the acceleration sensor 1120; FIG. 30 a diagram showing the required air-fuel ratio change increment qA/F of the engine corresponding to the relative vacuum, i.e., the ratio of the intake manifold vacuum to the atmospheric pressure. In FIG. 28, 1120 designates the acceleration sensor whose output signal is the output of the time constant circuit whose input is a voltage signal proportional to the opening speed of the engine throttle valve 1180 designates a command signal generator; J_{Acc} a command signal input for computing the acceleration increment, which will be explained later; $I(A_{co})$ a discriminator which determines whether the output signal a_{cc} of the acceleration sensor 1120 is greater or smaller than the value at point a_{co} on the graph of FIG. 29. Numerals 3101 and 3103 designate NAND elements; 3102, 3104 and 3105 inverters; A_{cc5} a coder for producing a five-place code in which the most significant position contains the most significant digit of the input code applied to this coder by way of the inverter 3104; A_{cc3} a coder for producing a three-place code; K_{12} a coder for producing a code which represents a constant, 00 a coder for producing a code which represents zero; J_{Acc5} , J_{Acc3} , J_{K12} and J_0 circuits which supply inputs to the coders A_{cc5} , A_{cc3} , K_{12} and 00; A/F the switch which detects the throttle opening to vary the air-fuel ratio; 3106 a NAND element which detects whether the output signal qA/F of the switch A/F is H or L; 3107 an inverter; $A/F - qA/F$ a function generator which determines, whether if any, increase in the fuel quantity is necessary.

With the arrangement described above, when the command signal input J_{Acc} for initiating the computation of an increased fuel quantity for acceleration changes from L to H, the discriminator $I(A_{co})$ receives the acceleration increment signal a_{cc} from the acceleration sensor 1120 to determine whether the acceleration increment signal a_{cc} is greater or smaller than a_{co} . If the result shows that $a_{cc} > a_{co}$, the discriminator $I(A_{co})$ produces an H signal, whereas it produces an L signal if the result is contrary. Whether the signal is H or L determines which of the coders are to be connected, that is, the coders A_{cc5} , A_{cc3} and K_{12} are to be connected, or the coder 00 is to be connected to the operational circuit S_2 . This is determined by the circuits J_{Acc5} , J_{Acc3} , K_{12} and J_0 and the inputs to these circuits are supplied by way of the inverters 3104 and 3105. It is to be noted here that while it is illustrated that the H signal is applied to the circuit including the NAND elements 3101 and 3103, this circuit may operate without receiving such an H signal and therefore the practical circuit can be simplified. However, for purposes of explanation, it is assumed that the circuit produces an H signal upon the application of an H input thereto. In like manner,

an H signal is also added to other figures. The coder 00 is provided to indicate the absence of any input to the operational circuit S_2 and therefore it can be eliminated in a practical circuit. On the other hand, if the signal output of the switch 1160 is H, the function generator A/F - qA/F comes into operation, while it does not operate, that is, it produces an L output, if the output of the switch 1160 is L. Now returning to the explanation of the manner in which the acceleration increment is computed, in the process of producing the acceleration increment signal qA_{cc} corresponding to the output signal a_{cc} of the acceleration sensor 1120, the coders A_{cc5} , A_{cc3} and K_{12} are connected to the operational circuit, so that in effect the acceleration increment signal qA_{cc} is given in the present embodiment, as follows:

$$qA_{cc} = a_{cc5} + a_{cc3} + K_{12}$$

where a_{cc5} , a_{cc3} and K_{12} are the output signals of the coders A_{cc5} , A_{cc3} and K_{12} . While, in this case, it is given that $qA_{cc} = a_{cc5} + a_{cc3} + K_{12}$, many other combinations than this one are possible among the coders A_{cc5} , A_{cc3} and K_{12} . Thus, if $a_{cc5} = 1.00$, then $a_{cc3} = 0.25$. If a coder A_{cc1} is provided, $a_{cc1} = 0.0625$ may be available, so that with the minimum unit of 0.0625 straight lines at varying angles may be obtained. Thus, a combination can be selected which would ensure an increased fuel quantity characteristic required for an engine, such as the one which is very close to the characteristic shown in FIG. 29. Now, by increasing the amount of fuel for acceleration and changing the air-fuel ratio in the manner as described hereinbefore, various special qualities in the operation of the engine can be ensured as will be explained hereinafter. In the first place, when the engine throttle valve is opened rather quickly to increase the speed of the engine, there results a rapid increase in the amount of air drawn in, and since this quick opening of the throttle valve does not produce a corresponding rapid increase of the engine speed, the pressure in the intake manifold temporarily approaches a level which is close to atmospheric pressure. Under these circumstances, the output value of the vacuum sensor 1 cannot rapidly follow such development, resulting in a lean air-fuel mixture being supplied to the engine. This lean air-fuel mixture is compensated by the aforesaid increased fuel supply for acceleration, so that the leaning out of the air-fuel mixture due to any rapid variation of the throttle valve opening may be prevented, thereby obtaining efficient operation of the engine without any misfiring. On the other hand, when the throttle valve is almost in the fully opposed position, it is required that instead of operating the engine so as to accomplish the minimum rate of fuel consumption, the engine should be operated at its fuel-power to obtain a full efficient operation of the engine. To meet this requirement, the air-fuel ratio of the engine must be made richer than is needed to attain the minimum rate of fuel consumption and this is attained by the use of the switch 1160 and function generator A/F - qA/F . And this requirement must be satisfied under all the operating conditions of the engine. In other words, when the engine is operated with an almost wideopen throttle on the road where the atmospheric pressure is low, the vacuum sensor 1 produces the absolute pressure output and it is impossible to measure the throttle opening from this output value, thus making it necessary to increase the supply of fuel according to the output of the switch 1160. FIG. 31 illustrates a block diagram of a

function generator for computing the volume of fuel injection and the amount of spark advance according to the intake manifold vacuum. FIG. 32 illustrates a diagram showing, in relation to the intake manifold vacuum V_a , the fuel injection quantity Q_r required for the engine and the fuel injection quantity Q representing Q_r plus the acceleration increment Q_{Acc} and the air-fuel ratio changing increment QA/F , and in the figure the segments Q_{Acc} and QA/F as related to the intake manifold vacuum V_a show examples where an increased fuel supply is required.

The construction and operation of the arrangement will be explained with reference to FIG. 31. In this figure, designated as 1180 is the command signal generator as aforeexplained; J_{qv} represents a command signal for computing the volume of fuel injection according to the intake manifold vacuum; $F(V_a \alpha)$, $F(V_a \beta)$ discriminators as explained with reference to FIG. 8; 3110, 3111, 3115 and 3116 inverters; 3112, 3113 and 3114 NAND elements which, depending on the regions of the output signals of the vacuum sensor 1 on the graph shown in FIG. 3, open the gates corresponding to the regions: J_{θ} , a command signal for computing the spark advance according to the intake manifold vacuum; $I(V_1 \beta)$ and $I(V_1 \alpha)$ discriminators for determining the regions of the intake manifold vacuum V_a in relation to the break points $V_1 \beta$ and $V_1 \alpha$; 3117, 3118 and 3119 NAND elements for opening the relevant gates according to the regions as determined by the last-mentioned discriminators; V_{A5} a binary coder for converting the maximum numerical value of the output of the vacuum sensor V_a into a five-place code; V_{A4} , V_{A3} , V_{A2} and V_{A1} similar binary coders for producing four-place, three-place, two-place and single-place codes, with the coder V_{A1} producing an H code only when the most significant digit of the vacuum sensor output is an H. While this coding method will be explained later, it is identical to the method employed in the computation of the acceleration increment explained with reference to FIG. 28. Designated as J_{A5} may be a connecting circuit for coupling to the operational circuit S_2 (which is also S_4 in another sequence) the coder V_{A5} which produces the five-place code or a gate circuit which issues commands to the coder V_{A5} to indicate whether the coding operation is to be initiated. In the current explanation of the present embodiment, J_{A5} is assumed to be the latter gate circuit. When this gate circuit J_{A5} does not cause the coder V_{A5} to produce any binary code signal, the coder V_{A5} contains an L in every digit positions so that the result of the addition in the operational circuit S_2 shows the same value as that obtained before the addition. Designated as J_{A4} , J_{A3} , J_{A2} and J_{A1} are similar gate circuits for the coders V_{A4} , V_{A3} , V_{A2} and V_{A1} ; K_1 , K_2 , K_7 and K_8 coders for producing the constant codes; AL_1 a coder for producing a code in which all the digit positions are H's. While in the arrangement of the preceding embodiments the output code of the vacuum sensor 1 is first inverted and the computation of the spark advance related to the intake manifold vacuum is performed on the basis of this inverted code, the same result may be obtained by a method in which the output code of the vacuum sensor 1 is utilized in its uninverted form on the assumption that the necessary inversion would eventually take place, and the inversion is carried out after computation. In this embodiment, the latter method of the computation is used.

With the arrangement shown in FIG. 3, now assume that the command signal J_{qv} for computing the volume of fuel injection is H, then the output of the vacuum sensor 1 at this time, i.e., the value of the intake manifold vacuum V_a is located on the graph of FIG. 3 to see in which portion of the broken lines the value lies. In other words, the discriminator $F(V_a \alpha)$ determines whether there is the condition $V_a > V_{a\alpha}$ or $V_a < V_{a\alpha}$ and concurrently the discriminator $F(V_a \beta)$ determines whether there is the condition $V_a \leq V_{a\beta}$, whereupon any one of the NAND elements 3112, 3113 and 3114 produces an L signal. For example, if there is the condition $V_a > V_{a\alpha}$, then the output of the NAND element 3112 is L and the other NAND elements 3113 and 3114 respectively produces an H signal. Consequently, the gate circuits J_{A5} , J_{A4} and J_{K1} are opened such that the coders V_{A5} and V_{A4} convert the output value of the vacuum sensor V_a into the corresponding binary codes. The coder K_1 produces its constant code. Since the outputs of the remaining coders are all L's, the result of the addition in the operational circuit S_2 indicates the fuel injection quantity $qv = V_{A5} + V_{A4} + K_1$. Then, as the value of the steady state fuel injection quantity q , the value representing this quantity qv plus the quantities of the previously mentioned acceleration increment signal qA_{cc} and the air-fuel ratio change increment signal qA/F , i.e., $q = qv + qA_{cc} + qA/F$ is performed in the operational circuit S_2 . As will be explained latter, the value of the steady state fuel injection quantity q must be compensated according to the engine temperature. Next, if it is the time that the degree of spark advance according to the intake manifold vacuum must be computed, then a command signal of the command signal generator 1180 $J_{\theta_v} = 1$. Of course, it also follows that $J_{qv} = 0$. The output code of the vacuum sensor 1 is then compared in the discriminators $I(V_1 \beta)$ and $I(V_1 \alpha)$ with the two values at the break points $V_1 \beta$ and $V_1 \alpha$ on the graph of FIG. 4 showing the required spark advance characteristics of the engine in relation to the intake manifold vacuum, thereby determining whether this output code is greater or smaller than these two values. The outputs of the discriminators $I(V_1 \beta)$ and $I(V_1 \alpha)$ cause any one of the NAND elements 3117, 3118 and 3119 to produce an L output, depending on the output value of the vacuum sensor 1 at this time, and according to the L output the gate circuits J_{A5} to J_{A1} actuate the coders V_{A5} to V_{A1} . Similarly, any one of the gate circuits J_{K7} , J_{K8} and J_{AL1} is opened by the NAND elements 3117, 3118 or 3119 so that any one of the coders K_7 , K_8 and K_{AL1} produces its predetermined code. As will be seen from FIG. 4, in the circuit shown in FIG. 31, if $V_a > V_1 \beta$, then the degree of spark advance is zero; if $V_1 \alpha < V_a < V_1 \beta$, then the spark advance has a certain slope; if a $V_a < V_1 \alpha$ the spark advance has a certain value. Now, if $V_a > V_1 \beta$, then the degree of spark advance is zero, the code contain H's in all the digit positions. This is the constant code which is produced by the coder AL_1 . This code is then introduced into the operational circuit $S_4(S_2)$ so that if the inverse is read out, it directly represents the degree of vacuum advances. On the other hand, when the engine is idling or operating at a speed below the idling speed, the intake manifold vacuum should not be taken into as a parameter. Thus, the discriminator $I(R \gamma)$ is provided to produce an H output when it detects the condition that the output code signal rpm of the engine speed sensor 7 is

rpm < $R \gamma$ (see FIG. 5), where $R \gamma$ is the idle speed or the like. Accordingly, if the output of the inverter 3120 is H, then rpm < $R \gamma$, so that the gate circuit J_{AL1} is opened to actuate the coder AL_1 , where rpm is the output signal of the engine speed sensor 7. Numeral 3121 designates a NAND element for the NAND element 3119 and the inverter 3120. Numeral 3122 designates an inverter for the operational circuit $S_4(S_2)$. Then, at this time all the other gate circuits must be in their closed states and therefore the output of the discriminator is coupled to the NAND elements 3117, 3118 and 3119 as an input thereto. In this way, the degree of vacuum advance is given, as follows:

If rpm > $R \gamma$, then with $V_a < V_1 \alpha$, $\theta_v = \bar{K}_7$.

If rpm > $R \gamma$, then with $V_1 \alpha < V_a < V_1 \beta$, $\theta_v = \bar{V}_{A4} + \bar{V}_{A5} + \bar{V}_{A1} + \bar{K}_8$.

If rpm > $R \gamma$, then with $V_a > V_1 \beta$, $\theta_v = \bar{AL}_1 = 0$.

If rpm < $R \gamma$, then $\theta_v = 0$ independent of the value of V_a .

In this way, the degree of spark advance is obtained which meets the required spark advance characteristic of the engine. The output θ_v is the inverted output read out from the operational circuit S_4 through the inverter 3122.

Next, the function generator for computing the additional amount of fuel injection that must be provided for starting and in consideration of the engine speed, will be explained with reference to the block diagram shown in FIG. 32. In this connection, FIG. 33 illustrates a diagram showing the additional fuel supply requirements of the engine for the starting and engine warming up operation, with the abscissa representing the engine temperature and the ordinate representing the ratio of the totals amount Q of fuel injection to the steady state fuel injection quantity q . In FIG. 33, letter ST designates the additional amount of fuel injection required for the engine for starting, T the additional amount of fuel required for the engine warming up operation; T_1 and $T \gamma$ the break points for the starting fuel increment curve; $T \beta$ and $T \alpha$ the break points for the engine warming up fuel increment curve. In FIG. 32, designated as 1130 is the temperature sensor; $I(T \beta)$ and $I(T \alpha)$ discriminators for the engine warming up operation; $I(T)$, $I(T \gamma)$ and $I(T \beta)$ discriminators for the start of the engine; JT a command signal generated from the command signal generator 1180 which will be at H when the computation of temperature increment is to be performed, 1110 the start sensor. Numerals 3131, 3132, 3133, 3134 and 3135 designate inverters; 3136, 3137, 3138, 3139, 3140, 3141 and 3142 NAND elements selected one of which will be in the H state depending on the engine operating conditions as determined by the temperature of the engine and by the fact that the engine is starting or not; T_5 , T_3 and T_2 coders for converting the temperature input code into the corresponding five-place, three-place and two-place codes; K_3 , K_4 , K_5 , K_6 and 1.0 coders for producing the constant codes; J_{T5} , J_{T3} , J_{T2} , J_{K3} , J_{K4} , J_{K5} , J_{K6} and $J_{1.0}$ gate circuits connected to the corresponding coders; S_1 an operational circuit.

In operation, in the same manner as previously explained, a selected one of the NAND elements 3136 through 3142 is caused to produce an L output according to the output of the temperature sensor 1130 and the start sensor 1110. This opens certain designated gate circuits to actuate the corresponding coders to produce their output codes. These output codes are

then added in the operational circuit S_1 and the sum thus obtained is stored in the memory therein. As will be seen from FIG. 33, all what is needed for the computation of the temperature increment is to determine a percentage by which the value of the steady state fuel injection quantity q must be increased, and thus the value obtained from the addition is the value by which the initial value of the steady state fuel injection quantity q is to be multiplied. The code thus obtained opens the corresponding gate circuits and at the same time the value of the previously computed steady state fuel injection quantity q is supplied as the input code, so that the total sum formed represents the total fuel injection quantity Q . This process is explained as in the same manner as the function generators previously mentioned. In this manner, the steady state fuel quantity q is converted into the five-place, four-place, three-place, two-place and single-place binary codes, q_5, q_4, q_3, q_2 and q_1 , respectively shifted to the right by the corresponding number of positions. When the steady state injection quantity q and the stored code of the operational circuit S_1 are made available, the codes q_5 through q_1 are added selectively in accordance with the code of S_1 .

Referring now to FIG. 34, there is shown a block diagram of a function generator for computing the degree of rotational spark advance related to the engine rpm. In FIG. 34, the binary coded output signal rpm of the engine speed sensor RPM is selected into four portions, i.e., $\text{rpm} > R_\alpha$, $R_\beta < \text{rpm} < R_\alpha$, $R_\gamma < \text{rpm} < R_\beta$ and $\text{rpm} < R_1$, by the broken line curve. In the figure, JR is a command signal of the command signal generator 1180 which provides an H signal when the rotational advance is to be computed, $I(R_\alpha)$, $I(R_\beta)$, and $I(R_\gamma)$ discriminators for comparing the output code rpm of the engine speed sensor 7 with the values at points R_α , R_β , and R_γ on the graph of FIG. 5; 3150, 3151 and 3152 inverters; 3153, 3154, 3155 and 3156 NAND elements which produce an H signal depending in which region on the abscissa on the graph of FIG. 5 contains the output code rpm; R_5, R_4, R_3 and R_1 coders for converting the output code rpm into the corresponding codes shifted to the right by appropriate positions; K_9, K_{10}, K_{11} and O coders for establishing the constant codes; J_{R5}, J_{R4}, J_{R3} and J_{R1} gate circuits for the coders R_5, R_4, R_3 and R_1 ; J_{K9}, J_{K10}, J_{K11} and J_O gate circuits for the corresponding constant coders; θ_R the output of the operational circuit.

With the arrangement described above, the process of computation which takes place when $R_\beta < \text{rpm} < R_\alpha$ will be explained by way of example. In this situation, the discriminator $I(R_\alpha)$ produces L output and the discriminator $I(R_\beta)$ an H output, so that only the NAND element 3154 produces an L output to open the gate circuits J_{R3}, J_{R1} and J_{K10} . This causes the coders R_3 and R_1 to convert the output binary code of the engine speed sensor RPM into the right-shifted three-place and single-place codes, respectively, and the coder K_{10} establishes its predetermined constant code. Then, the operational circuit S_4 forms the sum of these codes and the sum thus obtained is stored therein. Consequently, the engine speed spark advance θ_R is obtained. The similar process of computation can take place in exactly the same manner with respect to the remaining regions of the output of the engine speed sensor 7. If $\text{rpm} < R_\gamma$, then the amount of rotational advance is zero and hence the 0 code is established by way of the

NAND element 3156. However, in a practical circuit it is possible to arrange matters so that the 0 code will not be established.

In the foregoing, the gate circuits are provided for the respective coders. However, the result will be the same, if to the contrary the gate codes are applied to the NAND elements which are provided in like number as the regions of the engine speed sensor output. Then, the sum of the rotational advance θ_R and the output representing the spark advance θ_V according to the engine intake manifold vacuum is formed to obtain the total spark advance θ_T required for the engine.

As will be apparent from the foregoing explanation, each time the addition is performed in the course of computing the acceleration increment qA_{cc} , the fuel injection quantity q_V according to the intake manifold vacuum, the steady state injection quantity q , the temperature increment code K , the vacuum spark advance θ_v , the rotational spark advance θ_R and the total spark advance θ_T , the operation of addition is performed according to the similar patterns. The method of performing these separate additions in a consolidated manner which is similar as previously explained in reference to FIG. 10 will be explained later.

Referring now to FIG. 35, there is illustrated an arrangement in which a single coder is employed for the above described several input codes from the engine to establish the converted codes corresponding to the input codes, so that the converted codes are successively delivered to the output at different times according to the inputs. In this way, the previously described several additions of the similar pattern can be performed entirely in a single operational circuit. In FIG. 35, numeral 3161 designates a NAND element for setting up the most significant digit input of the five-place input from the vacuum sensor 1; 3166, 3171, 3176 and 3181 NAND elements for setting up the lower order fourth-place, third-place, second-place and first-place or the lowest order digits of the same five-place input, respectively. Similarly, numerals 3162, 3167, 3172, 3177 and 3182 designate NAND elements for setting up the most significant digit and the fourth-place, third-place, second-place and first-place digits of the acceleration signal a_{cc} from the acceleration sensor 1120. Numerals 3163, 3168, 3173, 3178 and 3183 designate NAND elements for setting up the similar digit positions of the output signal of the temperature sensor 1130; 3164, 3169, 3174, 3179 and 3184 NAND elements for setting up the similar digit positions of the output signal of the engine speed sensor 7; 3165, 3170, 3175, 3180 and 3185 NAND elements for setting up the similar digit positions of the steady state fuel injection quantity q . Designated as V_{a5} is the fifth-place signal from the vacuum sensor V_a ; V_{a4}, V_{a3}, V_{a2} and V_{a1} the similar codes from the vacuum sensor 1 having the digit positions as indicated by their suffixes; $A_{cc5}, A_{cc4}, A_{cc3}, A_{cc2}$ and A_{cc1} the similar codes of the acceleration signal 1120; T_5, T_4, T_3, T_2 and T_1 the similar codes from the temperature sensor 1130; $\text{rpm}_5, \text{rpm}_4, \text{rpm}_3, \text{rpm}_2$ and rpm_1 the similar codes of the output signal from the engine speed sensor 7; D_5 through D_1 the similar codes of the steady state fuel injection quantity. Numeral 3186 designates a NAND element for the most significant digit input codes; 3187, 3188, 3189 and 3190 NAND elements for the fourth-place, third-place, second-place and first-place or the lowest order place digits, respectively. Designated as J_{rv} is a command sig-

nal which provides an H output at the time that the output code of the vacuum sensor 1 is to be converted; J_{acc} , J_T , J_{RPM} and J_D the similar command signals which produce an H output when the acceleration signals A_{cc} , the output signals of the temperature sensor 1130 and the engine temperature sensor 7 and the steady state fuel injection quantity q , respectively, are to be converted. According to the arrangement described herein the five-place input can be converted into the codes including from the five-place code down to the single-place code. By following the similar procedures, the six-place code, the seven-place code and so on can be readily obtained. Numerals 3191 through 3195 designate the fifth-place to first-place NAND elements for setting up the five-place code; Numerals 3197 through 3200 designate NAND elements for setting up the four-place code, 3202 through 3204 NAND elements for setting up the three-place code. Similarly, numerals 3206 through 3207, and 3209, respectively, designate NAND elements for setting up the two-place and signal-place codes, J_5 , J_4 , J_3 , J_2 and J_1 signals for initiating the setting up of the five-place through single-place codes, respectively.

With the arrangement described above, assume that it is the time that the output code of the vacuum sensor 1 is to be converted and that the NAND element 3112 in FIG. 3 is in its established state. Then, the outputs of the NAND elements J_{A5} , J_{A4} and J_{K1} in FIG. 31 are all H's. In this coordinated coder, the NAND elements constituting the gate circuits are no longer used exclusively for any sensors, such as, the vacuum sensor 1 and the engine speed sensor 7, and therefore in this case the gate circuits J_{A5} , J_{A4} and J_{K1} are simply opened or producing an H output, respectively. Particularly, so far as the variable codes are concerned the gate circuits J_{A5} and J_{A4} respectively produce an H output. Now, since the codes related to the intake manifold vacuum are to be set up, $J_{en} = 1$ and then the output of the vacuum sensor V_a are now established in the five NAND elements 3186, 3187, 3188, 3189 and 3190. Since all other signals J_{acc} , J_T , J_{RPM} and J_D are L's, there is no possibility that any other signal input is established in the NAND elements 3186 through 3190. Then, since the input signals J_5 and J_4 are in the H state, the fifth-place signal V_{a5} is introduced at the inputs of the NAND elements 3191 and 3197 thereby producing at the output thereof a code which is the inverse of the fifth-place signal V_{a5} . In like manner, the inverted signal of the fourth-place signal V_{a4} appears at the output of the NAND elements 3192 and 3198, respectively, the inverted signal of the third-place signal V_{a3} at the outputs of the NAND elements 3193 and 3199, the inverted signal of the second-place signal V_{a2} at the outputs of the NAND elements 3194 and 3200, and the inverted signal of the first-place signal V_{a1} at the outputs of the NAND element 3195. The outputs of the remaining NAND elements are all H signals thus establishing no outputs. By this inversion of all the codes, the intended codes are obtainable. This may be readily attained by means of inverters connected in series to these NAND elements or by employing the flip-flop as a memory so that the element whose state is inverted with respect to the input may be read out.

Referring now to FIG. 36, there is illustrated the construction of a circuit for connecting the outputs of the above-mentioned coders to the operational circuit. To avoid any complexity which may arise if the circuits of all the digit positions are explained, the circuit con-

struction will be illustrated for the lowest digit positions only. In FIG. 36, designated as X_5 , X_4 , X_3 , X_2 and X_1 are coders for producing the codes having as many digits as indicated by their suffixes; M_2 , M_3 , M_4 , M_1 and M_5 memories, X, Y, and Z input terminals, and A an adder; 3195, 3204, 3207, 3200 and 3209 the same NAND elements as designated by the reference numerals in FIG. 35; 3122, an OR element; 3213, 3214, 3215, 3216 and 3217 inverters whose inverted outputs represent the desired converted codes; 3218, 3219, 3220, 3221, 3222, 3223, 3224 and 3225 NAND elements which indicate the timing of computations; 3226 and 3227 NAND elements which determine whether the data obtained after the addition should be stored in the memory M_1 or the memory M_5 ; 3228 and 3229 NAND elements for applying the data to the input terminals X and Y, respectively; 3230 a NAND element for connecting the final result of the addition to the output circuit; R_1 through R_8 signals indicating the sequence of computations which are to be performed in the order as indicated by the suffixes. In the first step of the addition where R_1 is in the H state, the codes from the coders X_5 , X_4 and X_1 are coupled to the input terminals X, Y and Z respectively by way of the inverters 3215, 3216, 3217 and the NAND elements 3218 and 3222, and the sum of these codes is applied to the input of the memory M_1 by way of the adder A. Since the code produced in the coder X_1 is a single-place code, no circuit will be connected to the input terminal Z during the succeeding operations on the next least significant position et seq. Next, with R_2 in the H state the memory M_2 storing the output code of the coder X_3 is coupled to the input terminal X by way of NAND elements 3219, and 3228 and the result of the first addition stored in the memory M_1 is connected to the input terminal Y by way of the NAND elements 3219, 3223 and 3229, so that the second addition is performed in the adder A and the result of the addition is then stored in the memory M_5 . In this state, there is no memory available to store the result of the succeeding addition unless one of the previously set memories M_1 and M_5 is reset. Thus, with R_3 in the H state, the memory M_1 is reset to erase its content which is utilized in the second addition and is now useless. Then, with R_4 in the "H" state, the two-place code from the coder X_2 is coupled to the input terminal X and the memory M_5 is coupled to the input terminal Y with the memory M_1 being coupled to the output of the adder A, and a further addition now takes place in the adder A. Thereafter, with R_5 in the "H" the memory M_5 is reset, and with R_6 in the "H" state the memory M_4 storing the constant code is coupled to the input terminal X and the memory M_1 is coupled to the input terminal Y, with the memory M_5 being coupled to the output of the adder A. With the end of this step, the whole operation of the addition is finally completed, and now with R_7 in the H state the output of the memory M_5 storing the final result of the addition is coupled to the output circuit by way of the NAND element 3230. Then, with R_8 representing the eighth step of the addition now in the H state, the whole procedure is over and the contents of all the memories are reset. In fact, the memories M_2 , M_3 and M_4 may be reset earlier in the addition cycle, since these memories are such that they could be reset upon completion of the operations to which these memories are pertinent.

With the operational circuit illustrated in FIG. 36, the addition of any arbitrary code independent of the established codes is only possible by way of the mem-

ory M_4 which stores the constant code from the coder K. This problem is solved by the circuit shown in FIG. 37. In this figure, only those portions which relate to the addition of first-place digits of the respective codes are shown. The component parts designated by the identical reference numerals as used in FIG. 36 will not be explained. While numerals 3213 and 3214 designate the inverters in FIG. 36, the same numerals designate NAND elements in this figure, since these inverters can act as NAND elements by simply adding one more input to each of the inverters. Numerals 3240, 3241 and 3242 designate NAND elements for setting up the most significant digits of the codes qA_{cc} , qA/F and qv ; R_1 designates the time that the computation of the steady state fuel injection quantity $q = qA_{cc} + qA/F + qv$ should be initiated. As already mentioned, the memories M_2 , M_3 and M_4 may be reset as soon as the computations to which they are related are over and thus these memories are reset at R_3 , R_5 and R_7 , respectively, in this figure. At the time that the steady fuel injection quantity q is to be computed, it is only necessary to store the values of qA_{cc} , qA/F and qv in the memories M_2 , M_3 and M_4 in place of the outputs of the coders X_3 , X_2 and K. Accordingly, when the timing signal R'_1 is in the "H" state, the values of qA_{cc} , qA/F and qv are stored in the memories M_2 , M_3 and M_4 by way of the NAND elements 3122; 3214 and 3213 and the addition is performed according to the same procedure as shown in FIG. 36 to thereby attain the desired result. Of course, at this time the signals J_3 , J_2 and J_K are all L's.

Next, referring to FIG. 38 there is shown a part of command signal generator for indicating the timing and sequence of computations to be performed. In this figure, designated as FF_1 , FF_2 and FF_3 are flip-flop circuits which are set upon receipt of clock pulses t_c ; FF_4 , FF_5 and FF_6 flip-flop circuits connected in series with the flip-flops FF_1 , FF_2 and FF_3 ; 3250, 3251 and 3252 inverters; 3253 through 3260 NAND elements which sequentially produce outputs according to the outputs of the flip-flop circuits FF_1 , FF_2 and FF_3 ; 3261 through 3268 inverters; 3270, 3271 and 3272 inverters; 3273 through 3280 NAND elements; 3281 through 3288 inverters; R_1 through R_8 signals adapted to successively assume the H output state in accordance with the output codes of the flip-flops FF_1 , FF_2 and FF_3 , with the inverters 3281 through 3288 similarly successively assuming the H output state so that R_{Acc} , R_{qv} , R_q , R_T , R_q , $R_{\theta R}$, $R_{\theta v}$ and R_θ successively assume the H state. In the first-place, if the flip-flops FF_1 through FF_6 are all in the L state, then the memories are reset altogether. Then, upon arrival of the first clock pulses, since R_{Acc} is in the H state, with R_1 now assuming the H state the output code of the acceleration sensor A_{cc} is converted through the circuit of FIG. 35 so that as shown in FIG. 36 the result of the addition of the five-place, four-place and single-place codes is stored in the memory M_1 by way of the adder A and the other codes are stored in the memories M_2 , M_3 and M_4 ; thereafter the addition procedures are followed as previously described in accordance with the signals R_2 , R_3 , . . . , R_8 . At R_2 through R_8 , these signals have nothing to do with the input codes and thus these signals are simply employed for the purposes of computation. When the flip-flops FF_1 through FF_6 all contain L's, upon completion of the above-mentioned process, the flop-flips are reset to L altogether and as also shown in FIG. 37, all the

memories are cleared to L so that they are available for new inputs.

Referring to FIG. 39, there is illustrated a diagram of another part of command signal generated and showing the relations and connections of the various gate signals with the above-described circuit of FIG. 38 for directing the sequence of computations. In FIG. 39, numerals 3300 through 3307 designate NAND elements for generating gate signals; 3308 through 3315 inverters; 3316 a NAND element for establishing the engine intake manifold vacuum. Assuming that now is the time to compute the additional amount of fuel supply for acceleration, then the acceleration increment signal a_{cc} must be introduced at the input of the corresponding coders. Thus, in FIG. 35 it is necessary that $J_{Acc} = 1$. To attain this, it is designed such that J_{Acc} assumes the H state when each of the outputs R_1 and R_{Acc} change from the L to H signal simultaneously, and, at the same time, all the data of the acceleration increment signal acc are stored. This procedure is entirely applicable to the other inputs. As shown in FIG. 36, the signals R_1 through R_6 have nothing to do with the input signals and they simply control the sequency of computations. Since the codes of the vacuum sensor 1 are employed for computing the fuel injection quantity qv and also for computing the spark advance θ_v according to the engine intake manifold vacuum, the NAND element 3314 generates the signal $J_{\theta v}$. However, since the comparison operation for the spark advance θ_v must be made with entirely different value, the separate signals J_{qv} and $J_{\theta v}$ are generated. On the other hand, the same timing signal R'_1 is employed in the computation of both the steady state fuel injection quantity q and the total spark advance θ_T of the engine as will be explained later. And in this case, the adder operates on the contents of the memories and not on the contents of the coders. This situation is shown in FIG. 37. FIG. 37 is referred to, since it is related to the computation of the steady state fuel injection quantity q and the contents of the memories are the values of qA_{cc} , qv and qA/F .

FIG. 40 illustrates the interconnections between the memories and the adder. In this figure, numerals 3320 through 3325 designate NAND elements for determining the contents of the memories; 3326, 3327 and 3328 NAND elements which function upon receipt of the signals from the NAND elements 3320 through 3325; 3329 through 3334 NAND elements for resetting the contents of the memories; 3336 and 3337 NAND elements; 3338 and 3339 NAND elements for detecting whether the contents of the memories should be inverted; 3340 an inverter; 3341 a NAND element; M_a , M_b and M_c memories. If the computation of the fuel injection quantity q required for an engine is performed without involving any computation of the spark advance for the engine so that the memories store information as needed and they are reset as soon as the relevant computations are over, sharing of the memories is possible. Furthermore, if the air-fuel ratio change signal qA/F is stored in the memory M_c in the course of the computation of the steady state injection quantity q and the memory M_c is utilized in the manner shown in FIG. 37, the memory M_c may be reset when $R_q = R_5 = 1$ so that it is used again at $R_q = R_7 = 1$ during the computation. When computing the vacuum spark advance θ_v , the content of the memory M_a must be inverted and the inverter 3340 is inserted to effect this inversion. While the foregoing explanation has been

made only in respect of the least significant digits, the whole circuit may be connected in exactly the same manner to effect the required addition.

FIG. 41 illustrates the sequence of operations of the whole system on the basis of the description made hereinbefore. Initially, the outputs of the flip-flops FF₄, FF₅ and FF₆ are all Ls and when R₁ = 1, then J_{Acc} = 1 initiating the computation of qA_{cc}. This computational pattern is the same as shown in FIG. 28. Then, the output code of the acceleration sensor 1120 is suitably selected as qA_{cc} on which an addition is performed, and the result of this addition is stored in a memory M_{qA_{cc}}, that is, the memory M_a in FIG. 40. Simultaneously, the air-fuel ratio change signal qA/F is stored in the memory M_c. Next, at J_{qv} = 1, the codes established according to the engine intake manifold are suitably selected and added so that the result of the addition is stored as qv in a memory M_{qv} which is the memory M_b. Then, at the signal J_q, all of the thus stored qA_{cc}, qA/F and qv are introduced into the memories according to the computation pattern shown in FIG. 37 and the addition is performed according to the addition pattern shown in FIG. 36. The result of the addition is restored as q in a memory M_q, i.e., the memory M_c. Then, at J_T = 1, the pattern by which the volume of fuel injection is corrected for the engine temperature is determined. This computational scheme is established as a pattern which determines a percentage by which the steady state fuel injection quantity q is increased, and it is then stored in the memory MT shown in FIG. 32. Consequently, at J_q = 1, the said pattern P is coupled to the gate circuit J_i for the codes, and the previously stored q is established in the various coders according to the pattern in the gate circuit J_i, so that the sum of these codes is formed to determine the total injection quantity Q. The value of this total injection quantity Q is transferred at R_q = R₇ = 1 to the memory 1710 shown in FIG. 27, from which it is coupled to the injection circuit. The output of the vacuum sensor 1 is converted into the codes for the second time. This conversion is determined according to J_{θ_r} in FIG. 31, and the result of the addition is set up as the inverted code of the vacuum spark advance. This value is stored as θ_r in a memory M_{θ_r}, i.e., the memory M_a so that it is inverted as shown in FIG. 40 when it is to be supplied to the output circuit. Then, at R_{θ_r} = 1, the spark advance according to the engine speed is computed and its value is stored in the memory M_b. Thereafter, at R_θ = 1, the sum of the vacuum advance θ_r = M_a and the rotational advance θ_R or the content of the memory M_b is formed to give the total spark advance θ_T which is in turn stored in the memory 1720. At R_θ = R₇ = 1, the total spark advance θ_T is transferred as the output, whereupon all the memories are reset by the second clock pulses.

In the foregoing explanation, the manner in which the memories are reset and the addition procedures are not described in detail. The whole cycle of operations starts at R_{Acc} = R₁ = 1 and ends at R_θ = R₈ = 1 and a new cycle of operations is initiated upon arrival of the succeeding clock pulses.

Embodiment 4:

According to the present embodiment, a system is provided in which a single operational circuit adapted to control the fuel injection system, the ignition system and the like which have direct effects on the performance of an engine, is also employed to perform the

necessary computational operations to control the power and drive systems which are not directly related to the operation of the engine, such as, the automatic transmission with a fluid torque converter, the automatic anti-skid device and the direction indicator. The system of the present embodiment thus contemplates the standardization of the operational circuit employed in vehicles, particularly automotive vehicles to thereby eliminate unnecessary complexity and disadvantages which may arise if a plurality of operational circuits are incorporated.

Referring now to FIG. 42, there is illustrated an arrangement for determining the operating characteristic to control the fluid torque converter automatic transmission installed in an automobile. While the computational operations for the control of this automatic transmission have nothing to do with the control of the fuel injection and the spark advance of the engine as described hereinbefore, the procedures by which the parameters of the various parts of the automobile indicating the conditions of the engine and the automobile are derived as binary code signals and the operating characteristics are then determined utilizing these binary code signals, are all the same. In the system which will be described hereinafter, the same operational circuit as employed for the previously described control of the engine is also utilized for the control of the automatic transmission. In FIG. 42, designated as Φ is a throttle opening sensor for producing a binary code signal φ corresponding to the opening of the engine throttle valve; MAX₁ a coder for producing a reference code in which only the most significant position contains an H and all the remaining lower order positions contain Ls; (AS + B) + 1 a coder for producing a gear shifting code (as + b) + 1; S a sensor for producing a binary code signal corresponding to the vehicle speed or the slip factor between the input and output shafts of the torque converter (in the discussion to follow, this will be referred to as a vehicle speed sensor for producing a binary code signal corresponding to the vehicle speed); C_o a coder; LS₁, LS₂, LS'₂ and LS₃ discriminators for determining whether the binary coded output signal s of the vehicle speed sensor S is greater or smaller than predetermined values; J₁, J₂, J'₂ and J₃ gate circuits which enable the coder C_o to produce codes. Designated as A₇ is an operational circuit which forms the sum of the codes from the coder C_o, and the output binary code (as + b) + 1 of the coder (AS + B) + 1 represents the result of the addition of the codes in the adder A₇; A₁₁ an operational circuit (If the addition in this adder is performed at a time different from that of the operational circuit A₇ which forms the sum of the codes from the coder C_o, both the additions can be performed by the same adder); G₁, G₂ and G₃ gear position signal generators for producing gear position signals corresponding to the conditions in the automatic transmission in the first-speed, second-speed and third-speed, the gear position signal generator including actuators for changing the engagement of the gears into the first-speed, second-speed and third-speed gears upon application of an H signal thereto; H₁, H₂ and H₃ hold circuits for the gear position signal generators G₁, G₂ and G₃; MG a gear shift changing memory for receiving the most significant position signal which is either H or L; 4350 an inverter; 4351, 4352, 4353 and 4354 NAND elements for the gear shifting; 4355, 4356 and 4357 NAND elements for the gear shifting; T₀₁ a

gear shifting signal, i.e., a gearshift timing signal for the gear shifts from the 1st to 2nd speed, the 2nd to 3rd speed and the 3rd to 2nd speed; T_{02} a gearshift timing signal for the gear shift from the second to the first speed; ①, ② and ③ terminals for connection to the inputs of the corresponding NAND elements 4355, 4356 and 4357.

With the arrangement described above, the vehicle speed sensor S for detecting the car speed first produces a binary code signal. In this case, as shown in FIG. 43 (the abscissa = the binary coded output signal s of the vehicle speed sensor S, the ordinate = the binary coded output signal ϕ of the throttle opening sensor Φ), it is prearranged so that the gear position is determined according to the relation between the vehicle speed and the throttle opening. In FIG. 43, a line I designates a gear shift up line from the 1st to 2nd speed; II a gear shift up line from the 2nd to 3rd speed; III a gear shift down line from the 2nd to first speed; IV a gear shift down line from the 3rd to 2nd speed. Now, if the gears are in the first speed and the binary coded output signal of the vehicle sensor S indicates that $s_2 > s$, then the gears are unconditionally retained in the first speed; if $s_2 < s < s_5$, then, in relation with the opening of the engine throttle valve, and depending on whether the condition is located above or below the shift up line I on the graph of FIG. 43, the gears are retained in the first speed if the condition is above the line I, while the upshift to the second speed is effected if the condition is located below the line I. On the other hand, if the binary coded output signal s of the vehicle sensor S indicates that $s > s_5$, then the gears are unconditionally shifted to the second speed. Similarly, the gear positions are determined as shown in Table 1.

Table 1

Gear position before shift	Vehicle speed sensor S output	Gear position after shift
G_1	Binary code s $s < s_2$	G_1
G_1	$s_2 < s < s_5$	Upshift G_1 (above line I), G_2 (below I)
G_1	$s > s_5$	G_2
G_2	$s < s_4$	G_2
G_2	$s_4 < s < s_7$	Upshift G_2 (above line II), G_3 (below II)
G_2	$s > s_7$	G_3
G_2	$s < s_1$	G_1
G_2	$s_1 < s < s_4$	Downshift G_1 (above line III), G_2 (below III)
G_2	$s > s_4$	G_2
G_3	$s < s_3$	G_2
G_3	$s_3 < s < s_6$	Downshift G_2 (above line IV), G_3 (below IV)
G_3	$s > s_6$	G_3

The gear positions as shown in the above table must be obtained in relation with the various values of the binary coded output signal s of the vehicle speed sensor S. Accordingly, upon arrival of the output code s of the vehicle speed sensor S, if the gears are in the first speed position G_1 , the discriminator LS_1 examines whether the condition is located above or below the shift up line I in FIG. 43. Now, if the value of the output binary code s of the vehicle sensor S is smaller than s_2 , the comparison between s and s_2 alone is sufficient to determine that the first speed gear is to be maintained. In like manner, if $s > s_5$, then the upshift to the second speed

is directed by the comparison between s and s_5 alone. All these operations are performed by the discriminator LS_1 . On the other hand, if $s_2 < s < s_5$, the value of s must be converted so that the gear position is determined according to the opening of the throttle valve. When the gear positions indicate the second and third speeds, the discriminators LS_2 , LS'_2 and LS_3 similarly perform the required comparison operations. With the gears in the second speed, however, the gear shift signal produced must be either a 2-3 upshift signal or a 2-1 downshift signal. Therefore, the discriminators LS_2 and LS'_2 perform the comparison operation on these two possibilities.

Next, explanation will be made of the situation in which there is the condition $s_2 < s < s_5$ which the gears in the first speed. Firstly, that portion of the gear shift up line I which corresponds to the condition $s_2 < s < s_5$ can be given as $a_{1s} + b_1$. This is obtainable by performing the characteristic conversion operation on the binary coded output signal s of the vehicle sensor S in the manner as described in relation with the computation of the amount of fuel injection and the amount of spark advance. On the other hand, since no gearshift takes place in the region to the left of the gear shift up line I, the relation between the binary coded output signal ϕ of the throttle opening sensor Φ and the above-mentioned portion $a_{1s} + b_1$ is determined by $\phi - (a_{1s} + b_1) \leq 0$. If $\phi - (a_{1s} + b_1) > 0$, the portion is on the left side of the gear shift up line I and so the first speed gear is maintained. If $\phi - (a_{1s} + b_1) < 0$, the portion is on the right side of the gear shift up line I and in this case the gearshift to the second speed is effected. When $\phi - (a_{1s} + b_1) < 0$, then a negative code is produced. Then, the coder MAX_1 for producing a reference code produces a code max_1 which has more digits than any of the codes ϕ and $(a_{1s} + b_1)$ with the most significant position containing an H and all the lower order positions containing Ls, and now it is possible to compute $max_1 + \phi - (a_{1s} + b_1)$. In this case, if $\phi - (a_{1s} + b_1) < 0$, then the H in the most significant position of the code max_1 changes to L. In this way, the comparison $\phi - (a_{1s} + b_1) \geq 0$ can be performed. In this connection, the computation $\phi - (a_{1s} + b_1)$ requires the provision of a subtractor. To perform this subtraction with an adder, it is only necessary to produce the inverted code $(as + b) + 1$ of the code $a_{1s} + b$ and add this to the code ϕ . This code is then added to the code max_1 so that by examining whether the most significant position of the code max_1 retains H; the comparison $\phi - (as + b) \geq 0$ can be performed. This operation will be explained hereunder.

In operation, the output binary code s of the vehicle speed sensor S is first introduced and it is determined that the gear position is the first speed gear G_1 . Then, as the discriminator LS_1 finds that $s_2 < s < s_5$, the codes produced in the coder C_0 according to the predetermined pattern are added in the operational circuit AI, so that the shift coder $(AS + B) + 1$ produces the code $(a_{1s} + b_1) + 1$. Then, the sum of this value and those of ϕ and max_1 are formed in the operational circuit AII, and only that particular digit position of max_1 into which an H was previously introduced is stored in the memory MG. If the content of the memory MG is L, then it indicates that the comparison $\phi < (a_{1s} + b_1)$ is met and hence the gear shift to the second speed is directed. At this time the gears are still in first, so that the gear position signal generator G_1 is in the H state and

hence the hold circuit H_1 is also in the H state, and moreover the 1 - 2 upshift timing signal T_{01} is also H. Consequently, only the NAND element 4351 produces an L output. Whereupon, the NAND element 4356 produces an H output, thereby changing the gear into second. In this case, if the hold circuit H_2 is allowed to assume the H state upon the upshift to the second speed, a further upshifting into the third speed may result. To prevent this, a preset time delay is provided for each of the hold circuits H_1 , H_2 and H_3 so that when the hold circuit H_1 is in the H state, this H output of the hold circuit H_1 is not permitted to appear at the output of the hold circuit H_2 .

The circuit which introduces such a preset time delay is illustrated in FIG. 44 by way of example. In this figure, designated as g_1 is the output of the gear position signal generator G_1 representing the first speed gear; 4358 a resistor, 4359 a capacitor, 4360 a NAND element; 4361 and inverter; Out H_1 and output terminal. In operation, when the first speed gear signal g_1 is applied to the hold circuit H_1 , the capacitor 4359 is charged by way of the resistor 4358. Eventually, the capacitor 4359 charged up to a level equal to the H level of the NAND element 4360 so that the output of the NAND element 4360 changes from H to L. This L output is then inverted by way of the inverter 4361 to deliver an H output at the output terminal Out H_1 . As compared with the first speed gear signal g_1 , this H output appears after a delay determined by the time constant of the resistor 4358 and the capacitor 4359. By making this delay time larger than the shift commanding time, the desired effect can be attained. As with the upshift from the second speed to the third speed, the upshift from the first speed to the second speed is effected similarly depending upon the result of the comparison operation performed on $\phi - (a_{2s} + b_2) \geq 0$ according to the gear shift up line II. Furthermore, the downshift from the third speed to the second speed takes place when the comparison $\phi - (a_{4s} + b_4) > 0$ is found. In this connection, the result of the comparison operation is reversed in relation to that which is obtained when the 1 - 2 upshift occurs. Consequently, if $s_3 < s < s_6$ in the third speed, then the computation $\phi + \max_1 + (a_{4s} + b_4) + 1$ is performed, and the gearshift command is issued if the stored code of the memory MG is H. This comparison is performed by means of the NAND element 4352, so that when the output of the NAND element 4352 assumes L, the NAND element 4356 produces an H output to thereby effect the downshift to the second speed. Similarly, the downshift from the second to the first speed takes place depending upon the result of the comparison $\phi + (a_{3s} + b_4) \geq 0$ performed according to the shift down line III.

The operation of producing the code $(as + b) + 1$ is made substantially in the same manner as explained with reference to the function generator of preceding embodiments.

Based on the foregoing description, the sequence of the operations as a whole are illustrated in FIG. 45. The operation pattern is the same as explained with reference to FIG. 41 except for the final process. At the final process $J_{T0} = 1$, the computational operation relating to the automatic transmission is initiated. In the first step of the operation, the value of the binary coded output signal s of the vehicle sensor S is examined to determine whether the gear should be shifted unconditionally or left unchanged, or whether the value lies in a re-

gion which necessitates a further computation for its determination. When no further computation is necessary, a command signal is issued to leave the gear unchanged. If any further computation is necessary, the computation $T_o = (as + b) + 1$ is first performed. Then, $GS = \max_1 + T_o + \phi$ is computed. Consequently, the gearshift is directed depending on whether an H is retained in the most significant position of the code $\max_1$ where there previously was an H and depending also on the gear position at this time.

We claim:

1. A control system for an internal combustion engine comprising:

first sensor means for producing a first digital signal responsive to a first parameter of the engine condition,

first discriminating means, connected in circuit with said first sensor for detecting one of a plurality of predetermined first parameter ranges which includes said first parameter as represented by said first digital signal, and producing a number of output signals as determined by said detected first parameter range;

second sensor means for producing a second digital signal responsive to a second parameter of the engine condition,

second discriminating means connected in circuit with said second sensor for detecting one of a plurality of predetermined second parameter ranges which includes said second parameter as represented by said second digital signal, and producing a number of output signals as determined by said second parameter ranges;

shifted code setting circuit means for shifting an input digital code signal applied thereto,

selecting means connected to said first and second discriminating means for selecting an input signal applied thereto in accordance with the output signals of said first and second discriminating means,

first circuit means connected to said first and second sensor means and including said shifted code setting circuit means and said selecting means for producing coded digital signals in codes which are obtained by subjecting said first and second digital signals to shifting and selecting operations by said shifted code setting circuit means and said selecting means in accordance with the output signals of said first and second discriminating means,

second circuit means, connected to said first circuit means and including an adder and a memory, for producing a digital control signal by adding the coded digital signal outputs of said first circuit means;

command signal generating means, connected to said second circuit means, for producing command signals to control a set-reset operation of said memory in the time sharing manner,

third circuit means connected to said second circuit means for producing a drive signal in accordance with said digital control signal of said second circuit means; and

electrically actuating means connected to said third circuit for operating in accordance with the drive signal of said third circuit means.

2. A control system for an internal combustion engine according to claim 1, wherein said first discriminating means comprises a plurality of discriminators

connected to said command signal generating means for determining whether the first digital signal of said first sensor means is greater or smaller than a predetermined value in response to said command signals.

3. A control system for an internal combustion engine according to claim 1, wherein
said selecting means of said first circuit means comprises

a plurality of logical elements connected to said first and second discriminating means and

a plurality of gate means connected to said shifted code setting circuit means of said first circuit means.

4. A control system for an internal combustion engine according to claim 1, wherein

said first and second digital signals of said first and second sensor means are produced in a binary code of a predetermined number of places.

5. A control system for an internal combustion engine according to claim 4, wherein

said shifted code setting circuit means produces digital signals in binary codes which indicate respectively numbers represented by binary codes obtained by shifting said binary code of one of said first digital signal and second digital signal to the right successively by one place each shift.

6. A control system for an internal combustion engine according to claim 1, wherein

said command signal generating means comprises

a clock pulse generator,

a flip-flop circuit connected to said clock pulse generator for dividing the time cycle of the clock pulse of said clock pulse generator, and

logical circuit means connected to said flip-flop circuit.

7. A control system according to claim 1, wherein said third circuit means comprises:

a memory circuit connected in circuit with said second circuit means for retaining said digital control signal of said second circuit means;

an angular sensor for periodically producing pulses in accordance with rotations of the engine

a timing sensor for producing a timing pulse responsive to a predetermined position each cycle of each cylinder;

a counter for counting pulses of said angular sensor transmitted thereto and producing an output digital signal of binary code corresponding to the count

a comparator for producing said drive signal upon coincidence of said digital signal of said memory circuit and that of said counter;

a distributor comprising means responsive to said timing pulse for permitting said pulses of said angular sensor being transmitted therethrough to said counter.

8. A control system for an internal combustion engine according to claim 7, wherein said first parameter sensed by said first sensor means is intake manifold vacuum, said second parameter sensed by said second sensor means is speed of the engine and said electri-

cally actuating means is an ignition system.

9. A control system for an internal combustion engine according to claim 1, wherein

said third circuit means comprises;

a memory circuit connected in circuit with said second circuit means for retaining said digital control signal of said second circuit means;

a clock pulse generator for producing clock pulses with a predetermined frequency;

means for producing a timing pulse which determines the starting of fuel injection during each cycle for each cylinder;

a counter for counting said clock pulses transmitted thereto and producing an output digital signal in a binary code corresponding to the count;

a comparator for producing an output signal for ending the operation of said electrically actuating means under coincidence of the digital signal retained in said memory and that of said counter, and

a distributor including means responsive to said timing pulse for starting and continuing operation of said electrically actuating means and simultaneously permitting said clock pulses being transmitted to said counter from said clock pulse generator to pass therethrough and means responsive to an output signal of said comparator for ending the operation of said electrically actuating means and simultaneously preventing thereafter said clock pulse from being transmitted to said counter.

10. A control system according to claim 9, wherein said first parameter sensed by said first sensor means is intake manifold, said second parameter sensed by said second sensor means is the acceleration of the engine and said electrically actuating means is an electromagnetic valve for injecting fuel into the engine.

11. A control system according to claim 1, wherein said first sensor means comprises vacuum sensor means for producing a signal responsive to the intake manifold vacuum,

said second sensor means comprises speed sensor means for producing a signal responsive to the speed of the engine,

said electrically actuating means comprises an electromagnetic valve for injecting fuel into the engine and an ignition system for producing an ignition spark of the engine, and

said third circuit means comprises injection circuit means having first selector switch means for energizing said electromagnetic valve and ignition circuit means having second selector switch means for energizing said ignition system;

said control system further comprising selection signal generating means connected to said first and second switch means for controlling the transmission of said digital control signal of said second circuit means to said injection circuit means and to said ignition circuit means.

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