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(54) Title: POWER SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SUCH A POWER SEMICONDUCTOR DEVICE

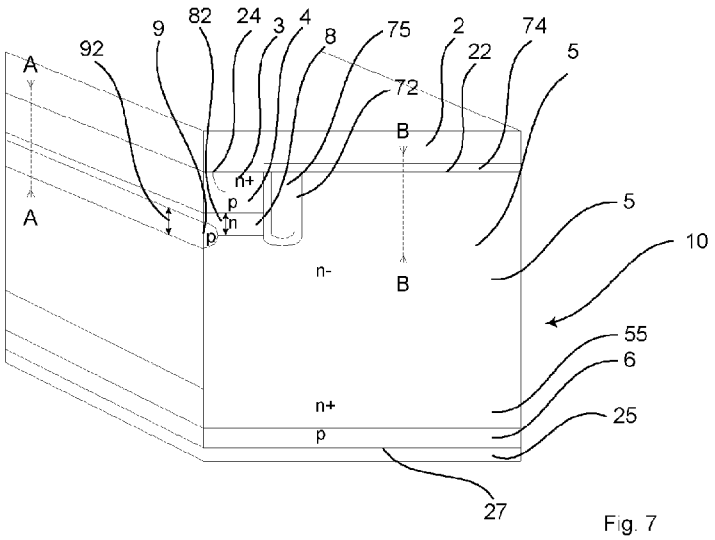

Fig. 7

(57) Abstract: An insulated gate bipolar device (1) is provided having layers of different conductivity types between an emitter electrode (2) on an emitter side (22) and a collector electrode (25) on a collector side (27) in the following order: a source region (3) of a first conductivity type, a base layer (4) of a second conductivity type, which contacts the emitter electrode (2) in a contact area (24), an enhancement layer (8) of the first conductivity type, a floating compensation layer (9) of the second conductivity type having a compensation layer thickness t_p (92), a drift layer (5) of the first conductivity type having lower doping concentration than the enhancement layer (8) and a collector layer (6) of the second conductivity type. The compensation layer (9) is arranged in a projection of the contact area (24) between the enhancement layer (8) and the drift layer (5), such that a channel between the enhancement layer (8) and the drift layer (5) is maintained. The enhancement layer (8) has an enhancement layer thickness tn (82), which is measured in the same plane as the compensation layer thickness (92), and the following rule applies: $N_p t_p = kN_n t_n$, wherein N_n and N_p are the doping concentration of the enhancement layer and compensation layer, respectively; and k is a factor between 0.67 and 1.5.

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Power Semiconductor Device and Method for Manufacturing such a Power Semiconductor Device

Description

Technical Field

The invention relates to the field of power electronics and more particularly to a power semiconductor device according to the preamble of the independent claim 1.

Background Art

In Fig. 1 and 3 a prior art insulated gate bipolar transistor (IGBT) 10 is shown, which comprises an active cell with layers of different conductivity types in the following order between an emitter electrode 2 on an emitter side 22 and a collector electrode 25 on a collector side 27 opposite to the emitter side 22: an (n+) doped source region 3, a p doped base layer 4, which contacts the emitter electrode 25 in a contact area 24, an (n-) doped drift layer 5, an (n+) doped buffer layer 52 and a p doped collector layer 6. A gate electrode is arranged on the emitter side 22. In the Fig.s 1 to 4 an IGBT with planar gate electrode 7 is shown, whereas in Fig. 5 a prior art IGBT is shown, which has a trench gate electrode 75.

Fig. 2, 4 and 5 show an improved prior art IGBT, in which an n doped enhancement layer 8' is arranged between the base layer 4 and the drift layer 5. The enhancement layer 8' has a higher doping concentration than the drift layer 5.

Typical enhancement layer doping concentrations are limited to $1 * 10^{16}$ cm^{-3} in order to prevent excessive electric fields and therefore degradation of the blocking performance.

As the carrier concentration near the active cell is enhanced by such an enhancement layer 8', such IGBTs with an enhancement layer 8' are superior compared to prior art IGBTs having no enhancement layer in view of higher safe operating area (SOA) and low on-state losses.

Fig. 3 shows electrical properties and effects for a prior art IGBT without enhancement layer and Fig. 4 such effects for a prior art device having an enhancement layer 8'. It is shown how an n-type enhancement layer 8' improves the carrier spreading from the cell by creating a barrier and reducing the amount of holes that can reach the cathode (PNP hole drainage effect). This improves the PIN effect, increases the plasma concentration and lowers the on-state losses.

However, the electric field at the n-enhancement / p-base junction 8', 4 also increases. Practical enhancement layer doping concentrations are therefore limited to $1 * 10^{16}$ cm^{-3} to prevent excessive electric fields and therefore degradation of the blocking performance.

US 6 147 381 A shows a prior art IGBT having a planar gate, which comprises a p doped base layer, an (n+) doped enhancement layer below the base layer as well as (n+) doped layers on both sides of the base layer, thus completely surrounding the base layer. A floating p layer is arranged below the enhancement layer. The p floating layer is heavily doped and completely covers the area below the contact area and extends laterally far beyond the contact area.

The floating layer forms a main blocking junction which shields the p base junction from high fields, i.e.to prevent the course of the equipotential lines from reaching as far as the lower edge of the base layer. However, due to the main blocking junction, the charge will only have a restricted access from the channel in terms of spreading.

US 2008/258208 A1 shows an IGBT having a rather complex structure, in which field plates at source potential are arranged below a trench gate. P doped layers are arranged as bubbles below the rounded trench gate bottom. Within such a highly doped p bubble a small highly doped n bubble is arranged. The bubbles are used to improve blocking, or to shield the field since the trench gate rounding results in high peak fields.

As the trench electrode / field plates are terminated within the enhancement layer, the electric field will be even higher due to the higher doping of the enhancement layer compared to an arrangement, in which the trench gate is terminated within the drift layer. The p bubble is needed in the device known from US 2008/258208 A1 to achieve the blocking. Due to the presence of the p bubbles the highly doped enhancement layer can extend further in direction of the drift layer for having lower on resistance.

Disclosure of Invention

It is an object of the invention to provide a power semiconductor device, in which the on-state losses are further reduced compared to prior art devices.

This object is achieved by providing an inventive power semiconductor device which comprises an active cell having layers of different conductivity types in the following order between an emitter electrode on an emitter side and a collector electrode on a collector side opposite to the emitter side:

- a source region of a first conductivity type,
- a base layer of a second conductivity type, which contacts the emitter electrode in a contact area,
- an enhancement layer of the first conductivity type having high doping concentration, which separates the base layer from the drift layer,
- a drift layer of the first conductivity type having lower doping concentration than the enhancement layer,
- a collector layer of the second conductivity type.

A gate electrode is arranged on the emitter side.

A compensation layer of the second conductivity type is arranged between the enhancement layer and the drift layer, which has a compensation layer thickness t_p. The compensation layer thickness is a maximum thickness of the compensation layer in a plane perpendicular to the emitter side. The compensation layer is arranged in a projection of the contact area between the enhancement layer and the drift layer, such that a channel between the enhancement layer and the drift layer is maintained. The compensation layer is restricted to an area inside the projection of the contact area. The compensation layer is floating, i.e. it is not connected to the base layer.

The enhancement layer has an enhancement layer thickness t_{ni}, which is the maximum thickness of the enhancement layer within the projection of the central area.

$$N_p t_p = kN_n t_n$$

wherein N_n is a doping concentration of the enhancement layer;
wherein N_p is the doping concentration of the compensation layer;
k is a factor between 0.67 and 1.5.

The compensation layer is introduced to compensate the doping of the enhancement layer. This allows to increase the doping concentration in the enhancement layer.

In an exemplary embodiment the enhancement layer has a doping concentration higher than 1 * 10^{16} cm^{-3}, in a further exemplary embodiment even higher than 2 * 10^{16} cm^{-3}. This results in a more effective barrier, which blocks the hole flow into the emitter, thereby increasing the plasma concentration and reducing on-state losses.

Due to the inventive compensation layer lower electric fields occur even when very high enhancement layer concentrations are used, which doping concentrations are exemplarily higher than those used in prior art devices.

The compensation layer is not connected to the base layer, i.e. it is a floating layer. That means that the compensation layer does not create a conductive path to the emitter electrode via the base layer, by which path holes would be enabled to reach the emitter electrode. Thereby, the on-state voltage of the device is reduced while keeping the same or even a higher breakdown voltage.

The compensation layer is arranged adjacent to the enhancement layer so that the overall electric field decreases and blocking performance is maintained.

Figure 9 shows how the compensated structure enables to increase the doping concentration of the n-type enhancement layer 8 of an inventive device compared to a prior art enhancement layer 8'. The marked area shows the increase in doping concentration that can be achieved by the doping of the compensation layer. Furthermore, the doping concentration of the compensation layer 9 is shown in the figure.

In Fig. 10 the electric field is shown along a line A – A and B – B respectively for an inventive IGBT according to the Figs. 6 and 7. The electric field for a prior art device of Fig. 5 (line along A' – A') shows that the peak field can be efficiently reduced due to the presence of the compensation layer.

Figure 11 and 12 show the simulated performance improvement in breakdown voltage and on-state losses due to the charge compensated structure. It is shown that for a higher equivalence of the product of doping concentration and thickness of the enhancement layer and compensation layer the effects are improved.

The better the doping concentrations times thickness of the enhancement and compensation layer correspond, the better are the performance improvements. However, even with a structure with a compensation layer the product of doping concentration and thickness are 20 % lower than the theoretical optimum yields significant improvement over a conventional structure.

Brief Description of Drawings

The subject matter of the invention will be explained in more detail in the following text with reference to the attached drawings, in which:

FIG 1 shows a prior art insulated gate semiconductor device having a planar gate electrode;

FIG 2 shows another prior art insulated gate semiconductor device having an enhancement layer and planar gate electrode;

FIG 3 shows electrical effects in a prior art insulated gate semiconductor device according to FIG 1;

FIG 4 shows electrical effects in a prior art insulated gate semiconductor device according to FIG 2;

FIG 5 shows another prior art insulated gate semiconductor device having an enhancement layer and trench gate electrode;

FIG 6 shows an inventive insulated gate semiconductor device having a planar gate electrode;

FIG 7 shows an inventive insulated gate semiconductor device having a trench gate electrode;

FIG 6 shows another embodiment of an inventive insulated gate semiconductor device having a planar gate electrode;

FIG 9 shows doping concentrations of a prior art IGBT and an inventive IGBT;

FIG 10 shows the electrical field of a prior art IGBT and an inventive IGBT;

FIG 11 shows the breakdown voltage of a prior art IGBT and an inventive IGBT; and

FIG 12 shows the on state losses of a prior art IGBT and an inventive IGBT.

The reference symbols used in the figures and their meaning are summarized in the list of reference symbols. Generally, alike or alike-functioning parts are given the same reference symbols. The described embodiments are meant as examples and shall not confine the invention.

Modes for Carrying out the Invention

In Fig. 6 an inventive IGBT 1 is shown having an active cell with layers of different conductivity types in the following order between an emitter electrode 2 on an emitter side 22 and a collector electrode 25 on a collector side 27 opposite to the emitter side 22:

- an (n+) doped source region 3,
- a p doped base layer 4, which contacts the emitter electrode 2 in a contact area 24,
- an n doped enhancement layer 8 having a high doping concentration,
- a p doped compensation layer 9, which has a compensation layer thickness t_p 92, which is a maximum thickness of the compensation layer 9 in a plane perpendicular to the emitter side 22,
- an (n-) doped drift layer 5 having lower doping concentration than the enhancement layer 8,
- a p doped collector layer 6 of the second conductivity type.

The emitter electrode 2 comprises the contact area 24, at which the emitter electrode 2 contacts the base layer 4 and the source region 3. The active semiconductor cell is formed within a wafer, which comprises such layers or parts of such layers, which lie in orthogonal projection with respect to the emitter side 22 of the contact area 24, to which the source region 3 is in contact, said source

region 3, and such part of the base layer 4, at which an electrically conductive channel, through which charge carriers can flow, can be formed. The active cell furthermore comprises in projection to these layers or the described parts of these layers, part of the drift layer 5 and the collector layer 6. The wafer may be made of silicon or GaN or SiC.

The figures 6 to 8 show the right hand part of an inventive semiconductor device, i.e. the whole device comprises additionally another left hand part, which is the result of mirror-imaging of the right-hand part.

In FIG. 6, the device comprises a planar gate electrode 7 design. The planar gate electrode 7 is arranged on top of the emitter side 22 electrically insulated from the base layer 4, the source region 3 and the drift layer 5 by an insulating layer 72. Typically, a further insulating layer 74 is arranged between the planar gate electrode 7 and the emitter electrode 2.

The compensation layer 9 is arranged in a projection of the contact area 24 between the enhancement layer 8 and the drift layer 5, such that a channel between the enhancement layer 8 and the drift layer 5 is maintained. The enhancement layer 8 and the drift layer 5 are thereby directly connected. The compensation layer 9 does not extend into an area outside the projection of the contact area 24. The compensation layer 9 is arranged such that the channel can be formed within the projection of the active cell. The compensation layer 9 on the other hand is floating, i.e. it is not connected to the base layer 4. In an exemplary embodiment, this connection between enhancement layer 8 and drift layer 5 is outside the projected area of the contact area 24.

In an exemplary embodiment, the compensation layer thickness t_p 92 is arranged in the center of the contact area 24. It may be arranged such that the compensation layer 9 does not extend into an area outside the projection of the contact area 24.

The enhancement layer 8 is arranged between and thereby separates the drift layer 5 and the base layer 4. It has an enhancement layer thickness t_n 82, which is measured as the maximum thickness of the enhancement layer within the projection of the contact area 24. The product of the doping concentration N_n and thickness t_n 82 of the enhancement layer corresponds to the product of the doping concentration N_p and thickness t_p 92 of the compensation layer, whereas a difference between these products corresponding to a factor k, wherein k is

between 0.67 and 1.5, is allowed. The doping concentrations are to be understood as maximum doping concentrations of the layers.

$$N_p t_p = kN_n t_n$$

In an exemplary embodiment, the factor k is between 0.8 and 1.2 or between 0.9 and 1.1 or even varying only between 0.95 and 1.05. In the Figs. 11 and 12 it is shown that for a better equivalence of these products the breakdown voltage is further improved and on-state losses are further reduced.

In another exemplary embodiment, the compensation layer thickness 92 is between 0.1 and 10 µm, in particular between 0.5 and 5 µm.

A buffer layer 55 of the first conductivity type having higher doping concentration than the drift layer 5 may be arranged between the drift layer 5 and the collector layer 6.

A maximum doping concentration of the enhancement layer N_n may be as high as at least $1* 10^{16}$ cm^{-3}. In an exemplary embodiment, the maximum doping concentration of the enhancement layer N_n is at least preferably $2* 10^{16}$ cm^{-3}. The maximum doping concentration of the enhancement layer may be up to $1* 10^{17}$ cm^{-3}, so that the doping concentration of the compensation layer may be as high as at least $0.67* 10^{16}$ cm^{-3}, in particular $1.34 * 10^{16}$ cm^{-3} and up to $1.5* 10^{17}$ cm^{-3}.

Typically, the doping concentration of the enhancement layer is lower than of the source region. The doping concentration of the base layer and the compensation layer can be freely chosen due to the application needs and the rules for the doping concentrations given above. For devices above 600 V the doping concentration of the drift layer is typically below $5*10^{14}$ cm^{-3}. The base layer has a doping concentration below $2*10^{18}$ cm^{-3}.

Alternatively to planar gate electrode 7 designs as shown in Fig. 6, the IGBT may comprise trench electrode designs as shown in FIG. 7, in which a trench gate electrode 75 is electrically insulated from the base layer 4, the source region 3 and the drift layer 5 by an insulating layer 72. The trench gate electrode 75 is arranged in the same plane (which plane is arranged parallel to the emitter side 22) and lateral to the base layer 4 and extends deeper into the drift layer 5 than the base layer 4. Typically, a further insulating layer 74 is arranged between the gate electrode 75 and the emitter electrode 2.

The IGBT device may comprise only one active cell as disclosed above, but it is also possible that the device comprises at least two or more such active cells. This results in devices in case of planar gate electrodes similar to the prior art device as shown in Fig. 4, but of course with the addition of the inventive compensation layers 9 in the projection of the contact area 24.

Fig. 8 shows another inventive embodiment, in which the enhancement layer 8 comprises in a first depth a continuous part and in a second depth, which is greater than the first depth, another part, in which the enhancement layer 8 alternates with the compensation layer 9, so that the enhancement layer 8 is comb-shaped with the teeth of the comb directed towards the collector side 27. The first and second depth are measured as distances from the emitter side 22. Typically, the layers alternate in such a direction, which is perpendicular to the direction, in which the source region 3 connects the emitter electrode 2 and the gate electrode 7.

These examples shall not limit the scope of the invention. The above mentioned designs and arrangements are just examples for any kinds of possible designs and arrangements for the base layer(s) and well (zones).

In another embodiment, the conductivity types are switched, i.e. all layers of the first conductivity type are p type (e.g. the drift layer 5, the source region 3) and all layers of the second conductivity type are n type (e.g. base layer 4, the collector layer).

It should be noted that the term “comprising” does not exclude other elements or steps and that the indefinite article “a” or “an” does not exclude the plural. Also elements described in association with different embodiments may be combined. It should also be noted that reference signs in the claims shall not be construed as limiting the scope of the claims.

It will be appreciated by those skilled in the art that the present invention can be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restricted. The scope of the invention is indicated by the appended claims rather than the foregoing description and all changes that come within the meaning and range and equivalence thereof are intended to be embraced therein.

For manufacturing the structure of an incentive IGBT on the emitter side 22, a first mask is applied on the emitter side 22 with an opening, through which particles are applied, e.g. by implantation in order to create the compensation layer 9. Afterwards, another mask is applied, which has a larger opening than the first mask, through which mask the particles for the n doped enhancement layer are applied, afterward the particles for the p doped base layer and then the particles for the source region. Diffusion steps are made to drive the particles into the wafer.

The layers on the collector side 27 of the device and the gate electrode are made by methods well known to experts and finally, after the layers have been created in the wafer, the electrodes 2, 25 are applied as metal layers on the wafer.

Reference List

1	Inventive IGBT
10	Prior art IGBT
2	emitter electrode
22	emitter side
24	contact area
25	collector electrode
27	collector side
3	source region
4	base layer
5	drift layer
55	buffer layer
6	collector layer
7	trench gate electrode
75	planar gate electrode
8	enhancement layer
8'	enhancement layer of a prior art device
82	enhancement layer thickness t_n
9	compensation layer
92	compensation layer thickness t_p

C L A I M S

1. Insulated gate bipolar device (1) with a gate electrode, which device comprises an active cell with layers of different conductivity types in the following order between an emitter electrode (2) on an emitter side (22) and a collector electrode (25) on a collector side (27) opposite to the emitter side (22):
a source region (3) of a first conductivity type,
a base layer (4) of a second conductivity type, which contacts the emitter electrode (2) in a contact area (24),
an enhancement layer (8) of the first conductivity type having high doping concentration,
a drift layer (5) of the first conductivity type having lower doping concentration than the enhancement layer (8),
a collector layer (6) of the second conductivity type,
wherein the gate electrode is arranged on the emitter side (22) and wherein the enhancement layer (8) separates the base layer (4) from the drift layer (5),
characterized in that
a compensation layer (9) of the second conductivity type is arranged between the enhancement layer (8) and the drift layer (5), which has a compensation layer thickness t_p (92), which is a maximum thickness of the compensation layer (9) in a plane perpendicular to the emitter side (22),
in that the compensation layer (9) is arranged in a projection of the contact area (24) between the enhancement layer (8) and the drift layer (5), such that a channel between the enhancement layer (8) and the drift layer (5) is maintained,
in that the compensation layer (9) is not connected to the base layer (4), in that the compensation layer (9) does not extend into an area outside the projection of the contact area (24),
in that the enhancement layer (8) has an enhancement layer thickness t_n (82), which is measured in the same plane as the compensation layer thickness (92),
in that $N_p t_p = kN_n t_n$,
wherein N_n is a doping concentration of the enhancement layer;
wherein N_p is the doping concentration of the compensation layer; and

k is a factor between 0.67 and 1.5.

2. Bipolar device (1) according to claim 1, characterized in that the bipolar device (1) comprises a buffer layer (55) of the first conductivity type having higher doping concentration than the drift layer (5), which buffer layer (55) is arranged between the drift layer (5) and the collector layer (6).
3. Bipolar device (1) according to any of the claims 1 and 2, characterized in that a maximum doping concentration of the enhancement layer (8) is at least $1^* 10^{16}$ cm^{-3}.
4. Bipolar device (1) according to any of the claims 1 and 2, characterized in that a maximum doping concentration of the enhancement layer (8) is at least $2^* 10^{16}$ cm^{-3}.
5. Bipolar device (1) according to any of the claims 1 to 4, characterized in that a maximum doping concentration of the enhancement layer is at maximum up to $1^* 10^{17}$ cm^{-3}.
6. Bipolar device (1) according to any of the claims 1 to 5, characterized in that compensation layer thickness (92) is between 0.1 and 10 µm, in particular between 0.5 and 5 µm.
7. Bipolar device (1) according to any of the claims 1 to 6, characterized in that k is between 0.8 and 1.2.
8. Bipolar device (1) according to any of the claims 1 to 6, characterized in that k is between 0.9 and 1.1.
9. Bipolar device (1) according to any of the claims 1 to 6, characterized in that k is between 0.95 and 1.05.
10. Bipolar device (1) according to any of the claims 1 to 9, characterized in that the gate electrode is one of a trench gate electrode (75) and a planar gate electrode (7).
11. Bipolar device (1) according to any of the claims 1 to 10, characterized in that the compensation layer (9) does not extend into an area outside the projection of the contact area (24).
12. Bipolar device (1) according to any of the claims 1 to 11, characterized in that the bipolar device (1) comprises at least two active cells.
13. Bipolar device (1) according to any of the claims 1 to 12, characterized in that the compensation layer thickness t_p (92) is arranged in the center of the contact area (24).

14. Bipolar device (1) according to any of the claims 1 to 13, characterized in that the bipolar device (1) is made on a basis of a wafer made of silicon or GaN or SiC.

15. Bipolar device (1) according to any of the claims 1 to 14, characterized in that the enhancement layer (8) comprises in a first depth a continuous part and in a second depth, which is greater than the first depth, another part, in which the enhancement layer (8) alternates with the compensation layer (9), and in that the first and second depth are measured from the emitter side (22).

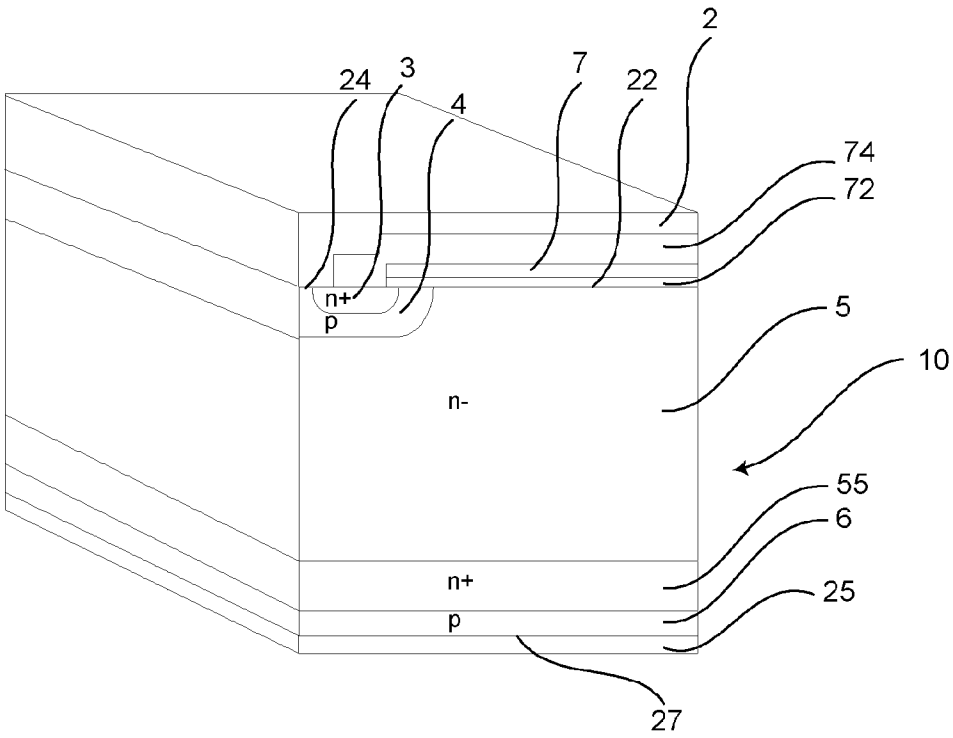


FIG. 1 Prior Art

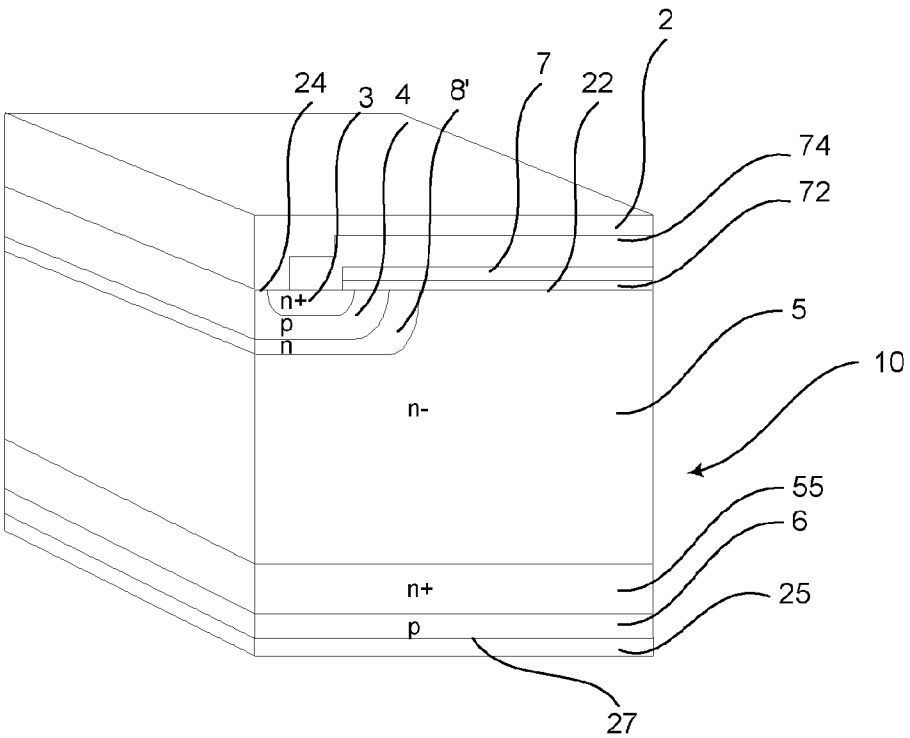


FIG. 2 Prior Art

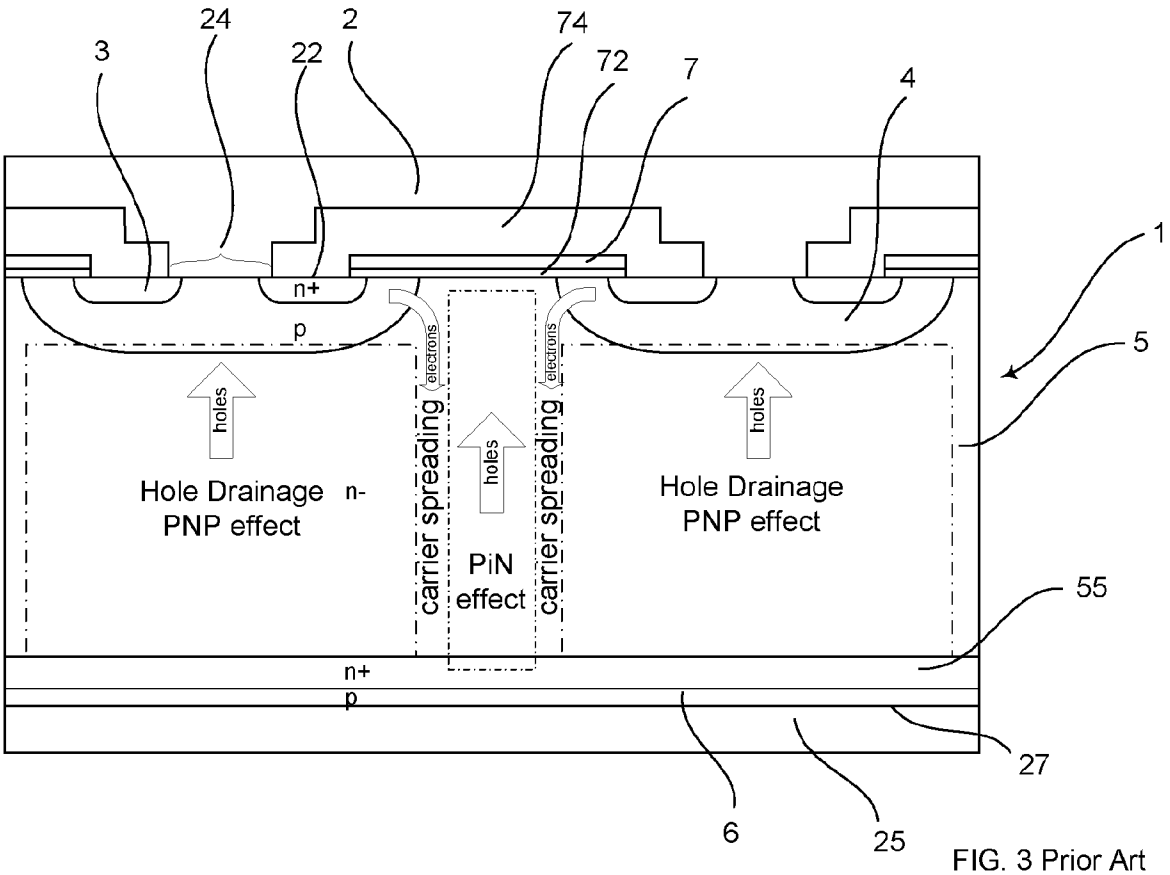


FIG. 3 Prior Art

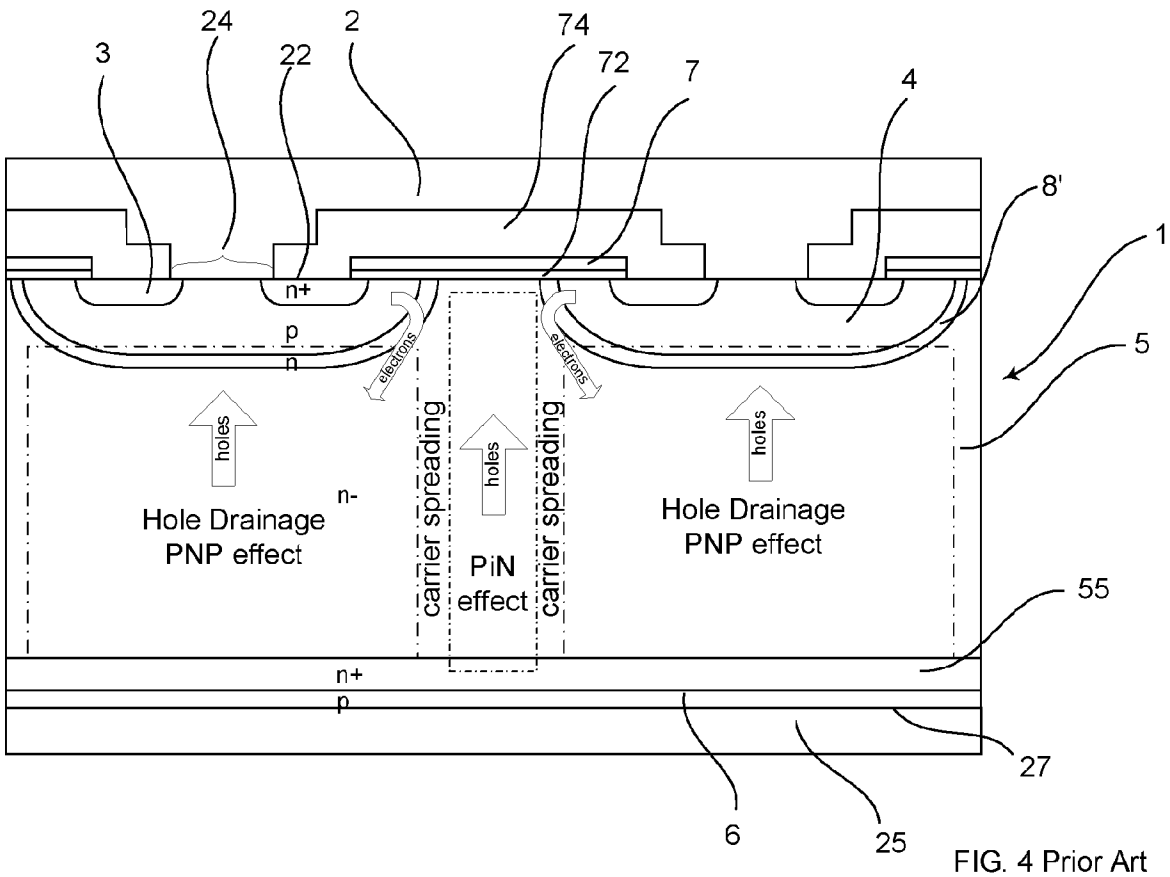


FIG. 4 Prior Art

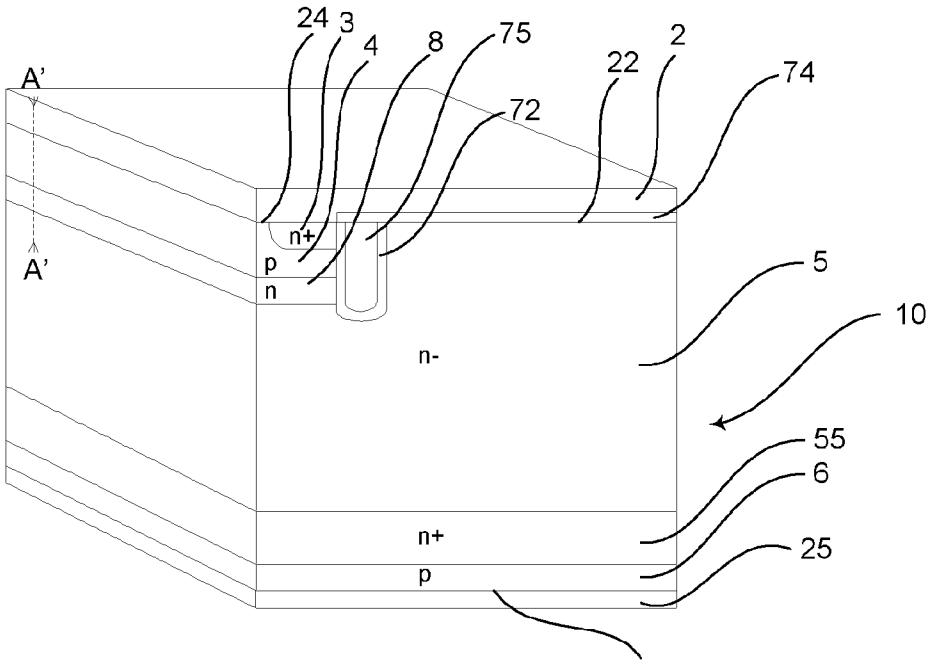


FIG. 5 Prior Art

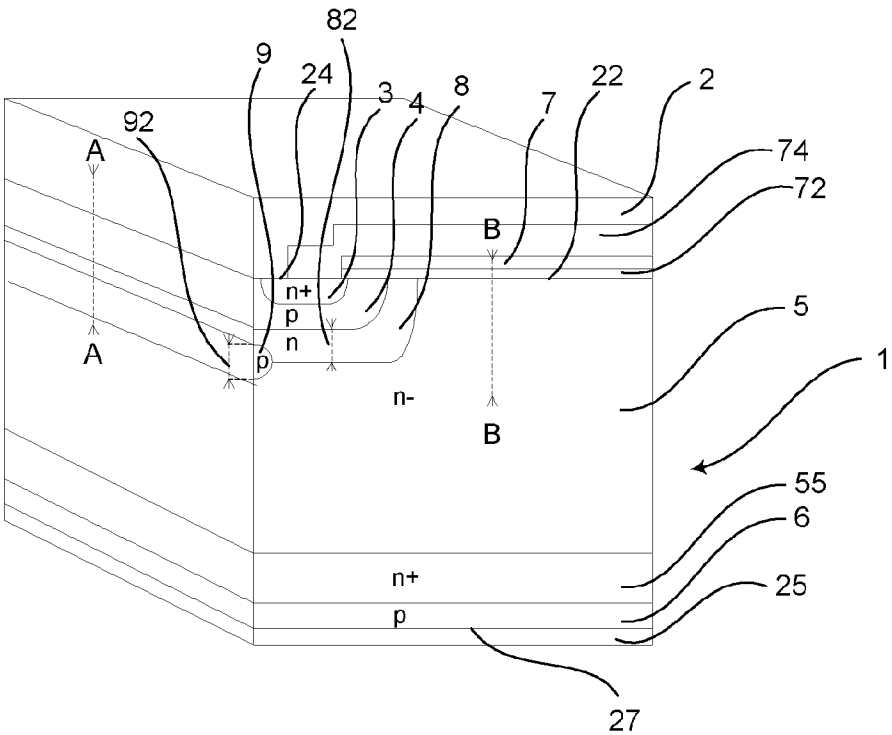
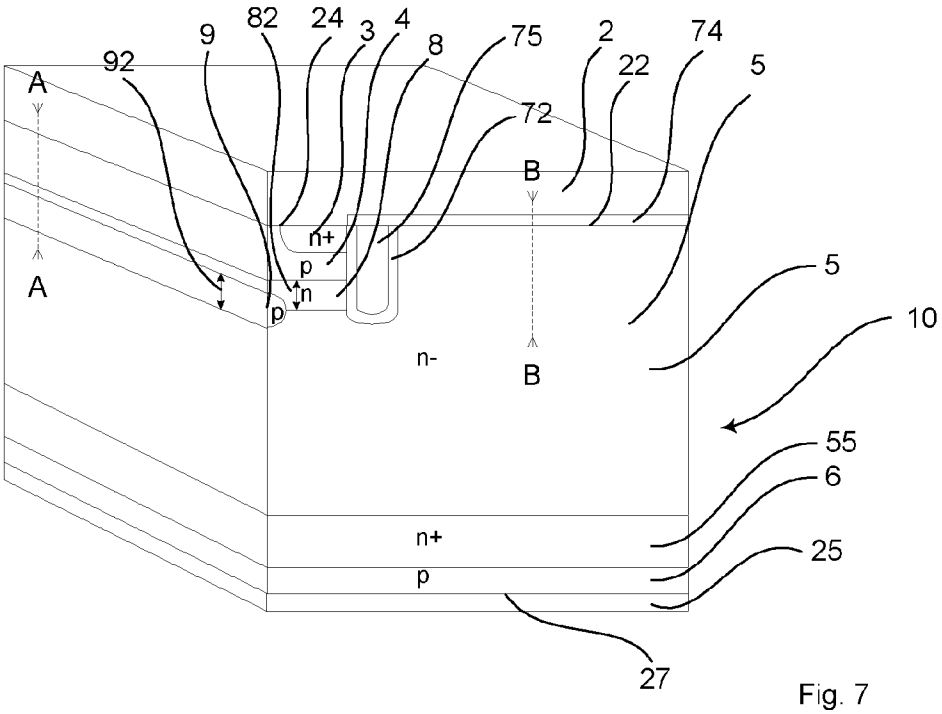


FIG. 6


9
82
24
3
4
8
75
2
74
92
22
5
A
72
B
n+
p
n
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n+
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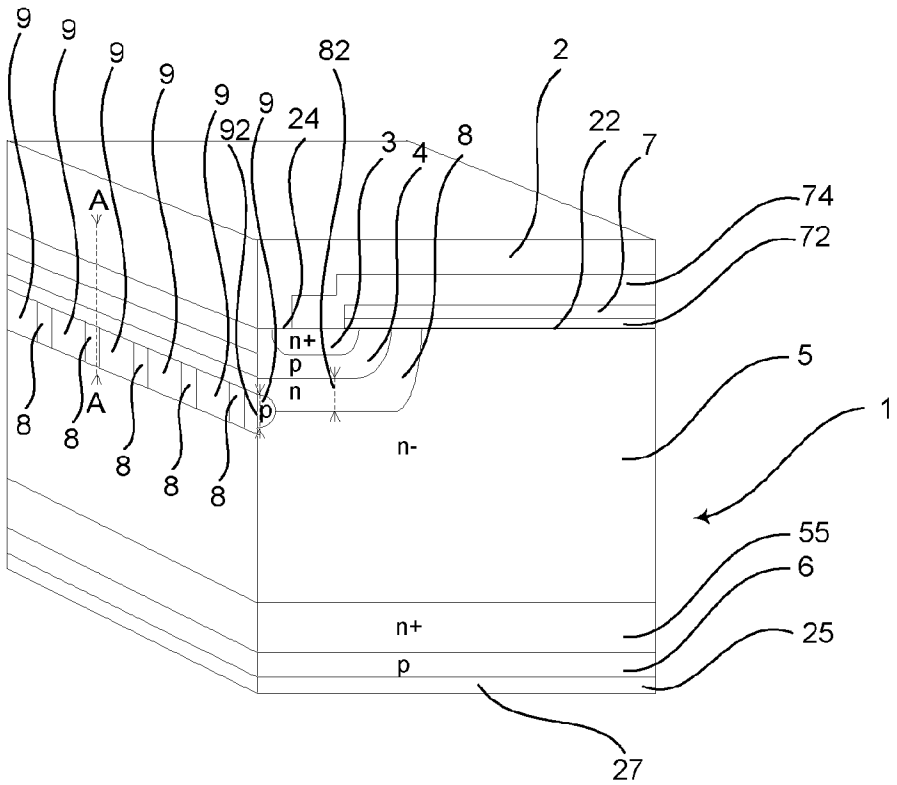
p
27

Fig. 7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92
24
3
4
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7
A
74
72
n+
p
n
5
8
8
A
p
1
n-
8
8
8
55
6
n+
25
p
27

FIG. 8

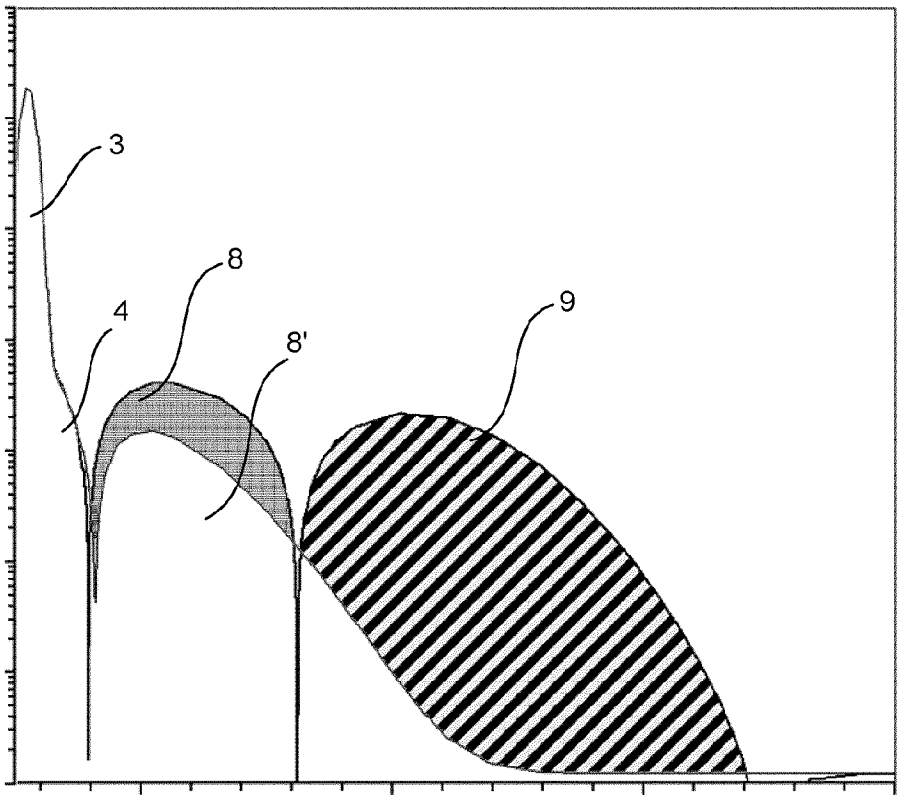

FIG. 9

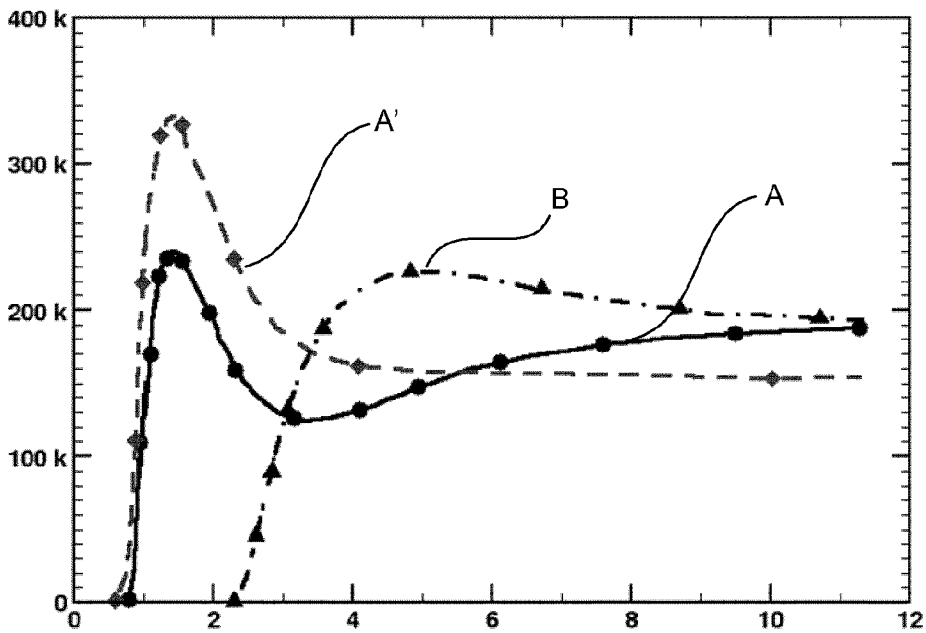

FIG. 10

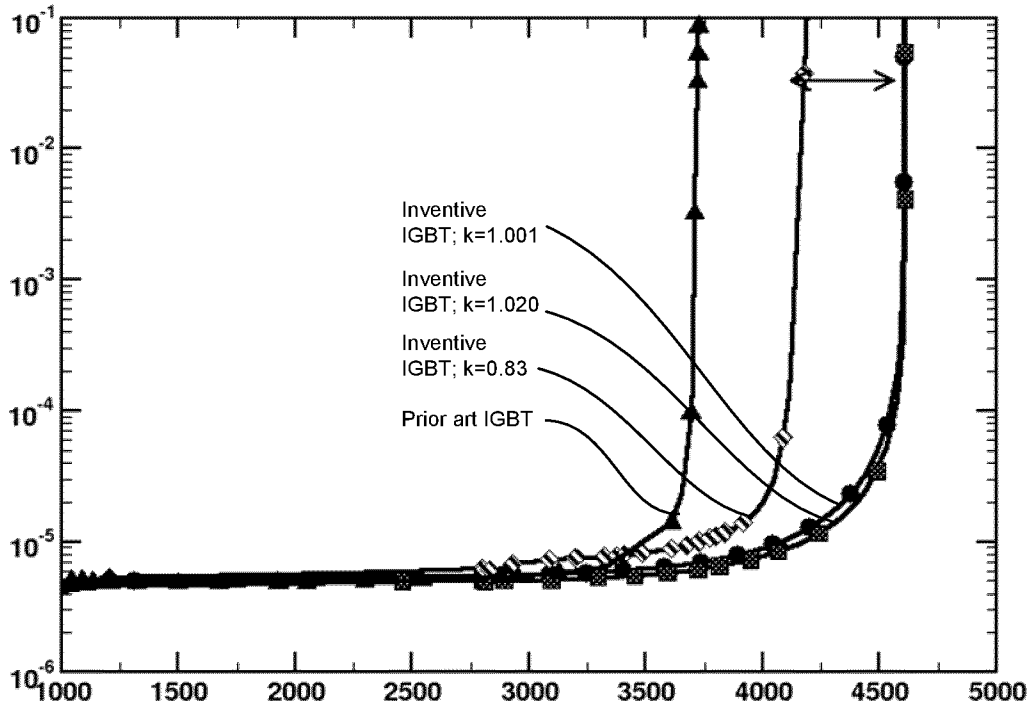
Inventive
IGBT; k=1.001
Inventive
IGBT; k=1.020
Inventive
IGBT; k=0.83
Prior art IGBT
10-1
10-2
10-3
10-4
10-5
10-6
1000
1500
2000
2500
3000
3500
4000
4500
5000

FIG. 11

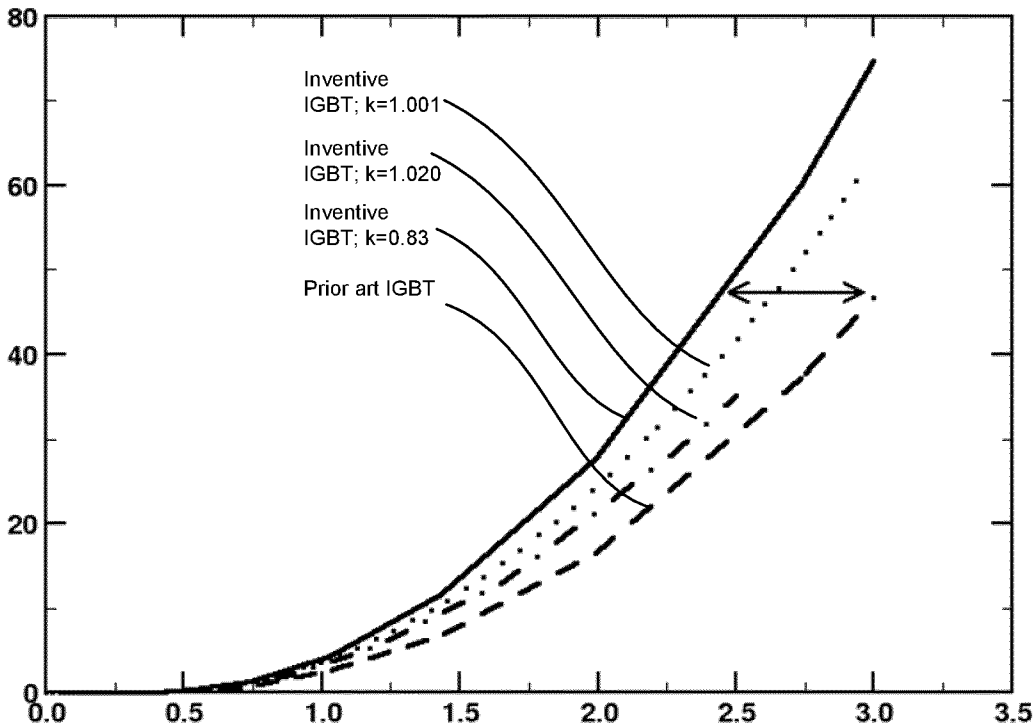
Inventive
IGBT; k=1.001
Inventive
IGBT; k=1.020
Inventive
IGBT; k=0.83
Prior art IGBT
80
60
40
20
0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5

FIG. 12