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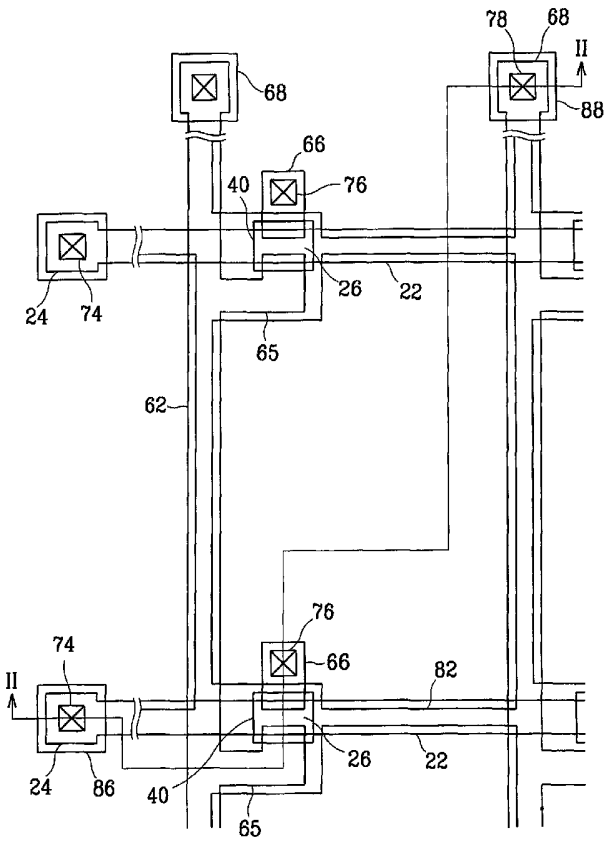

(57) Abstract: A thin film transistor array substrate includes an insulating substrate, a gate line assembly formed on the substrate, and a data line assembly crossing over the gate line assembly while being insulated from the gate line assembly. Thin film transistor are connected to the gate line assembly, and the data line assembly. A passivation layer is formed on the thin film transistors with a-Si:C:O, or a-Si:O:F. The a-Si:C:O or a-Si:O:F-based layer is deposited through PECVD. Pixel electrodes are formed on the passivation layer while being connected to the thin film transistors. In this structure, the problem of parasitic capacitance is solved while enhancing the opening ratio, and reducing the processing time.

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A THIN FILM TRANSISTOR SUBSTRATE OF USING INSULATING LAYERS HAVING LOW DIELECTRIC CONSTANT AND A METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a thin film transistor array substrate with a low dielectric insulating layer, and a method of fabricating the same.

(b) Description of the Related Art

Generally, a thin film transistor array substrate is used as a circuit substrate for independently driving the respective pixels in a liquid crystal display or an organic electroluminescence display. The thin film transistor array substrate has gate lines for carrying scanning signals, data lines for carrying picture signals, thin film transistors connected to the gate and the data lines, pixel electrodes connected to the thin film transistors, a gate insulating layer covering the gate lines, and a passivation layer covering the thin film transistors and the data lines. Each thin film transistor is formed with a gate electrode connected to the gate line, a channel-forming semiconductor layer, a source electrode connected to the data line, a drain electrode, a gate insulating layer, and a passivation layer. The thin film transistor functions as a switching circuit where the picture signal from the data line is transmitted to the pixel electrode in accordance with the scanning signal from the gate line.

Meanwhile, as large-sized high definition liquid crystal displays have

been the choice of electronic consumers, there exists a problem of solving signal deformation due to the increase of various kinds of parasitic capacity. Furthermore, as the liquid crystal displays for notebook computers have involved the decrease in the consumption power and those for TVs have involved improvement in the brightness for increasing the space of visibility, it is required to increase the opening ratio of the liquid crystal displays. In order to increase the opening ratio, it is required to extend the pixel electrodes over the data line assembly such that they are overlapped with the data line assembly. In this case, the parasitic capacity between the pixel electrodes and the data lines is increased. In order to solve the problem of increase in the parasitic capacitance, the vertical spacing between the pixel electrodes and the data lines should be made in a sufficient manner. For this purpose, a passivation layer is usually formed with an organic insulating film. However, the formation of the passivation layer using the organic insulating film involves the following shortcomings. First, the material cost is high particularly in that the amount of material loss is large at the spin coating process. Second, the organic insulating film involves limited thermostability while making the post-processing steps to be restricted by various conditions. Third, the layer formation process based on the organic insulating film involves high frequency of occurrence of impure particles due to the material conglomeration. Fourth, the organic insulating film-based layer involves weak adhesive strength with respect to the neighboring layers. Fifth, when pixel electrodes are formed on the passivation layer, the possibility of etching

error is significantly high.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a thin film transistor array substrate which bears a high opening ratio while not involving the problem of parasitic capacitance.

This and other objects may be achieved through using a CVD layer having dielectric constant 4.0 or less.

According to one aspect of the present invention, the thin film transistor array substrate includes an insulating substrate, a first signal line formed on the insulating substrate, a first insulating layer formed on the first signal line, and a second signal line formed on the first insulating layer while crossing over the first signal line. A thin film transistor is connected to the first and the second signal lines. A second insulating layer is formed on the thin film transistor with a CVD layer having dielectric constant 4.0 or less. The second insulating layer has a first contact hole exposing a predetermined electrode of the thin film transistor. A first pixel electrode is formed on the second insulating layer while being connected to the predetermined electrode of the thin film transistor through the first contact hole.

The first insulating layer has a bottom layer portion based on a CVD layer having dielectric constant 4.0 or less, and a top layer portion based on a silicon nitride layer. The first pixel electrode is formed with an opaque conductive material of light reflection. The second insulating layer has a

pattern of prominence and depression. The thin film transistor array substrate may further include a third insulating layer formed on the first pixel electrode with a CVD layer having dielectric constant 4.0 or less. The third insulating layer has a second contact hole exposing a predetermined portion of the first pixel electrode. A second pixel electrode is formed on the third insulating layer with an opaque conductive material of light reflection while being connected to the predetermined portion of the first pixel electrode through the second contact hole. The first pixel electrode is formed with a transparent conductive material, and the second pixel electrode has a predetermined opening portion capable of passing the light transmitted through the first pixel electrode. The CVD layer having dielectric constant 4.0 or less is formed with a-Si:C:O, or a-Si:C:O. The CVD layer has a dielectric constant of 2-4.

According to another aspect of the present invention, the thin film transistor array substrate includes a data line assembly formed on an insulating substrate, the data line assembly including data lines, color filters of red, green and blue formed on the insulating substrate, and a buffer layer formed on the data line assembly and the color filters with a CVD layer having dielectric constant 4.0 or less. The buffer layer has a first contact hole exposing a predetermined portion of the data line assembly. A gate line assembly is formed on the buffer layer. The gate line assembly includes gate lines crossing over the data lines while defining pixel regions, and gate electrodes connected to the gate lines. A gate insulating layer is

formed on the gate line assembly with a second contact hole partially exposing the first contact hole. A semiconductor pattern is formed on the gate insulating layer over the gate electrodes. A pixel line assembly is further provided at the substrate. The pixel line assembly includes source electrodes connected to the data lines through the first and the second contact holes while partially contacting the semiconductor pattern, drain electrodes facing the source electrodes over the semiconductor pattern, and pixel electrodes connected to the drain electrodes.

The semiconductor pattern has a first amorphous silicon layer with a predetermined band gap, and a second amorphous silicon layer with a band gap lower than the band gap of the first amorphous silicon layer. The thin film transistor array substrate may further include light interception members formed at the same plane as the data lines with the same material as the data lines while being placed corresponding to the semiconductor pattern.

In a method of fabricating the thin film transistor array substrate, a data line assembly including data lines is first formed on an insulating substrate. In the second step, color filters of red, green and blue are formed at the substrate. In the third step, a buffer layer is formed through depositing a CVD layer having dielectric constant 4.0 or less such that the buffer layer covers the data line assembly and the color filters. In the fourth step, a gate line assembly is formed on the insulating layer. The gate line assembly includes gate lines, and gate electrodes. In the fifth step, a gate insulating layer is formed such that the gate insulating layer covers the gate

line assembly. In the sixth step, an island-shaped ohmic contact pattern and an island-shaped semiconductor pattern are formed on the gate insulating layer while forming first contact holes at the gate insulating layer and the buffer layer such that the contact holes partially expose the data lines. In the seventh step, a pixel line assembly is formed such that it includes source and drain electrodes formed on the island-shaped ohmic contact pattern at the same plane while being separated from each other, and pixel electrodes connected to the drain electrodes. In the eighth step, the ohmic contact pattern is divided into two pattern parts through removing the portions of the ohmic contact pattern exposed between the source and the drain electrodes.

In the sixth step, an amorphous silicon layer and an impurities-doped amorphous silicon layer are sequentially deposited onto the gate insulating layer. A photoresist pattern is formed such that the photoresist pattern has a first portion covering a predetermined area of the gate electrode with a predetermined thickness, and a second portion covering the remaining area except for the regions of first contact holes to be formed later with a thickness smaller than the thickness of the first portion. The impurities-doped amorphous silicon layer, the amorphous silicon layer, the gate insulating layer and the buffer layer are etched using the first and second portions of the photoresist pattern as a mask to thereby form the first contact holes. The second portion of the photoresist pattern is then removed. The impurities-doped amorphous silicon layer and the amorphous silicon layer

are etched using the first portion of the photoresist pattern as a mask to thereby form the island-shaped semiconductor pattern and the island-shaped ohmic contact pattern. The first portion of the photoresist pattern is then removed.

According to still another aspect of the present invention, the thin film transistor array substrate for a liquid crystal display includes an insulating substrate, and a gate line assembly formed on the substrate. The gate line assembly has gate lines, gate electrodes, and gate pads. A gate insulating layer is formed on the gate line assembly. The gate insulating layer has contact holes exposing the gate pads. A semiconductor pattern is formed on the gate insulating layer. An ohmic contact pattern is formed on the semiconductor pattern. A data line assembly is formed on the ohmic contact pattern while bearing substantially the same shape as the ohmic contact pattern. The data line assembly has source electrodes, drain electrodes, data lines, and data pads. A passivation pattern is formed on the data line assembly with a CVD layer having dielectric constant 4.0 or less. The passivation pattern has contact holes exposing the gate pads, the data pads, and the drain electrodes. A transparent electrode pattern is electrically connected to the gate pads, the data pads, and the drain electrodes.

The thin film transistor array substrate may further include storage capacitor lines formed at the same plane as the gate line assembly, a storage capacitor semiconductor pattern overlapped with the storage

capacitor lines while being placed at the same plane as the semiconductor pattern, a storage capacitor ohmic contact pattern formed on the storage capacitor semiconductor pattern while bearing the same outline as the storage capacitor semiconductor pattern, and a storage capacitor conductive pattern formed on the storage capacitor ohmic contact pattern while bearing the same outline as the storage capacitor semiconductor pattern. The storage capacitor conductive pattern is partially connected to the transparent electrode pattern.

In a method of fabricating the thin film transistor array substrate, a gate line assembly is first formed with gate lines, gate electrodes connected to the gate lines, and gate pads connected to the gate lines. A gate insulating layer is then formed on the gate line assembly, and a semiconductor layer is formed on the gate insulating layer. A data line assembly is then formed through depositing and patterning a conductive layer. The data line assembly includes data lines crossing over the gate lines, data pads connected to the data lines, source electrodes connected to the data lines while being placed close to the gate electrodes, and drain electrodes facing the source electrodes around the gate electrodes. A passivation layer is formed through depositing a low dielectric CVD. The gate insulating layer is patterned together with the passivation layer to thereby form contact holes exposing the gate pads, the data pads, and the drain electrodes. A transparent conductive layer is deposited, and patterned to thereby form subsidiary gate pads connected to the gate pads, subsidiary

data pads connected to the data pads, and pixel electrodes connected to the drain electrodes.

The formation of the passivation layer is made through PECVD using a gaseous material selected from the group consisting of $SiH(CH_3)_3$, $SiO_2(CH_3)_4$ and $(SiH)_4O_4(CH_3)_4$ as a basic source while introducing an oxide agent of N_2O or O_2. Alternatively, the formation of the passivation layer may be made through PECVD using a gaseous material selected from the group consisting of SiH_4 and SiF_4 as a basic source while adding CF_4 and O_2 thereto.

The data line assembly and the semiconductor layer are formed through photolithography using a photoresist pattern with a first portion bearing a predetermined thickness, a second portion bearing a thickness larger than the thickness of the first portion, and a third portion bearing a thickness smaller than the thickness of the first portion. The first photoresist pattern portion is placed between the source and the drain electrodes, and the second photoresist pattern portion is placed over the data line assembly. The gate insulating layer may be formed through depositing a CVD layer having dielectric constant 4.0 or less in a vacuum state, and depositing a silicon nitride layer also in a vacuum state. The CVD layer has a dielectric constant of 2-4.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes

better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a plan view of a thin film transistor array substrate for a liquid crystal display according to a first preferred embodiment of the present invention;

Fig. 2 is a cross sectional view of the thin film transistor array substrate taken along the II-II' line of Fig. 1;

Figs. 3A, 4A, 5A and 6A sequentially illustrate the steps of fabricating the thin film transistor array substrate shown in Fig. 1;

Fig. 3B is a cross sectional view of the thin film transistor array substrate taken along the IIIb-IIIb' line of Fig. 3A;

Fig. 4B is a cross sectional view of the thin film transistor array substrate taken along the IVb-IVb' line of Fig. 4A;

Fig. 5B is a cross sectional view of the thin film transistor array substrate taken along the Vb-Vb' line of Fig. 5A;

Fig. 6B is a cross sectional view of the thin film transistor array substrate taken along the VIb-VIb' line of Fig. 6A;

Fig. 7 is a plan view of a thin film transistor array substrate for a liquid crystal display according to a second preferred embodiment of the present invention;

Figs. 8 and 9 are cross sectional view of the thin film transistor array substrate taken along the VIII-VIII' line and the IX-IX' line of Fig. 7,

respectively;

Fig. 10A illustrates the first step of fabricating the thin film transistor array substrate shown in Fig. 7;

Figs. 10B and 10C are cross sectional views of the thin film transistor array substrate taken along the Xb-Xb' line and the Xc-Xc' line of Fig. 10A, respectively;

Figs. 11A and 11B illustrate the step of fabricating the thin film transistor array substrate following the step illustrated in Figs. 10B and 10C;

Fig. 12A illustrates the step of fabricating the thin film transistor array substrate following the step illustrated in Fig. 10A;

Figs. 12B and 12C are cross sectional views of the thin film transistor array substrate taken along the XIIb-XIIb' line and the XIIc-XIIc' line of Fig. 12A, respectively;

Figs. 13A to 15B illustrate the steps of fabricating the thin film transistor array substrate following the step illustrated in Fig. 12A;

Figs. 16A and 16B illustrate the step of fabricating the thin film transistor array substrate following the step illustrated in Figs. 15A and 15B;

Fig. 17A illustrate the step of fabricating the thin film transistor array substrate following the step illustrated in Figs. 16A and 16B;

Figs. 17B and 17C are cross sectional views of the thin film transistor array substrate taken along the XVIIb-XVIIb' line and the XVIIc-XVIIc' line of Fig. 17A, respectively;

Fig. 18 is a plan view of a thin film transistor array substrate

according to a third preferred embodiment of the present invention;

Fig. 19 is a cross sectional view of a thin film transistor array substrate taken along the XIX-XIX' line of Fig. 18;

Fig. 20A illustrates the first step of fabricating the thin film transistor array substrate shown in Fig. 18;

Fig. 20B is a cross sectional view of the thin film transistor array substrate taken along the XXb-XXb' line of Fig. 20A;

Fig. 21A illustrates the step of fabricating the thin film transistor array substrate following the step illustrated in Fig. 20A;

Fig. 21B is a cross sectional view of the thin film transistor array substrate taken along the XXIb-XXIb' line of Fig. 21A;

Fig. 22A illustrates the step of fabricating the thin film transistor array substrate following the step illustrated in Fig. 21A;

Fig. 22B is a cross sectional view of the thin film transistor array substrate taken along the XXIIb-XXIIb' line of Fig. 22A;

Fig. 23 illustrates the step of fabricating the thin film transistor array substrate following the step illustrated in Fig. 22A;

Fig. 24A illustrates the step of fabricating the thin film transistor array substrate following the step illustrated in Fig. 23;

Fig. 24B is a cross sectional view of the thin film transistor array substrate taken along the XXIVb-XXIVb' line of Fig. 24A;

Figs. 25 and 26 illustrate the sub-steps of fabricating the thin film transistor array substrate during the steps illustrated in Figs. 23 and 24A;

Fig. 27A illustrates the step of fabricating the thin film transistor array substrate following the step illustrated in Fig. 24A;

Fig. 27B is a cross sectional view of the thin film transistor array substrate taken along the XXVIIb-XXVIIb' line of Fig. 27A;

Fig. 28 is a plan view of a thin film transistor array substrate according to a fourth preferred embodiment of the present invention;

Fig. 29 is a plan view of a thin film transistor array substrate for a reflection type liquid crystal display according to a fifth preferred embodiment of the present invention;

Fig. 30 is a cross sectional view of the thin film transistor array substrate taken along the XXX-XXX' line of Fig. 29;

Figs. 31A, 32A, 33A and 34A sequentially illustrate the steps of fabricating the thin film transistor array substrate shown in Fig. 29;

Fig. 31B is a cross sectional view of the thin film transistor array substrate taken along the XXXIb-XXXIb' line of Fig. 31A;

Fig. 32B is a cross sectional view of the thin film transistor array substrate taken along the XXXIIb-XXXIIb' line of Fig. 32A;

Fig. 33B is a cross sectional view of the thin film transistor array substrate taken along the XXXIIIb-XXXIIIb' line of Fig. 33A;

Fig. 34B is a cross sectional view of the thin film transistor array substrate taken along the XXXIVb-XXXIVb' line of Fig. 34A;

Fig. 35 is a plan view of a thin film transistor array substrate for a semi-transparent liquid crystal display according to a sixth preferred

embodiment of the present invention;

Fig. 36 is a cross sectional view of the thin film transistor array substrate taken along the XXXVI-XXXVI' line of Fig. 35;

Figs. 37A, 38A and 39A sequentially illustrate the steps of fabricating the thin film transistor array substrate shown in Fig. 35;

Fig. 37B is a cross sectional view of the thin film transistor array substrate taken along the XXXVIIb-XXXVIIb' line of Fig. 37A;

Fig. 38B is a cross sectional view of the thin film transistor array substrate taken along the XXXVIIIb-XXXVIIIb' line of Fig. 38A;

Fig. 39B is a cross sectional view of the thin film transistor array substrate taken along the XXXIXb-XXXIXb' line of Fig. 39A; and

Fig. 40 is a cross sectional view of a thin film transistor array substrate according to a seventh preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

Fig. 1 is a plan view of a thin film transistor array substrate for a liquid crystal display according to a first preferred embodiment of the present invention, and Fig. 2 is a cross sectional view of the thin film transistor array substrate taken along the II-II line of Fig. 1.

A gate line assembly is formed on an insulating substrate 10 with a double-layered structure. The gate line assembly has a first layer 221, 241

and 261 formed with chrome Cr alloy or molybdenum Mo alloy, and a second layer 222, 242 and 262 formed with aluminum Al or silver Ag alloy. The gate line assembly includes gate lines 22 proceeding in the horizontal direction, gate pads 24 connected to the gate lines 22 to receive gate signals from the outside and transmit them to the gate lines 22, and gate electrodes 26 connected to the gate lines 22 to function as parts of thin film transistors.

A gate insulating layer 30 is formed on the substrate 10 with silicon nitride SiNx such that it covers the gate line assembly.

A semiconductor layer 40 is formed on the gate insulating layer 30 over the gate electrodes 24 with amorphous silicon while bearing the shape of island. An ohmic contact layer 54 and 56 is formed on the semiconductor layer 40 with silicide, or n^+ hydrogenated amorphous silicon where n-type impurities are doped at high concentration.

A data line assembly is formed on the ohmic contact layer 54 and 56 and the gate insulating layer 30 with a double-layered structure. The data line assembly has a first layer 621, 651, 661 and 681 formed with Cr alloy or Mo alloy, and a second layer 622, 652, 662 and 682 formed with Al alloy or Ag alloy. The data line assembly includes data lines 62 proceeding in the vertical direction, source electrodes branched from the data lines 62 while being extended over the one-sided portion 54 of the ohmic contact layer, data pads 68 connected to the one-sided ends of the data lines 62 to receive picture signals from the outside, and drain electrodes 66 separated from the source electrodes 65 around the gate electrodes 26 while being placed on

the other-sided portion 56 of the ohmic contact layer. The data lines 62 cross over the gate lines 22 while defining pixel regions.

A passivation layer 70 is formed on the data line assembly and the semiconductor layer 40 through depositing a layer of a-Si:C:O or a-Si:O:F (a low dielectric CVD film) by way of plasma enhanced chemical vapor deposition (PECVD). The a-Si:C:O or a-Si:O:F-based layer bears a dielectric constant of 4 or less (the dieletric constant being ranged from 2 to 4). Therefore, the passivation layer 70 does not involve the problem of parasitic capacitance even if it bears a thin thickness. Furthermore, the passivation layer 70 involves good adhesion characteristic and step coverage characteristic in relation to other layers. As the passivation layer 70 is based on a low dielectric CVD film, it bears excellent thermostabiliy compared to that based on an organic insulating film. In addition, the a-Si:C:O or a-Si:O:F-based layer deposited through PECVD exhibits an advantage in the processing time as the deposition speed or etching speed related thereto is rapid by four to ten times compared to that related to a silicon nitride-based layer.

The passivation layer 70 has contact holes 76 and 78 exposing the drain electrodes 66 and the data pads 68, and contact holes 74 exposing the gate pads 24 together with the gate insulating layer 30. The contact holes 74 and 78 exposing the pads 24 and 68 may be formed with various shapes, for example, with an angled shape, or a circular shape. The area of the contact holes 74 and 78 may be established to be 2mmx60 ㎛ or less,

preferably to be in the range of 0.5mmx15 ㎛-2mmx60 ㎛.

Pixel electrodes 82 are formed on the passivation layer 70 at the pixel regions while being electrically connected to the drain electrodes 66 through the contact holes 76. Furthermore, subsidiary gate and data pads 86 and 88 are formed on the passivation layer 70 while being connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78. The pixel electrodes 82 and the subsidiary gate and data pads 86 and 88 are formed with indium tin oxide (ITO) or indium zinc oxide (IZO).

As shown in Figs. 1 and 2, the pixel electrodes 82 are overlapped with the gate lines 22 to form storage capacitors. In case the storage capacity is short of the required amount, a storage capacitor line assembly may be additionally formed at the same plane as the gate line assembly.

The pixel electrodes 82 are overlapped with the data lines 62 while optimizing the opening ratios. Even with the overlapping of the pixel electrodes 82 and the data lines 62, as the passivation layer 70 bears a low dielectric property, the parasitic capacitance between the pixel electrodes 82 and the data lines 62 is extremely small.

A method of fabricating the thin film transistor array substrate will be now explained with reference to Fig. 3A to 7B.

As shown in Figs. 3A and 3B, a Cr alloy or Mo alloy-based layer is deposited onto the substrate 10 to form a first layer 221, 241 and 261 for a gate line assembly, and a Al alloy or Ag alloy-based layer is formed onto the first layer to form a second layer 222, 242 and 262 for the gate line assembly.

The first and second layers are patterned to thereby form a gate line assembly proceeding in the horizontal direction. The gate line assembly includes gate lines 22, gate electrodes 26, and gate pads 24.

In case the first layer 221, 241 and 261 is formed with a Mo alloy and the second layer 222, 242 and 262 with an Ag alloy, the two layers are all etched with an Ag alloy etching materials where phosphoric acid, nitric acid, acetic acid and deionized water are mixed together. Therefore, the double-layered gate line assembly can be formed through only one etching process. As the etching ratio of the Ag alloy by way of a mixture of phosphoric acid, nitric acid, acetic acid and deionized water is greater than that of the Mo alloy, a tapering angle of about 30° required for the gate line assembly can be obtained.

Thereafter, as shown in Figs. 4A and 4B, a silicon nitride-based gate insulating layer 30, an amorphous silicon-based semiconductor layer 40 and a doped amorphous silicon-based layer 50 are sequentially deposited onto the substrate 10. The semiconductor layer 40 and the doped amorphous silicon-based layer 50 are etched through photolithography to thereby form an island-shaped semiconductor layer 40 and an ohmic contact layer 50 on the gate insulating layer 30 over the gate electrode 24.

As shown in Figs. 5A and 5B, a Cr alloy or Mo alloy-based layer is deposited onto the substrate 10 to form a first layer 651, 661 and 681 for a data line assembly, and an Al alloy or Ag alloy-based layer is formed onto the first layer to form a second layer 652, 662 and 682 for the data line assembly.

The first and second layers are patterned through photolithography to thereby form a data line assembly. The data line assembly includes data lines 62 proceeding in the vertical direction while crossing over the gate lines 22, source electrodes 65 branched from the data lines 62 while being extended over the gate electrodes 26, data pads 68 connected to the one-sided ends of the data lines 62 to receive picture signals from the outside, and drain electrodes 66 separated from the source electrodes 65 around the gate electrodes 26 while facing them.

The doped amorphous silicon-based layer 50 exposed through the data line assembly is then etched, and divided into two portions 55 and 56 around the gate electrode 26 while exposing the semiconductor layer 40. It is preferable that oxygen plasma is made with respect to the exposed portion of the semiconductor layer 40 to stabilize the surface thereof.

As shown in Figs. 6A and 6B, an a-Si:C:O or a-Si:O:F-based layer is grown through chemical vapor deposition (CVD) to thereby form a passivation layer 70. In the case of the a-Si:C:O-based layer, the deposition thereof is made using a gaseous material such as $SiH(CH_3)_3$, $SiO_2(CH_3)_4$, $(SiH)_4O_4(CH_3)_4$ and $Si(C_2H_5O)_4$ as a basic source while introducing a mixture of an oxide agent such as N_2O or O_2, and Ar or He. In the case of the a-Si:O:F-based layer, the deposition thereof is made while introducing a mixture of SiH_4 or SiF_4 with O_2. In this case, CF_4 may be added thereto as a subsidiary source for fluorine.

Thereafter, the passivation layer 70 is patterned together with the

gate insulating layer 30 to thereby form contact holes 74, 76 and 78 exposing the gate pads 24, the drain electrodes 66 and the data pads 68. The contact holes 74, 76 and 78 may be formed with an angled or circular shape. The area of the contact holes 74 and 78 exposing the pads 24 and 68 is established to be 2mmx60 ㎛ or less, preferably to be in the range of 0.5mmx15 ㎛-2mmx60 ㎛.

Finally, as shown in Figs. 1 and 2, an ITO or IZO-based layer is deposited, and etched through photolithography to thereby form pixel electrodes 82, and subsidiary gate and data pads 86 and 88. The pixel electrodes 82 are connected to the drain electrodes 66 through the first contact holes 76. The subsidiary gate and data pads 86 and 88 are connected to the gate and data pads 24 and 68 through the second and third contact holes 74 and 78. Nitrogen is preferably used as a gas for the pre-heating process before the formation of the ITO or IZO-based layer. This is to prevent a metallic oxide layer from being formed on the metallic layers 24, 66 and 68 exposed through the contact holes 74, 76 and 78.

As described above, the passivation layer 70 is formed through depositing a low dielectric CVD layer based on a-Si:C:O or a-Si:O:F by way of PECVD. In this way, the problem of parasitic capacitance can be solved while optimizing the opening ratio. Furthermore, the speed of deposition and etching becomes rapid while reducing the processing time.

Fig. 7 is a plan view of a thin film transistor array substrate for a liquid crystal display according to a second preferred embodiment of the present

invention, and Figs. 8 and 9 are cross sectional views of the thin film transistor array substrate taken along the VIII-VIII' line and the IX-IX' line of Fig. 7.

A gate line assembly is formed on an insulating substrate 10 with a double-layered structure. The gate line assembly has a first layer 221, 241 and 261 formed with Cr alloy or Mo alloy, and a second layer 222, 242 and 262 formed with Al alloy or Ag alloy. The gate line assembly includes gate lines 22, gate pads 24, and gate electrodes 26.

Storage capacitor lines 28 are formed on the substrate 10 while proceeding parallel to the gate lines 22. The storage capacitor lines 28 also have a first layer 281, and a second layer 282. The storage capacitor lines 28 are overlapped with storage capacitor conductive patterns 68 connected to pixel electrodes 82 to thereby form storage capacitors for improving the pixel electric potential storage capacity. In case the storage capacity accruing to the overlapping of the pixel electrodes 82 and the gate lines 22 is sufficiently enough, the storage capacitor lines 28 may be omitted. A common electrode voltage is usually applied to the storage capacitor lines 28.

A gate insulating layer 30 is formed on the gate line assembly and the storage capacitor lines 28 with silicon nitride SiNx while covering the gate line assembly.

Semiconductor patterns 42 and 48 are formed on the gate insulating layer 30 with hydrogenated amorphous silicon. First to third ohmic contact patterns 55, 56 and 58 are formed on the semiconductor patterns 42 and 48

with amorphous silicon where n-type impurities such as phosphorous P are doped at high concentration.

A data line assembly is formed on the first to third ohmic contact patterns 55, 56 and 58 with Cr alloy or Mo alloy with a double-layered structure. The data line assembly has a first layer 621, 641, 651, 661 and 681, and a second layer 622, 642, 652, 662 and 682. The data line assembly includes data lines 62 proceeding in the vertical direction, data pads 68 connected to the one-sided ends of the data lines 62 to receive picture signals from the outside, and source electrodes 65 branched form the data lines 62. The data line assembly further includes drain electrodes 66 separated from the source electrodes 65 around the gate electrodes 26 or the channel portions C, and storage capacitor conductive patterns 64 placed over the storage capacitor lines 28. In case the storage capacitor lines 28 are absent, the storage capacitor conductive patterns 64 are also omitted.

The data lines assembly may be formed with a single-layered structure bearing an Al or Ag-based layer.

The first to third ohmic contact patterns 55, 56 and 58 lower the contact resistance between the underlying semiconductor patterns 42 and 48 and the overlying data line assembly while bearing the same outline as the data line assembly. That is, the first ohmic contact patterns 55 have the same shape as the data lines 62, the data pads 68, and the source electrodes 65. The second ohmic contact patterns 56 have the same shape as the drain electrodes 66. The third ohmic contact patterns 58 have the

same shape as the storage capacitor conductive patterns 64.

Meanwhile, the semiconductor patterns 42 and 48 have the same shape as the data line assembly and the ohmic contact patterns 55, 56 and 58 except for the channel portions C. Specifically, the storage capacitor semiconductor patterns 48 have the same shape as the storage capacitor conductive patterns 64 and the third ohmic contact patterns 58, but the thin film transistor semiconductor patterns 42 are slightly differentiated from the relevant components of the data line assembly and the ohmic contact patterns. That is, the source and the drain electrodes 65 and 66 are separated from each other at the channel portions C, and the first and the second ohmic contact patterns 55 and 56 are also separated from each other at those portions. However, the thin film transistor semiconductor patterns 42 continuously proceed at those portions to thereby form channels for the thin film transistors.

A passivation layer 70 is formed on the data line assembly with a low dielectric CVD layer based on a-Si:C:O or a-Si:O:F by way of plasma enhanced chemical vapor deposition PECVD. As the low dielectric CVD layer bears a dielectric contact of 4 or less, the problem of parasitic capacitance is not present even if the thickness of the CVD layer is thin. Furthermore, such a layer bears good contact characteristic and good step coverage characteristic in relation to other layers. Furthermore, as it is a low dielectric CVD layer, the thermostability thereof is excellent compared to an organic insulating layer. In addition, the speed of deposition and etching

is rapid by four to ten times compared to that of a silicon nitride-based layer while reducing the processing time.

The passivation layer 70 has contact holes 76, 78 and 72 exposing the drain electrodes 66, the data pads 68, and the storage capacitor conductive patterns 64. Furthermore, the passivation layer 70 has contact holes 74 exposing the gate pads 24 together with the gate insulating layer 30.

Pixel electrodes 82 are formed on the passivation layer 70 to receive picture signals from the thin film transistors while generating electric fields together with a common electrode of a color filter substrate. The pixel electrodes 82 are formed with a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO). The pixel electrodes 82 are physico-electrically connected to the drain electrodes 66 to receive picture signals from them. The pixel electrodes 82 are overlapped with the neighboring gate and data lines 22 and 62 to enhance the opening ratio. The overlapping may be omitted. The pixel electrodes 82 are connected to the storage capacitor conductive patterns 64 through the contact holes 72 to transmit picture signals thereto. Meanwhile, subsidiary gate and data pads 86 and 88 are connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78. The subsidiary gate and data pads 86 and 88 serve to enhance the adhesive relation between the pads 24 and 68 and external circuits and to protect the pads, but may be selectively introduced.

A method of fabricating the thin film transistor array substrate using four masks will be now explained with reference to Figs. 10A to 17C.

As shown in Figs. 10A to 10C, a Cr alloy or Mo alloy-based layer is deposited onto the substrate 10 to form a first layer 221, 241, 261 and 281 for a gate line assembly, and an Al alloy or Ag alloy-based layer is formed onto the first layer to form a second layer 222, 242, 262 and 282 for the gate line assembly. The first and second layers are patterned photolithography to thereby form a gate line assembly, and storage capacitor lines 28. The gate line assembly includes gate lines 22, gate pads 24, and gate electrodes 26.

Thereafter, as shown in Figs. 11A and 11B, a gate insulating layer 30, a semiconductor layer 40 and an ohmic contact layer 50 are sequentially deposited onto the substrate 10 through chemical vapor deposition such that they bear a thickness of 1500-5000Å, 500-2000 Å, and 300-600 Å, respectively. A Cr alloy or Mo alloy-based first conductive layer 601 and an Al alloy or Ag alloy-based second conductive layer 602 are deposited onto the ohmic contact layer 50 through sputtering to thereby form a conductive layer 60. A photoresist film 110 is then coated onto the conductive layer 60 by a thickness of 1-2 ㎛.

As shown in Figs. 12B and 12C, the photoresist film 110 is exposed to light through a mask, and developed to thereby form a photoresist pattern. The photoresist pattern has a first portion 114 to be placed at the channel area C between the source and the drain electrodes 65 and 66, and a second portion 112 to be placed at the data line assembly area A. The first portion 114 has a thickness smaller than the second portion 112. The

remaining portion B of the photoresist film is all removed. The thickness ratio of the first photoresist portion 114 to the second photoresist portion may be varied depending upon the processing conditions to be described later. It is preferable that the thickness ratio of the first portion 114 to the second portion 112 should be established to be 1/2 or less. For instance, the first portion 114 may bear a thickness of 4000 Å or less.

In order to control the light transmission at the A area, the mask may bear a slit or lattice pattern, or a semitransparent film. It is preferable that the slit width should be smaller than the light decomposition capacity of the light exposing device. In the case of a semitransparent film, thin films differentiated in the light transmission or the thickness may be used to control the light transmission.

When the light exposing is made using such a mask, the high molecules at the area directly exposed to light are completely decomposed, those at the area exposed to light through a slit pattern or a semitransparent film are decomposed at some degree, and those at the area intercepted by an opaque film are not nearly decomposed. When the light-exposed photoresist film is developed, the portion thereof where the high molecules are not decomposed is left over, and the portion thereof where the high molecules are decomposed at some degree has a thickness smaller than the portion thereof where the high molecules are not nearly decomposed. As the light exposing time is too long, all of the molecules are liable to be decomposed.

The portion 114 of the photoresist pattern bearing a relatively thin thickness may be formed using a photoresist film capable of making reflow. The photoresist film is exposed to light using a usual mask with a transparent portion and an opaque portion, developed, and made reflowing such that it is partially flown toward the non-film portion.

The photoresist pattern 114, and the underlying conductive layer 60, ohmic contact layer 50 and semiconductor layer 40 are then etched. At this time, the data line assembly and the underlying layers are left over at the A area, only the semiconductor layer is left over at the C area, and the gate insulating layer 30 is exposed at the B area with the removal of the overlying layers 60, 50 and 40.

As shown in Figs. 13A and 13B, the conductive layer 60 exposed at the B area is removed while exposing the underlying ohmic contact layer 50. Either wet etching or dry etching may be used in this process. The etching condition is preferably established such that the conductive layer 60 is etched while the photoresist pattern portions 112 and 114 being not nearly etched. However, in the case of dry etching, it is difficult to find the condition such an etching condition, the photoresist pattern portions 112 and 114 may be etched together. In this case, the first photoresist pattern portion 114 is established to be so thick that the underlying conductive layer 60 cannot be exposed to the outside.

Consequently, as shown in Figs. 13A and 13B, the source/drain conductive pattern 67 at the C area and the storage capacitor conductive

pattern 68 at the B area are left over, and the conductive layer 60 at the B area is removed while exposing the underlying ohmic contact layer 50. At this time, the source/drain conductive pattern 67 has the same shape as the data line assembly except that the source and the drain electrodes 65 and 66 are not yet separated from each other. In the case of dry etching, the photoresist pattern portions 112 and 114 are also etched by a predetermined thickness.

Thereafter, as shown in Figs. 14A and 14B, the ohmic contact layer 50 at the B area and the underlying semiconductor layer 40 are simultaneously removed together with the first photoresist pattern portion 114 through dry etching. The etching should be made in condition that the photoresist pattern portions 112 and 114, the ohmic contact layer 50 and the semiconductor layer 40 are simultaneously etched while not etching the gate insulating layer 30. Particularly, it is preferable that the etching ratios with respect to the photoresist pattern portions 112 and 114 and the semiconductor layer 40 should be established to be nearly the same. For instance, a mixture of SF_6 and HCL or a mixture of SF_6 and O_2 may be used for that purpose. In case the etching ratios with respect to the photoresist pattern portions 112 and 114 and the semiconductor layer 40 are the same, the thickness of the first photoresist pattern portion 114 should be established to be the same or less than the sum in thickness of the semiconductor layer 40 and the ohmic contact layer 50.

Consequently, as shown in Figs. 14A and 14B, the first photoresist

pattern portion at the C area is removed while exposing the source/drain conductive pattern 67, and the ohmic contact layer 50 and the semiconductor layer 40 at the B area are removed while exposing the underlying gate insulating layer 30. The second photoresist pattern portion 112 at the A area is also etched while being reduced in thickness. Furthermore, in this process, semiconductor patterns 42 and 48 are completed. The reference numerals 57 and 58 indicate the ohmic contact pattern under the source/drain conductive pattern 67, and the ohmic contact pattern under the storage capacitor conductive pattern 64.

Thereafter, the photoresist residue on the source/drain conductive pattern 67 is removed through ashing.

As shown in Figs. 15A and 15B, the source/drain conductive pattern 67 at the C area and the underlying ohmic contact pattern 57 are removed through etching. Dry etching may be made with respect to all of the source/drain conductive pattern 67 and the ohmic contact pattern 57. Alternatively, wet etching may be made with respect to the source/drain conductive pattern, and dry etching with respect to the ohmic contact pattern 57. In the former case, the etching is preferably made in condition that the etching selection ratios of the conductive pattern 67 and the ohmic contact pattern 57 are high. This is because it is difficult to find the final point of etching with the lower etching selection ratio so that the thickness of the semiconductor pattern 42 to be left over at the C area cannot be easily controlled. By contrast, in the latter case where the wet etching and the dry

etching are alternated, the lateral side of the source/drain conductive pattern 67 suffering the wet etching is etched, whereas the ohmic contact pattern 57 suffering the dray etching is not nearly etched. Consequently, stepped area is existent in that case. A mixture of CF_4 and HCl or CF_4 and O_2 may be used for the etching gas. In the case of the mixture of CF_4 and O_2, the semiconductor pattern 42 is left over while bearing a uniform thickness. As shown in Fig. 15B, the semiconductor pattern 42 may be partially removed while being reduced in thickness. The second photoresist pattern portion 112 is also etched by a predetermined thickness. The etching is made in condition that the gate insulating layer 30 is not etched. The thickness of the second photoresist pattern portion 112 is so thick that the underlying data line assembly cannot be exposed to the outside through the etching.

Consequently, the source and the drain electrodes 65 and 66 are separated from each other while completing the data line assembly and the underlying ohmic contact patterns 55, 56 and 58.

Finally, the second photoresist pattern portion 112 at the A area is removed. The removal of the second photoresist pattern portion 112 may be made prior to the removal of the ohmic contact pattern 57 after the source/drain conductive pattern 67 is removed.

As described above, in the case of dry etching alone, the processing steps can be simplified, but it is difficult to fine the suitable etching conditions. By contrast, with the coexistence of dry etching and wet etching, it is relatively easy to find the suitable etching conditions, but the processing

steps are complicated.

Thereafter, as shown in Figs. 16A and 16B, an a-Si:C:O or a-Si:O:F-based layer is grown through chemical vapor deposition (CVD) to thereby form a passivation layer 70. In the case of an a-Si:C:O-based layer, a gaseous material such as $SiH(CH_3)_3$, $SiO_2(CH_3)_4$, $(SiH)_4O_4(CH_3)_4$ and $Si(C_2H_5O)_4$ is used as a basic source while introducing a mixture of an oxide agent such as N_2O and O_2, and Ar or He. Furthermore, in the case of an a-Si:O:F-based layer, a gaseous material such as SiH_4 and SiF_4 with the addition of O_2 is introduced during the deposition process. At this time, CF_4 may be added as a subsidiary source for fluorine.

Thereafter, as shown in Figs. 17A to 17C, the passivation layer 70 is etched through photolithography together with the gate insulating layer 30 to thereby form contact holes 76, 74, 78 and 72 exposing the drain electrodes 66, the gate pads 24, the data pads 68 and the storage capacitor conductive patterns 64, respectively. The area of the contact holes 74 and 78 exposing the pads 24 and 68 is established to be 2mmx60 ㎛ or less, preferably to be in the range of 0.5mmx15 ㎛-2mmx60 ㎛.

Finally, as shown in Figs. 8 to 10, an ITO or IZO-based layer with a thickness of 400-500Å is deposited, and etched through photolithography to thereby form pixel electrodes 82 connected to the drain electrodes 66 and the storage capacitor conductive patterns 64, subsidiary gate pads 86 connected to the gate pads 24, and subsidiary data pads 88 connected to the data pads 68.

In case the pixel electrodes 82, the subsidiary gate pads 86 and the subsidiary data pads 88 are formed with IZO, a chrome solution is used as the etching solution to prevent the metallic material for the data line assembly or the gate line assembly exposed through the contact holes from being corroded during the etching process. The chrome solution may be selected from HNO_3, $(NH_4)_2Ce(NO_3)_6$, or H_2O. Furthermore, in order to minimize the contact resistance at the contact area, it is preferable that IZO is deposited in the temperature range of from ambient temperature to 200℃. The target material for the IZO-based layer preferably contains In_2O_3 and ZnO, and the content of ZnO is preferably in the range of 15-20%.

Meanwhile, nitrogen is preferably used at the pre-heating process before the deposition of ITO or IZO. This is to prevent a metallic oxide layer from being formed on the metallic layers 24, 64, 66 and 68 exposed through the contact holes 72, 74, 76 and 78.

In this preferred embodiment, the data line assembly, and the underlying ohmic contact patterns and semiconductor patterns are formed using only one mask, and the source and the drain electrodes 65 and 66 are also separated during that process. In this way, the processing steps can be simplified.

The low dielectric CVD layer based on a-Si:C:O or a-Si:O:F may be used as a buffer layer for separating the color filters from thin film transistors in the array on color filter (AOC) structure where the thin film transistor array is formed on the color filters.

Fig. 18 is a plan view of a thin film transistor array substrate according to a third preferred embodiment of the present invention, and Fig. 19 is a cross sectional view of the thin film transistor array substrate taken along the XIX-XIX' line of Fig. 18. A top substrate facing the thin film transistor array substrate being the bottom substrate is also illustrated in Fig. 19.

In the thin film transistor array substrate, a data line assembly is formed on an insulating substrate 100 with a double-layered structure. The data line assembly has a bottom layer 201 formed with copper, copper alloy, silver, silver alloy, aluminum or aluminum alloy, and a top layer 202 formed with chrome, molybdenum, molybdenum alloy, chrome nitride or molybdenum nitride.

The data line assembly includes data lines 120 proceeding in the vertical direction, data pads 124 connected to the data lines 120 to receive picture signals and transmit them to the data pads 124, and light interception members 121 branched from the data lines 120 to intercept the light incident upon the semiconductor layer 170. The light interception member 121 also functions as a black matrix for preventing light leakage. The light interception members 121 may be independently formed in separation of the data lines 120.

Alternatively, the data line assembly may be formed with a single-layered structure using a conductive material such as copper, copper alloy, aluminum, aluminum alloy, molybdenum, molybdenum-tungsten alloy,

chrome, and tantalum.

In the data line assembly bearing a double-layered structure, considering that pixel electrodes and subsidiary pads to be formed later are based on indium tin oxide (ITO), the bottom layer thereof is formed with a low resistance material, and the top layer thereof with a material bearing good contact characteristic with ITO. For instance, the bottom layer 201 of the data line assembly is formed with Al-Nd, and the top layer 202 thereof with CrNx.

In case the pixel electrodes and the subsidiary pads are based on indium zinc oxide (IZO), it is preferable that the data line assembly is formed with a single-layered structure using aluminum or aluminum alloy. As copper exhibits good contact characteristic with respect to IZO and ITO, the data line assembly may be formed with a copper-based layer.

Color filters of red R, green G and blue B 131 to 133 are formed at the substrate 100 such that the periphery thereof is overlapped with that of the data line assembly. The color filters 131 to 133 may entirely cover the data lines 120.

A buffer layer 140 is formed on the data line assembly and the color filters 131 to 133 with a-Si:C:O, or a-Si:O:F. The deposition of the a-Si:C:O or a-Si:O:F-based layer (the low dielectric CVD layer) is made through plasma enhanced chemical vapor deposition (PECVD). The buffer layer 140 is provided to intercept outgassing from the color filters 131 to 133, and to prevent the color filters 131 to 133 from being damaged due to the thermal

or plasma energy during the subsequent processing steps. Furthermore, as the buffer layer 140 separates the data line assembly from the thin film transistor array, it is advantageous that the buffer layer 140 bears a low dielectric property and a large thickness. For this reason, the a-Si:C:O or a-Si:O:F-based layer (the low dielectric CVD layer) suffering the PECVD is suitable for such a buffer layer. That is, the a-Si:C:O or a-Si:O:F-based layer exhibits a low dielectric property and a rapid deposition speed while involving lower cost compared to an organic insulating material such as bisbenzocyclobutene (BCB) and perfluorocyclobutene (PFCB). Furthermore, the a-Si:O:C-based layer exhibits good insulating characteristic in the wide temperature range of from ambient temperature to 400℃.

A gate line assembly is formed on the buffer layer 140 with a double-layered structure. The data line assembly has a bottom layer 501 formed with copper, copper alloy, silver, silver alloy, aluminum or aluminum alloy, and a top layer 502 formed with chrome, molybdenum, molybdenum alloy, chrome nitride or molybdenum nitride.

The gate line assembly includes gate lines 150 crossing over the data lines 120 while defining pixel regions, gate pads 152 connected to the gate lines 150 to receive scanning signals from the outside and transmit them to the gate lines 150, gate electrodes 151 for thin film transistors being parts of the gate lines 150.

The gate lines 150 are overlapped with pixel electrodes 410 to form storage capacitors for improving the pixel electric potential storage capacity.

In case the storage capacity due to the overlapping of the pixel electrodes 410 and the gate lines 150 is not enough, a storage capacitor common electrode may be additionally formed.

In case the gate line assembly is formed with a multiple-layered structure, one layer is formed with a low resistance material, and the other layer is formed with a material bearing good contact characteristic with other materials. For instance, layers of Al (or Al alloy)/Cr or Cu/Cr may be provided as the double-layered structure. Furthermore, in order to improve the contact characteristic, a chrome nitride-based layer or a molybdenum nitride-based layer may be additionally formed.

The gate line assembly may be formed with a single-layered structure using a low resistance material such as copper, aluminum and aluminum alloy.

A low temperature deposition gate insulating layer 160 is formed on the gate line assembly, and the buffer layer 140. The low temperature deposition gate insulating layer 160 may be formed with an organic insulating material; low temperature amorphous silicon oxide, or low temperature amorphous silicon nitride. As the color filters are formed at the bottom substrate, the gate insulating layer 160 is formed with a low temperature deposition insulating layer that can be deposited at lower temperatures of 250℃ or less.

An island-shaped semiconductor layer 171 is formed on the gate insulating layer over the gate electrodes 151 with a double-layered structure.

The semiconductor layer 171 has a bottom layer portion 701 formed with amorphous silicon exhibiting a relatively high band gap, and a top layer portion 702 formed with amorphous silicon exhibiting a band gap lower than the bottom layer portion 701. For instance, the band gap of the bottom layer portion 701 may be established to be 1.9-2.1eV, and the band gap of the top layer portion 702 to be 1.7-1.8eV. The thickness of the bottom layer portion 701 is established to be 50-200Å, and the thickness of the top layer portion 702 to be 1000-2000Å.

A band offset is formed between the top and the bottom semiconductor layer portions 702 and 701 differentiated in the band gap while corresponding to the difference in the band gap thereof. When the TFT is in an ON state, channel is formed at the band offset region between the top and bottom semiconductor layer portions 702 and 701. As the respective band offset regions basically bear the same atomic structure while accompanying with minimized device failures, it can be expected to obtain good TFT characteristics.

Alternatively, the semiconductor layer 171 may be formed with a single-layered structure.

Ohmic contact layers 182 and 183 are formed on the semiconductor layer 171 with amorphous silicon where n-type impurities such as phosphorous P are doped at high concentration, micro-crystalline silicon or metallic silicide while being separated from each other.

A pixel line assembly is formed on the ohmic contact layers 182 and

183 with ITO. The pixel line assembly includes source and drain electrodes 412 and 411, and pixel electrodes 410. The source electrodes 412 are connected to the data lines 120 through contact holes 161 formed at the gate insulating layer 160 and the buffer layer 140. The drain electrodes 411 are connected to the pixel electrodes 410 to receive picture signals from the thin film transistors and transmit them to the pixel electrodes 410. The pixel line assembly is formed with a transparent conductive material such as ITO and IZO.

Subsidiary gate and data pads 413 and 414 are formed at the same plane as the pixel line assembly while being connected to the gate and the data pads 152 and 124 through the contact holes 162 and 164, respectively. The subsidiary gate pads 413 directly contact the chrome-based top layer 502 of the gate pads 152, and the subsidiary data pads 414 also directly contact the chrome-based top layer 202 of the data pads 124. In case the gate pads 152 and the data pads 124 contain a chrome nitride-based layer or a molybdenum nitride-based layer, it is preferable that the subsidiary gate pads 413 and the subsidiary data pads 414 contact the chrome nitride-based layer or the molybdenum nitride-based layer. The subsidiary gate and data pads 413 and 414 are provided to enhance the adhesive strength between the pads 152 and 124 and external circuits while protecting them, but may be selectively introduced. The pixel electrodes 410 are overlapped with the neighboring gate and data lines 150 and 120 to enhance the opening ratios, but the overlapping thereof may not be made.

The ohmic contact layers 182 and 183 reduce the contact resistance between the ITO-based source and drain electrodes 412 and 411 and the semiconductor layer 171. The ohmic contact layers 182 and 183 may contain microcrystalline silicon or metallic silicide such as molybdenum, nickel and chrome while a metallic silicide film being left over.

A passivation layer 190 is formed on the source and the drain electrodes 412 and 411 to protect the thin film transistors. A photosensitive colored organic film 430 is formed on the passivation layer 190 while bearing a dark color of excellent light absorption. The colored organic film 430 intercepts the light incident upon the semiconductor layer 171. The colored organic film 430 is used as a spacer to maintain the distance between the bottom insulating substrate 100 and the top insulating substrate 200 while being controlled in height. The passivation layer 190 and the organic film 430 may be formed along the gate lines 150 and the data lines 120, and the organic film 430 may intercept the light leaked at the peripheral area of the gate line assembly and the data line assembly.

In case the organic film 430 is designed to entirely cover the gap between the pixel electrodes and the respective metallic layers, it is not necessary to provide a separate black matrix of light interception at the top substrate.

Meanwhile, a common electrode 210 is formed at the entire surface of the top substrate 200 with ITO or IZO such that it generates electric fields together with the pixel electrodes 410.

A method of fabricating the thin film transistor array substrate will be now explained with reference to Figs. 20A to 28B.

As shown in Figs. 20A and 20B, a data line assembly is formed on a bottom insulating substrate 100 with a double-layered structure. For this purpose, a low resistance conductive material such as aluminum, aluminum alloy, copper and copper alloy, and a conductive material bearing good contact characteristic with ITO such as chrome, molybdenum, titanium, chrome nitride and molybdenum nitride are sequentially deposited onto the substrate 100 through sputtering, and dry or wet-etched through photolithography based on a mask. The resulting data line assembly has a bottom layer 201 and a top layer 202. The data line assembly includes data lines 120, data pads 124, and light interception members 121.

Considering that a pixel line assembly 410 to 412 and subsidiary pads 413 and 414 to be formed layer would be based on indium tin oxide (ITO), the bottom layer 201 is formed with aluminum, aluminum alloy, copper or copper alloy, and the top layer 202 with chrome, molybdenum, or titanium. By contrast, in case the pixel line assembly and the subsidiary pads are formed with indium zinc oxide (IZO), the data line assembly may be formed with a single-layered structure. For instance, the data line assembly may be formed with a single layer based on aluminum, aluminum alloy, copper, or copper alloy.

Thereafter, as shown in Figs. 21A and 21B, photosensitive materials containing pigments of red R, green G and blue B are sequentially coated

onto the substrate 100 with the data line assembly, and patterned through photolithography to thereby form color filters 131 to 133 of red R, green G, and blue B. The RGB color filters 131 to 133 are formed using three masks. It is possible that one mask is used to form the RGB color filters 131 to 133 while being moved. Furthermore, it is also possible that the RGB color filters 131 to 133 are formed through laser illumination or printing without any mask. It is preferable that the peripheral portions of the RGB color filters 131 to 133 are overlapped with the data lines 120.

As shown in Figs. 22A and 22B, an a-Si:C:O or a-Si:O:F-based layer is grown at the insulating substrate 100 through chemical vapor deposition (CVD) to thereby form a buffer layer 140. In the case of an a-Si:C:O-based layer, a gaseous material such as $SiH(CH_3)_3$, $SiO_2(CH_3)_4$, $(SiH)_4O_4(CH_3)_4$ and $Si(C_2H_5O)_4$ is used as a basic source while introducing a mixture of an oxide agent such as N_2O and O_2, and Ar or He. Furthermore, in the case of an a-Si:O:F-based layer, a gaseous material such as SiH_4 and SiF_4 with the addition of O_2 is introduced during the deposition process. At this time, CF_4 may be added as a subsidiary source for fluorine.

Thereafter, a physico-chemically stable material such as chrome, molybdenum, titanium, chrome nitride and molybdenum nitride, and a low resistance conductive material such as aluminum, aluminum alloy, copper and copper alloy are sequentially deposited onto the buffer layer 140 through sputtering, and patterned through photolithography to thereby form a gate line assembly. The gate line assembly includes gate lines 150, gate

electrodes 151, and gate pads 152.

The gate line assembly may be formed with a single-layered structure.

As shown in Fig. 23, a low temperature deposition gate insulating layer 160, a first amorphous silicon layer 701, a second amorphous silicon layer 702 and an impurities-doped amorphous silicon layer 180 are sequentially deposited onto the gate line assembly and the organic insulating layer 140.

The low temperature deposition gate insulating layer 160 may be formed with an organic insulating material, low temperature amorphous silicon oxide, low temperature amorphous silicon nitride that can be deposited at 250℃ or less.

The first amorphous silicon layer 701 is formed with amorphous silicon exhibiting a relatively high band gap, and the second amorphous silicon layer 702 with amorphous silicon exhibiting a band gap lower than the first amorphous silicon layer 701. For instance, the band gap of the first amorphous silicon layer 701 may be established to be 1.9-2.1eV, and the band gap of the second amorphous silicon layer 702 to be 1.7-1.8eV. The first amorphous silicon layer 701 may be deposited through CVD while adding CH_4, C_2H_2 or C_2H_6 into the raw gaseous material of SiH_4 in an appropriate manner. For instance, when the deposition is made while injecting SiH_4 and CH_4 into a CVD device by the ratio of 1:9, an amorphous silicon layer containing 50% of C while bearing a band gap of 2.0-2.3eV can

be deposited. Like this, the band gap of the amorphous silicon layer is influenced by the deposition conditions. The band gap can be easily controlled in the range of 1.7-2.5eV depending upon the amount of addition of carbonaceous compounds.

The low temperature deposition gate insulating layer 160, the first amorphous silicon layer 701, the second amorphous silicon layer 702, and the impurities-doped amorphous silicon layer 180 can be sequentially deposited without breaking the vacuum state in the same CVD device.

Thereafter, as shown in Figs. 24A and 24B, the first amorphous silicon layer 701, the second amorphous silicon layer 702, and the impurities-doped amorphous silicon layer 180 are patterned through photolithography to thereby form an island-shaped semiconductor layer 171 and an ohmic contact layer 181. At the same time, contact holes 161, 162 and 164 are formed at the low temperature gate insulating layer 160 and the organic insulating layer 140 while exposing the data lines 120, the gate pads 152 and the data pads 124, respectively.

At this time, the first and the second amorphous silicon layers 701 and 702, and the impurities-doped amorphous silicon layer 180 should be all removed at the entire area except for the regions over the gate electrodes 151. The first and the second amorphous silicon layer 701 and 702 and the impurities-doped amorphous silicon layer 180 as well as the gate insulating layer 160 should be removed at the regions over the gate pads 152. The first and the second amorphous silicon layers 701 and 702, the impurities-

doped amorphous silicon layer 180 and the low temperature deposition gate insulating layer 160 as well as the organic insulating film 140 should be removed at the regions over the data lines 120 and the data pads 124.

The above process is performed through photolithography using one mask. For this purpose, a photoresist pattern differentiated in thickness is used for the mask. This will be explained with reference to Figs. 25 and 26.

As shown in Fig. 25, a photoresist film is coated onto the impurities-doped amorphous silicon layer 180 by a thickness of 1-2 ㎛, exposed to light through a mask, and developed to thereby form a photoresist pattern with first and second portions 312 and 314.

The first portion 312 of the photoresist pattern is placed over the gate electrodes 151 with a thickness larger than the second portion 314 thereof. The photoresist film over the data lines 120, the data pads 124 and the gate pads 152 is partially removed. The thickness of the second photoresist pattern portion 314 is established to be 1/2 or less of the thickness of the first photoresist pattern portion 312. For instance, the thickness of the second photoresist pattern portion 314 is established to be 4000Å or less.

The mask 1000 is provided with a semitransparent film or a slit or lattice pattern smaller than the light decomposition capacity of a light exposing device at the B area. When a positive photoresist film is exposed to light through the mask 1000, the decomposition degree of high molecules in the photoresist film is differentiated. When the light exposing stops when the high molecules at the C area directly exposed to light are completely

decomposed, the high molecules at the B area are also decomposed at some degree. In case the light exposing time is too long, all of the molecules are liable to be decomposed.

When the photoresist film is developed, the first photoresist pattern portion 312 where the high molecules are not nearly decomposed is left over with the original thickness, the second photoresist pattern portion 314 where the high molecules are decomposed at some degree is left over with a thickness smaller than that of the first photoresist pattern portion 312, and the remaining portion of the photoresist film at the C area where the high molecules are completely decomposed is removed.

In this way, the photoresist pattern differentiated in thickness can be made.

As shown in Fig. 26, the impurities-doped amorphous silicon layer 180, the second amorphous silicon layer 702, the first amorphous silicon layer 702 and the low temperature deposition gate insulating layer 160 are dry-etched using the photoresist pattern with the first and second portions 312 and 314 as an etching mask to thereby form contact holes 162 exposing the gate pads 152, and to expose the buffer layer 140 at the C area. Thereafter, the buffer layer 140 at the C area is dry-etched using the photoresist pattern with the first and second portions 312 and 314 as an etching mask to thereby form contact holes 161 and 164 exposing the data lines 120 and the data pads 124.

The second photoresist pattern portion 314 is then completely

removed. An ashing process using oxygen may be additionally performed to completely remove the photoresist residue of the second photoresist pattern portion 314.

Consequently, the second photoresist pattern portion 314 is removed while exposing the impurities-doped amorphous silicon layer 180. The first photoresist pattern portion 312 is left over while bearing a thickness reduced by the thickness of the second photoresist pattern portion 314.

Thereafter, the impurities-doped amorphous silicon layer 180 and the underlying first and second amorphous silicon layers 701 and 702 are etched using the first photoresist pattern portion 312 as an etching mask, and removed to thereby form an island-shaped semiconductor layer 171 and an island-shaped ohmic contact layer 181 on the low temperature deposition gate insulating layer 160 over the gate electrodes 151.

Finally, the first photoresist pattern portion 312 is removed. An ashing process using oxygen may be additionally performed to completely remove the photoresist residue of the first photoresist pattern portion 312.

As shown in Figs. 27A and 27B, an ITO-based layer is deposited onto the substrate 100, and patterned through photolithography to thereby form pixel electrodes 410, source electrodes 412, drain electrodes 411, subsidiary gate pads 413, and subsidiary data pads 414. At this time, IZO may be used instead of ITO.

Thereafter, the ohmic contact layer 181 is etched using the source electrodes 412 and the drain electrodes 411 as an etching mask to thereby

form ohmic contact patterns 182 and 183 while exposing the semiconductor layer between the source electrodes 412 and the drain electrodes 411.

Finally, as shown in Figs. 18 and 19, an insulating material such as silicon nitride and silicon oxide, and a photosensitive organic material containing black pigment are sequentially deposited onto the substrate 100, exposed to light, and developed to thereby form a colored organic film 430. The insulating material is etched using the colored organic film 430 as an etching mask to thereby form a passivation layer 190. The colored organic layer film 430 intercepts the light incident upon the thin film transistors. The colored organic film 430 may be formed over the gate line assembly or the data line assembly to prevent light leakage at the periphery of the gate line assembly or the data line assembly. Furthermore, the organic film 430 may be used as a spacer while being controlled in height.

In the meantime, a transparent conductive material such as ITO and IZO is deposited onto a top insulating substrate 200 to thereby form a common electrode 210.

In case the color organic film 430 is designed to entirely cover the gap between the pixel electrodes 410 and the respective metallic layers, it is not necessary to form a separate black matrix of light interception on the top substrate.

Fig. 28 is a plan view of a thin film transistor array substrate according to a fourth preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the thin film

transistor array substrate are the same as those related to the third preferred embodiment except that the data line assembly 120, 121 and 124 and the colored organic film 130 are differentiated.

In case the gate lines 150 and the pixel electrodes 410 are designed to be spaced apart from each other, it is necessary to cover the gap of light leakage between the pixel electrodes 410 and the gate lines 150. For this purpose, the data lines 120 formed under the color filters 131, 132 and 133 are partially extended toward the gate lines 150 such that they cover the gap between the gate lines 150 and the pixel electrodes 410. Furthermore, the colored organic film 430 may cover the gap between the neighboring data lines 120.

Meanwhile, a vertical black matrix portion may be formed at the same plane as the gate line assembly 150, 151 and 152 with a material for the gate line assembly to prevent light leakage at the periphery of the screen area. Furthermore, a horizontal black matrix portion may be formed at the same plane as the data line assembly 120, 121 and 124 with a material for the data line assembly to prevent light leakage at the periphery of the screen area.

With the above structure, as the regions of light leakage are all covered by the data line assembly, the gate line assembly and the spacer, it is not necessary to form a separate black matrix at the top substrate. Therefore, the opening ratios can be enhanced without the need of considering the alignment errors between the top substrate and the bottom

substrate. Furthermore, a gate insulating 160 and a low dielectric buffer layer 140 are formed between the data lines 120 and the pixel electrodes 410 while minimizing the parasitic capacitance there. In this way, the opening ratio can be maximized while improving the characteristic of the display device.

As described above, the thin film transistors are made at lower temperatures. That is, in order to prevent damage to the color filters due to the high temperature processing, the gate insulating layer is formed with a low temperature deposition insulating layer. Furthermore, in order to prevent deterioration in the characteristic of the channel induced in contact with the low temperature deposition gate insulating layer, the channel is not formed at the interface between the low temperature deposition gate insulating layer and the semiconductor layer, but formed at the bulk side of the semiconductor layer.

The above-described structure may be applied for use in various ways. For instance, such a structure is well adapted for use in a plastic liquid crystal display developed for reducing the weight and enhancing the shock-absorption effect while requiring the low temperature processing conditions.

The low dielectric CVD layer based on a-Si:C:O or a-Si:O:F may be used as an embossing insulating layer with prominence and depression to prevent the interception of reflection light at the thin film transistor array substrate for a reflection type liquid crystal display or a semitransparent liquid

crystal display.

Fig. 29 is a plan view of a thin film transistor array substrate for a reflection type liquid crystal display according to a fifth preferred embodiment of the present invention, and Fig. 30 is a cross sectional view of the thin film transistor array substrate taken along the XXX-XXX' line of Fig. 29.

A gate line assembly is formed on an insulating substrate 10 with a single-layered structure or a multiple-layered structure. The gate line assembly is formed with a low resistance material such as silver, silver alloy, aluminum, or aluminum alloy. The gate line assembly includes gate lines 22 proceeding in the horizontal direction, gate pads 24 connected to the gate lines 22 to receive gate signals from the outside and transmit them to the gate lines 22, and gate electrodes 26 for thin film transistors connected to the gate lines 22.

Storage capacitors may be formed on the substrate 10 to receive common electrode voltages from the outside. The storage capacitors are overlapped with a reflective layer 92 to be formed layer, thereby forming storage capacitors for improving the pixel electrode potential storage capacity.

A gate insulating layer 30 is formed at the substrate 10 with silicon nitride SiNx such that it covers the gate line assembly.

A semiconductor layer 40 is formed on the gate insulating layer 30 over the gate electrodes 26 with amorphous silicon. Ohmic contact layers 55 and 56 are formed on the semiconductor layer 40 with silicide, or n^+ hydrogenated amorphous silicon where n-type impurities are doped at high

concentration.

A data line assembly is formed on the ohmic contact layers 55 and 56 and the gate insulating layer 30 while bearing a conductive layer formed with a low resistance conductive material such as aluminum and silver. The data line assembly includes data lines 62 crossing over the gate lines 22 while defining pixel regions, source electrodes 65 connected to the data lines 62 while being extended over the ohmic contact layer 55, data pads 68 connected to the one-sided ends of the data lines 62 to receive picture signals from the outside, and drain electrodes 66 facing the source electrodes 65 around the gate electrodes 26 while being separated from the source electrodes 65. The drain electrodes 66 are formed on the ohmic contact layer 56 while being extended inside of the pixel regions.

A passivation layer 70 is formed on the data line assembly and the semiconductor layer 40 exposed through the data line assembly with a-Si:C:O or a-Si:O:F. The a-Si:C:O or a-Si:O:F-based layer (the low dielectric CVD layer) is deposited through plasma enhanced chemical vapor deposition (PECVD). The passivation layer 70 bears a pattern of prominence and depression to maximize the reflection efficiency of a reflective layer 92 to be formed later.

The passivation layer 70 has contact holes 76 and 78 exposing the drain electrodes 66 and the data pads 68, and contact holes 74 exposing the gate pads 24 together with the gate insulating layer 30.

A reflective layer 92 is formed on the passivation layer 70 at the pixel

regions while being electrically connected to the drain electrodes 66 through the contact holes 76. Subsidiary gate pads 96, and subsidiary data pads 98 are formed on the passivation layer 70 while being connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78. The subsidiary gate and data pads 96 and 98 protect the gate and data pads 24 and 68, but may be dispensed.

A method of fabricating the thin film transistor array substrate will be now explained with reference to Figs. 31A to 34B.

As shown in Figs. 31A and 31B, a low resistance conductive material is deposited onto a glass substrate 10, and patterned through photolithography to thereby form a gate line assembly proceeding in the horizontal direction. The gate line assembly includes gate lines 22, gate electrodes 26, and gate pads 24.

Thereafter, as shown in Figs. 32A and 32B, a silicon nitride-based gate insulating layer 30, an amorphous silicon-based semiconductor layer 40 and a doped amorphous silicon layer 50 are sequentially deposited onto the substrate 10 with the gate line assembly. The semiconductor layer 40, and the doped amorphous silicon layer 50 are patterned through photolithography to thereby form a semiconductor pattern 40 and an ohmic contact pattern 50 on the gate insulating layer 30 over the gate electrodes 24.

As shown in Figs. 33A and 33B, a conductive layer is deposited onto the substrate 10, and patterned through photolithography to thereby form a data line assembly. The data line assembly includes data lines 62 crossing

over the gate lines 22, source electrodes 65 connected to the data lines 62 while being extended over the gate electrodes 26, and data pads 68 connected to the one-sided ends of the data lines 62, and drain electrodes 66 facing the source electrodes 65 around the gate electrodes 26 while being separated from the source electrodes 65.

The ohmic contact pattern 50 exposed through the data line assembly is etched, and separated into two pattern portions with respect to the gate electrodes 26. In order to stabilize the surface of the semiconductor pattern 40, it is preferable that oxygen plasma is made with respect to the semiconductor pattern 40.

Thereafter, as shown in Figs. 34A and 34B, an a-Si:C:O or a-Si:O:F-based layer is grown through chemical vapor deposition (CVD) to thereby form a passivation layer 70. In the case of an a-Si:C:O-based layer, a gaseous material such as $SiH(CH_3)_3$, $SiO_2(CH_3)_4$, $(SiH)_4O_4(CH_3)_4$ and $Si(C_2H_5O)_4$ is used as a basic source while introducing a mixture of an oxide agent such as N_2O and O_2, and Ar or He. Furthermore, in the case of an a-Si:O:F-based layer, a gaseous material such as SiH_4 and SiF_4 with the addition of O_2 is introduced during the deposition process. At this time, CF_4 may be added as a subsidiary source for fluorine. The passivation layer 70 is patterned through photolithography together with the gate insulating layer 30 to thereby form contact holes 74, 76 and 78 exposing the gate pads 24, the drain electrodes 66 and the data pads 68. At the same time, a pattern of prominence and depression is formed on the passivation layer 70.

The half tone light exposing as employed in relation to the second preferred embodiment is made to form the contact holes 74, 76 and 78 and the pattern of prominence and depression together. That is, a photoresist film is exposed to light through a mask with a slit or lattice pattern or a semitransparent film, and developed such that the photoresist film portion at the area of contact holes 74, 76 and 78 is entirely removed while exposing the passivation layer 70, the photoresist film portion at the area of a prominence pattern is left over with a small thickness, and the photoresist film portion at the area of a depression pattern is left over with a large thickness.

Thereafter, the passivation layer 70 and the gate insulating layer 30 are etched using the photoresist pattern as an etching mask to thereby form contact holes 74, 76 and 78, and the thin photoresist pattern portion is removed through ashing. At this time, the thick photoresist pattern portion is also partially removed through the ashing while being reduced in thickness.

The passivation layer 70 is etched for a predetermined period of time to thereby form prominence portions. The etching time is determined in consideration of the etching rate of the passivation layer 70, and the depth of the prominence portions.

As shown in Figs. 29 and 30, a conductive layer is deposited onto the substrate 10 with a reflective conductive material such as silver and aluminum, and patterned through photolithography to thereby form a reflective layer 92 connected to the drain electrodes 66 through the contact

holes 76, and subsidiary gate and data pads 96 and 98 connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78, respectively.

Fig. 35 is a plan view of a thin film transistor array substrate for a semitransparent liquid crystal display according to a sixth preferred embodiment of the present invention, and Fig. 36 is a cross sectional view of the thin film transistor array substrate taken along the XXXVI-XXXVI' line of Fig. 35.

A gate line assembly is formed on an insulating substrate 10 with a single-layered structure or a multiple-layered structure. The gate line assembly is formed with a low resistance material such as silver, silver alloy, aluminum, or aluminum alloy. The gate line assembly includes gate lines 22 proceeding in the horizontal direction, gate pads 24 connected to the gate lines 22 to receive gate signals from the outside and transmit them to the gate lines 22, and gate electrodes 26 for thin film transistors connected to the gate lines 22. In case the gate line assembly has a multiple-layered structure, it preferably contains a pad material bearing good contact characteristic with other materials.

A gate insulating layer 30 is formed on the substrate 10 with silicon nitride SiNx such that it covers the gate line assembly.

A semiconductor layer 40 is formed on the gate insulating layer 30 over the gate electrodes 26 with amorphous silicon. Ohmic contact layers 55 and 56 are formed on the semiconductor layer 40 with silicide, or n+

hydrogenated amorphous silicon where n-type impurities are doped at high concentration.

A data line assembly is formed on the ohmic contact layers 55 and 56 and the gate insulating layer 30 while bearing a conductive layer formed with a low resistance conductive material such as aluminum and silver. The data line assembly includes data lines 62 crossing over the gate lines 22 while defining pixel regions, source electrodes 65 connected to the data lines 62 while being extended over the ohmic contact layer 55, data pads 68 connected to the one-sided ends of the data lines 62 to receive picture signals from the outside, and drain electrodes 66 facing the source electrodes 65 around the gate electrodes 26 while being separated from the source electrodes 65.

A passivation layer 70 is formed on the data line assembly and the semiconductor layer 40 exposed through the data line assembly with a-Si:C:O or a-Si:O:F. The a-Si:C:O or a-Si:O:F-based layer (the low dielectric CVD layer) is deposited through plasma enhanced chemical vapor deposition (PECVD). The a-Si:C:O or a-Si:O:F-based layer bears a dielectric constant of 4 or less. Therefore, the passivation layer 70 does not involve the problem of parasitic capacitance even if it bears a thin thickness. Furthermore, the passivation layer 70 involves good adhesion characteristic and step coverage characteristic in relation to other layers. As the passivation layer 70 is based on a low dielectric CVD film, it bears excellent thermostabiliy compared to that based on an organic insulating film. In

addition, the a-Si:C:O or a-Si:O:F-based layer deposited through PECVD exhibits an advantage in the processing time as the deposition speed or etching speed related thereto is rapid by four to ten times compared to that related to a silicon nitride-based layer.

The passivation layer 70 has contact holes 76 and 78 exposing the drain electrodes 66 and the data pads 68, and contact holes 74 exposing the gate pads 24 together with the gate insulating layer 30.

Transparent electrodes 82 are formed on the passivation layer 70 at the pixel regions while being electrically connected to the drain electrodes 66 through the contact holes 76. Furthermore, subsidiary gate and data pads 86 and 88 are formed on the passivation layer 70 while being connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78. The transparent electrodes 82 and the subsidiary gate and data pads 86 and 88 are formed with indium tin oxide (ITO) or indium zinc oxide (IZO).

An inter-layered insulating layer 34 is formed on the transparent electrodes 82 while bearing contact holes 36 partially exposing the transparent electrodes 82. The inter-layered insulating layer 34 is formed with a-Si:C:O or a-Si:O:F. The a-Si:C:O or a-Si:O:F-based layer (the low dielectric CVD layer) is deposited through plasma enhanced chemical vapor deposition (PECVD). It is preferable that the inter-layered insulating layer 34 passivation layer 70 bears a pattern of prominence and depression to maximize the reflection efficiency of a reflective layer 92 to be formed later.

A reflective layer 92 is formed on the inter-layered insulating layer 34

with light transmission windows 96 at transmission mode regions T while being electrically connected to the transparent electrodes 82 through the contact holes 36. The reflective layer 92 is formed with a high reflective conductive material such as aluminum, aluminum alloy, silver, silver alloy, molybdenum, and molybdenum alloy. The reflective layer 92 forms pixel electrodes in association with the transparent electrodes 82. The light transmission windows 96 of the reflective layer 92 may be formed with various shapes. Plural numbers of windows 96 may be formed at one pixel region. Even if a pattern of prominence and depression is formed at the inter-layered insulating layer 34, it is preferable that such a pattern of prominence and depression is not formed at the area of the windows 96.

The pixel electrodes 82 and 92 are overlapped with the front gate lines 22 to thereby form storage capacitors. If needed, a storage capacitor line assembly may be formed at the same plane as the gate line assembly to obtain the required storage capacity.

A method of fabricating the thin film transistor array substrate will be now explained in detail.

In this preferred embodiment, the procedures of processing are the same as those related to the fifth preferred embodiment up to the step of forming a data line assembly and hence, illustrated in Figs. 31A to 33B.

After the data line assembly is formed, as shown in Figs. 37A and 37B, an a-Si:C:O or a-Si:O:F-based layer is grown on the data line assembly through chemical vapor deposition (CVD) to thereby form a passivation layer

70. The passivation layer 70 is then patterned through photolithography together with the gate insulating layer 30 to thereby form contact holes 74, 76 and 78 exposing the gate pads 24, the drain electrodes 66, and the data pads 68. In this process, dry etching is used.

Thereafter, as shown in Figs. 38A and 38B, an ITO or IZO-based layer is deposited onto the substrate 10, and etched through photolithography to thereby form transparent electrodes 82, and subsidiary gate and data pads 86 and 88. The transparent electrodes 82 are connected to the drain electrodes 66 through the contact holes 76. The subsidiary gate and data pads 86 and 88 are connected to the gate and data pads 24 and 68 through the contact holes 74 and 78.

As shown in Figs. 39A and 39B, an a-Si:C:O or a-Si:O:F-based layer is grown through chemical vapor deposition (CVD), and patterned through photolithography to thereby form an inter-layered insulating layer 34 with contact holes 36 exposing the transparent electrodes 82. At this time, a pattern of prominence and depression may be formed at the inter-layered insulating layer 34. In this case, a half tone light exposing is made as in the process of patterning the passivation layer according to the fifth preferred embodiment.

Finally, as shown in Figs. 35 and 36, a conductive layer based on a high reflective material such as aluminum, silver and molybdenum is deposited, and patterned to thereby form a reflective layer 92 with light transmission opening windows 96.

The a-Si:C:O or a-Si:O:F-based layer (the low dielectric CVD layer) may be also used to form a gate insulating layer.

Fig. 40 is a cross sectional view of a thin film transistor array substrate according to a seventh preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the thin film transistor array substrate are the same as those related to the first preferred embodiment except that the gate insulating layer has a double-layered structure. The gate insulating layer has an a-Si:C:O or a-Si:O:F-based layer portion 31, and a silicon nitride-based layer portion 32. The a-Si:C:O or a-Si:O:F-based layer portion 31 (the low dielectric CVD layer) is formed through PECVD.

The gate insulating layer should be kept to bear a dense membranous structure in consideration of its interfacial characteristic with respect to the amorphous silicon-based semiconductor layer 40. As the membranous structure of the gate insulating layer is denser, the speed of deposition thereof becomes slower while increasing the processing time. Meanwhile, it is known that the thin film transistors are well operated when the dense membranous structure of the gate insulating layer is maintained up to the thickness of about 500Å from its interfacial surface in contact with the semiconductor layer 40. Accordingly, when the top layer portion of the gate insulating layer is formed with an a-Si:C:O or a-Si:O:F-based layer involving a rapid deposition speed and the bottom layer portion thereof with a silicon nitride-based layer involving a dense membranous structure, the capacity of

the thin film transistors is not deteriorated while reducing the processing time. The a-Si:C:O-based layer involves a deposition speed four to ten times greater than that of the silicon nitride-based layer. The a-Si:C:O-based layer, and the silicon nitride-based layer are sequentially deposited in a vacuum state.

Such a gate insulating layer with a low dielectric CVD layer portion and a silicon nitride-based layer portion may be applied for use in the thin film transistor array substrates according to the second to the sixth preferred embodiments.

As described above, the passivation layer is formed using a low dielectric CVD layer while not involving the problem of parasitic capacitance. This structure can serve to enhance the opening ratio, and to reduce the processing time. Furthermore, the problems of high material cost, poor thermostability and weak adhesive strength occurring to the use of an organic insulating layer can be solved.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A thin film transistor array substrate comprising:

an insulating substrate;

a first signal line formed on the insulating substrate;

a first insulating layer formed on the first signal line;

a second signal line formed on the first insulating layer while crossing over the first signal line;

a thin film transistor connected to the first and the second signal lines;

a second insulating layer formed on the thin film transistor with a CVD layer having dielectric constant 4.0 or less, the second insulating layer having a first contact hole exposing a predetermined electrode of the thin film transistor; and

a first pixel electrode formed on the second insulating layer while being connected to the predetermined electrode of the thin film transistor through the first contact hole.

2. The thin film transistor array substrate of claim 1 wherein the first insulating layer has a bottom layer portion based on a CVD layer having dielectric constant 4 or less, and a top layer portion based on a silicon nitride layer.

3. The thin film transistor array substrate of claim 1 wherein the first pixel electrode is formed with an opaque conductive material of light reflection.

4. The thin film transistor array substrate of claim 3 wherein the second insulating layer has a pattern of prominence and depression.

5. The thin film transistor array substrate of claim 1 further comprising:

a third insulating layer formed on the first pixel electrode with a CVD layer having dielectric constant 4.0 or less, the third insulating layer having a second contact hole exposing a predetermined portion of the first pixel electrode; and

a second pixel electrode formed on the third insulating layer with an opaque conductive material of light reflection while being connected to the predetermined portion of the first pixel electrode through the second contact hole;

wherein the first pixel electrode is formed with a transparent conductive material, and the second pixel electrode has a predetermined opening portion capable of passing the light transmitted through the first pixel electrode.

6. The thin film transistor array substrate of claim 1 wherein the a CVD layer is formed with a-Si:C:O.

7. The thin film transistor array substrate of claim 1 wherein the CVD layer is formed with a-Si:C:O.

8. The thin film transistor array substrate of claim 1 wherein the CVD layer has a dielectric constant of 2-4.

9. A thin film transistor array substrate comprising:

a data line assembly formed on an insulating substrate, the data line assembly including data lines;

color filters of red, green and blue formed on the insulating substrate;

a buffer layer formed on the data line assembly and the color filters with a CVD layer, the buffer layer having a first contact hole exposing a predetermined portion of the data line assembly;

a gate line assembly formed on the buffer layer, the gate line assembly including gate lines crossing over the data lines while defining pixel regions, and gate electrodes connected to the gate lines;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having a second contact hole partially exposing the first contact hole;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes; and

a pixel line assembly including source electrodes connected to the data lines through the first and the second contact holes while partially contacting the semiconductor pattern, drain electrodes facing the source electrodes over the semiconductor pattern, and pixel electrodes connected to the drain electrodes.

10. The thin film transistor array substrate of claim 9 wherein the semiconductor pattern has a first amorphous silicon layer with a predetermined band gap, and a second amorphous silicon layer with a band gap lower than the band gap of the first amorphous silicon layer.

11. The thin film transistor array substrate of claim 10 further comprising light interception members formed at the same plane as the data lines with the same material as the data lines while being placed corresponding to the semiconductor pattern.

12. The thin film transistor array substrate of claim 11 wherein the light interception members are extended toward the gate lines.

13. The thin film transistor array substrate of claim 1 wherein the buffer layer has a dielectric constant of 2-4.

14. A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly including gate lines, gate electrodes, and gate pads;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having contact holes exposing the gate pads;

a semiconductor pattern formed on the gate insulating layer;

an ohmic contact pattern formed on the semiconductor pattern;

a data line assembly formed on the ohmic contact pattern while bearing substantially the same shape as the ohmic contact pattern, the data line assembly including source electrodes, drain electrodes, data lines, and data pads;

a passivation pattern formed on the data line assembly with a CVD layer having dielectric constant 4.0 or less, the passivation pattern having

contact holes exposing the gate pads, the data pads, and the drain electrodes; and

a transparent electrode pattern electrically connected to the gate pads, the data pads, and the drain electrodes.

15. The thin film transistor array substrate of claim 14 further comprising:

storage capacitor lines formed at the same plane as the gate line assembly;

a storage capacitor semiconductor pattern overlapped with the storage capacitor lines while being placed at the same plane as the semiconductor pattern;

a storage capacitor ohmic contact pattern formed on the storage capacitor semiconductor pattern while bearing the same outline as the storage capacitor semiconductor pattern; and

a storage capacitor conductive pattern formed on the storage capacitor ohmic contact pattern while bearing the same outline as the storage capacitor semiconductor pattern;

wherein the storage capacitor conductive pattern is partially connected to the transparent electrode pattern.

16. The thin film transistor array substrate of claim 14 wherein the CVD layer has a dielectric constant of 2-4.

17. A method of fabricating a thin film transistor array substrate, the method comprising the steps of:

forming a gate line assembly, the gate line assembly including gate lines, gate electrodes connected to the gate lines, and gate pads connected to the gate lines;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data line assembly through depositing and patterning a conductive layer, the data line assembly including data lines crossing over the gate lines, data pads connected to the data lines, source electrodes connected to the data lines while being placed close to the gate electrodes, and drain electrodes facing the source electrodes around the gate electrodes;

forming a passivation layer through depositing a CVD layer having dielectric constant 4.0 or less;

patterning the gate insulating layer together with the passivation layer to thereby form contact holes exposing the gate pads, the data pads, and the drain electrodes; and

depositing and patterning a transparent conductive layer to thereby form subsidiary gate pads connected to the gate pads, subsidiary data pads connected to the data pads, and pixel electrodes connected to the drain electrodes.

18. The method of claim 17 wherein the passivation layer is formed through PECVD using a gaseous material selected from the group consisting of $SiH(CH_3)_3$, $SiO_2(CH_3)_4$ and $(SiH)_4O_4(CH_3)_4$ as a basic source

while introducing an oxide agent of N_2O or O_2.

19. The method of claim 17 wherein the passivation layer is formed through PECVD using a gaseous material selected from the group consisting of SiH_4 and SiF_4 as a basic source while adding CF_4 and O_2 thereto.

20. The method of claim 17 wherein the data line assembly and the semiconductor layer are formed through photolithography using a photoresist pattern with a first portion bearing a predetermined thickness, a second portion bearing a thickness larger than the thickness of the first portion, and a third portion bearing a thickness smaller than the thickness of the first portion.

21. The method of claim 20 wherein the first photoresist pattern portion is placed between the source and the drain electrodes, and the second photoresist pattern portion is placed over the data line assembly.

22. The method of claim 17 wherein the step of forming the gate insulating layer comprises the sub-steps of first depositing a CVD layer having dielectric constant 4.0 or less, and second depositing a silicon nitride layer, the first and second sub-steps being performed in a vacuum state.

23. A method of fabricating a thin film transistor array substrate, the method comprising the steps of:

(a) forming a data line assembly on an insulating substrate, the data line assembly including data lines;

(b) forming color filters of red, green and blue at the substrate;

(c) forming a buffer layer through depositing a CVD layer having dielectric constant 4.0 or less such that the buffer layer covers the data line assembly and the color filters;

(d) forming a gate line assembly on the insulating layer, the gate line assembly including gate lines, and gate electrodes;

(e) forming a gate insulating layer such that the gate insulating layer covers the gate line assembly;

(f) forming an island-shaped ohmic contact pattern and an island-shaped semiconductor pattern on the gate insulating layer while forming first contact holes at the gate insulating layer and the buffer layer such that the contact holes partially expose the data lines;

(g) forming a pixel line assembly, the pixel line assembly including source and drain electrodes formed on the island-shaped ohmic contact pattern at the same plane while being separated from each other, and pixel electrodes connected to the drain electrodes; and

(h) dividing the ohmic contact pattern into two pattern parts through removing the portions of the ohmic contact pattern exposed between the source and the drain electrodes.

24. The method of claim 23 wherein the (f) step comprises the sub-steps of:

sequentially depositing an amorphous silicon layer and an impurities-doped amorphous silicon layer onto the gate insulating layer;

forming a photoresist pattern such that the photoresist pattern has a

first portion covering a predetermined area of the gate electrode with a predetermined thickness, and a second portion covering the remaining area except for the regions of first contact holes to be formed later with a thickness smaller than the thickness of the first portion;

etching the impurities-doped amorphous silicon layer, the amorphous silicon layer, the gate insulating layer and the buffer layer using the first and second portions of the photoresist pattern as a mask to thereby form the first contact holes;

removing the second portion of the photoresist pattern;

etching the impurities-doped amorphous silicon layer and the amorphous silicon layer using the first portion of the photoresist pattern as a mask to thereby form the island-shaped semiconductor pattern and the island-shaped ohmic contact pattern; and

removing the first portion of the photoresist pattern.

25. The method of claim 17 wherein the CVD layer has a dielectric constant of 2-4.

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FIG.1

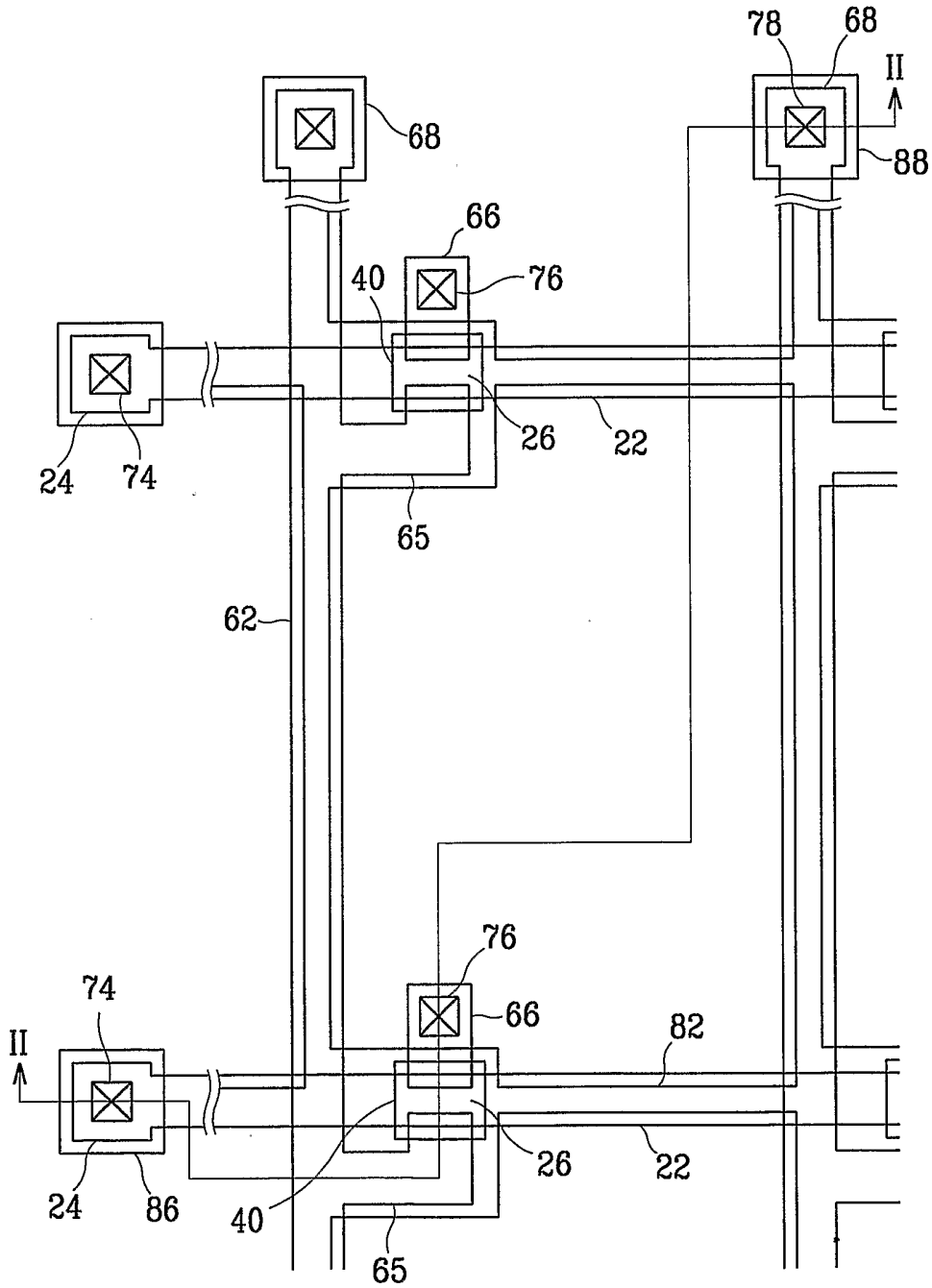

78
68
II
68
88
66
40
76
24
74
26
22
65
62
76
74
66
82
II
26
22
24
86
40
65

FIG.2

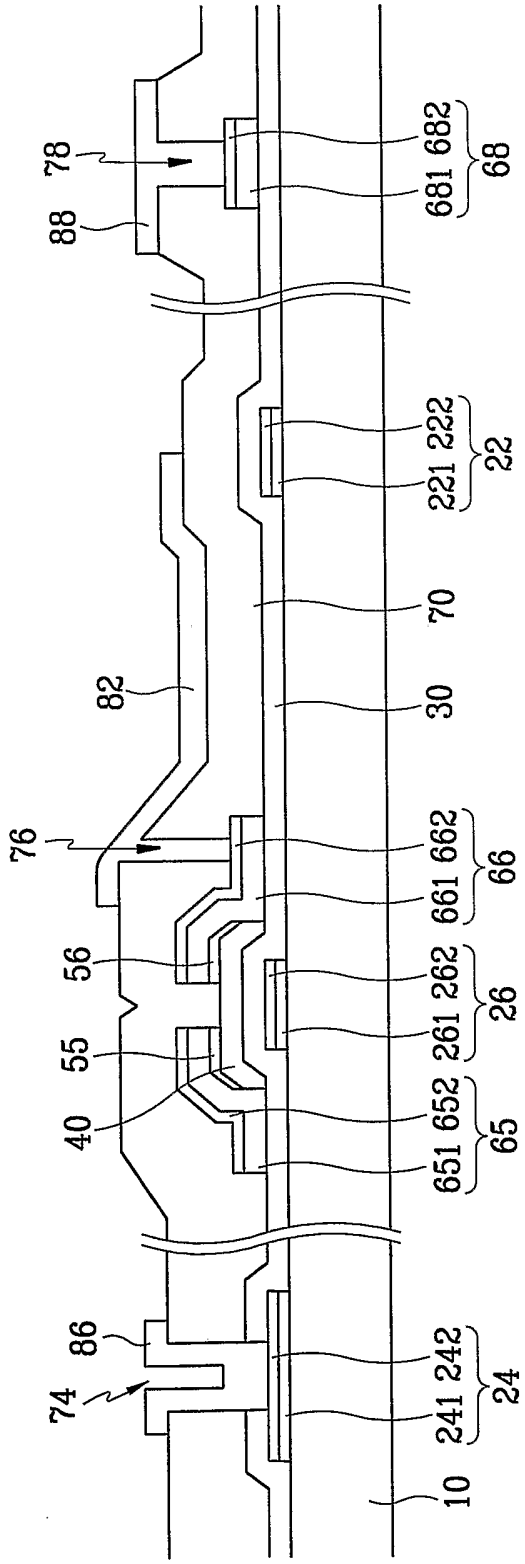

78
88
681 682
68
221 222
22
70
82
30
76
661 662
66
56
261 262
26
55
40
651 652
65
86
74
241 242
24
10

FIG.3A

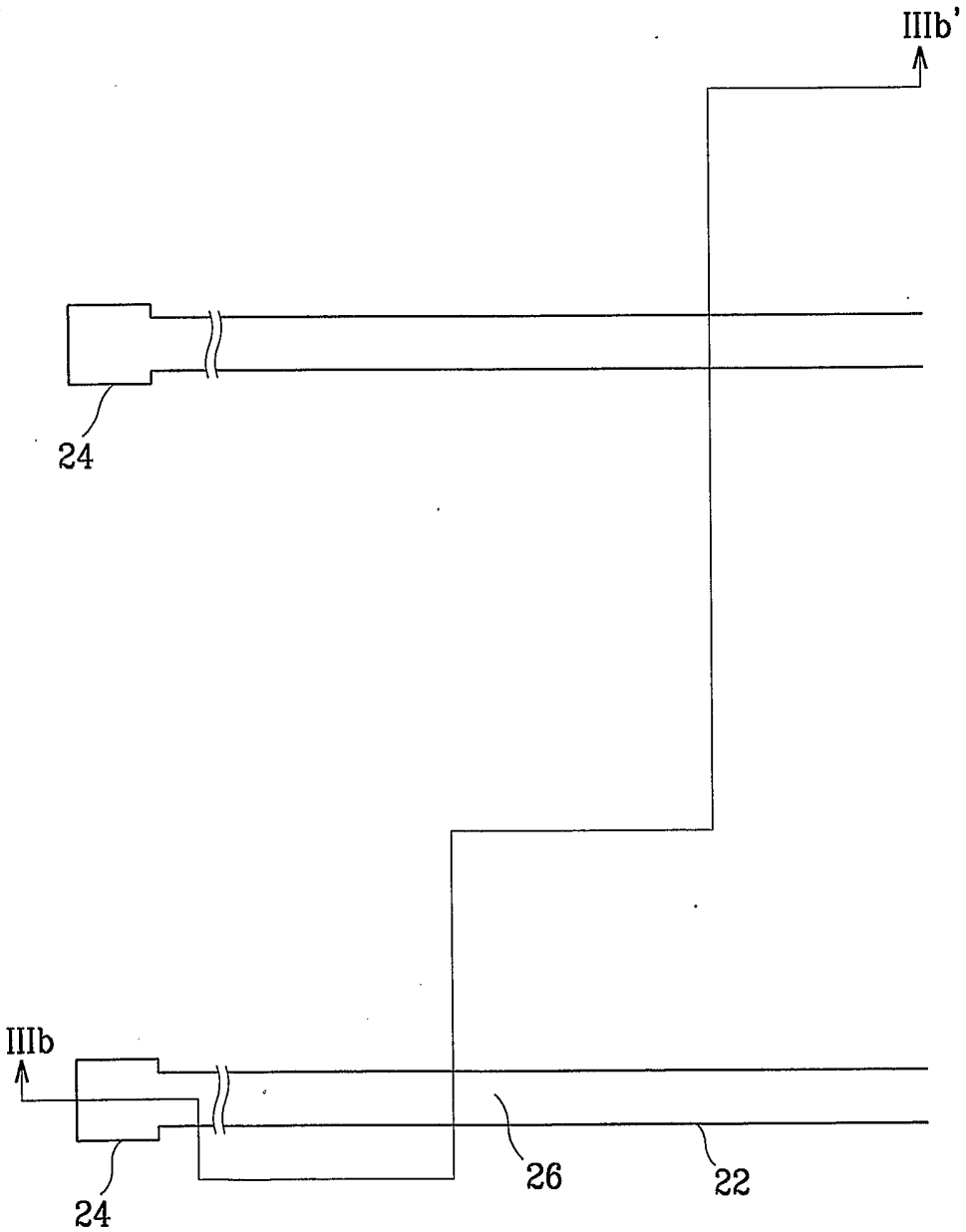


FIG.3B

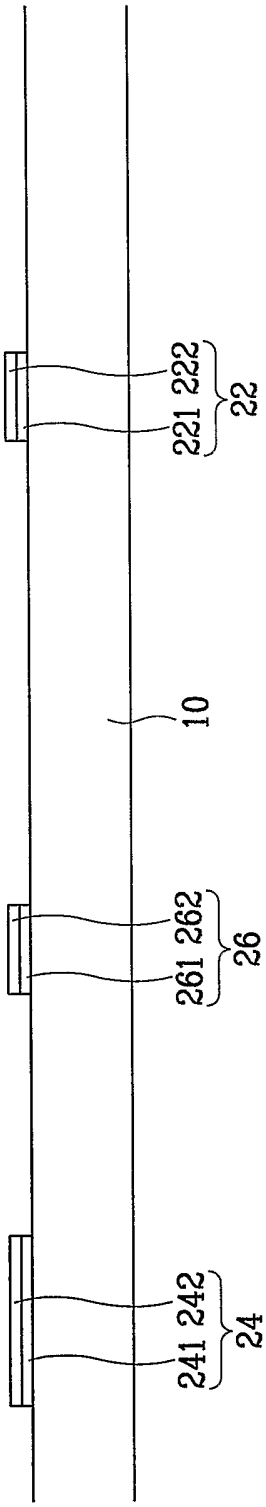


FIG.4A

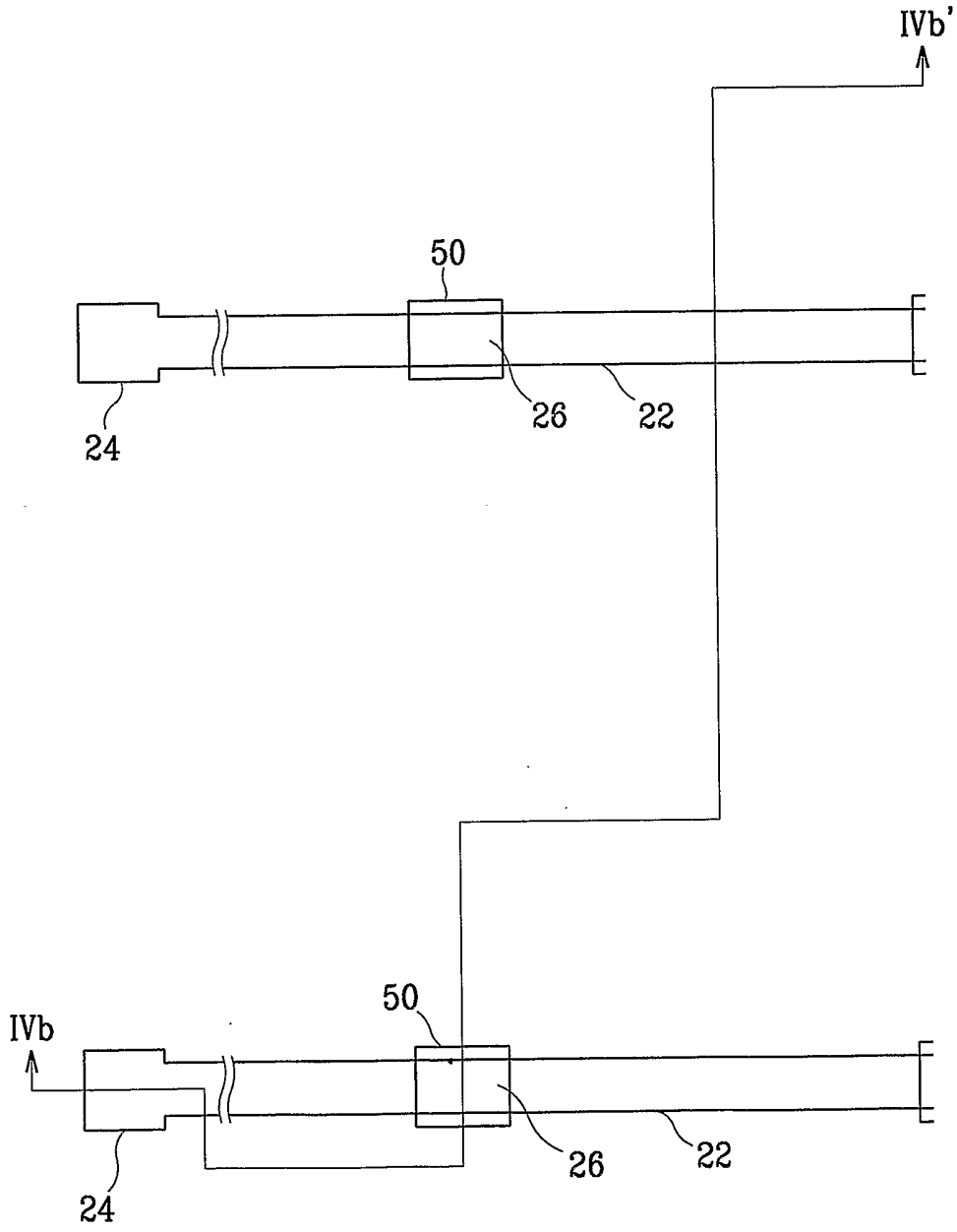
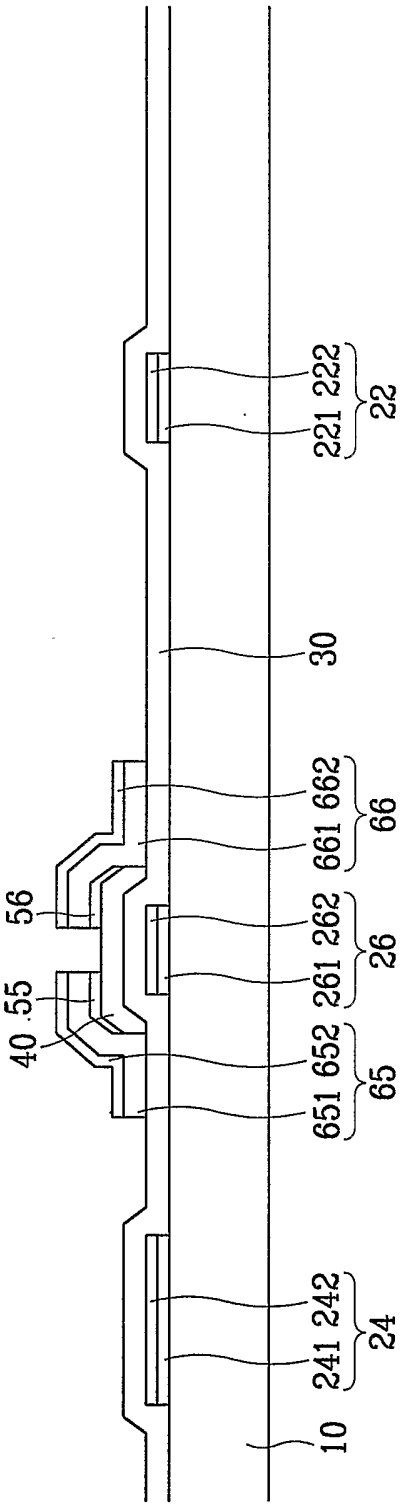


FIG.4B


222
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56
262
261
26
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40
652
651
65
242
241
24
10

FIG.5A

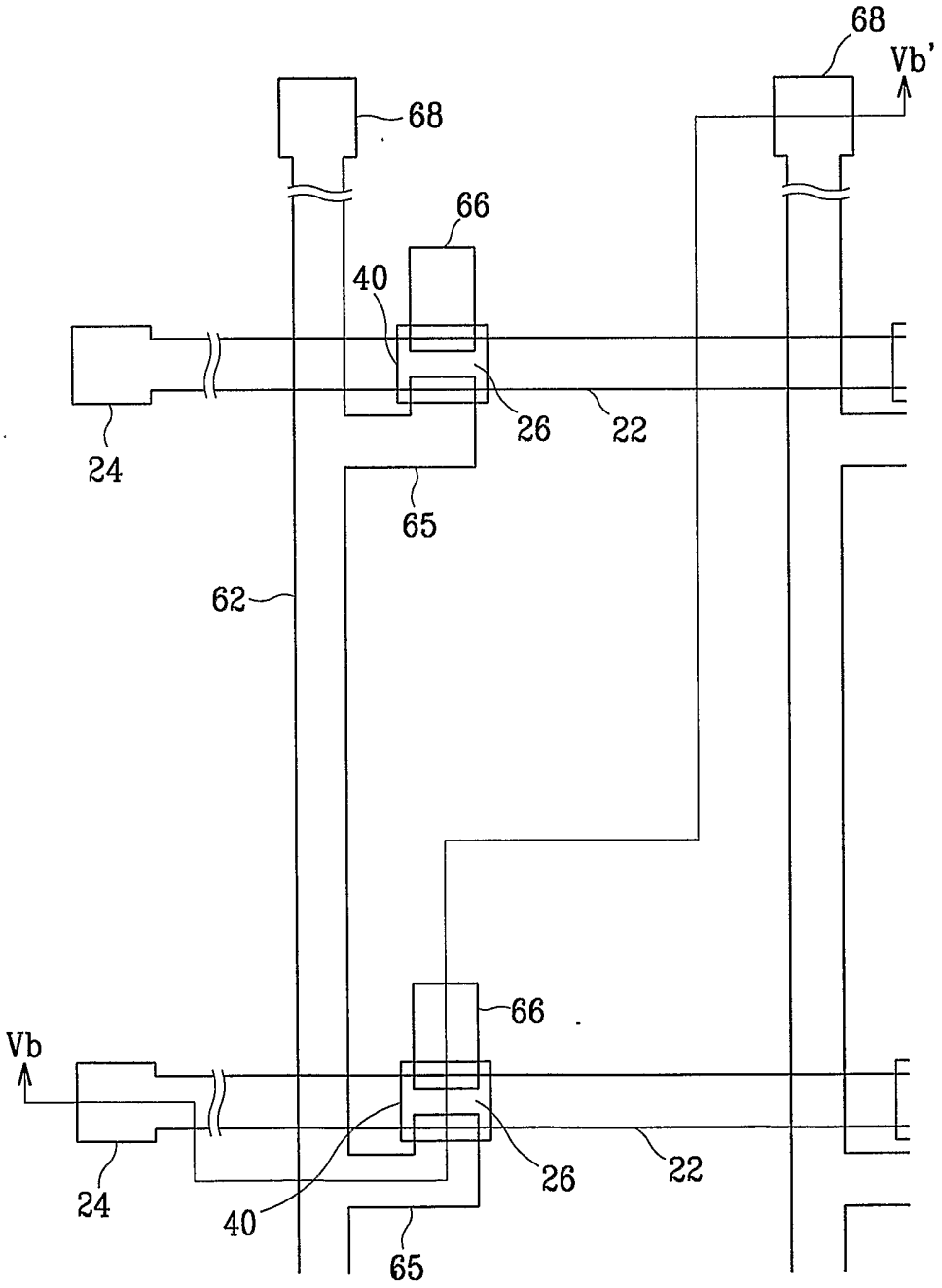
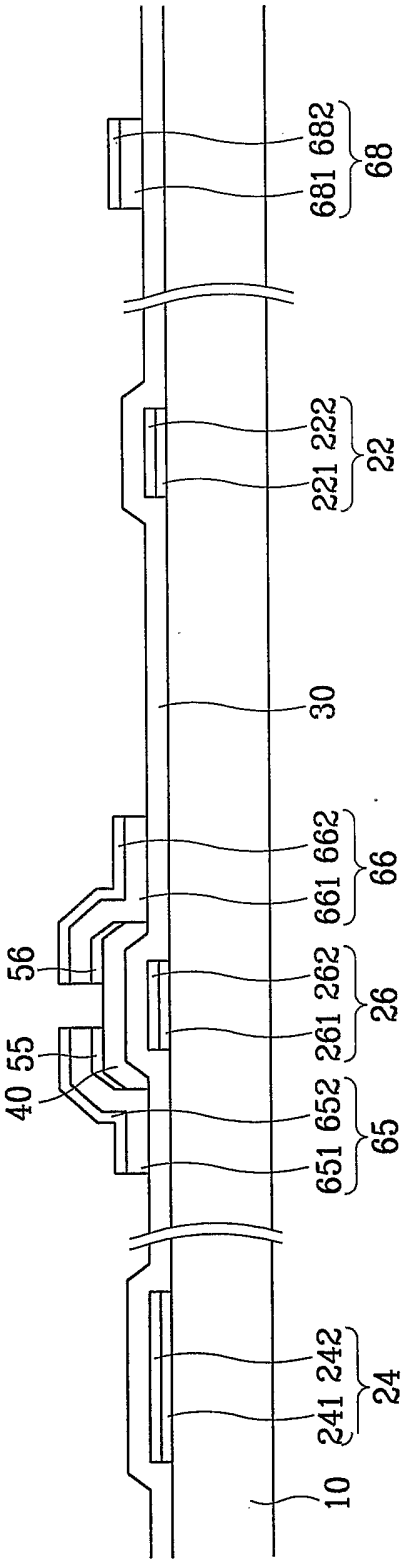


FIG.5B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222
221
22
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261
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55
652
651
65
242
241
24
10

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FIG.6A

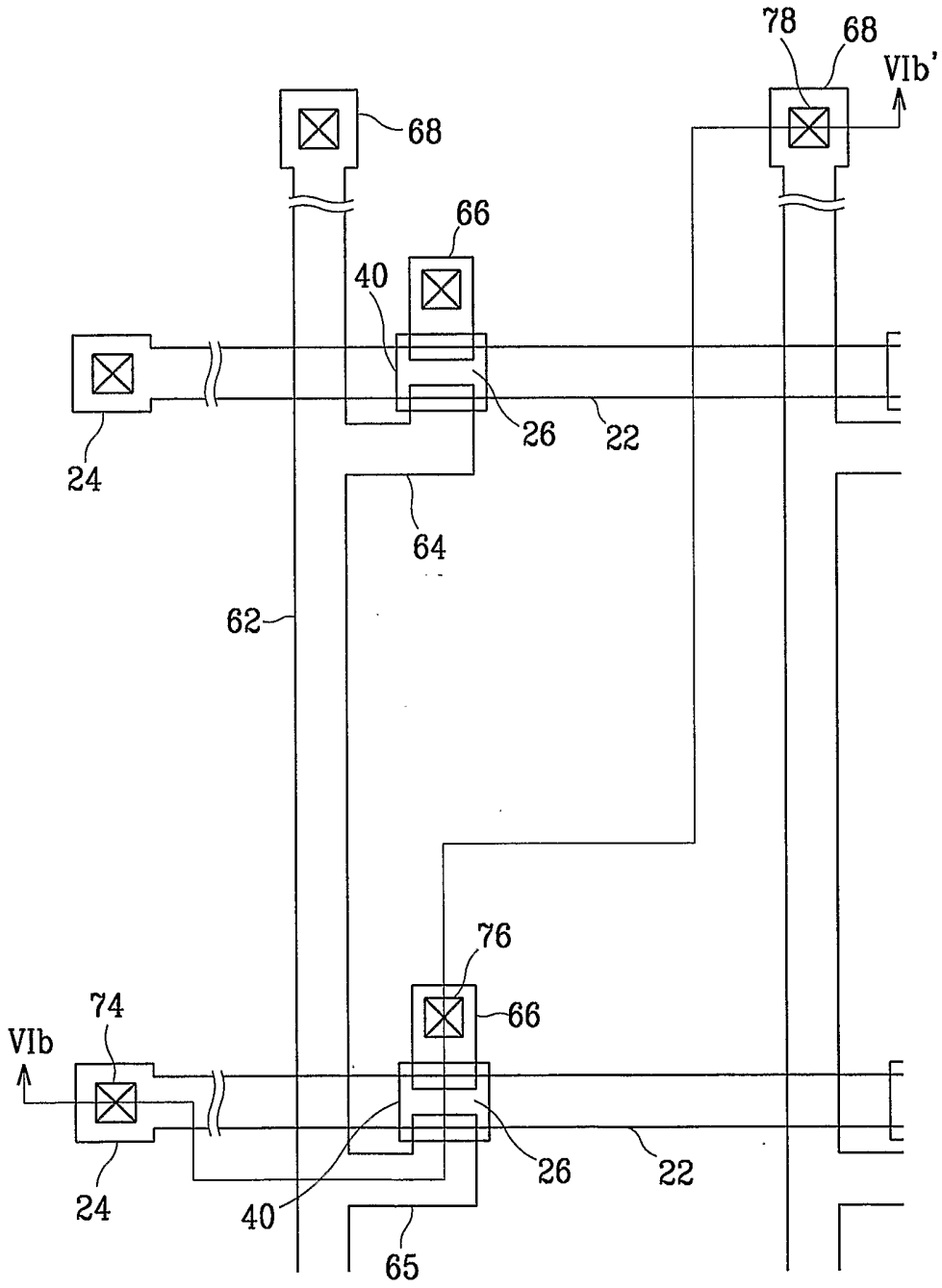
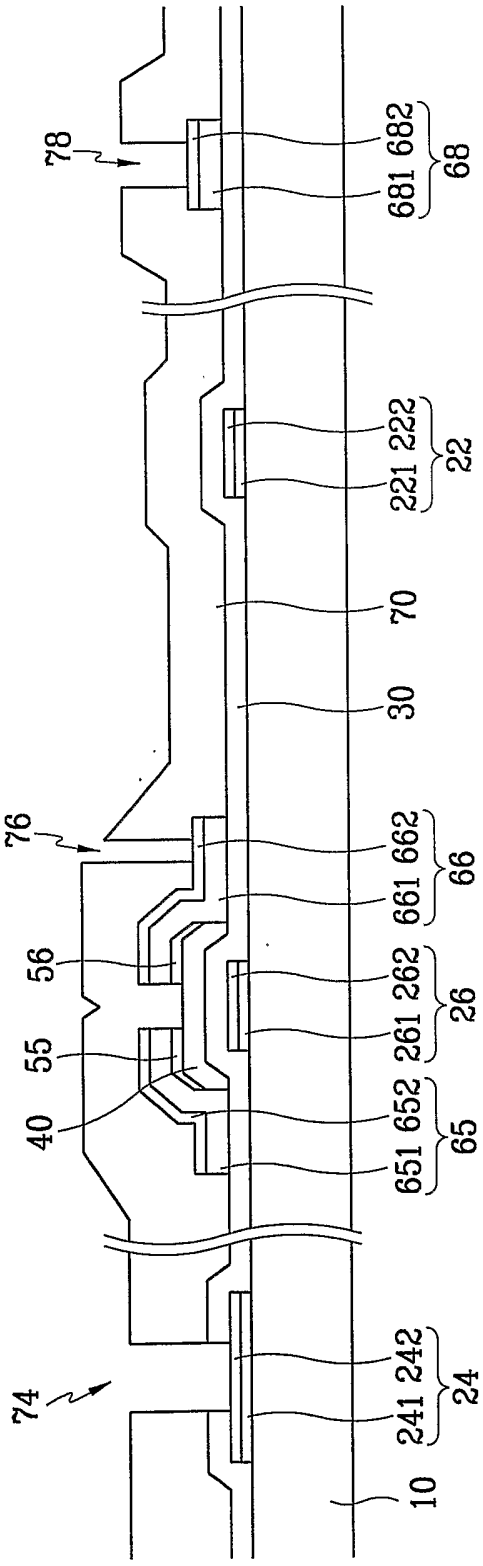


FIG.6B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681 682
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221 222
22
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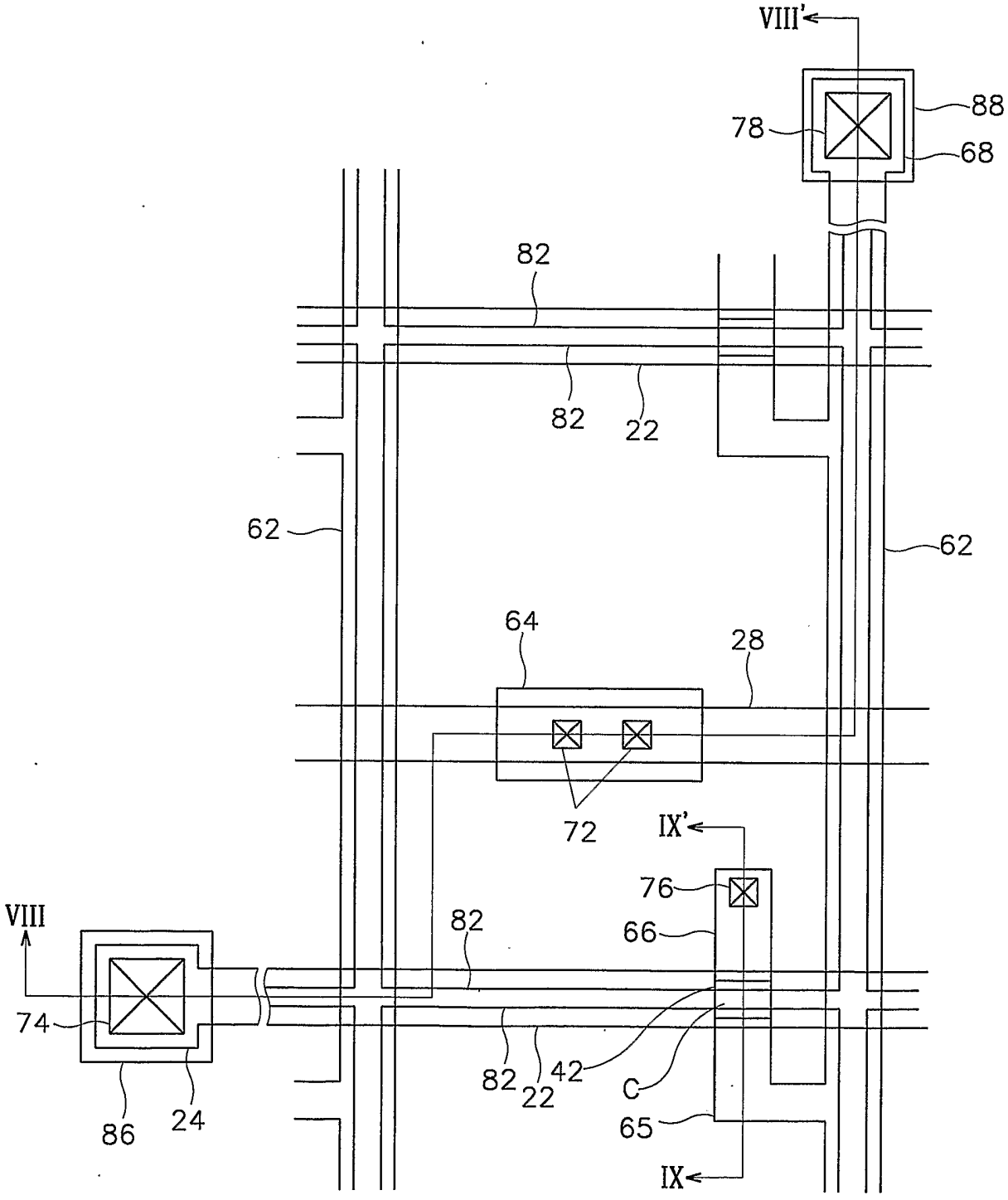
661 662
66
56
261 262
26
55
40
651 652
65
74
241 242
24
10

FIG.7


VIII'
88
78
68
82
82
22
62
62
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72
IX'
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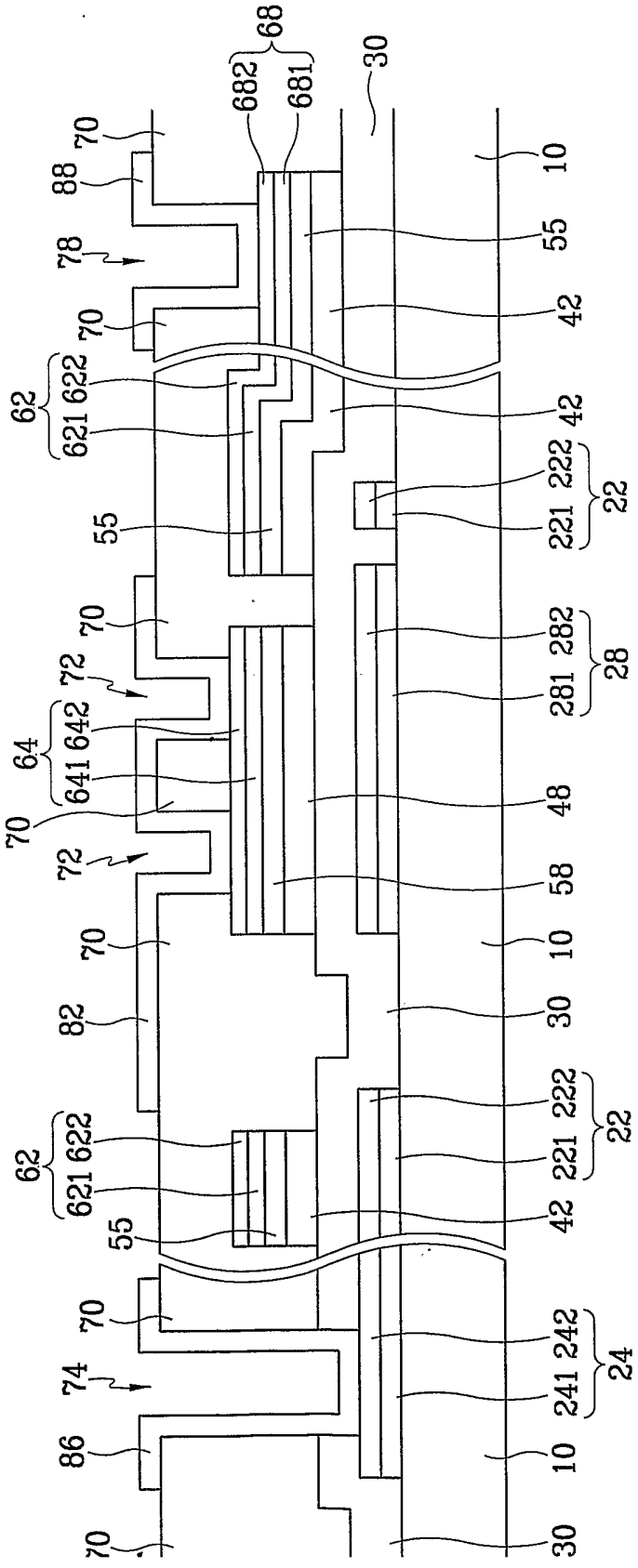
VIII
82
66
74
82
22
42
C
86
24
65
IX

FIG.8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682
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62
622
621
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42
222
221
22
72
642
641
64
48
58
10
82
241
242
24
74
86

FIG.9

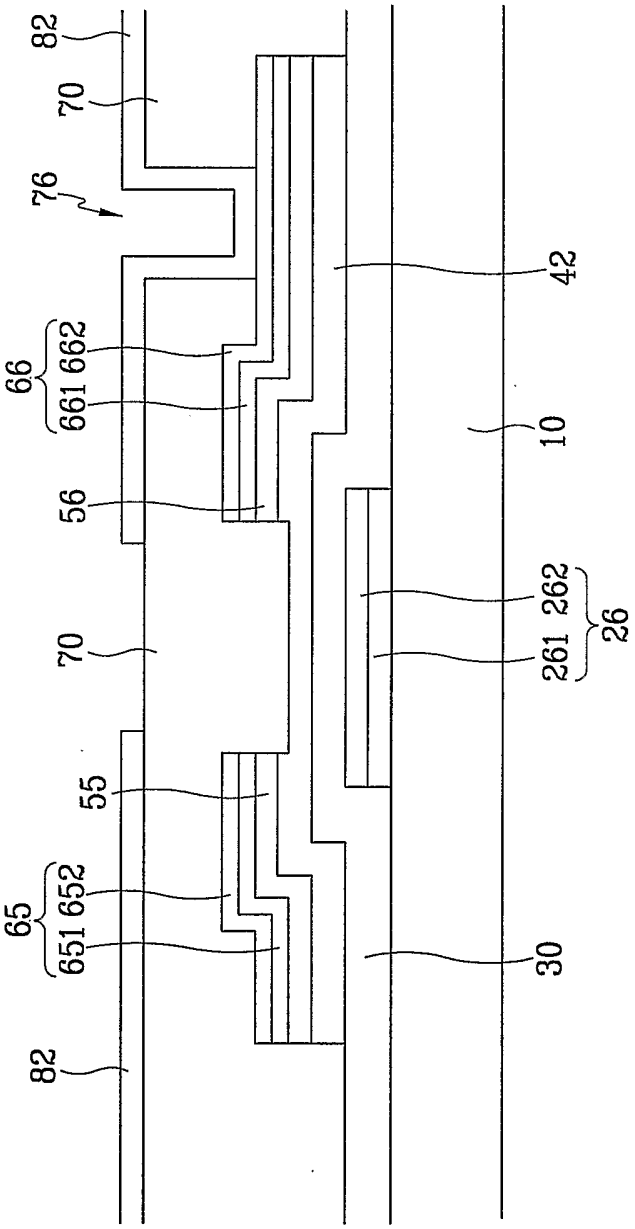

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FIG.10A

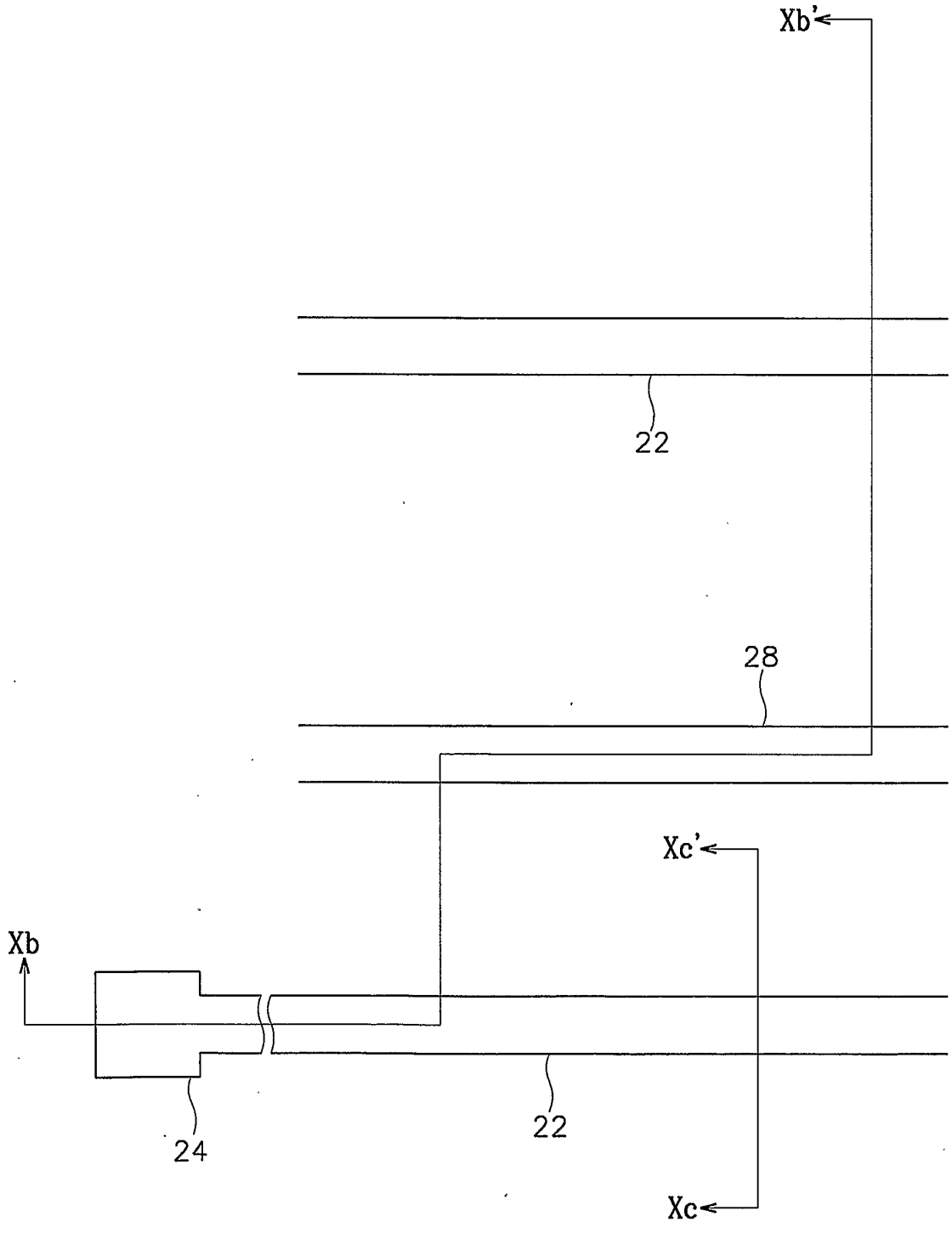


FIG.10B

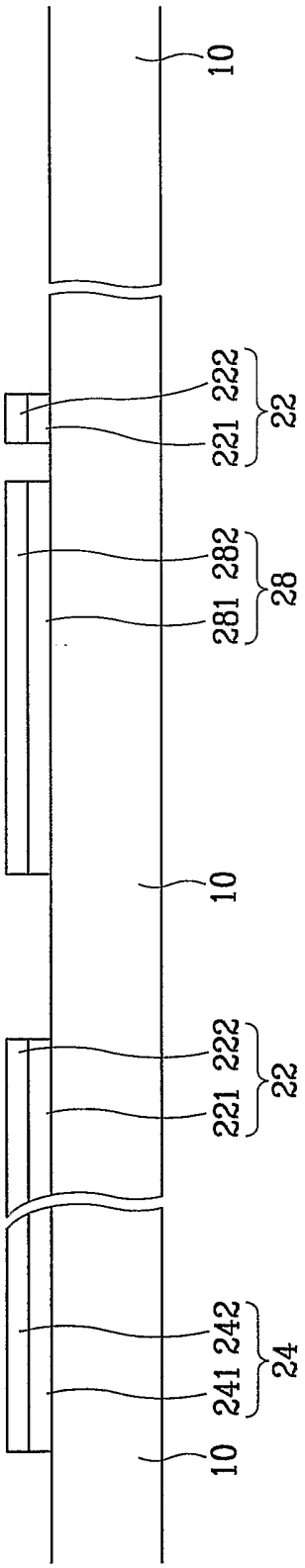


FIG.10C

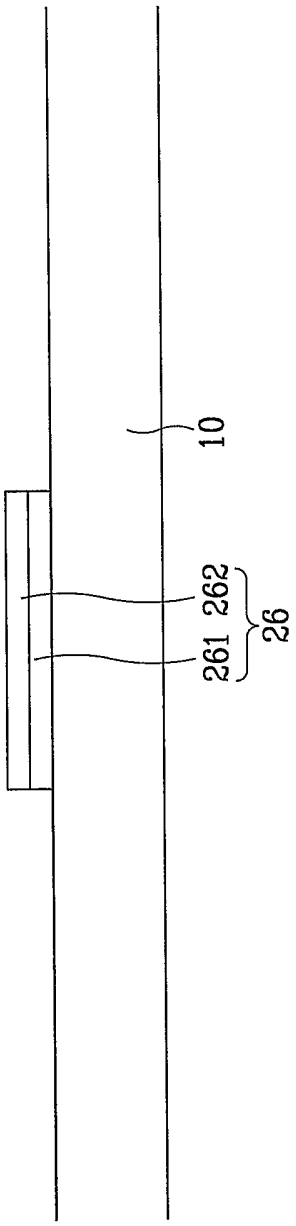
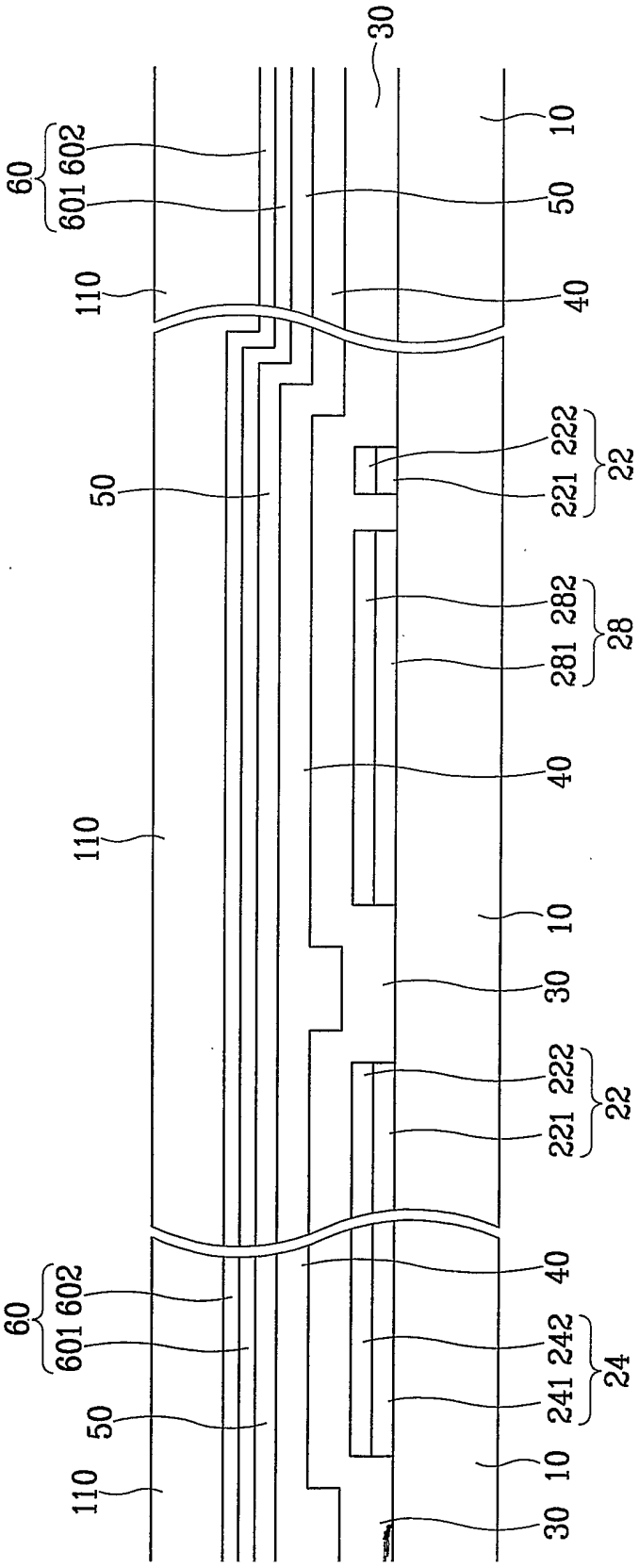


FIG.11A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221
22
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281
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221
22
40
60
602
601
242
241
24
50
110
10
30

FIG.11B

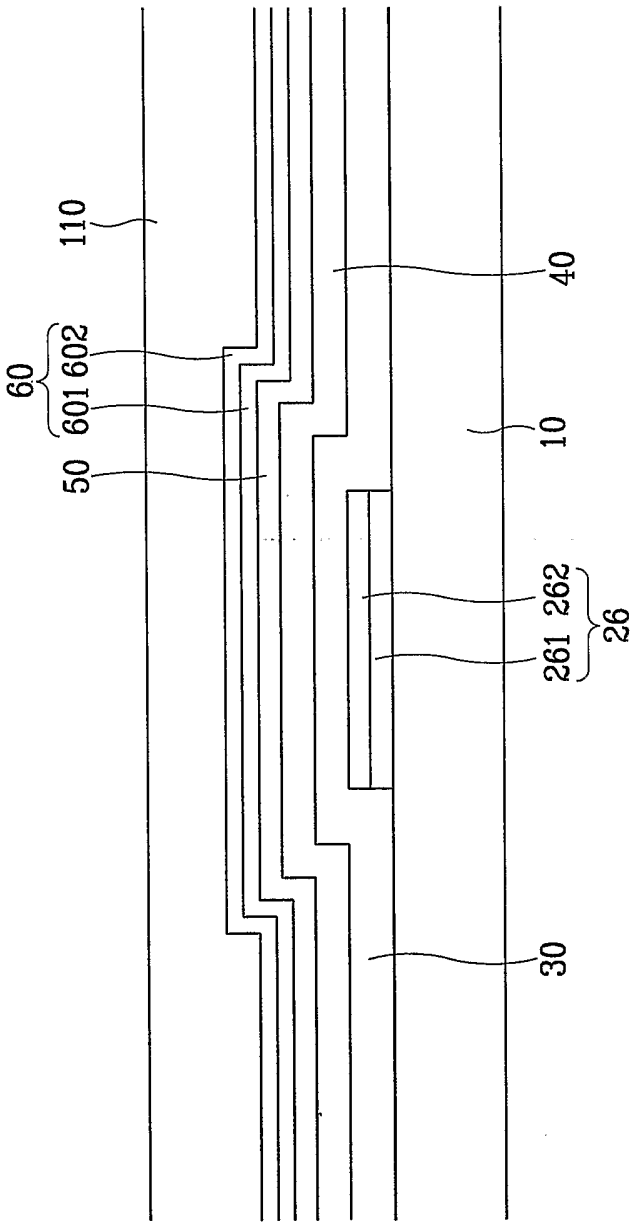


FIG.12A

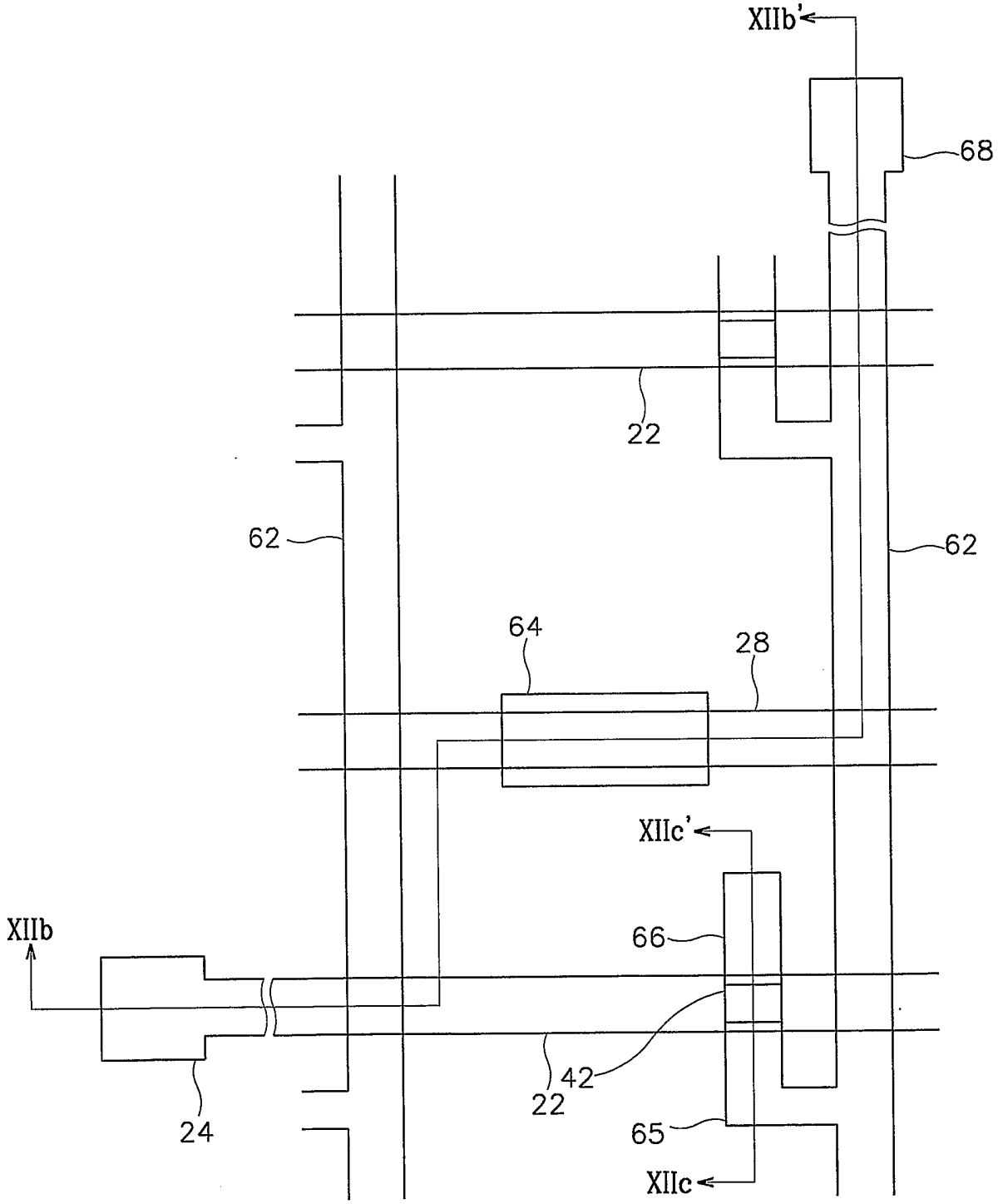
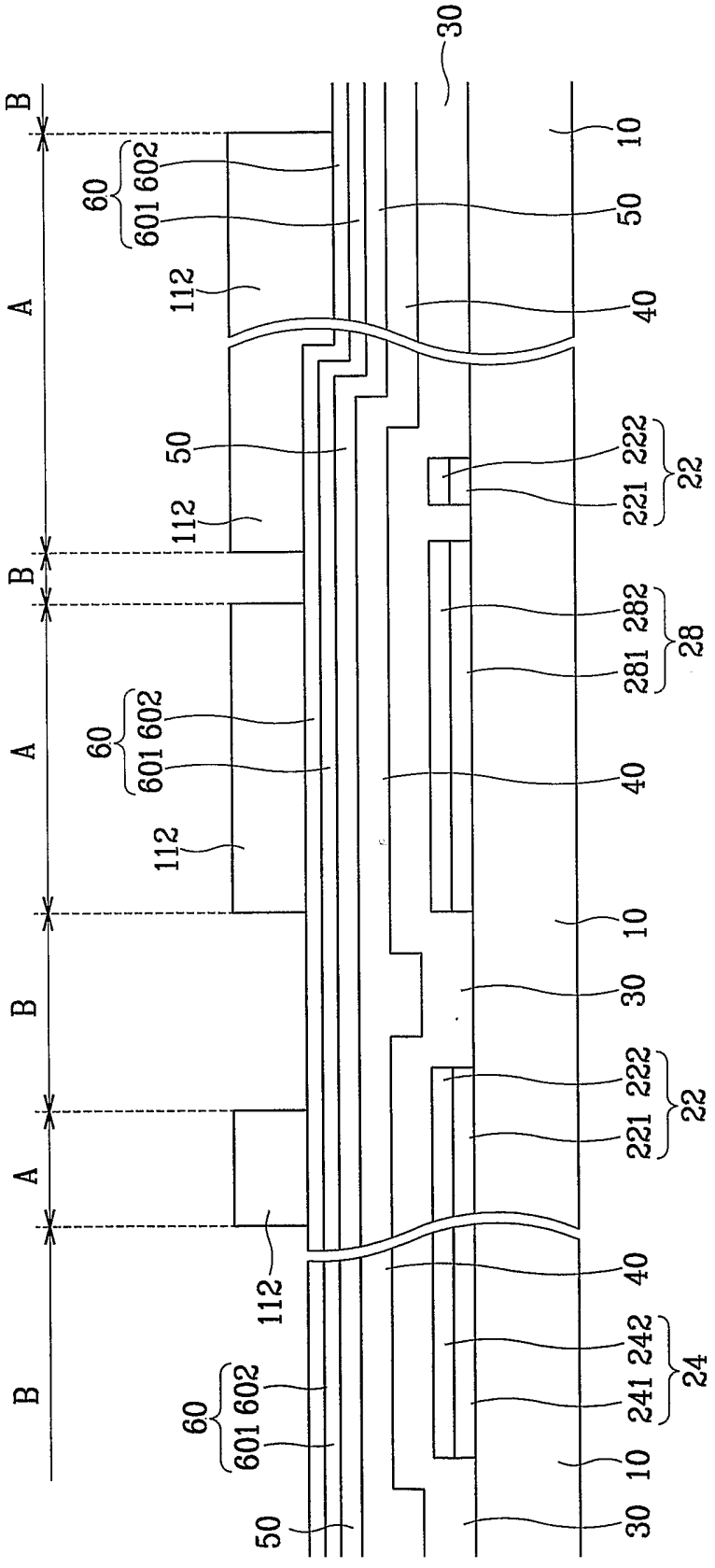


FIG.12B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B
A
B
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B
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B
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50
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10
22
221 222
28
281 282
24
241 242

FIG.12C

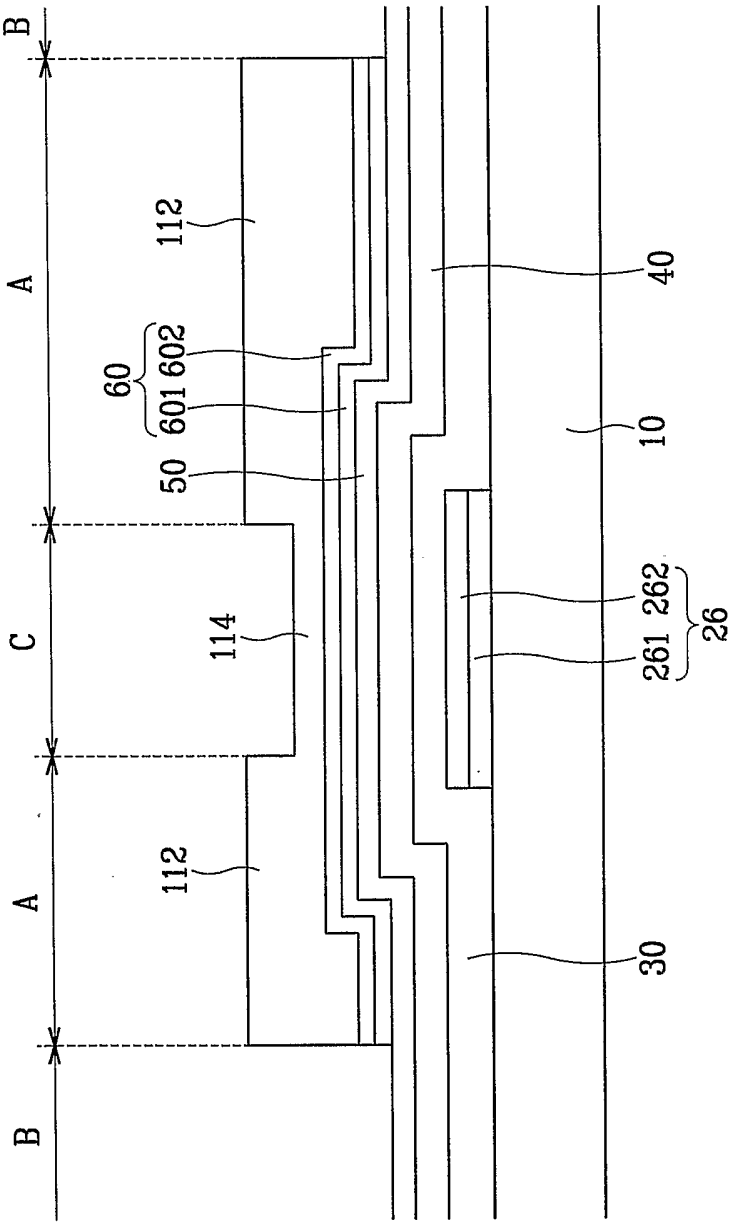
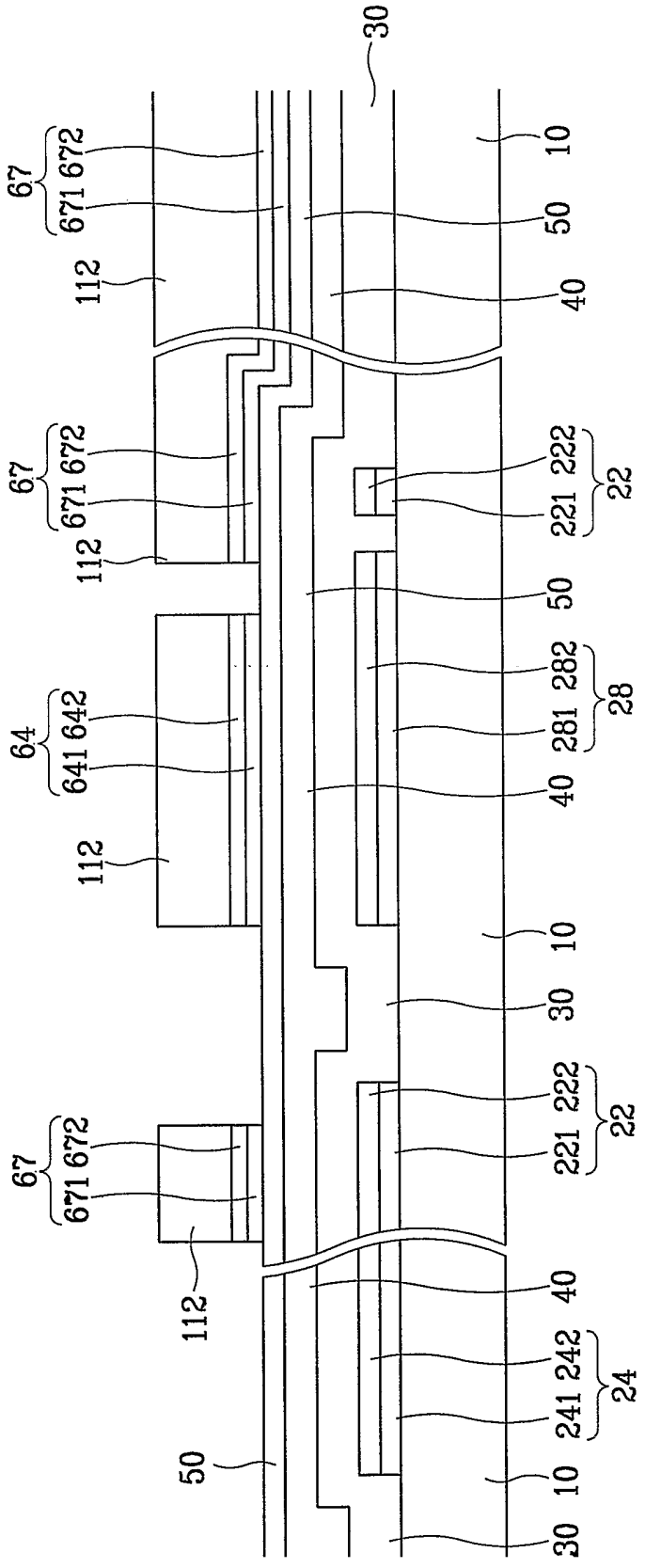


FIG.13A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112
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22
50
64
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641
112
282
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672
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112
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22
40
242
241
24
50
10
30

FIG.13B

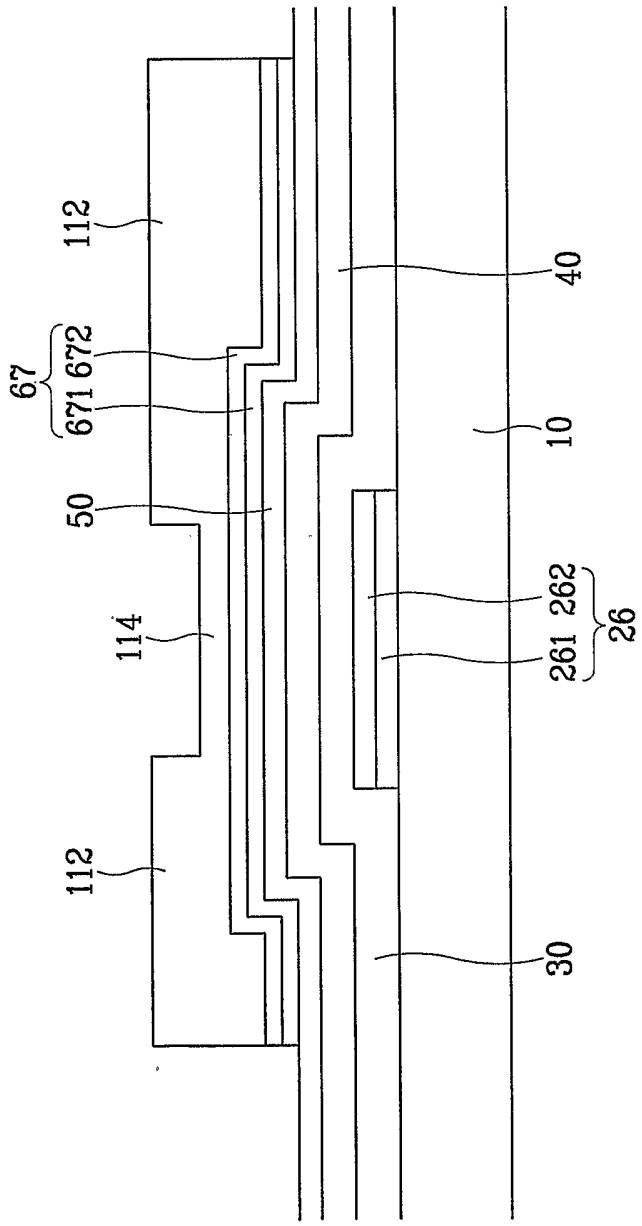
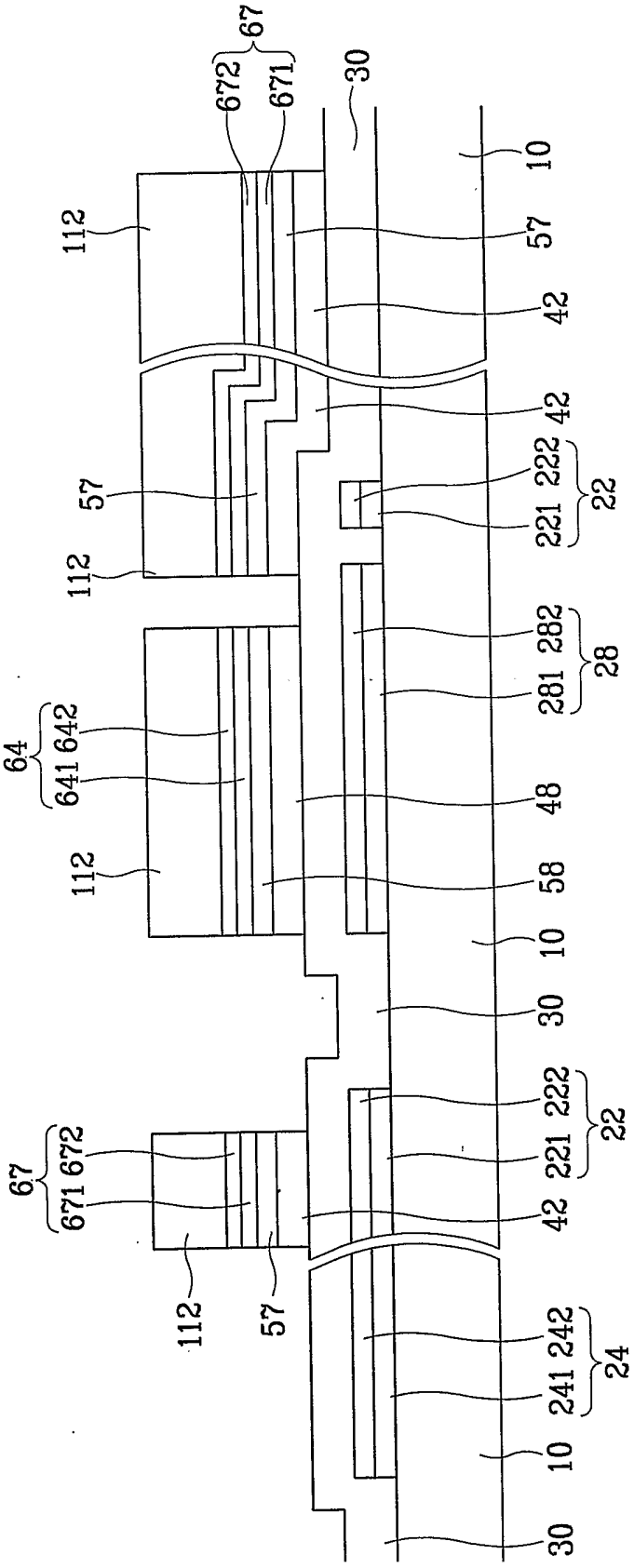


FIG.14A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22
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112
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42
112
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242
241
24
10
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FIG.14B

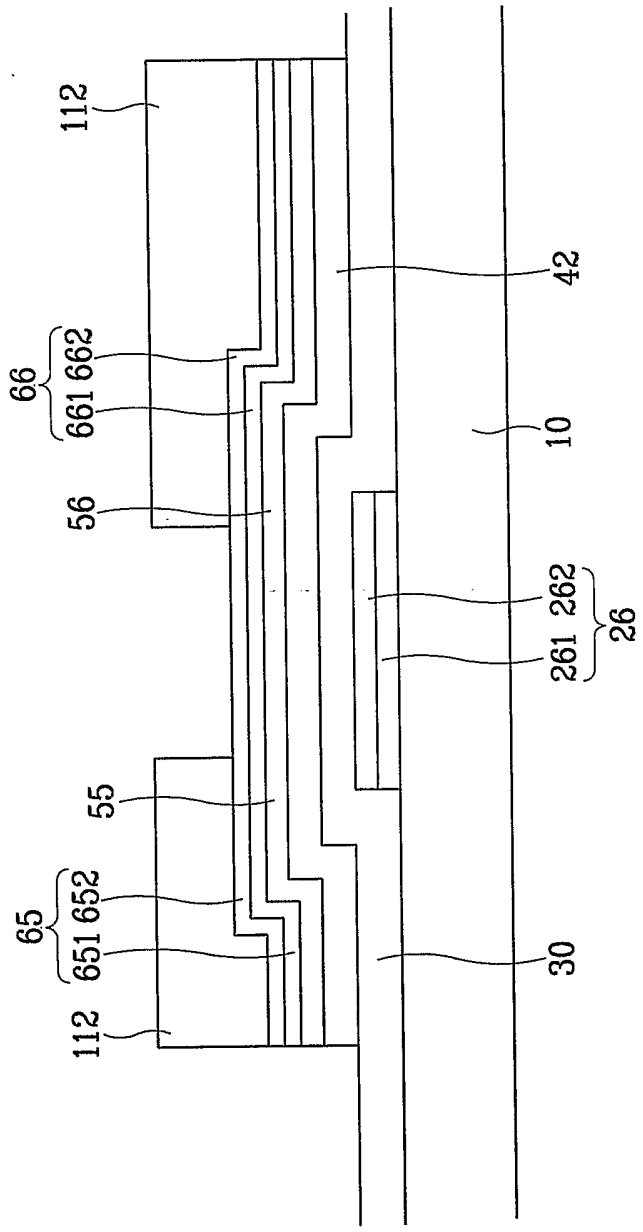
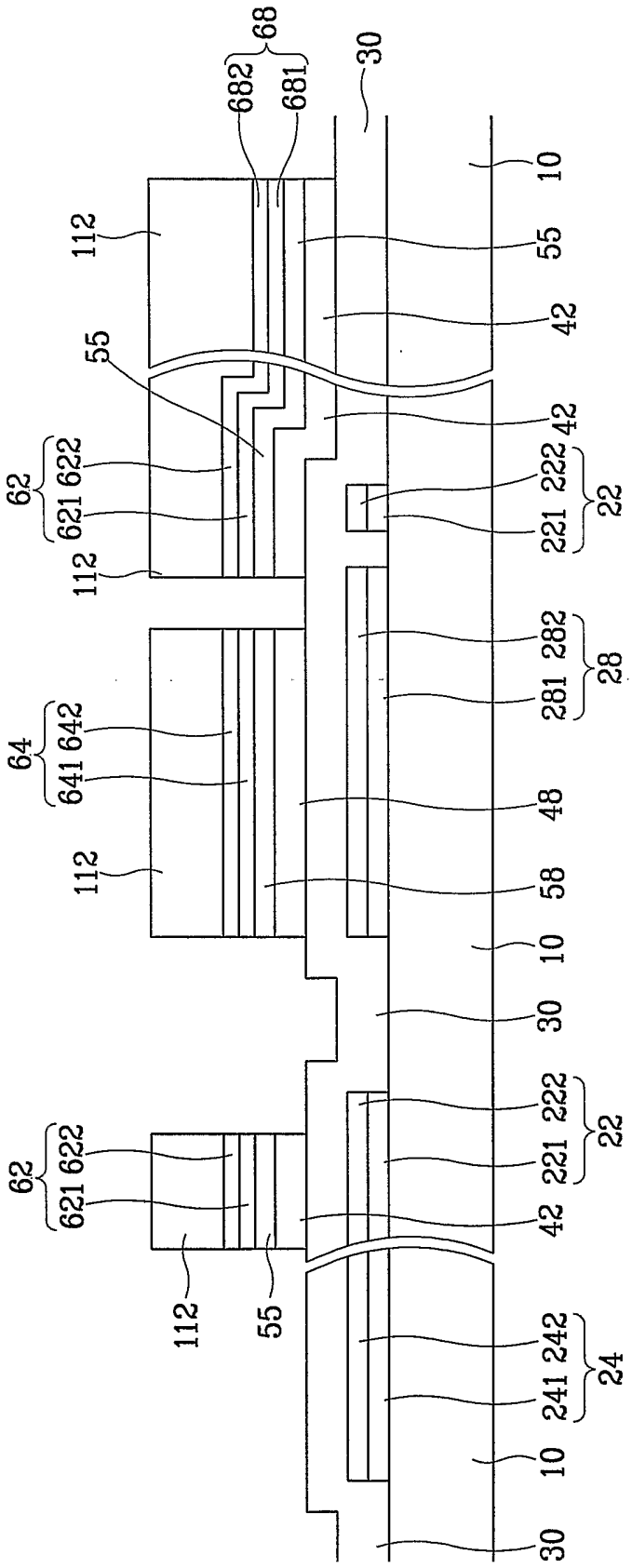


FIG.15A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642
641
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241
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FIG.15B

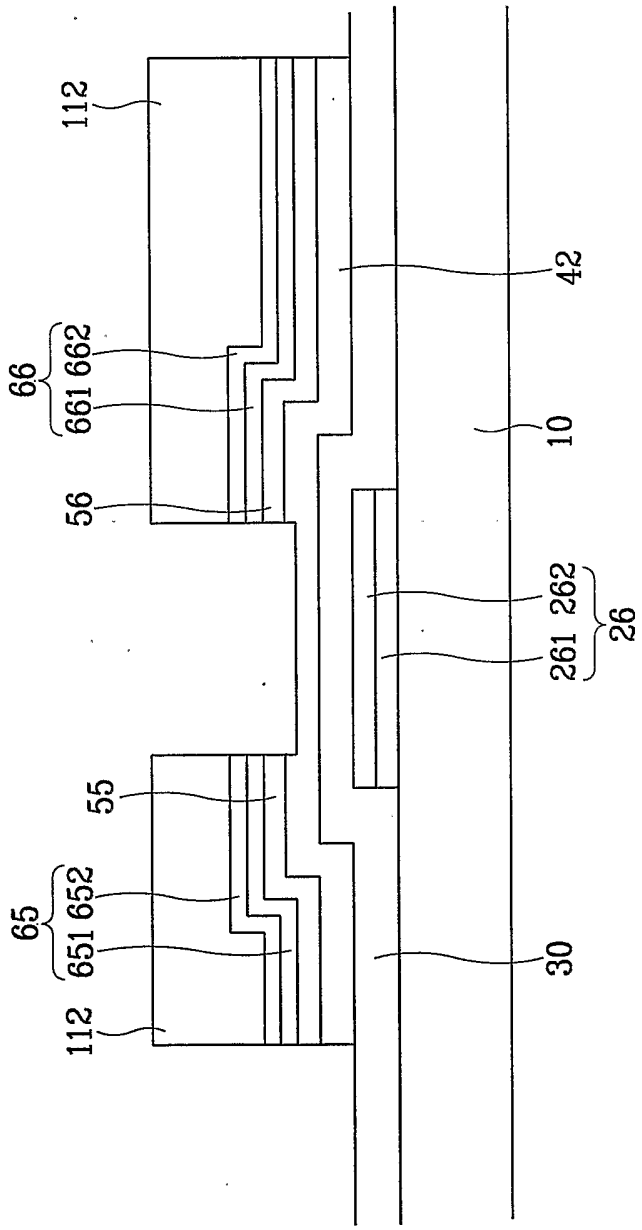
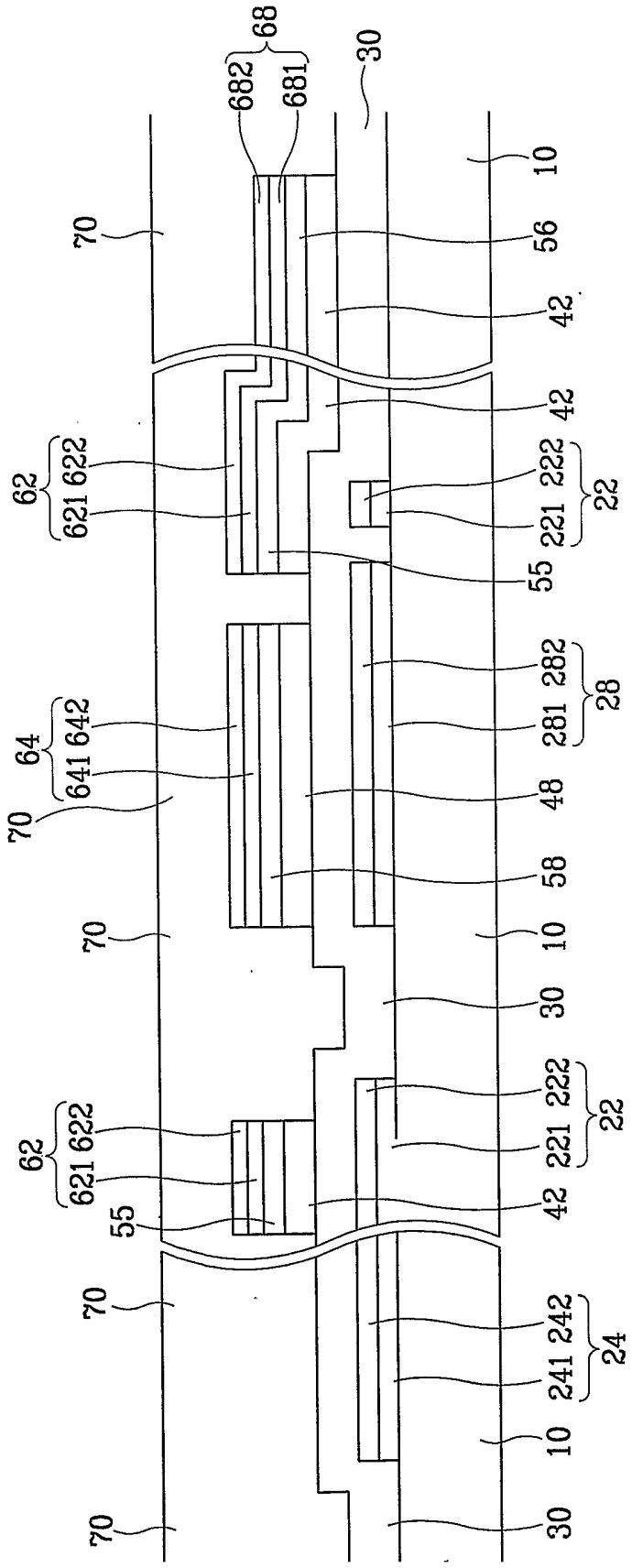


FIG.16A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282
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42
70
242
241
24
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70
30

FIG.16B

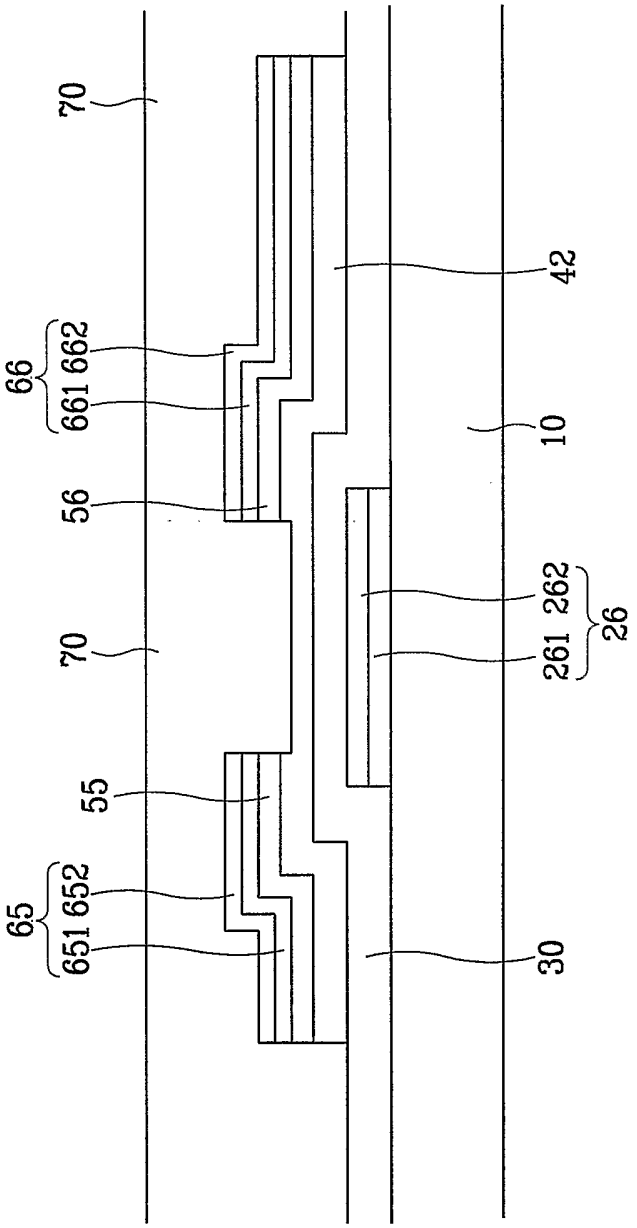
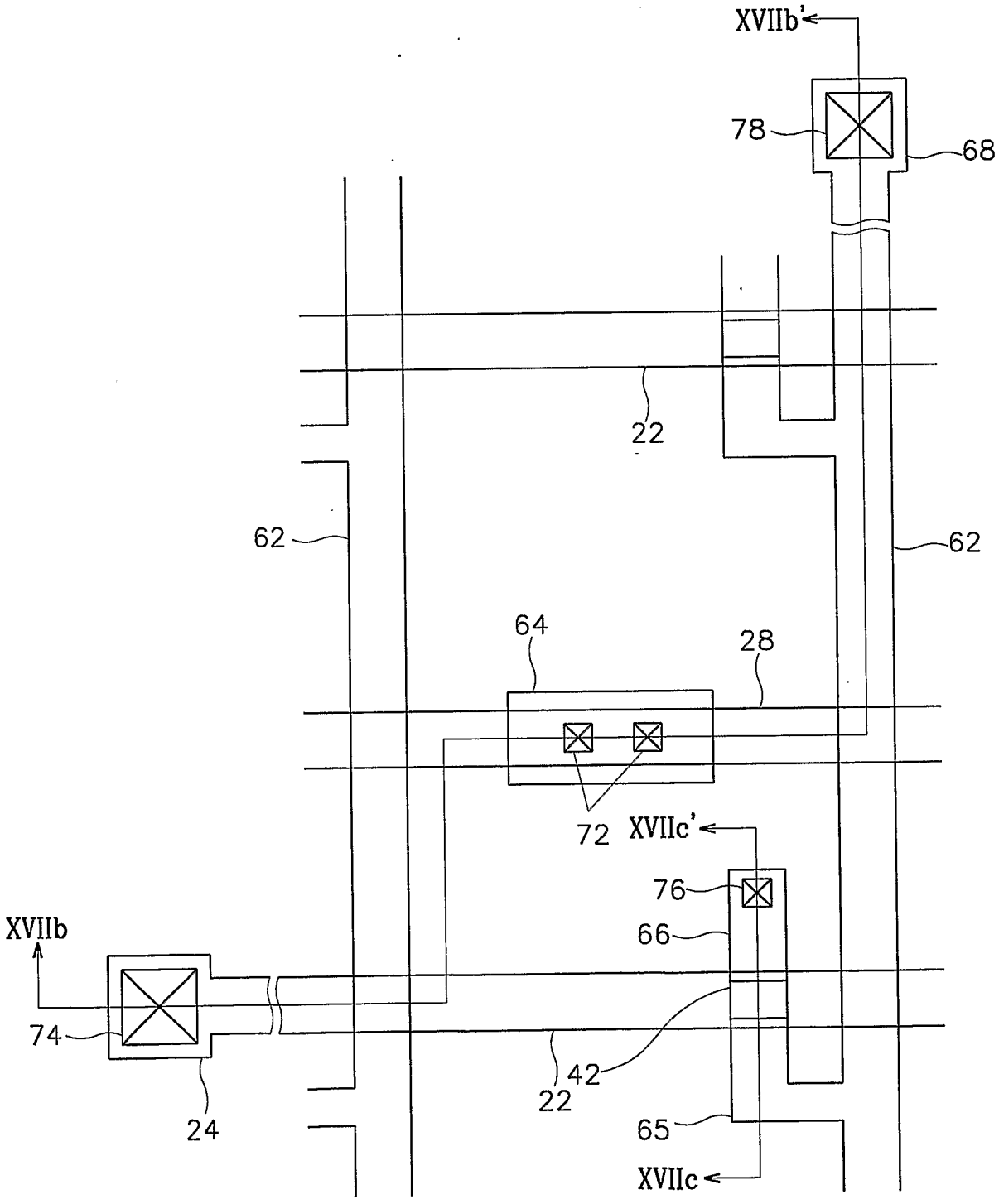


FIG.17A


XVIIb'
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68
22
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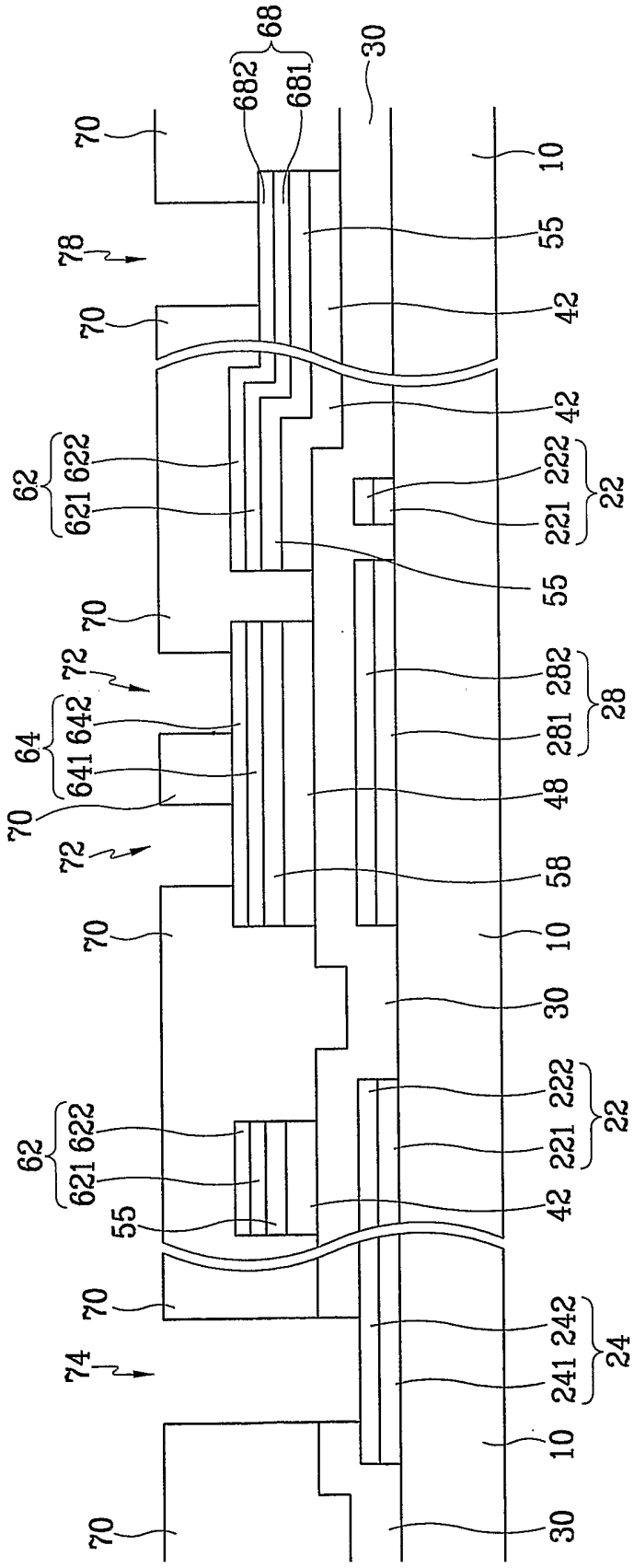
28
72
XVIIc'
76
66
XVIIb
74
24
22
42
65
XVIIc

FIG.17B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48
58
74
24
242
241

FIG.17C

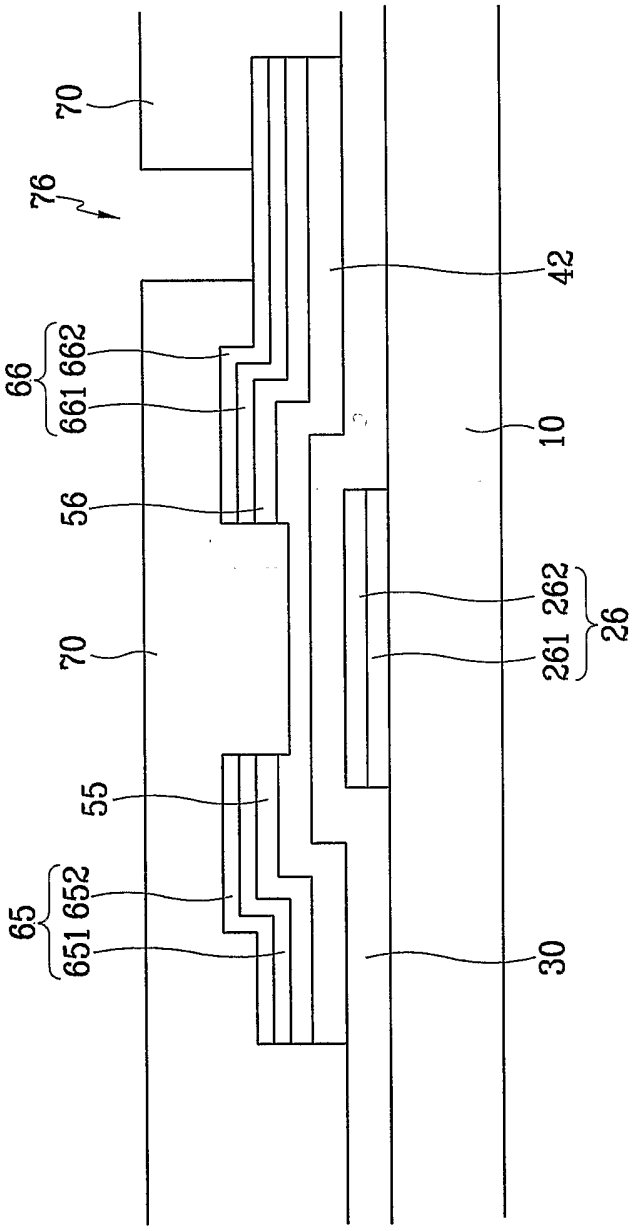
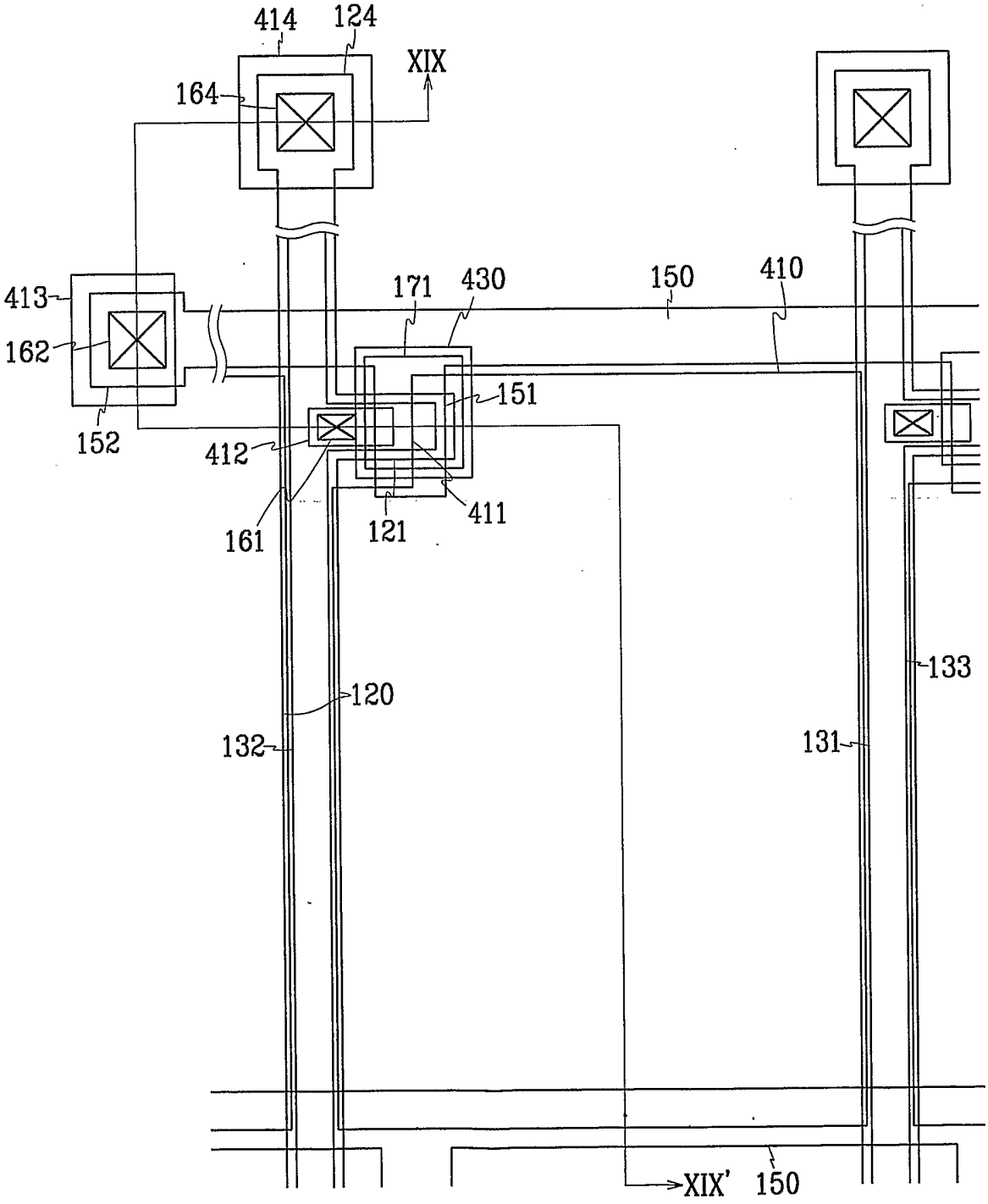


FIG.18


414
124
XIX
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413
162
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151
412
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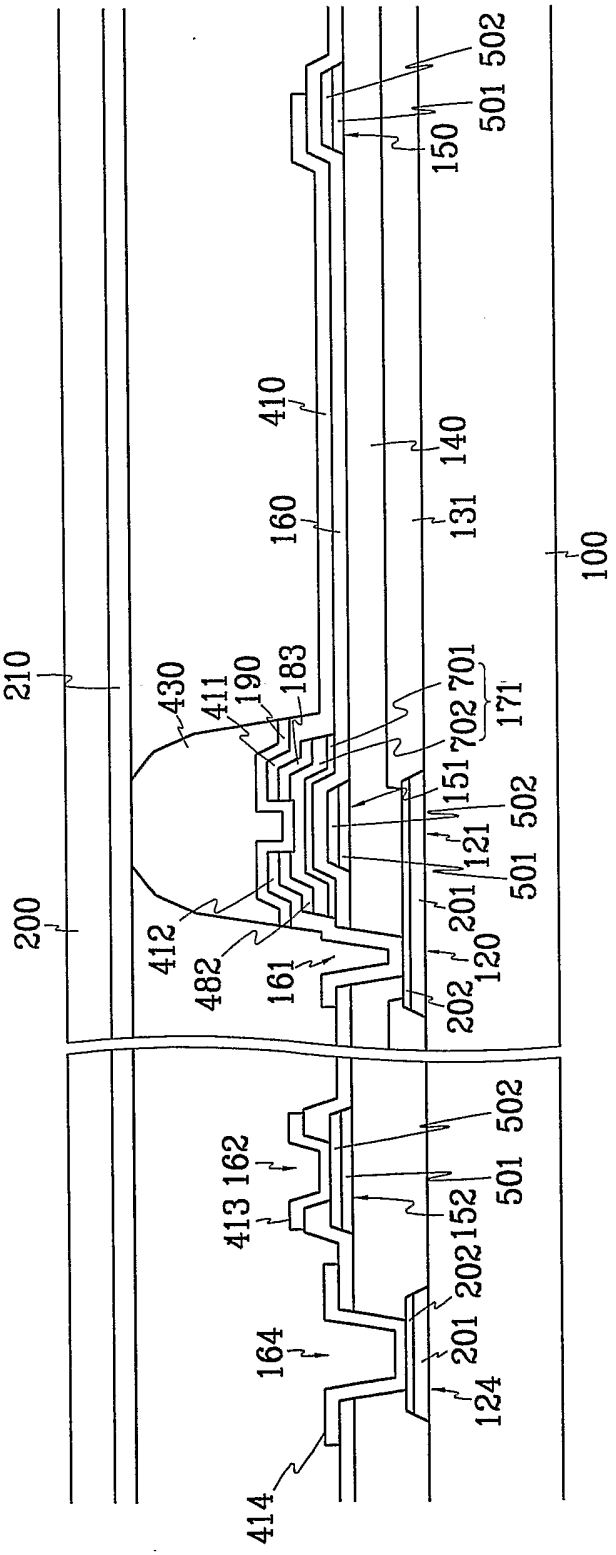
121
411
133
120
132
131
XIX'
150

FIG.19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140
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121
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201
202
162
413
152
164
124
414

FIG.20A

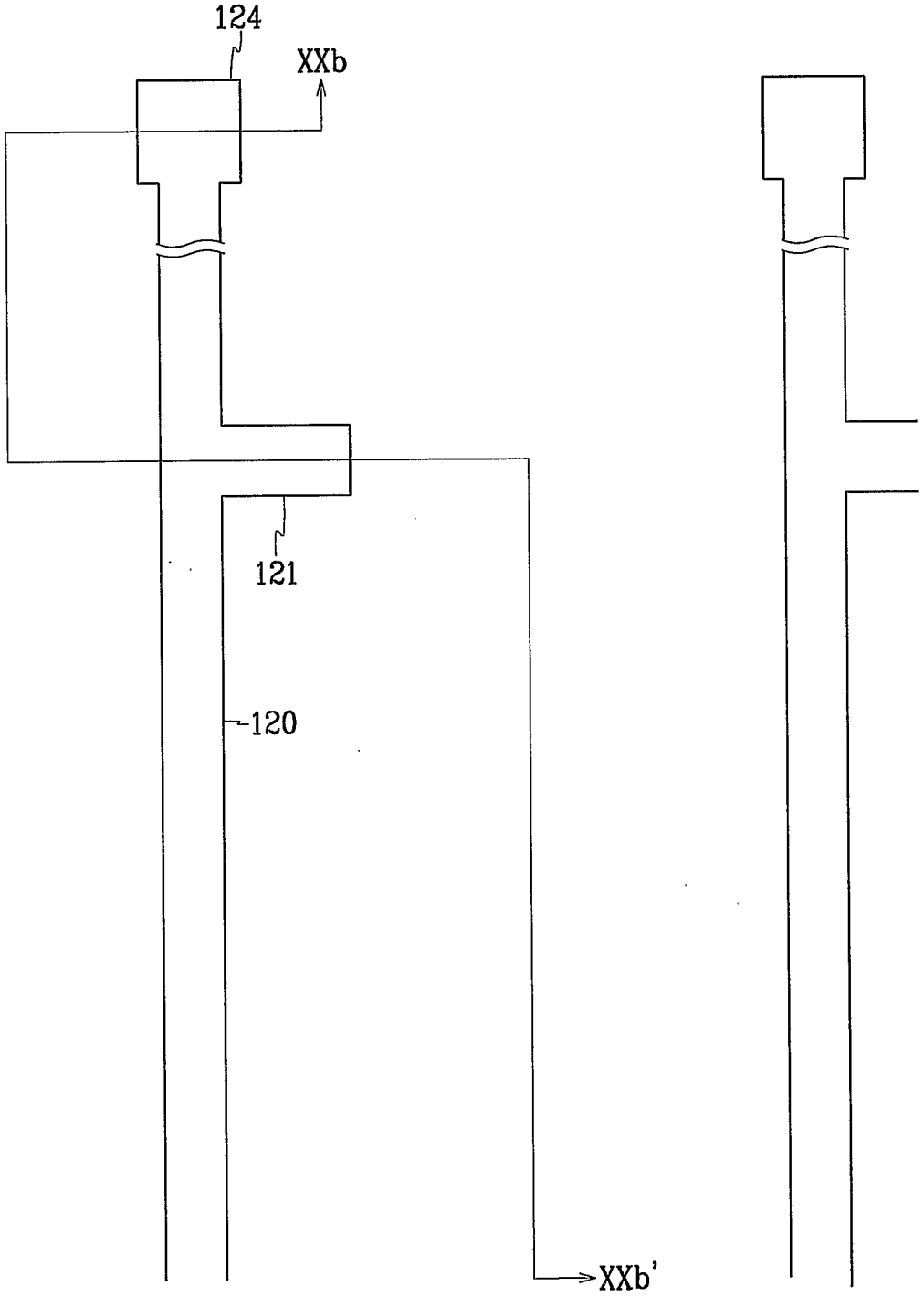


FIG.20B

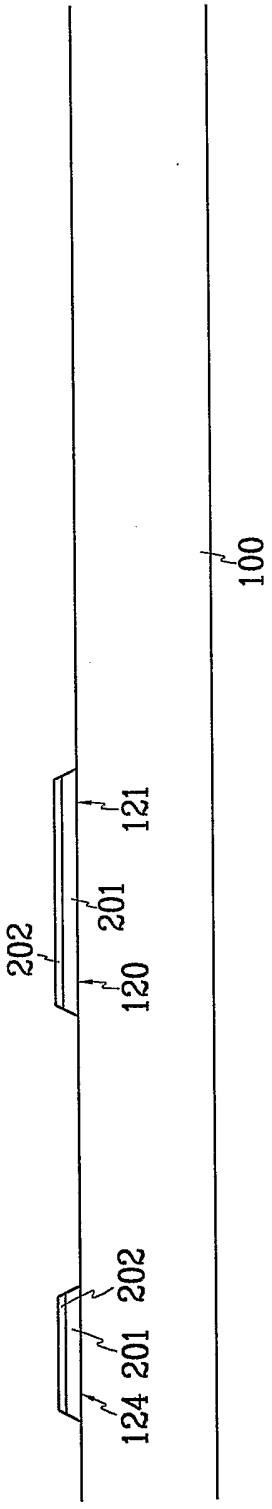


FIG.21A

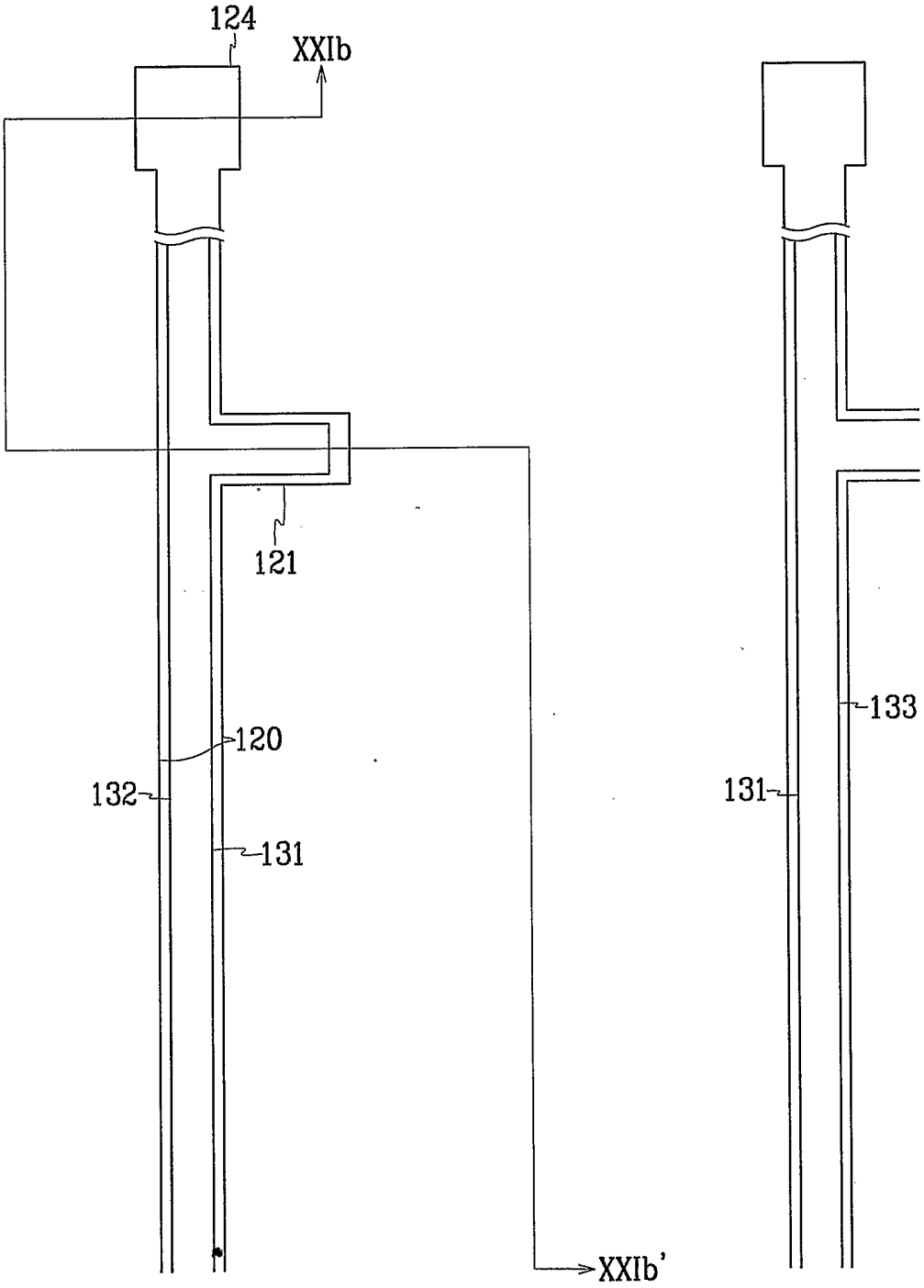


FIG.21B

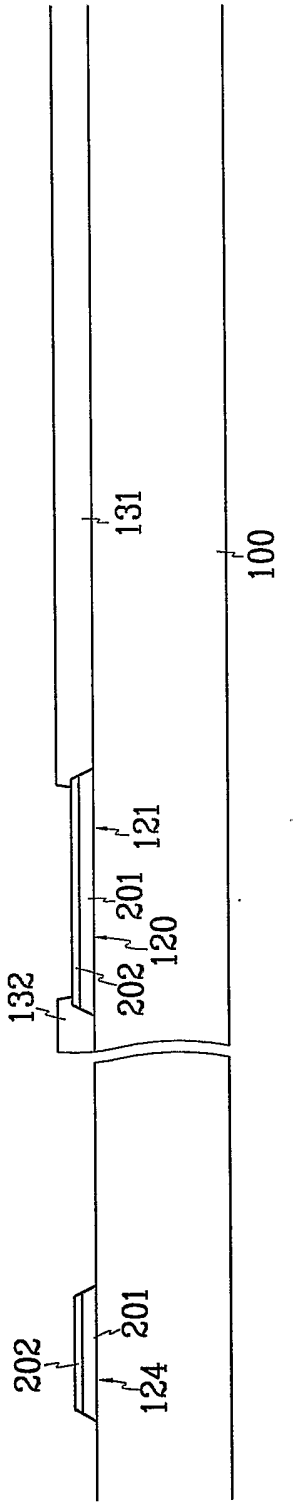


FIG.22A

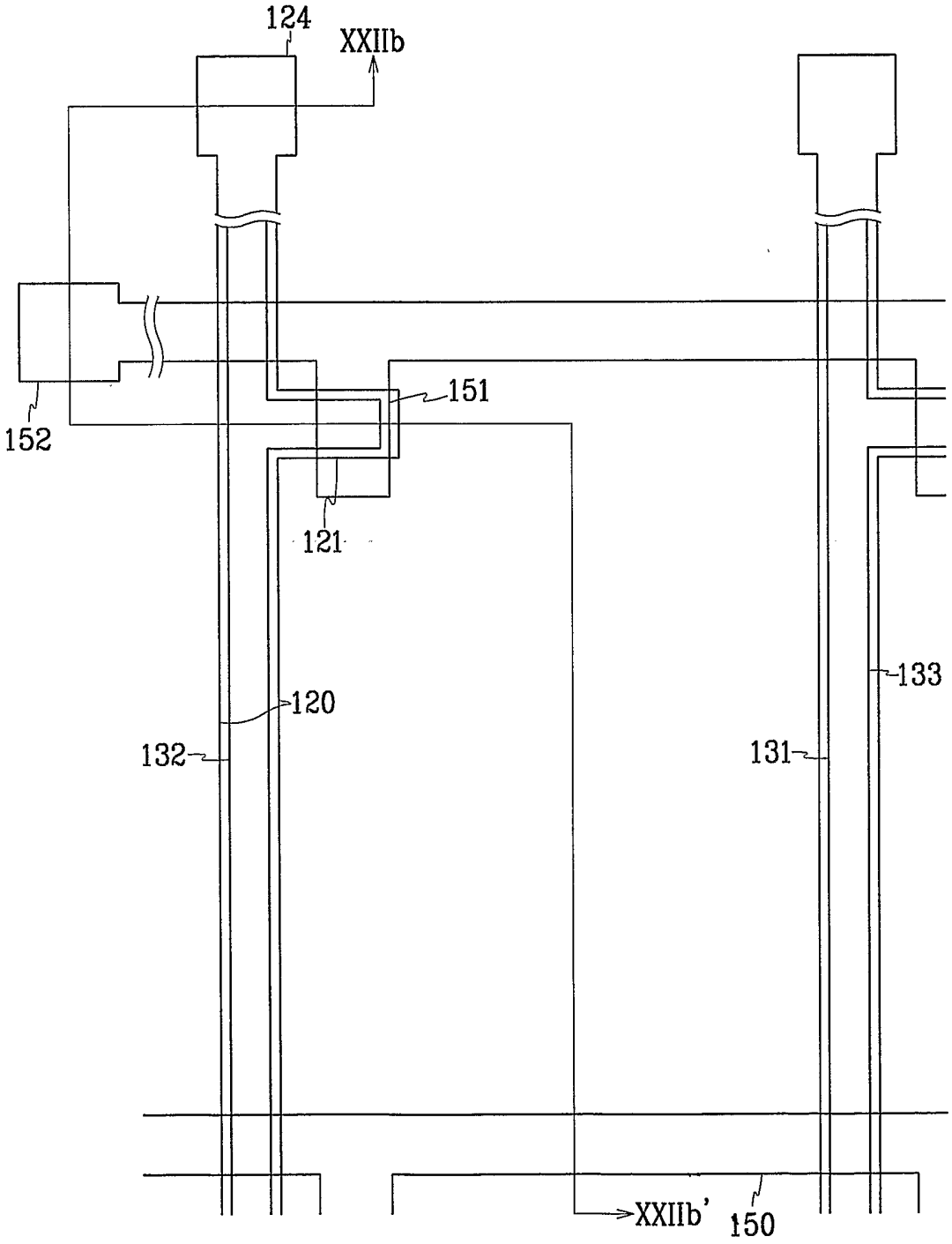
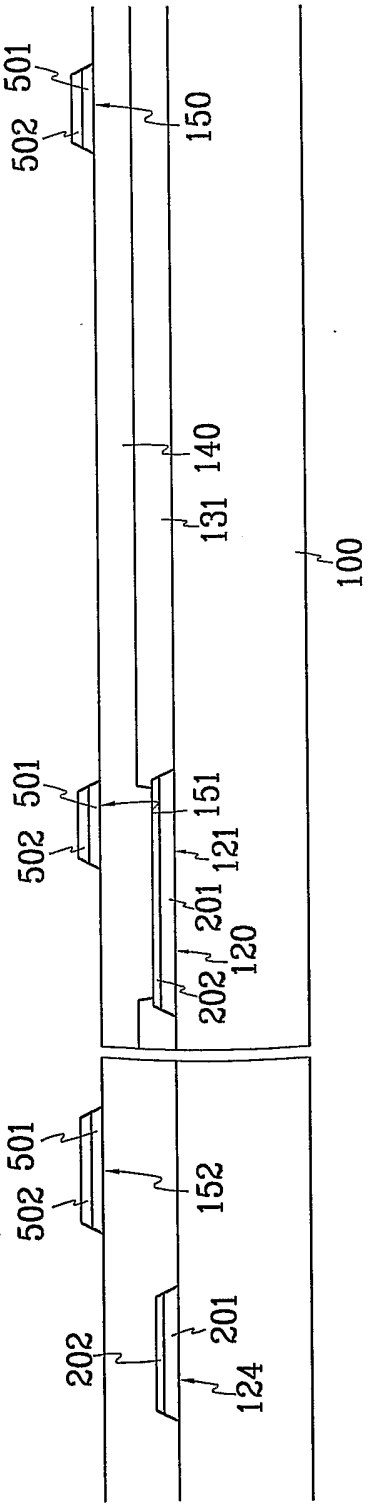


FIG.22B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121
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202
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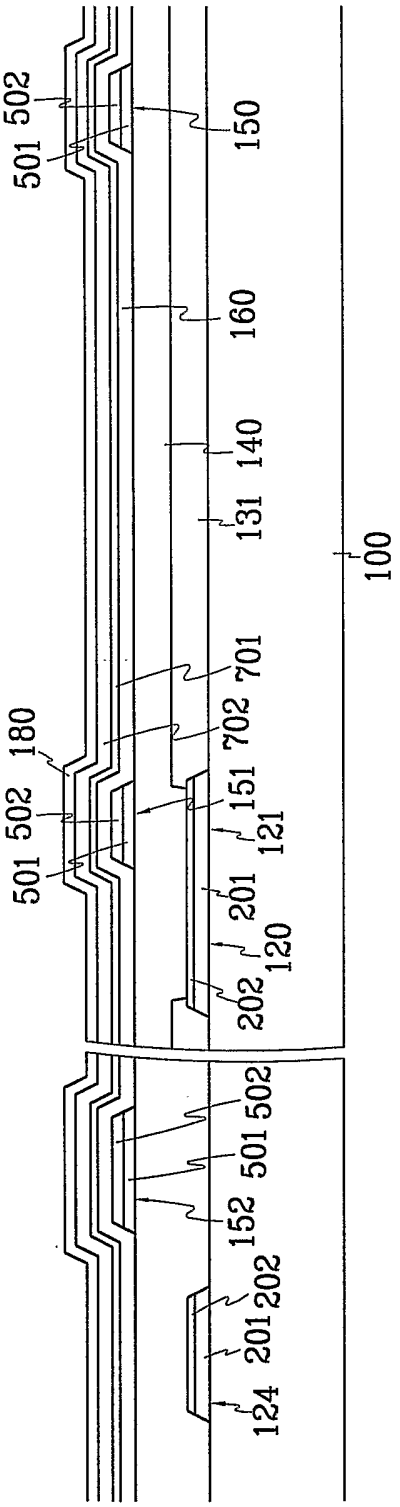
152
202
201
124

FIG.23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160
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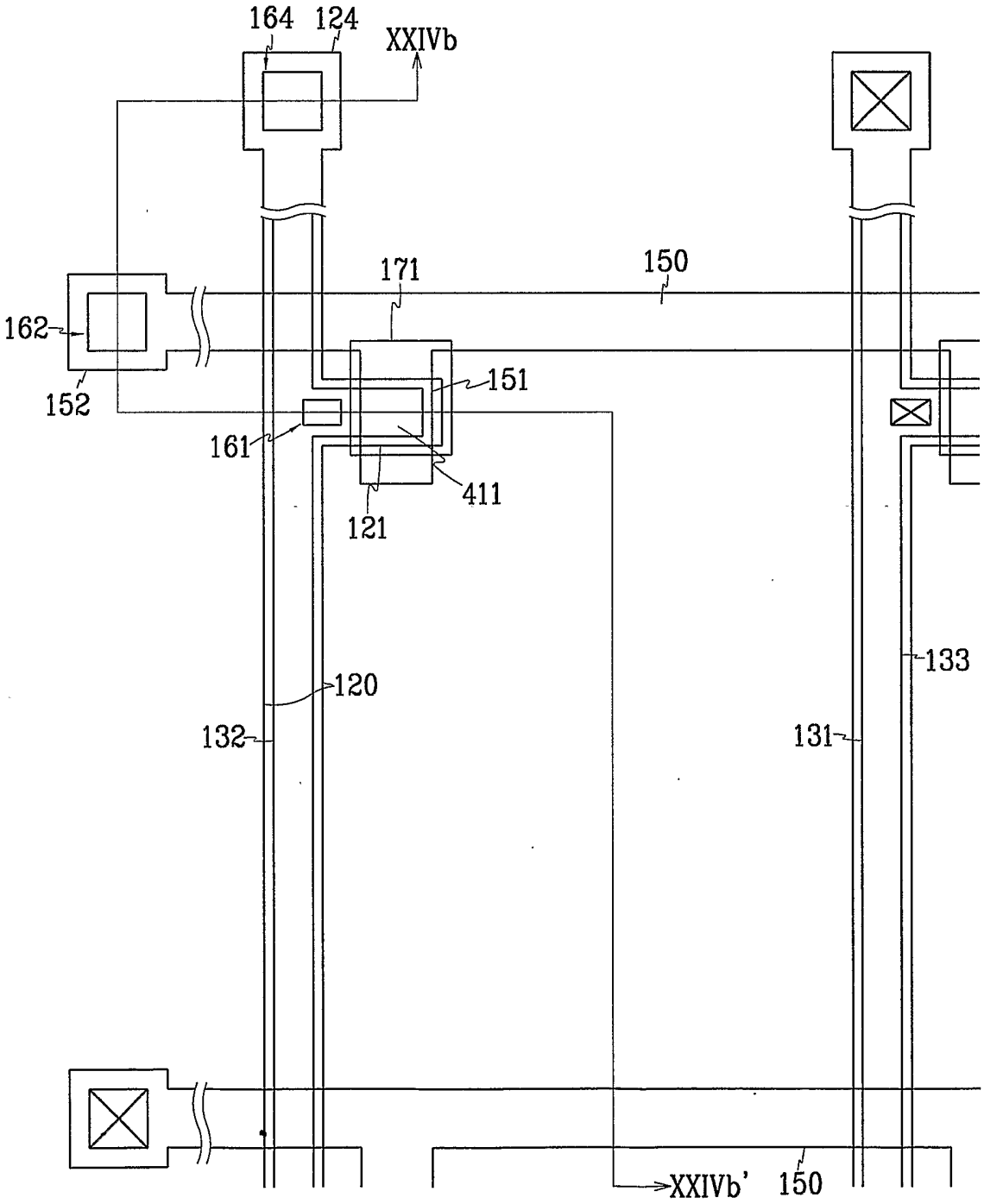
120
202
502
501
152
202
201
124

FIG.24A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124
XXIVb
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162
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152
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411
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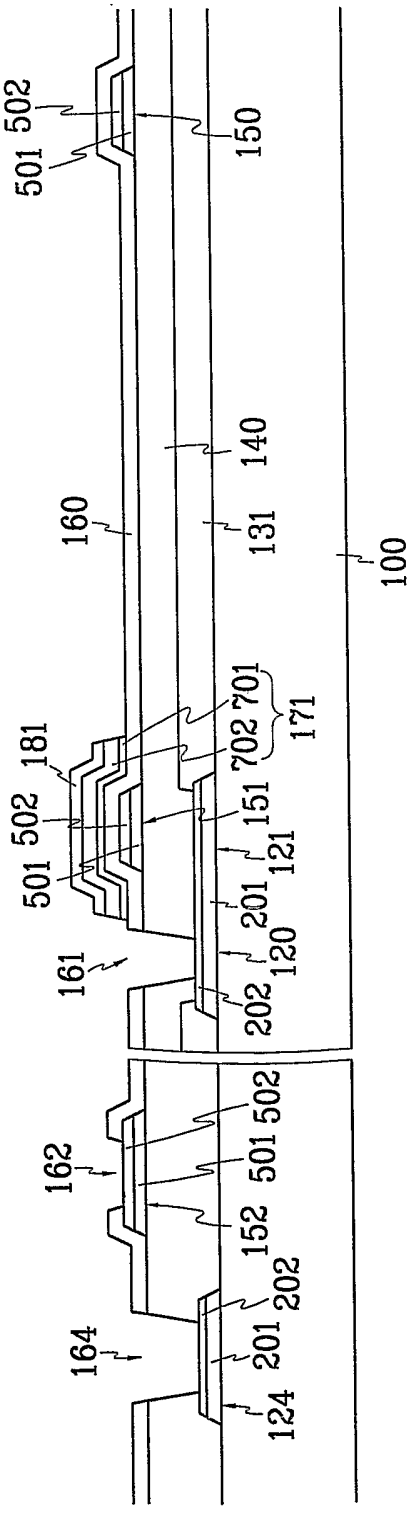
133
120
132
131
XXIVb'
150

FIG.24B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201
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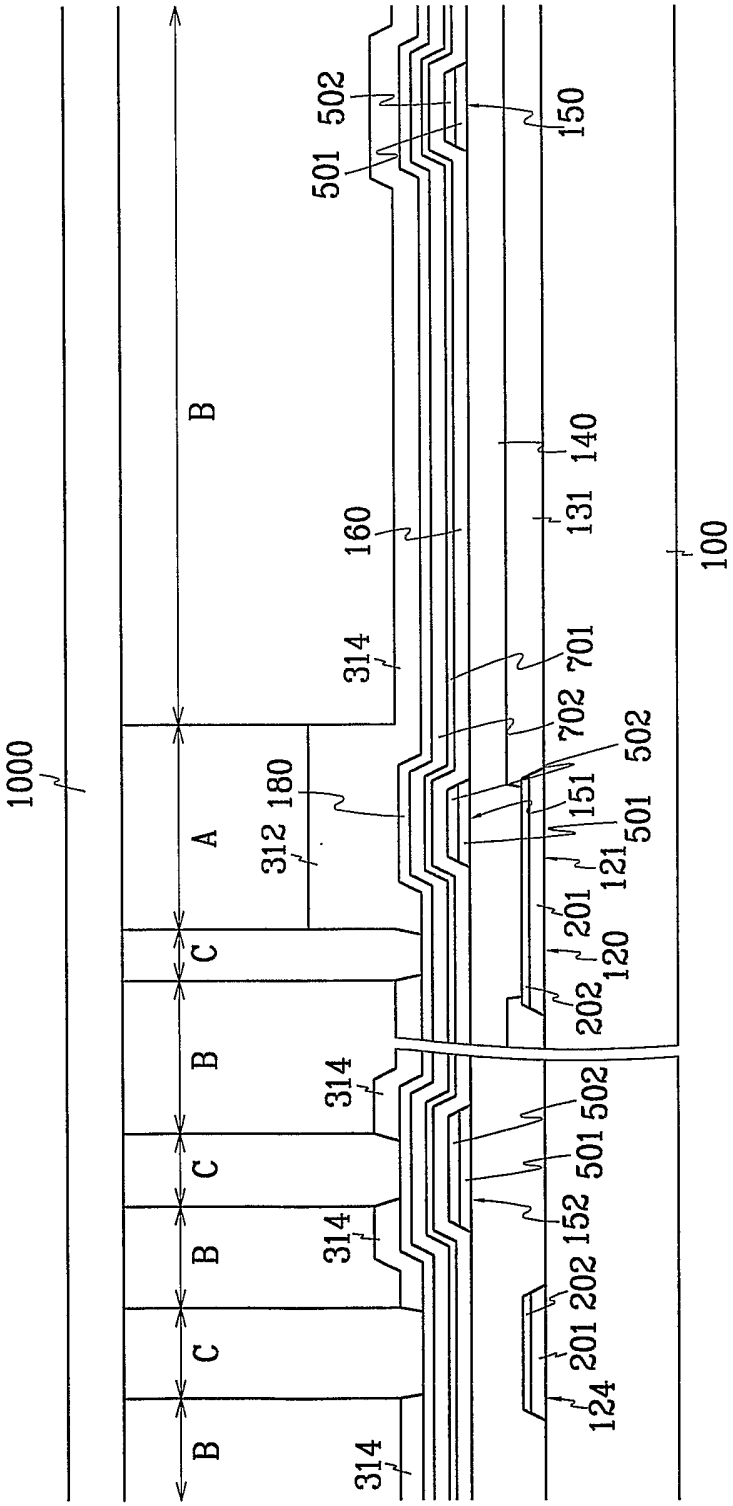
502
501
162
152
202
164
201
124

FIG.25


1000
B
A
C
B
C
B
C
B
314
312
180
160
314
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314
501
502
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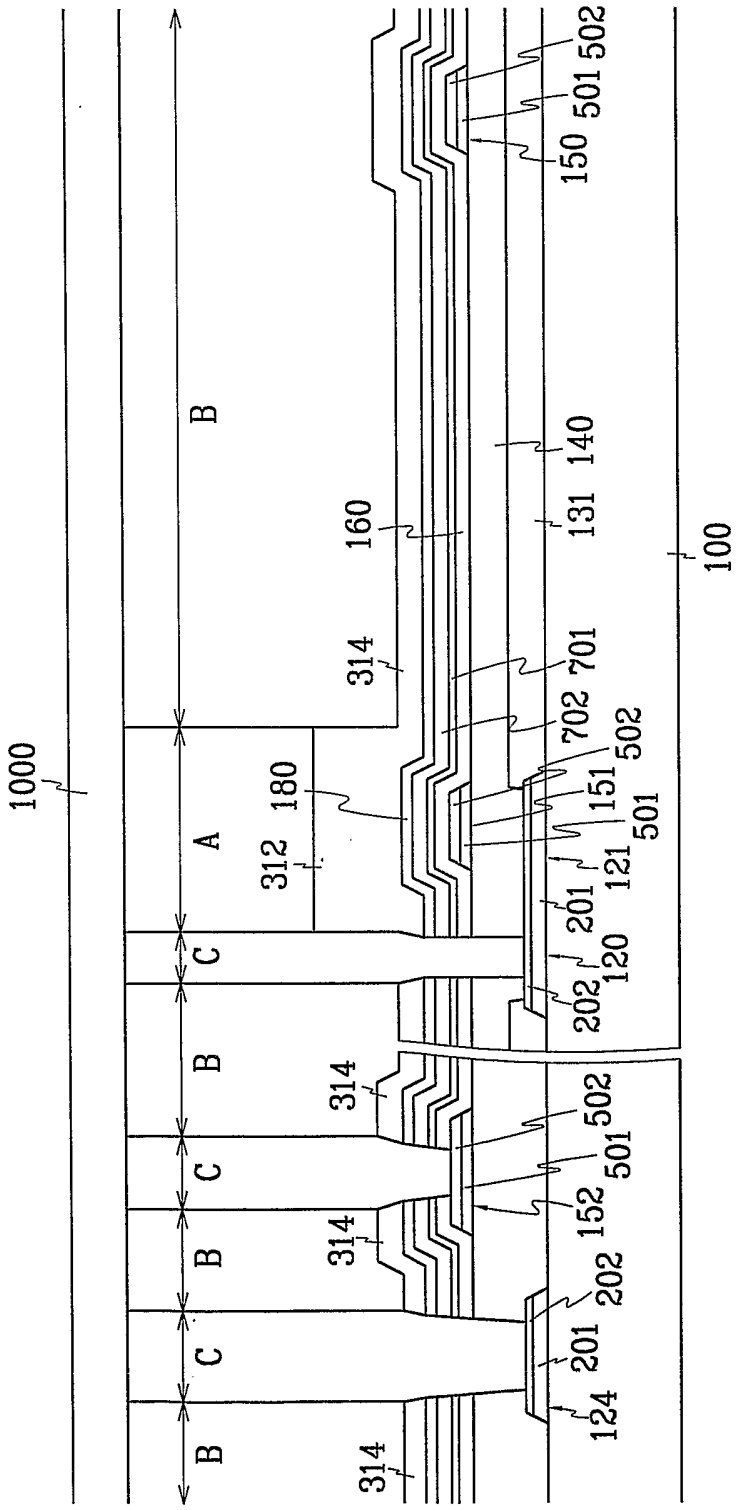
120
202
502
501
152
202
201
124

FIG.26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A
C
B
C
B
C
B
160
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180
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140
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701
702
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502
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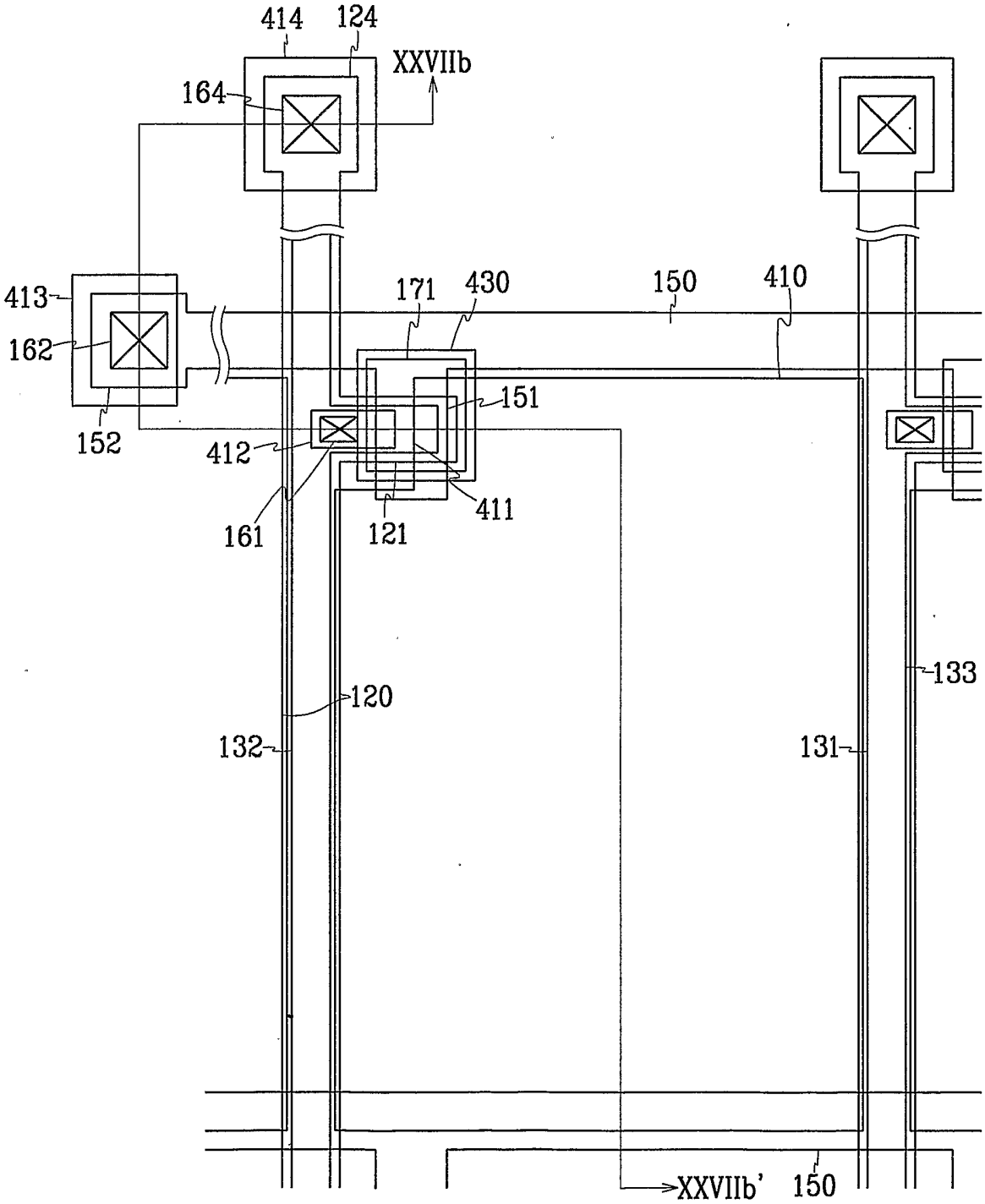
152
314
202
201
124
314

FIG.27A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XXVIIb
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161
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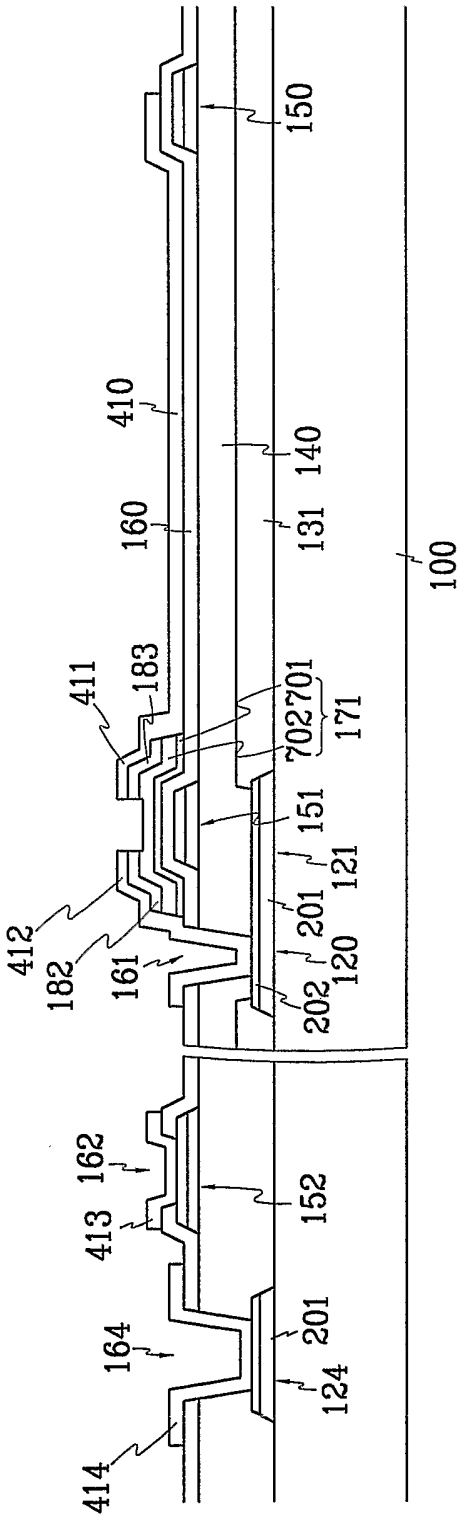
411
133
120
132
131
XXVIIb'
150

FIG.27B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411
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702
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412
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182
201
161
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202
162
152
413
164
201
124
414

FIG.28

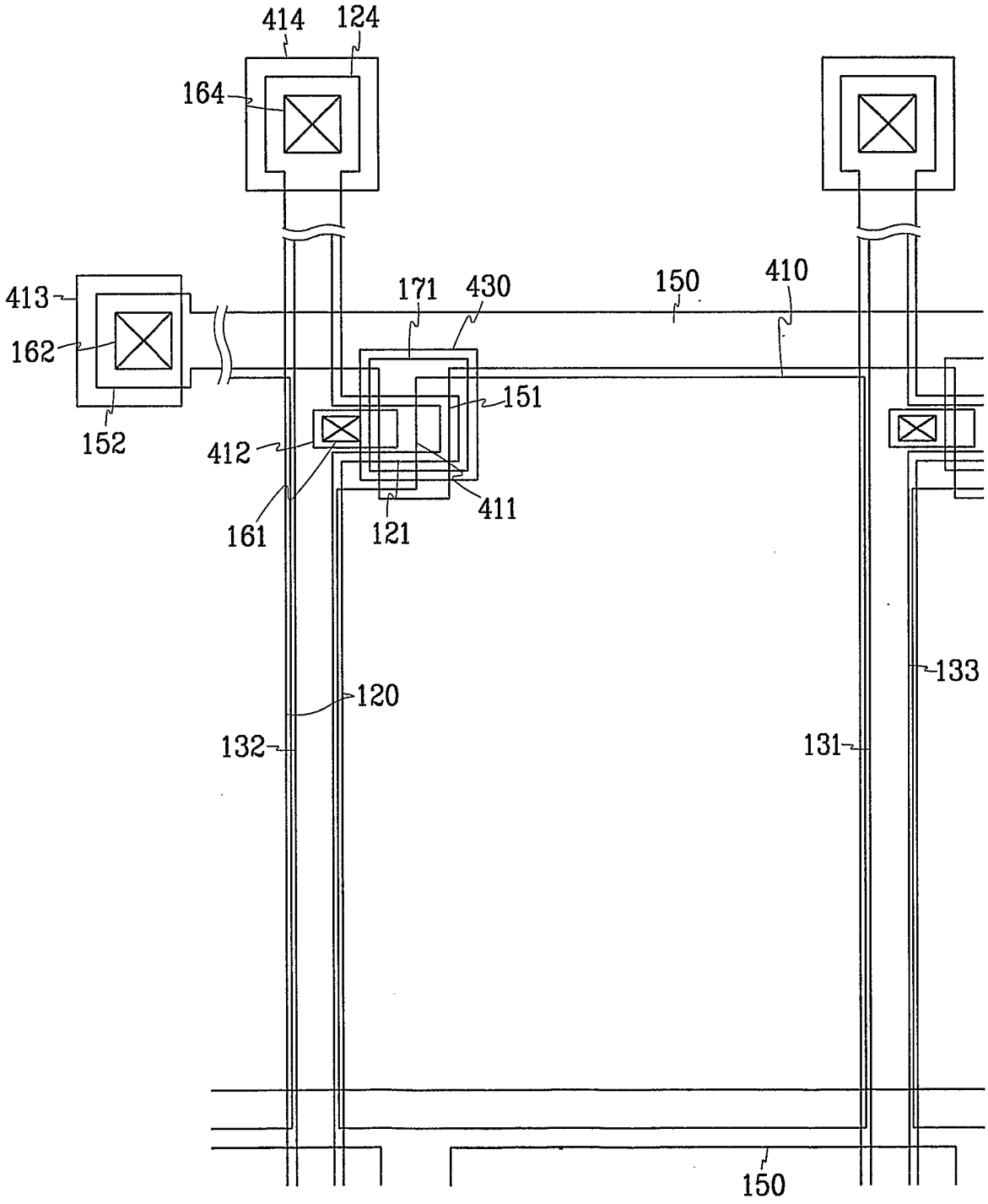
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FIG.29

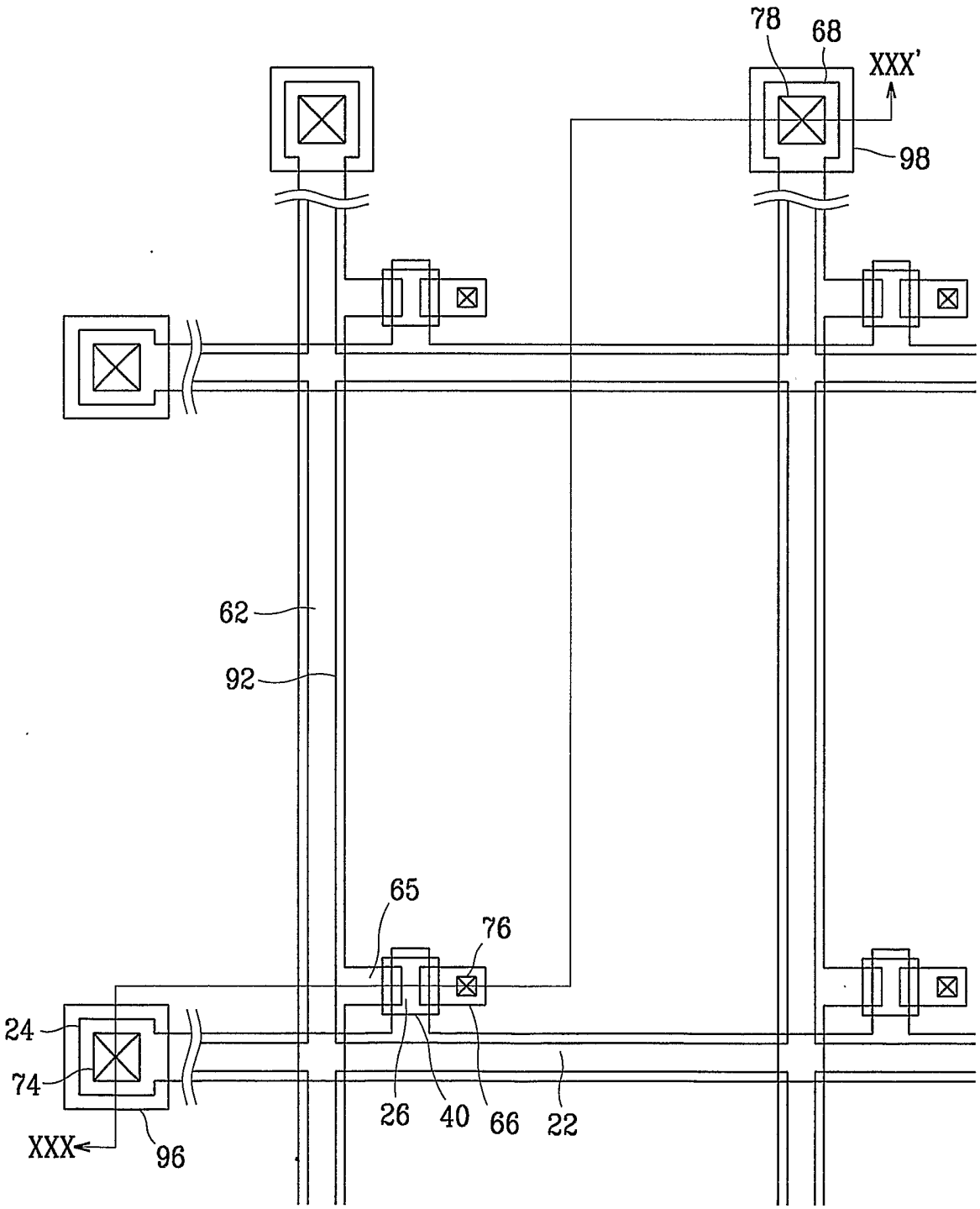

FIG.30

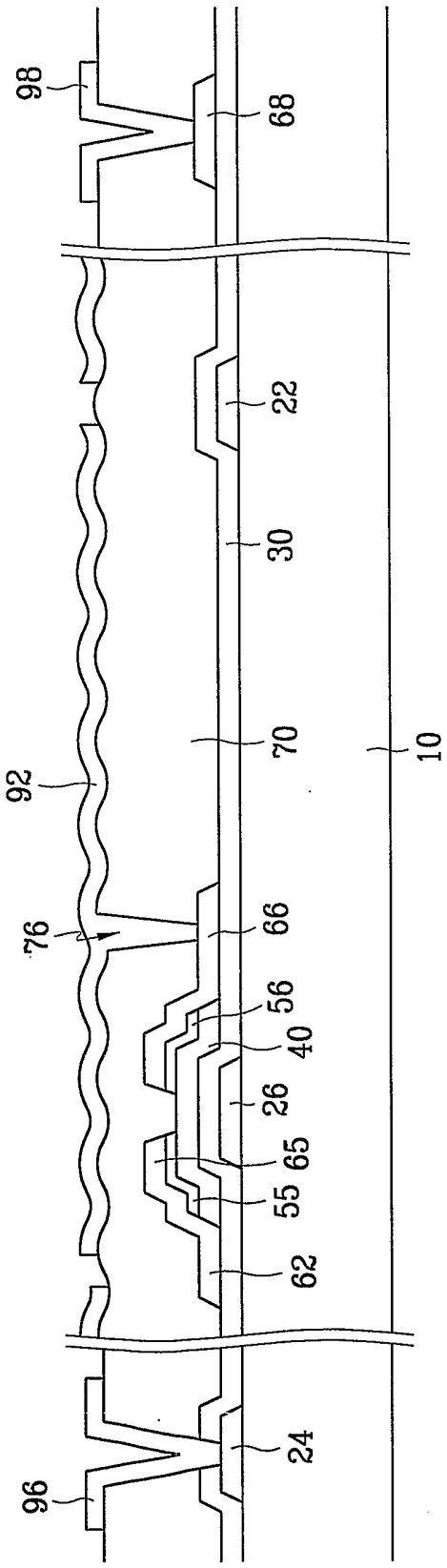

FIG.31A

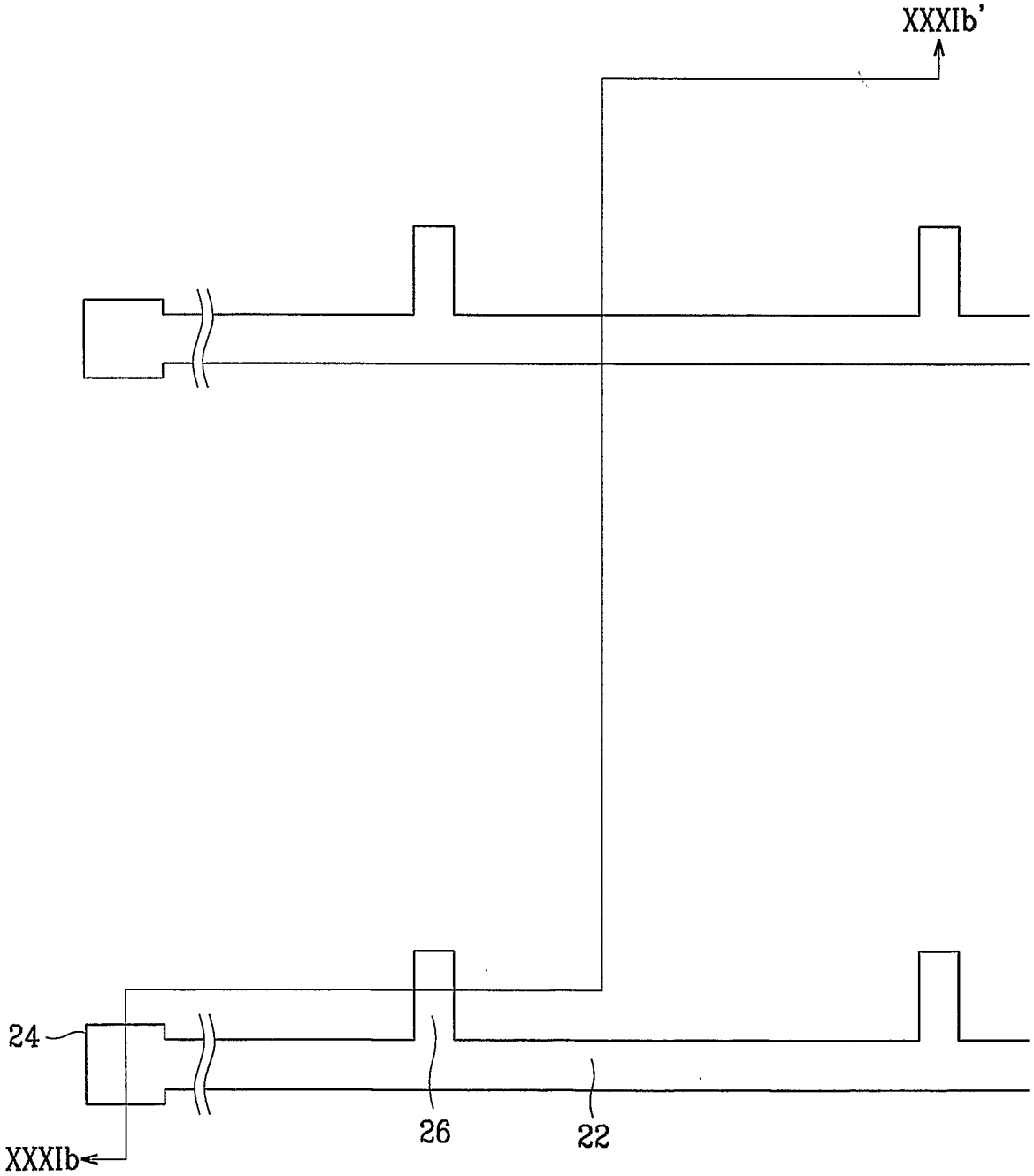

FIG.31B

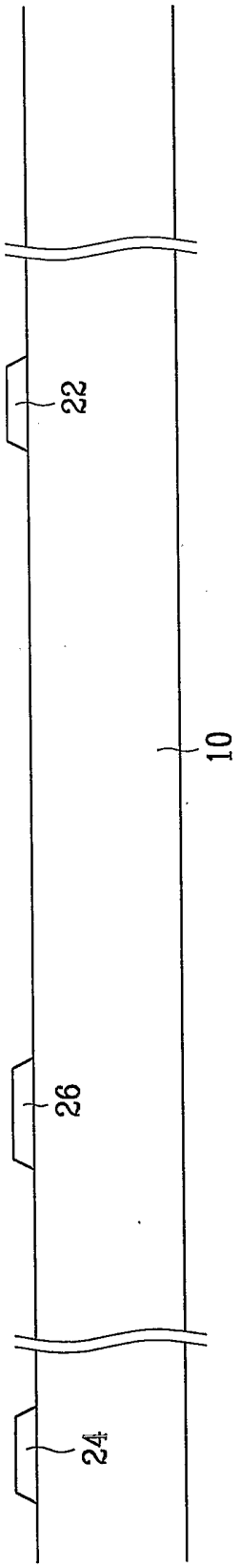

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FIG.32A

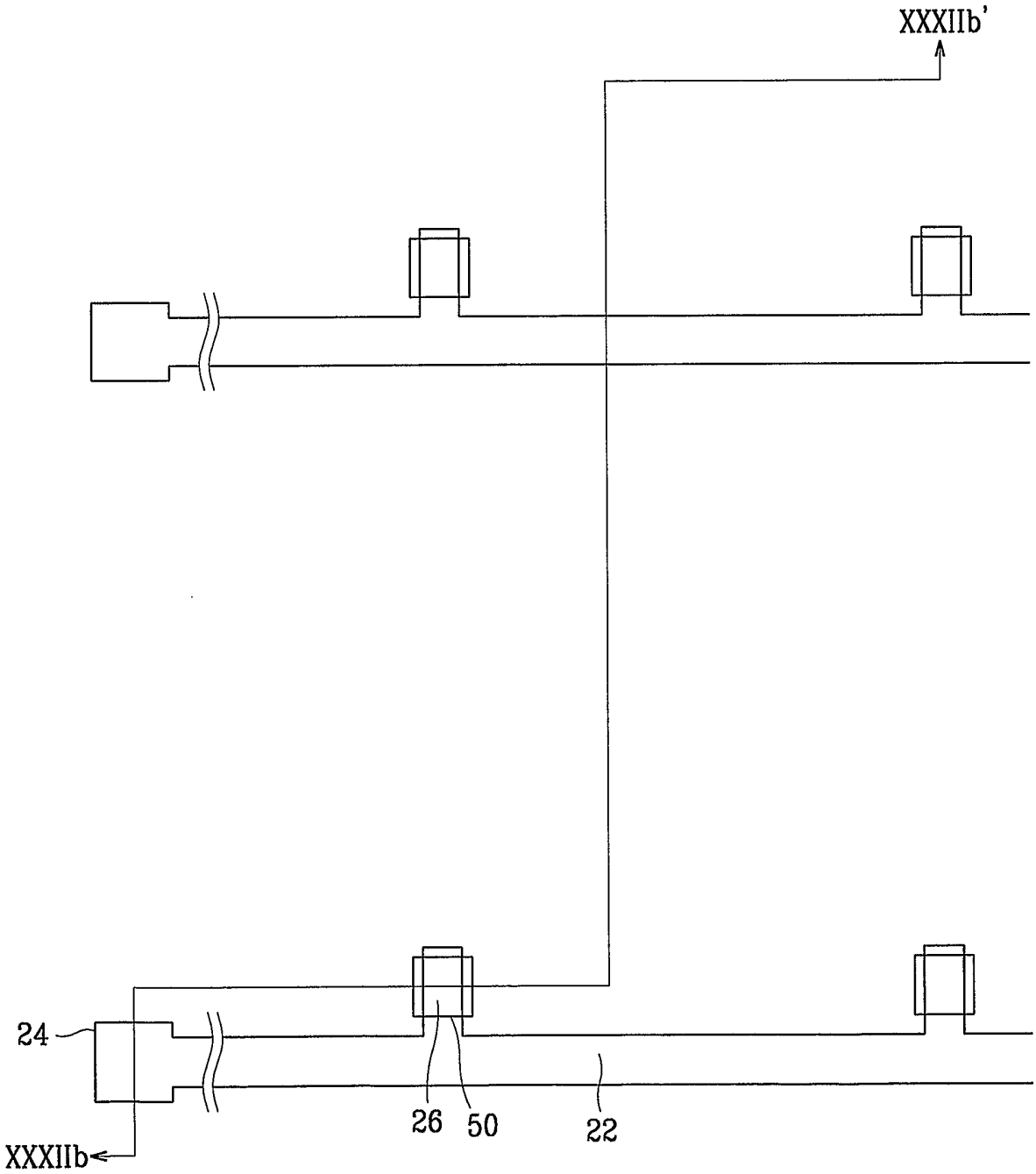

FIG.32B

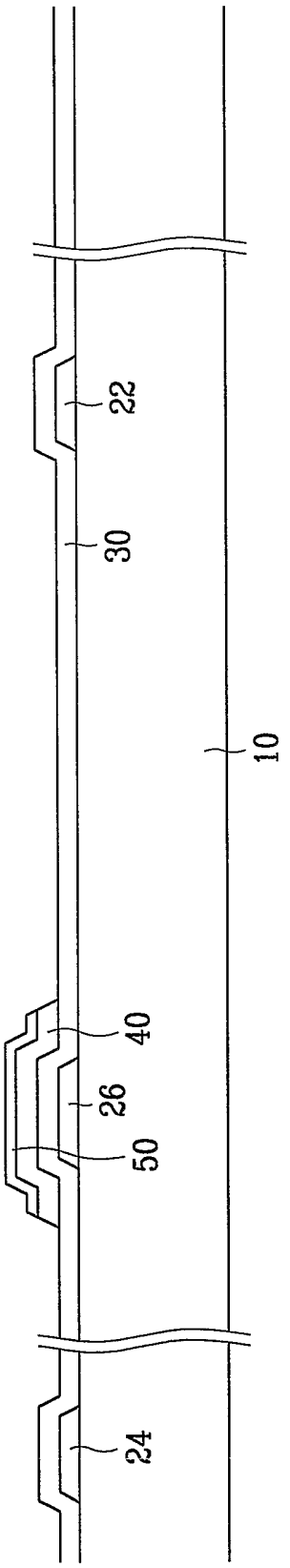

FIG.33A

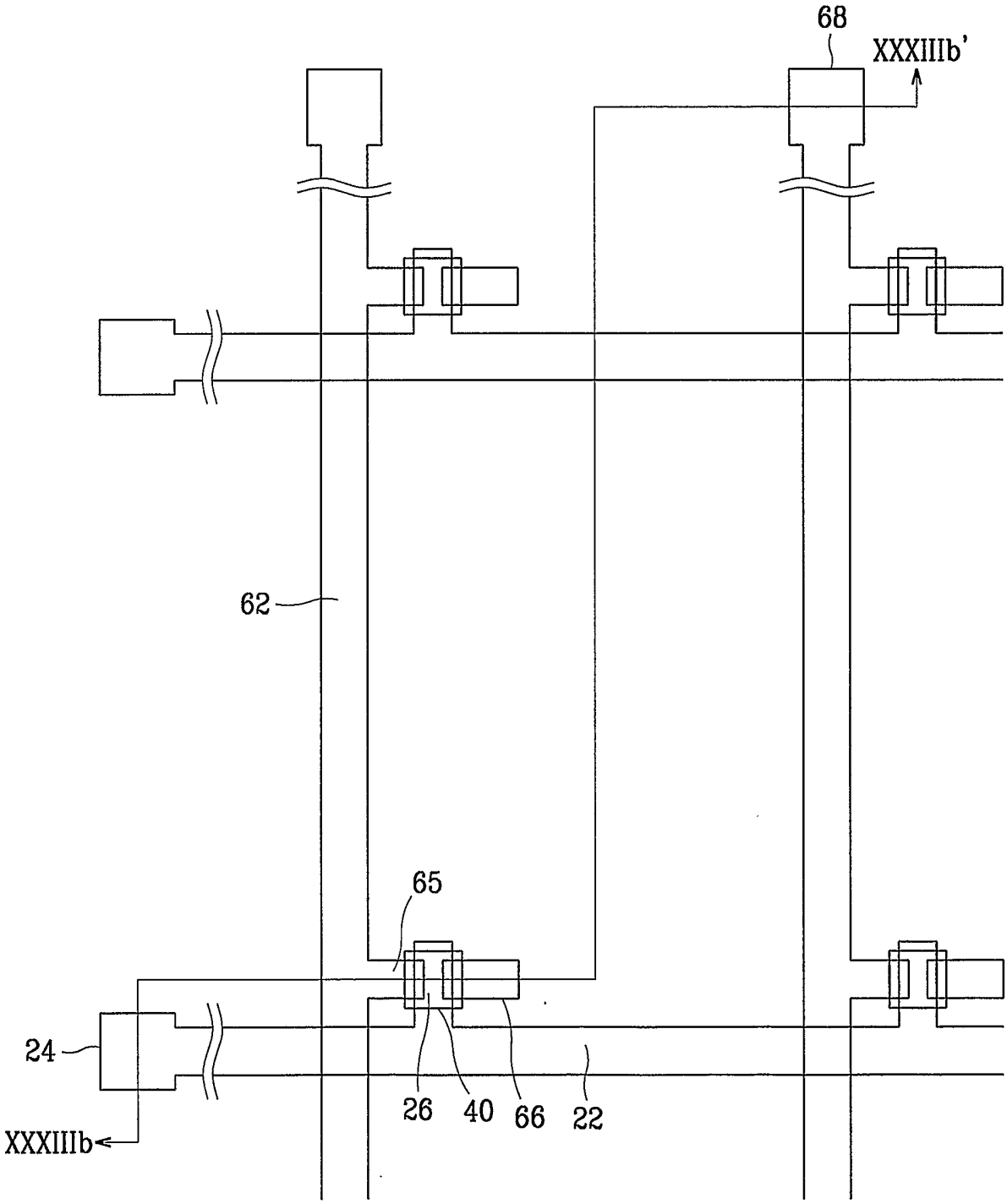

FIG.33B

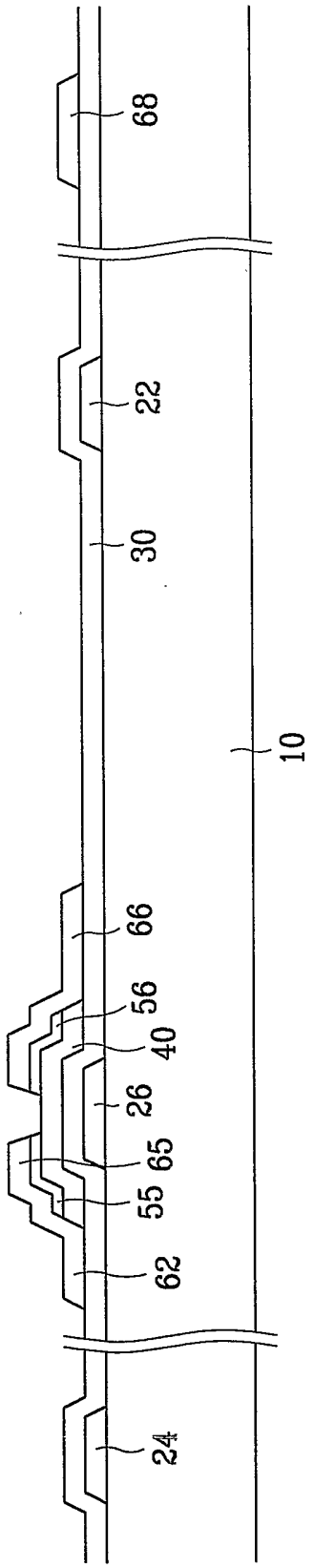

FIG.34A

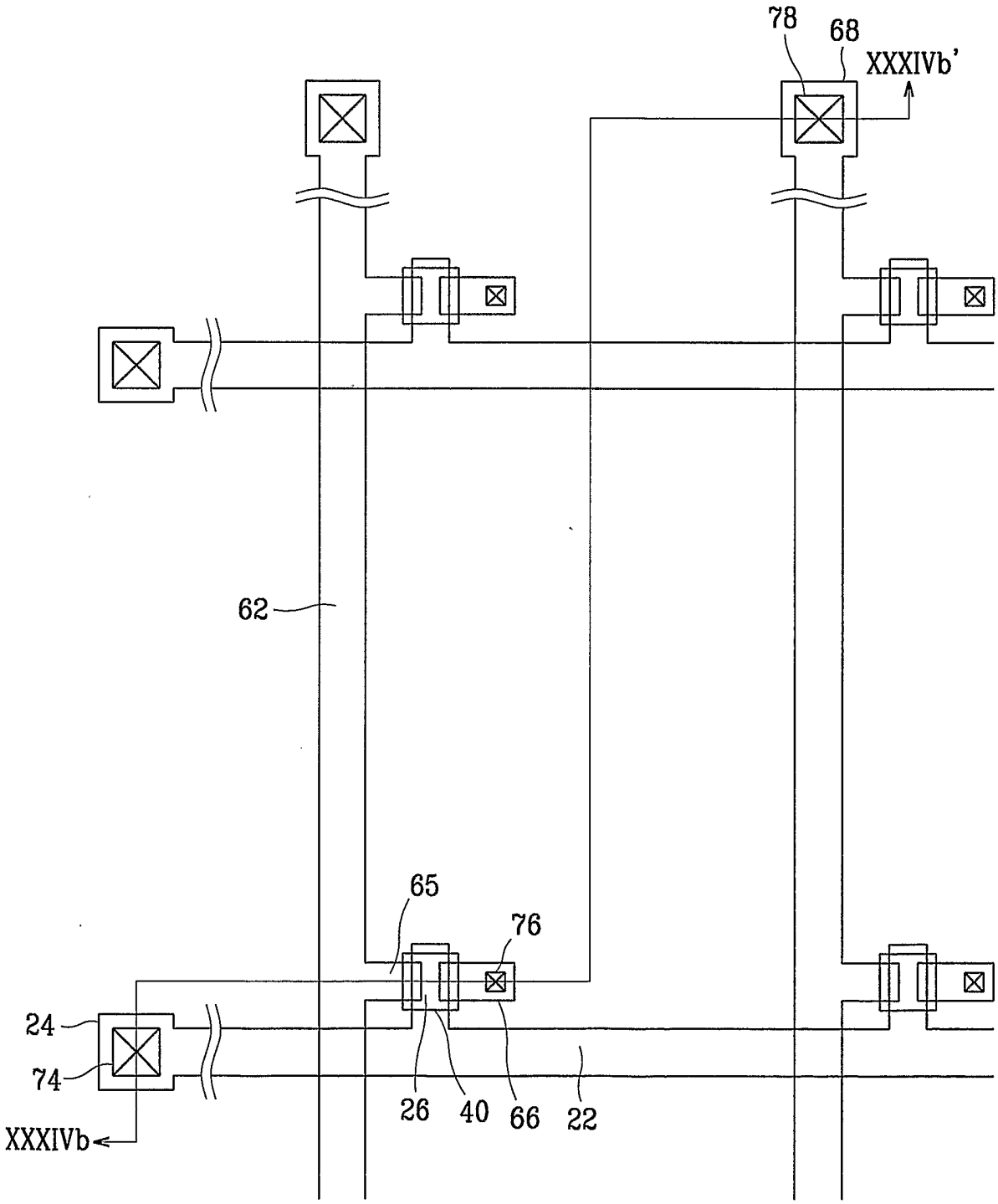

FIG.34B

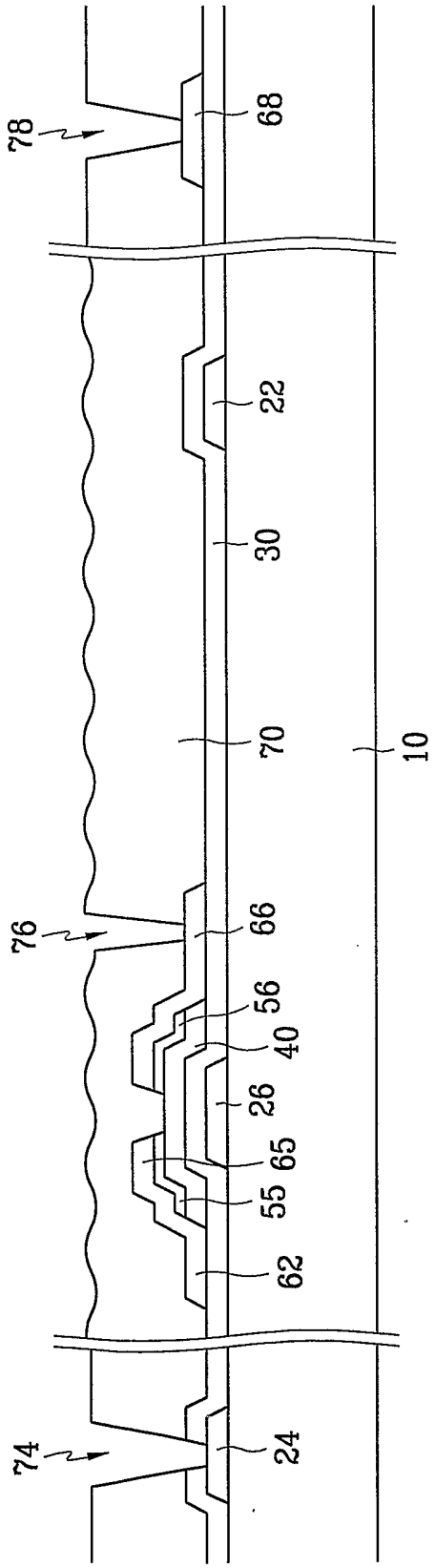

FIG.35

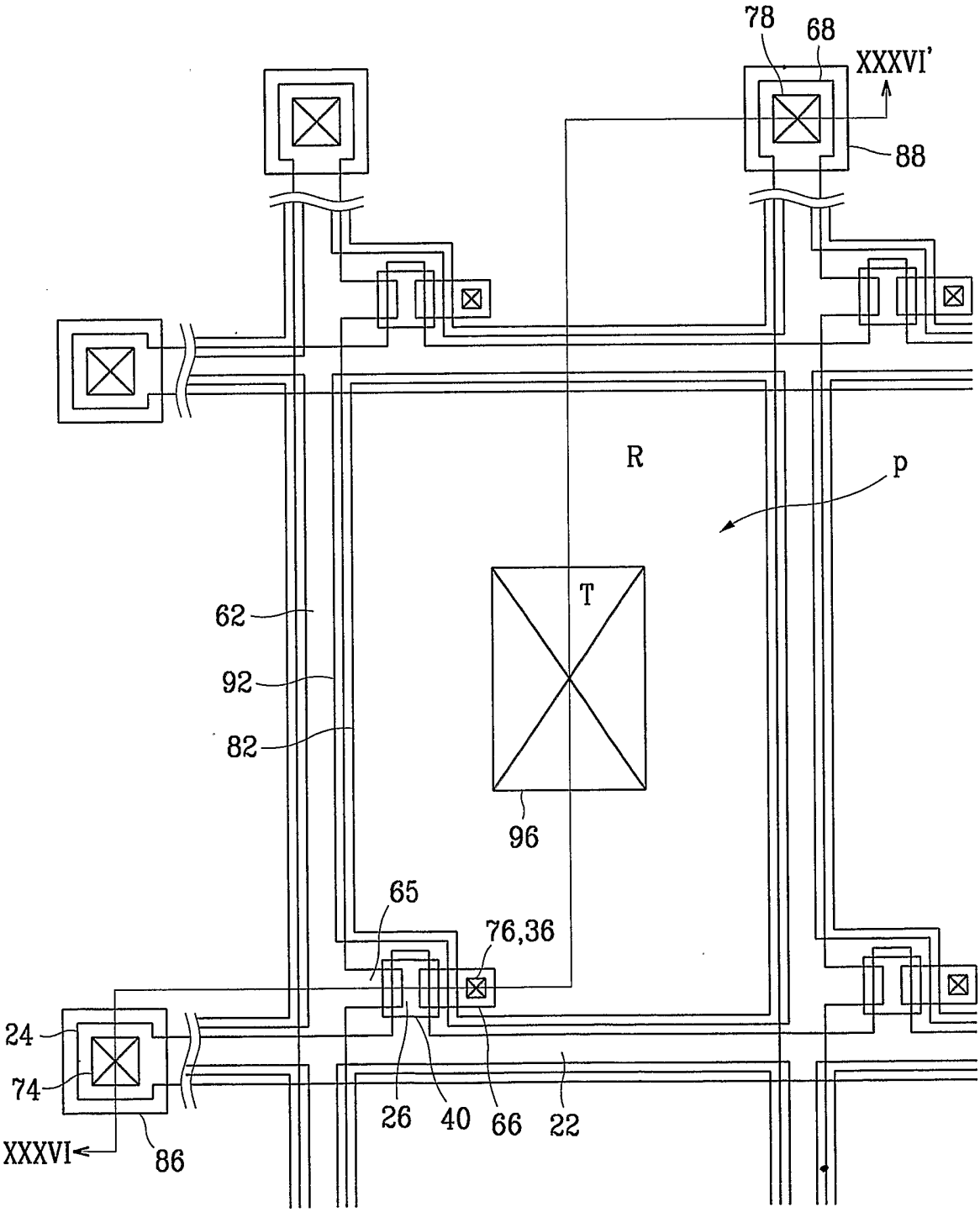

FIG.35B

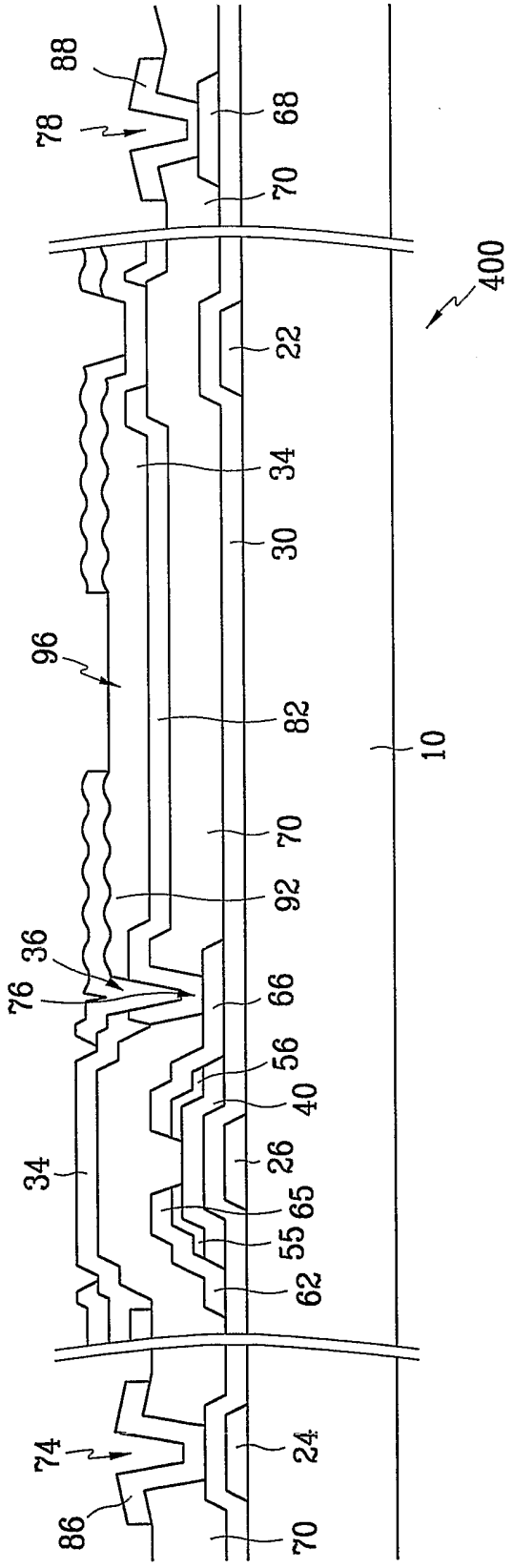
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FIG.37A

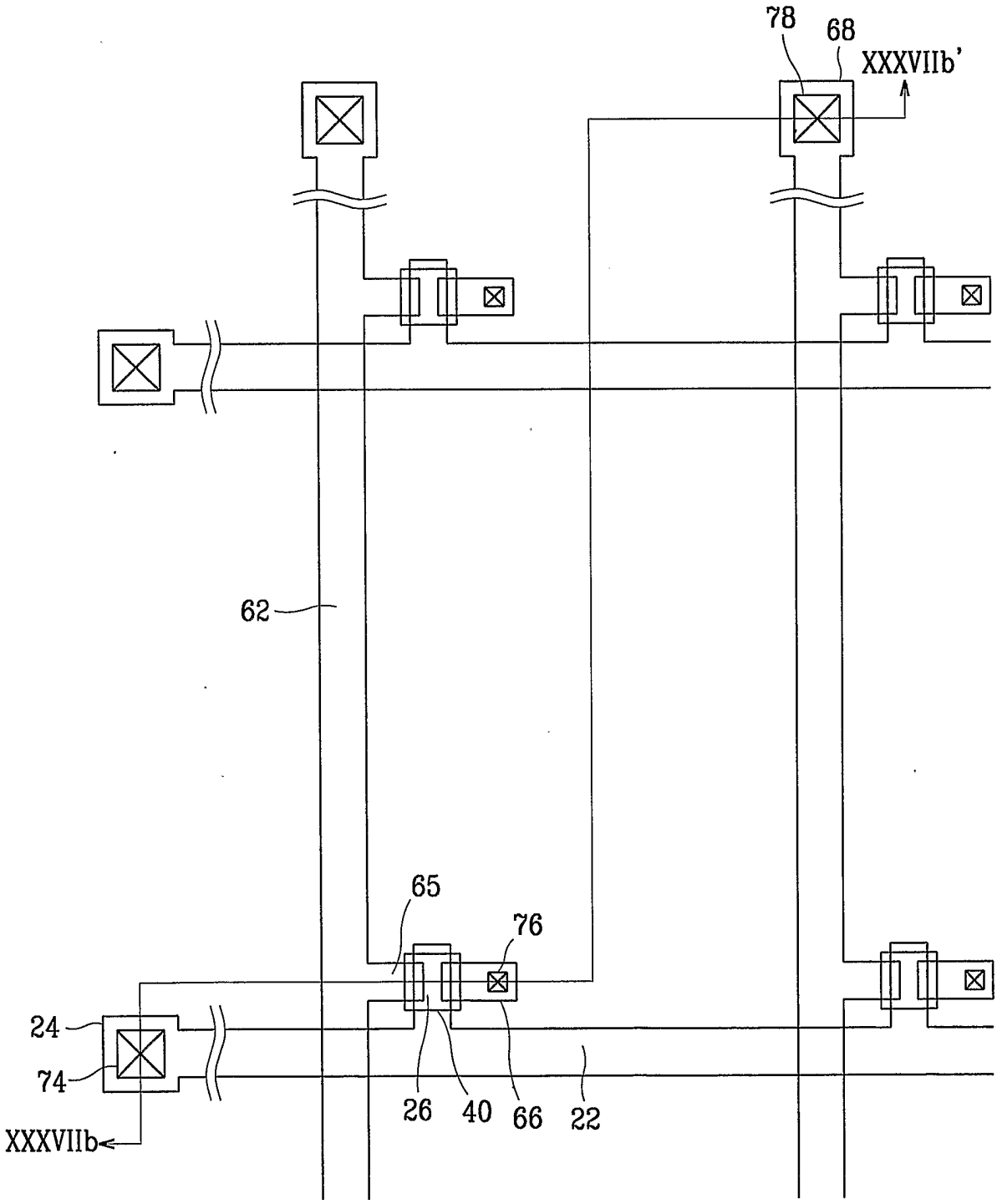

FIG.37B

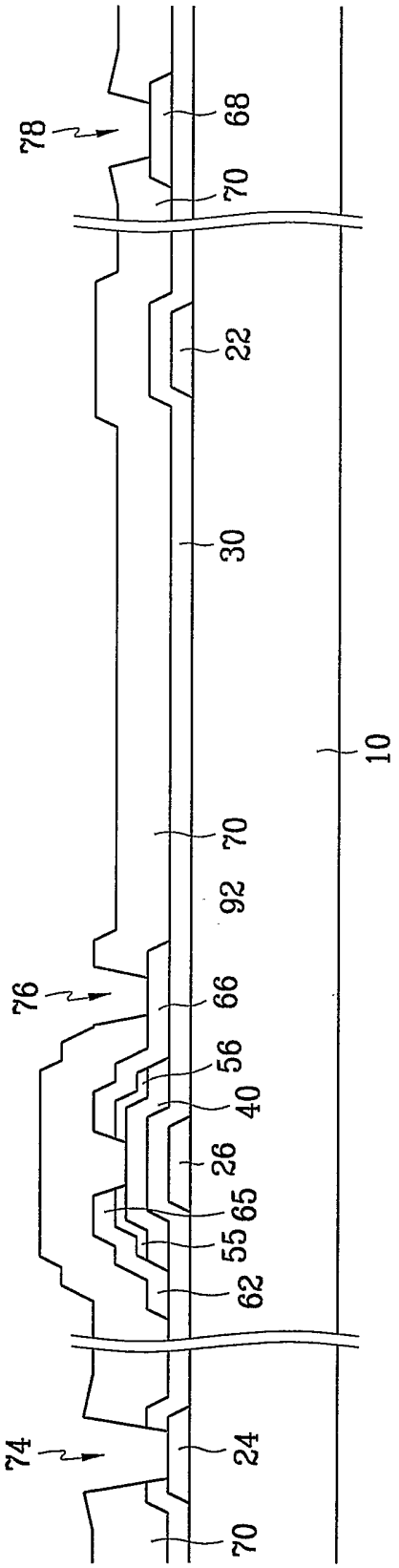

FIG.38A

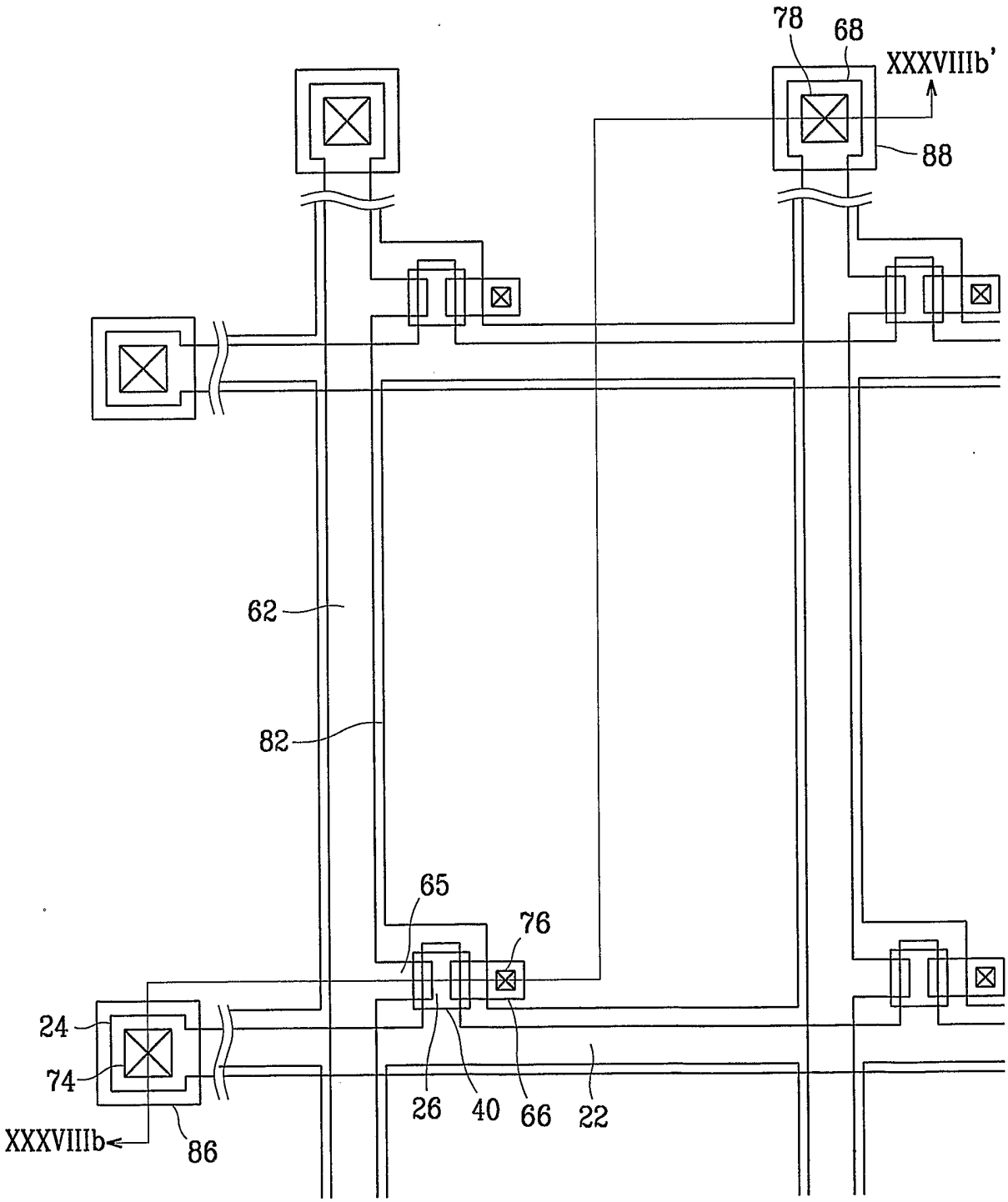

FIG.38B

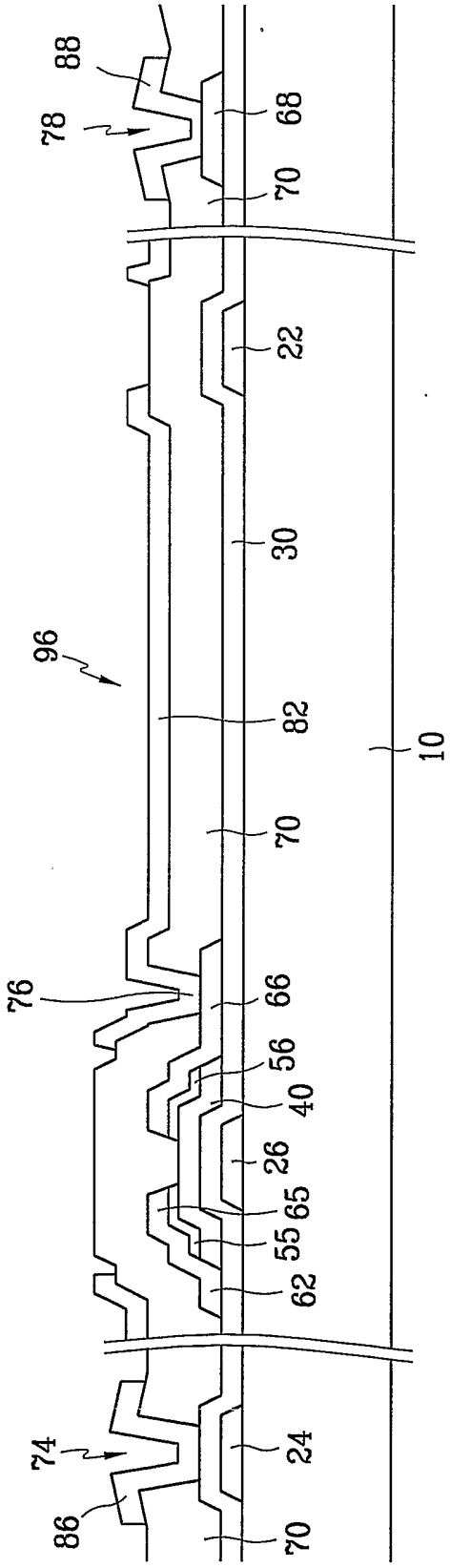

FIG.39A

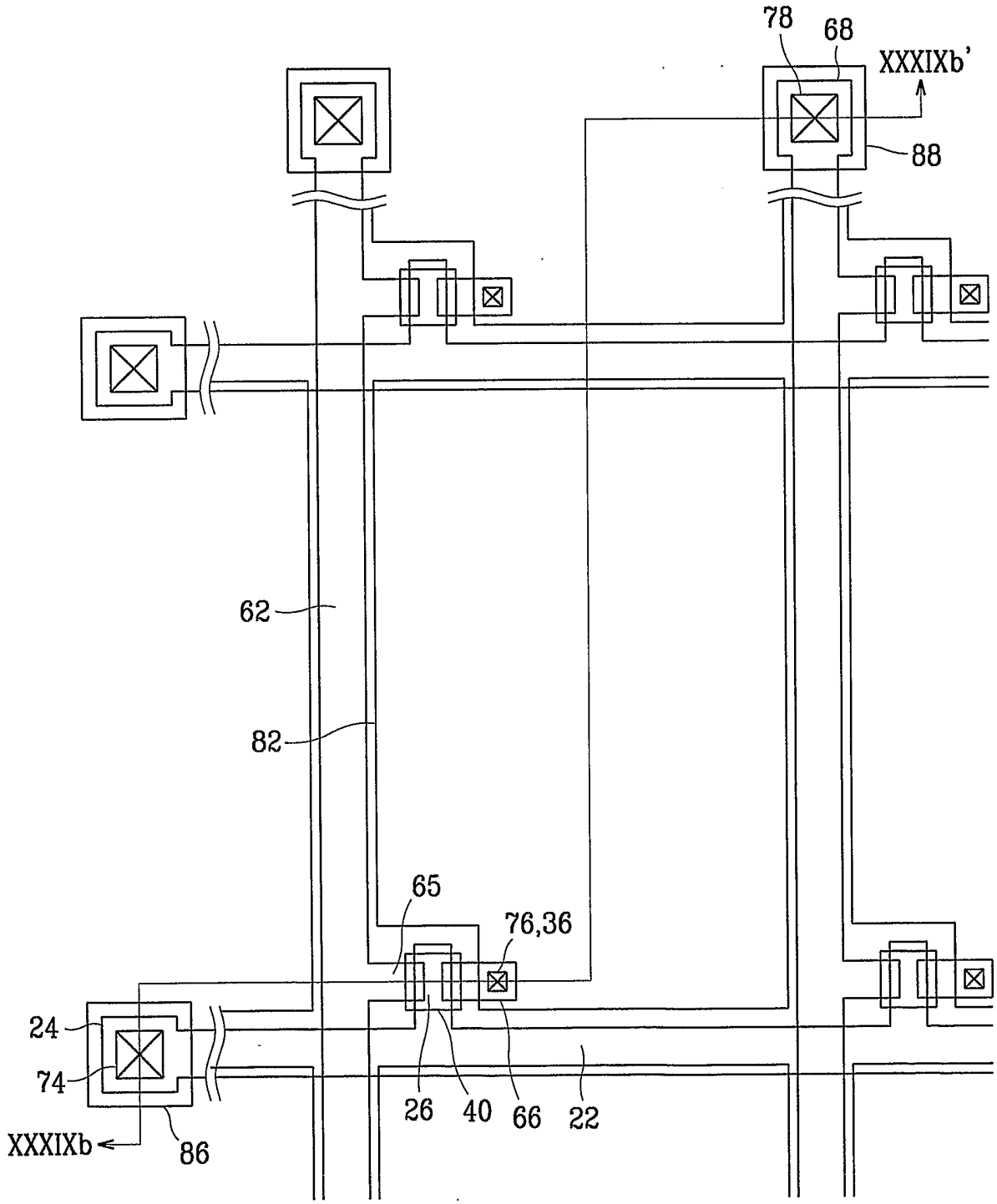

FIG.39B

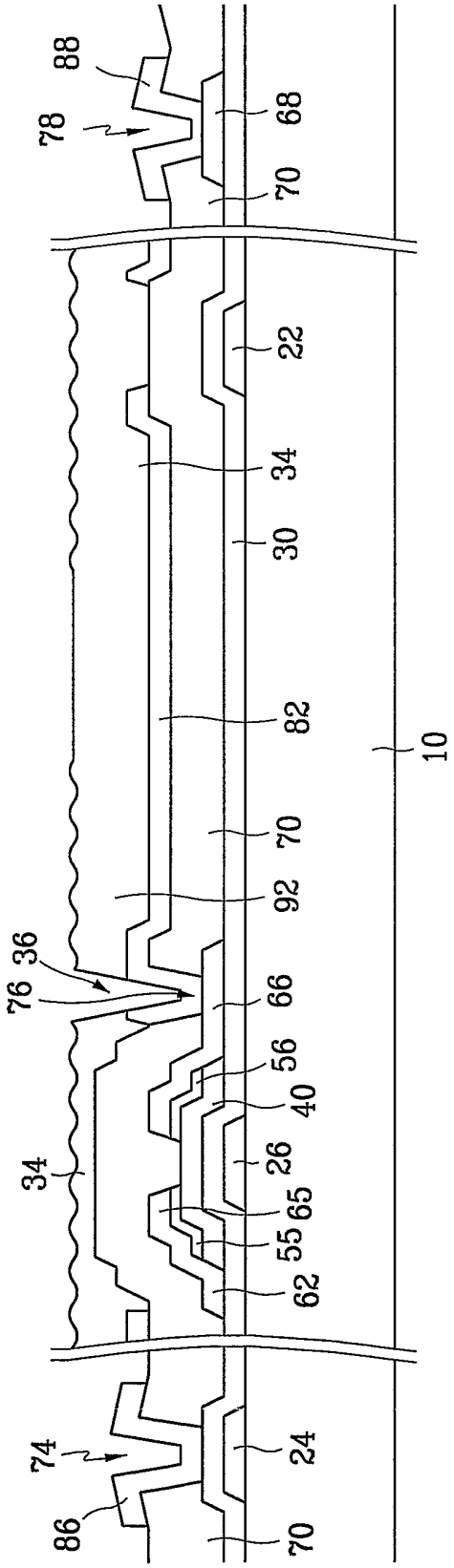
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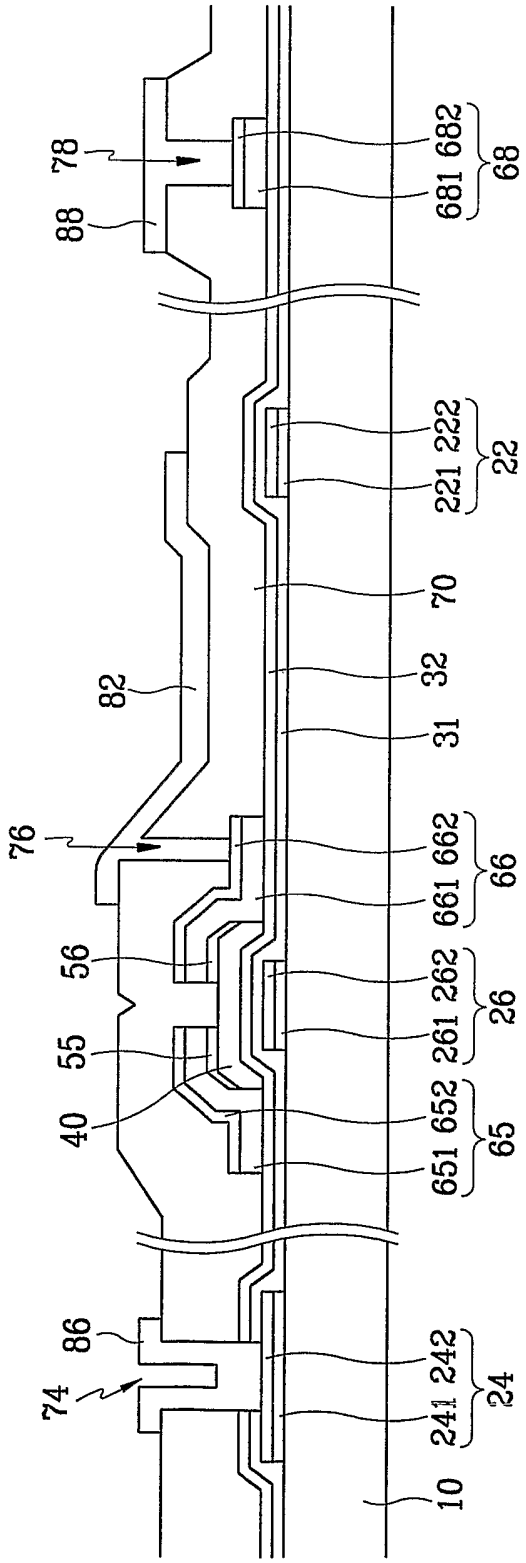
FIG.40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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR01/01896

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 G02F 1/136

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC7 G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
KR, JP: as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PAJ " pixel electrode" " TFT" "insulating layer" "dielectric constant" "amorphous silicon" " CVD"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP03-149884 (Toppan Printing Co Ltd) 26, Jun., 1991 see whole document	1-5
A	US 6,323,918 (Fujitsu Limited) 27, Nov., 2001 see whole document	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevence; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 JULY 2002 (03.07.2002)	03 JULY 2002 (03.07.2002)

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	CHO, Kyoung Hwa Telephone No. 82-42-481-5767

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR01/01896

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP03-149884	26-06-1991	None	
US 6,323,918	27-11-2001	JP 8-329838 JP 9-311904	10-12-1996 13-11-1997