



- (51) International Patent Classification:
H02M 1/088 (2006.01) H02M 3/157 (2006.01)
H02M 3/145 (2006.01) H02M 3/158 (2006.01)
- (21) International Application Number:
PCT/US2019/039814
- (22) International Filing Date:
28 June 2019 (28.06.2019)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
16/024,371 29 June 2018 (29.06.2018) US
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 16/024,371 (CON)
Filed on 29 June 2018 (29.06.2018)

- (71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. BOX 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (71) Applicant (for JP only): **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1 Nishi-Shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).
- (72) Inventors: **MEHDI, Syed, Wasif**; Kepserstr 66, Bayem, 85356 Freising (DE). **HERZER, Stefan**; Attoweg 2, 85417 Marzling (DE). **PRIEGO, Antonio**; Wippenhauserstrasse 15, 85354 Freising (DE).
- (74) Agent: **ABRAHAM, Ebby** et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,

(54) Title: DC-TO-DC VOLTAGE CONVERTERS WITH CONTROLLERS

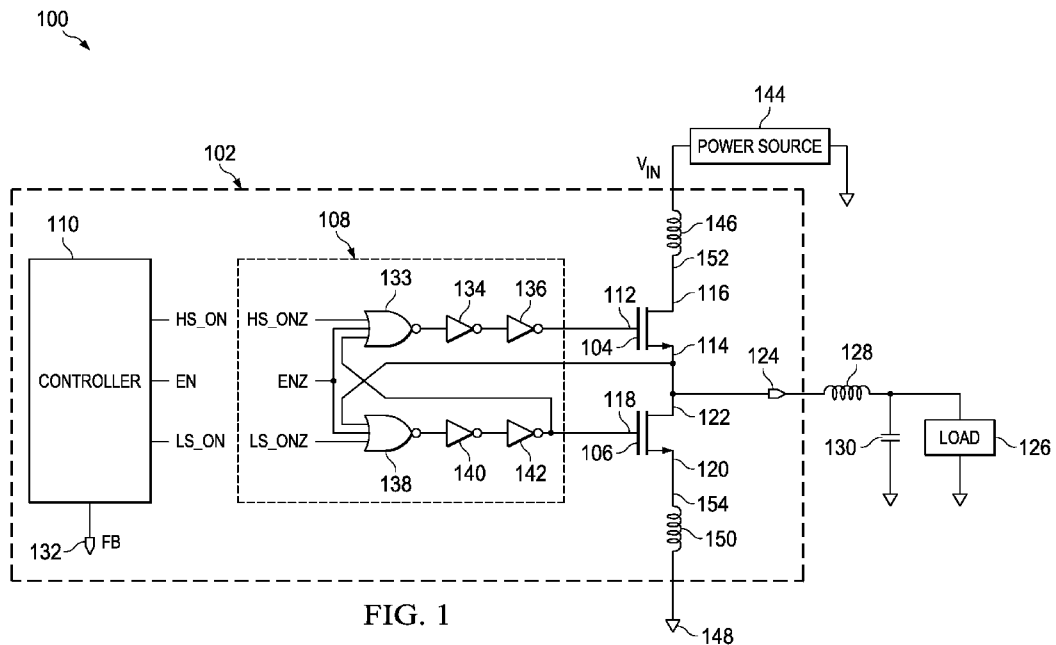


FIG. 1

(57) Abstract: A system (100) comprises a DC-to-DC voltage converter (102), the DC-to-DC voltage converter comprising: a high-side FET (104) comprising a gate, a source, and a drain; a node (124) coupled to the source of the high-side FET (104); a low-side FET (106) comprising a gate, a source, and a drain coupled to the node (124); and a controller (110) coupled to the gate of the high-side FET (104) to switch on and off the high-side FET (104), and coupled to the gate of the low-side FET (106) to switch on and off the low-side FET (106), the controller configured to switch on the low-side FET (106) for a time interval before switching on the high-side FET (104) and to switch off the low-side FET (106) before switching on the high-side FET (104).



HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

DC-TO-DC VOLTAGE CONVERTERS WITH CONTROLLERS

BACKGROUND

[0001] A step-down DC-to-DC voltage converter regulates a load voltage, where the load voltage is less in value than an input voltage provided by a power source. A buck converter topology denotes a class of DC-to-DC voltage converters with switching devices to control current through an inductor (and usually also a capacitor) to regulate the load voltage. A buck converter includes a high-side switching device to couple the inductor to the power source, and a low-side switching device to provide a current path from ground to the inductor when the high-side switching device is switched off. In some buck converters, the high-side switching device is a Field-Effect Transistor (FET), referred to as a high-side FET, and the low-side device is an FET, referred to as a low-side FET, or a diode, sometimes referred to as a flyback diode.

SUMMARY

[0002] In accordance with at least one example of the disclosure, a system comprises a DC-to-DC voltage converter, the DC-to-DC voltage converter comprising: a high-side FET comprising a gate, a source, and a drain; a node coupled to the source of the high-side FET; a low-side FET comprising a gate, a source, and a drain coupled to the node; and a controller coupled to the gate of the high-side FET to switch on and off the high-side FET, and coupled to the gate of the low-side FET to switch on and off the low-side FET, the controller configured to switch on the low-side FET for a time interval before switching on the high-side FET and to switch off the low-side FET before switching on the high-side FET.

[0003] In accordance with at least one example of the disclosure, a system comprises: an inductor; a first FET to conduct current to the inductor when switched on; a diode coupled to the inductor to conduct current to the inductor when the first FET is switched off; a second FET coupled in parallel with the diode; and a controller to switch on the second FET for a time interval before switching on the first FET and to switch off the second FET before switching on the first FET.

[0004] In accordance with at least one example of the disclosure, a method to operate a DC-to-

DC voltage converter comprises: switching on and off a high-side FET and a low-side FET in the DC-to-DC voltage converter to regulate a voltage at a node in the DC-to-DC voltage converter; during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for a time interval before switching on the high-side FET; and during asynchronous operation of the DC-to-DC voltage converter, switching off the low-side FET before switching on the high-side FET.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a detailed description of various examples, reference will now be made to the accompanying drawings in which:

[0006] FIG. 1 shows a system comprising a DC-to-DC voltage converter in accordance with various examples;

[0007] FIG. 2 shows a timing diagram in accordance with various examples;

[0008] FIG. 3 shows a system comprising a DC-to-DC voltage converter in accordance with various examples;

[0009] FIG. 4 shows a method in accordance with various examples;

[0010] FIG. 5 shows a controller in accordance with various examples;

[0011] FIG. 6 shows a timing diagram in accordance with various examples;

[0012] FIG. 7 shows a system comprising a DC-to-DC voltage converter in accordance with various examples; and

[0013] FIG. 8 shows a system comprising a DC-to-DC voltage converter in accordance with various examples.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0014] In many conventional DC-to-DC voltage converters having a buck converter topology with a high-side device and a low-side device, during asynchronous mode operation when the low-side device is forward diode-conducting, the conduction current of majority carriers in the low-side device causes charging of its space region. When the high-side device is switched on to provide current to a load, some of the current in the high-side device is used to discharge the space region, resulting in unwanted power consumption. Furthermore, because of parasitic inductance, the current used to discharge the space region can result in unwanted noise spikes, which may interfere with other circuits coupled to the conventional DC-to-DC voltage converter.

[0015] Embodiments include a DC-to-DC voltage converter with a controller so that during

asynchronous operation, the controller turns on a low-side FET for a time interval before turning on a high-side FET so as to discharge the space region.

[0016] FIG. 1 depicts an illustrative system 100 comprising a DC-to-DC voltage converter 102. In some embodiments, the DC-to-DC voltage converter 102 is a buck-converter. The DC-to-DC voltage converter 102 comprises a high-side FET 104, a low-side FET 106, a gate driver 108, and a controller 110. (The gate driver 108 may also include a charge pump for some embodiments.) The controller 110 is coupled to the high-side FET 104 and the low-side FET 106 by way of the gate driver 108. Embodiments can include other modules (not shown) in addition to the controller 110 and the gate driver 108.

[0017] The high-side FET 104 comprises a gate 112, a source 114, and a drain 116. A node 124 is coupled to the source 114 of the high-side FET 104. The node 124 is referred to as a switching node, and it can be a pin. The low-side FET 106 comprises a gate 118, a source 120, and a drain 122 coupled to the node 124.

[0018] By way of the gate driver 108, the controller 110 is coupled to the gate 112 of the high-side FET 104 to switch on and off the high-side FET 104 and is coupled to the gate 118 of the low-side FET 106 to switch on and off the low-side FET 106 so as to provide a load voltage to a load 126. The load 126 is coupled to the node 124 by way of an inductor 128 and a capacitor 130.

[0019] The drain 116 of the high-side FET 104 is coupled to a power source 144, where FIG. 1 illustrates the power source 144 providing a voltage V_{IN} as an input voltage to the DC-to-DC voltage converter 102. A parasitic inductor 146 represents parasitic inductance associated with the coupling of the drain 116 to the power source 144. This coupling can include an input-output (I/O) pin (not shown). The source 120 of the low-side FET 106 is coupled to a ground 148. A parasitic inductor 150 represents parasitic inductance associated with the coupling of the source 120 to the ground 148. This coupling can include an I/O pin (not shown).

[0020] In the particular embodiment illustrated in FIG. 1, the controller 110 provides to the gate driver 108 the logic signals HS_ON, EN, and LS_ON to switch on and off the high-side FET 104 and the low-side FET 106. The logical complements of these signals, denoted in FIG. 1 respectively as HS_ONZ, ENZ, and LS_ONZ, are indicated as signals in the gate driver 108.

[0021] The gate driver 108 comprises a NOR gate 132 coupled to serially-connected buffers 134 and 136, where the buffer 136 directly drives the gate 112 of the high-side FET 104. In practice, more than two buffers may be serially connected between the output of the NOR gate 132 and the

gate 112 of the high-side FET 104, but for ease of illustration only two such buffers, the buffers 134 and 136, are explicitly shown.

[0022] The gate driver 108 comprises a NOR gate 138 coupled to serially-connected buffers 140 and 142, where the buffer 142 directly drives the gate 118 of the low-side FET 106. In practice, more than two buffers may be serially connected between the output of the NOR gate 138 and the gate 118 of the low-side FET 106, but for ease of illustration only two such buffers, the buffers 140 and 142, are explicitly shown.

[0023] The signals HS_ONZ and ENZ are provided as two inputs to the NOR gate 132, and the output of the buffer 142 is provided as a third input to the NOR gate 132. The signals LS_ONZ and ENZ are provided as two inputs to the NOR gate 138, and the source 114 of the high-side FET 104 is connected to a third input of the NOR gate 138.

[0024] To enable the gate driver 108, the controller 110 asserts the signal EN to HIGH (the signal ENZ is de-asserted to LOW). With the gate driver 108 enabled, the controller 110 can operate the DC-to-DC voltage converter 102 in a synchronous mode or in an asynchronous (or non-synchronous) mode, depending upon the signals HS_ON and LS_ON.

[0025] When the controller 110 operates the DC-to-DC voltage converter 102 in synchronous mode, the signals HS_ON and LS_ON are alternatively cycled between HIGH and LOW without overlap, and such that the high-side FET 104 and the low-side FET 106 are not both simultaneously on. A feedback circuit (not shown) provides a feedback signal to a feedback node 132 so that the controller 110 can control the duty cycles of the signals HS_ON and LS_ON to provide a regulated load voltage to the load 126.

[0026] When the controller 110 operates the DC-to-DC voltage converter 102 in an asynchronous mode, the signal LS_ON is de-asserted to LOW (LS_ONZ is asserted to HIGH) so that the gate 118 of the low-side FET 106 is held LOW. The feedback circuit (not shown) provides a feedback signal to the feedback node 132 so that the controller 110 can control the duty cycle of the signal HS_ON so that a regulated load voltage is provided to the load 126. The low-side FET 106 operates as a flyback diode to conduct current to the inductor 128 when the low-side FET 106 is forward conducting. When the controller 110 de-asserts the signal HS_ON to LOW (the signal HS_ONZ is asserted HIGH) to switch off the high-side FET 104, the low-side FET 106 becomes forward conducting when the voltage at the node 124 falls to a forward voltage drop below ground voltage, about -0.7V. When the controller 110 asserts the signal HS_ON to HIGH (the signal

HS_ONZ is LOW), the high-side FET 104 is switched on to provide current to the inductor 128 by way of the node 124, and as the voltage at the node 124 rises, the low-side FET 106 becomes reversed biased.

[0027] During asynchronous mode operation when the low-side FET 106 is forward conducting, the conduction current of majority carriers in the low-side FET 106 causes charging of its space region. If the charge stored in the space region is not removed, then when the controller 110 switches on the high-side FET 104, some of the current provided by the high-side FET 104 would be used to discharge the space region. The current used to discharge the space region, referred to as a recovery space charge current, flows across a voltage drop of V_{IN} , resulting in unwanted power consumption. Furthermore, because of the parasitic inductance represented by the parasitic inductors 146 and 150, the recovery space charge current results in noise spikes at nodes 152 and 154. These noise spikes may interfere with other circuits (not shown) coupled to the DC-to-DC voltage converter 102.

[0028] During asynchronous operation, in the embodiment of FIG. 1, the controller 110 is configured to switch on the low-side FET 106 for a time interval before switching on the high-side FET 104 and to switch off the low-side FET 106 before switching on the high-side FET 104. The controller 110 is configured to switch on the low-side FET 106 for the time interval to discharge a space region in the low-side FET 106 developed during forward conduction of the low-side FET 106 when the DC-to-DC voltage converter 102 is in asynchronous operation. The value of the time interval can be chosen so that the space region is discharged, and this value can be a function of the size of the low-side FET 106 (and/or the size of a flyback diode if used).

[0029] FIG. 2 depicts an illustrative timing diagram 200 when an embodiment, such as the DC-to-DC voltage converter 102, is in an asynchronous mode, showing voltage as a function of time for the logic signals LS_ON and LS_ON, and a signal SW representing the voltage at the node 124. The timing diagram 200 does not represent realistic depictions of the signals LS_ON, LS_ON, and SW, but it serves to represent descriptive characteristics of an embodiment, such as the illustrative system 100.

[0030] Two cycles are shown in FIG. 2 starting at a time t_1 where the signals HS_ON and LS_ON are both LOW and the low-side FET 106 starts to forward conduct when the signal SW drops to about -0.7V. A portion of the signal SW labeled 202 indicates charging of the space region of the low-side FET 106 while forward conducting.

[0031] At a time t_1 when the signal HS_ON is LOW and before the controller 110 asserts HIGH the signal HS_ON, the controller 110 asserts HIGH the signal LS_ON to switch ON the low-side FET 106, indicated by a portion of the signal LS_ON labeled 204. While switched on, the low-side FET 106 discharges the space region, indicated by an event labeled 206, bringing the signal SW to 0V. The controller 110 switches off the low-side FET 106 at a time t_2 by de-asserting the signal LS_ON to LOW. At a time t_3 , the controller 110 asserts HIGH the signal HS_ON, causing the signal SW to rise in voltage indicated by an event labeled 208. Accordingly, the controller 110 is configured during asynchronous operation of the DC-to-DC voltage converter 102 to switch on the low-side FET 106 for a time interval (represented by the time difference t_2-t_1) before switching on the high-side FET 104 and to switch off the low-side FET 106 before switching on the high-side FET 104.

[0032] At a time t_4 , the controller 110 de-asserts the signal HS_ON to LOW so as to switch off the high-side FET 104, indicated by an event labeled 210, resulting in the low-side FET 106 forward conducting and charging of the space region. The cycle repeats, with an event labeled 212 denoting the assertion of the signal LS_ON to HIGH at a time t_5 to switch on the low-side FET 106 for a time interval lasting until a time t_6 . This event causes discharging of the space region, and at a time t_7 the controller 110 asserts the signal HS_ON to HIGH to again switch on the high-side FET 104, indicated by an event labeled 214.

[0033] FIG. 3 depicts an illustrative system 300 comprising a DC-to-DC voltage converter 302, with components similar to that of the DC-to-DC converter 102 in FIG. 1 sharing the same labels as in FIG. 1. Details of the gate driver 108 and the parasitic inductors 146 and 150 are not shown in FIG. 3. The DC-to-DC voltage converter 302 operates in similar fashion as the DC-to-DC voltage converter 102, but it includes a diode 304 to serve as a flyback diode. The diode 304 is coupled in parallel with the low-side FET 106. The 304 diode comprises an anode 306 coupled to the source 120 of the low-side FET 106, and comprises a cathode 308 coupled to the node 124.

[0034] During asynchronous operation, the diode 304 provides a current path from the ground 148 to the inductor 128 when the diode 304 is forward conducting. The space region within the diode 304 is charged during forward conduction, and the controller 110 switches on the low-side FET 106 to discharge the space region of the diode 304.

[0035] The descriptions of the illustrative system 100 of FIG. 1 and the illustrative timing diagram 200 of FIG. 2 are applicable to the illustrative system 300 of FIG. 3, where it is

understood that the space region in the diode 304 is discharged during asynchronous operation when the low-side FET 106 is switched on for a time interval, e.g., the time intervals in FIG. 2 from t_1 to t_2 , or from t_5 to t_6 . Accordingly, the controller 110 is configured to switch on the low-side FET 106 for the time interval to discharge a space region in the diode 304 developed during forward conduction of the diode 304.

[0036] FIG. 4 depicts an illustrative method 400 of operating the DC-to-DC voltage converter 102, where some or all of the steps in the illustrative method 400 can be performed with circuits that are hardwired, firmware controlled, software controlled, or a combination thereof. The illustrative method 400 to operate the DC-to-DC voltage converter 102 comprises: in step 402, switching on and off a high-side FET and a low-side FET in the DC-to-DC voltage converter to regulate a voltage at a node in the DC-to-DC voltage converter; in step 404, during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for a time interval before switching on the high-side FET; and in step 406, during asynchronous operation of the DC-to-DC voltage converter, switching off the low-side FET before switching on the high-side FET.

[0037] The illustrative method 400 further comprises, in step 408, during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for the time interval to discharge a space region in a diode developed during forward conduction of the diode, wherein the diode is coupled in parallel with the low-side FET. The illustrative method 400 further comprises, in step 410, during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for the time interval to discharge a space region in the low-side FET developed during forward conduction of the low-side FET when the DC-to-DC voltage converter is in asynchronous operation.

[0038] In the embodiments of FIG. 1 and FIG. 3, the high-side FET 104 and the low-side FET 106 are illustrated each as an n-Metal-Oxide-Semiconductor Field-Effect Transistor (nMOSFET). In some embodiments, a p-Metal-Oxide-Semiconductor Field-Effect Transistor (pMOSFET) can be used in place of a FET.

[0039] FIG. 5 depicts the illustrative controller 110 comprising logic and circuit elements to generate the logic signals HS_ON and LS_ON when in the asynchronous mode. FIG. 5 further illustrates various logic signals used in generating the logic signals HS_ON and LS_ON, labeled Low Qrr, HS, Block_LS, and LS. Not all circuit elements in the illustrative controller 110 are shown. FIG. 6 depicts an illustrative timing diagram 600 for the logic signals HS_ON, LS_ON,

Low Qrr, HS, Block_LS, and LS of FIG. 5.

[0040] The logic signal Low Qrr is asserted HIGH periodically to indicate operation in the asynchronous mode, so that the logic signal LS_ON is asserted HIGH for a time interval before HS_ON is asserted HIGH so as to discharge a space region in the low-side FET 106. The logic signal Low Qrr is provided as a preset signal a latch 502, and as an input signal to a timer 504. When the logic signal Low Qrr is asserted HIGH, the timer 504 de-asserts the logic signal HS to LOW, and the logic signal HS is again asserted HIGH at a later time specified by the timer 504, as indicated in the illustrative timing diagram 600 of FIG. 6. The logic signal HS is provided as a clock signal to the latch 502.

[0041] The output of the latch 502 is the logic signal Block_LS, illustrated in the illustrative timing diagram 600. The logic signal Block_LS, after a logical inversion, is provided as an input to an AND gate 506 and as an input to an AND gate 508 after a delay indicated by a delay element 510. The logic signal HS is provided as an input to the AND gate 508.

[0042] The output of the AND gate 508 is the logic signal HS_ON. A logical inversion of the logic signal HS_ON, denoted as the logic signal LS, is provided as an input to the AND gate 506. The output of the AND gate 506 is the logic signal LS_ON. The delay element 510 delays the output of the latch 502 so that the logic signal LS_ON is de-asserted to LOW before the logic signal HS_ON is asserted HIGH, as indicated in the illustrative timing diagram 600. In this way, the low-side FET 106 is switched off before the high-side FET 104 is switched on.

[0043] FIG. 5 provides a particular example of a circuit to generate the logic signals HS_ON and LS_ON, but many different circuit configurations can be employed to generate these logic signals.

[0044] In conventional switching, the power source 144 provides the reverse recovery charge via the high-side FET 104, resulting in lower efficiency and greater heat loss due to the power loss in both the high-side FET 104 and the low-side FET 106 (and/or the diode 304). By discharging the space charge region in the low-side FET 106 when the node 124 is close to 0V, there is relatively little power loss due to discharging the space charge region. Power efficiency is improved. Furthermore, ringing is reduced because the high-side FET 104 need not conduct extra current for a reverse recovery charge. There is no need for specially designed diodes or gate drivers.

[0045] Embodiments are also applicable to other types of DC-to-DC voltage converters where the space charge developed in a diode during asynchronous operation is discharged before energizing the inductor. FIG. 7 and FIG. 8 provide two such examples.

[0046] FIG. 7 depicts an illustrative system 700 comprising a DC-to-DC voltage converter 702. The illustrative system 700 is configured as a boost DC-to-DC voltage converter, comprising a first FET 704 to conduct current to the inductor 128 when switched on; a diode 706 coupled to the inductor 128 to conduct current to the inductor 128 when the first FET 704 is switched off; a second FET 708 coupled in parallel with the diode 706; and the controller 110 to switch on the second FET 708 for a time interval before switching on the first FET 704 and to switch off the second FET 708 before switching on the first FET 704. The load 126 is coupled to the diode 706 and the inductor 128 (by way of the diode 706 and the power source 144).

[0047] The first FET 704 conducts current from the power source 144 to the inductor 128 when switched on to energize the inductor 128 (increase the stored magnetic energy). The diode 706 provides a current path for the inductor 128 during asynchronous operation as the inductor 128 provides energy (from its decreasing magnetic field) to the load 126. The second FET 708 discharges the space charge region developed in the diode 706 when it has conducted current to the inductor 128 during asynchronous operation.

[0048] The timing diagram of FIG. 2 is applicable to the embodiment of FIG. 7, where the first FET 704 may be identified with the high-side FET 104 (HS_ON in FIG. 2) and the second FET 708 may be identified with the low-side FET 106 of FIG. 3 (LS_ON of FIG. 2). Accordingly, when describing the previous embodiments of FIG. 1 or FIG. 3, the high-side FET 104 can be referred to as a first FET, and the low-side FET 106 can be referred to as a second FET. Furthermore, in some embodiments the diode 706 may be part of the second FET 708, so that the second FET 708 includes the diode 706.

[0049] FIG. 8 depicts an illustrative system 800 comprising a DC-to-DC voltage converter 802. The illustrative system 800 is configured as a buck-boost DC-to-DC voltage converter, comprising a first FET 804 to conduct current to the inductor 128 when switched on; a diode 806 coupled to the inductor 128 to conduct current to the inductor 128 when the first FET 804 is switched off; a second FET 808 coupled in parallel with the diode 806; and the controller 110 to switch on the second FET 808 for a time interval before switching on the first FET 804 and to switch off the second FET 808 before switching on the first FET 804. The load 126 is coupled to the diode 806 and the inductor 128 (by way of the diode 806 and the power source 144).

[0050] The first FET 804 conducts current from the power source 144 to the inductor 128 when switched on to energize the inductor 128 (increase the stored magnetic energy). The diode 806

provides a current path for the inductor 128 during asynchronous operation as the inductor 128 provides energy (from its decreasing magnetic field) to the load 126. The second FET 808 discharges the space charge region developed in the diode 806 when it has conducted current to the inductor 128 during asynchronous operation.

[0051] The timing diagram of FIG. 2 is applicable to the embodiment of FIG. 8, where the first FET 804 may be identified with the high-side FET 104 (HS_ON in FIG. 2) and the second FET 808 may be identified with the low-side FET 106 of FIG. 3 (LS_ON of FIG. 2).

[0052] In the foregoing discussion and in the claims, the terms “including” and “comprising” are used in an open-ended fashion, and thus should be interpreted to mean “including, but not limited to... .” Also, the term “couple” or “couples” is intended to mean either an indirect or direct connection. Thus, if a first device couples to a second device, that connection may be through a direct connection or through an indirect connection via other devices and connections. Similarly, a device that is coupled between a first component or location and a second component or location may be through a direct connection or through an indirect connection via other devices and connections. An element or feature that is “configured to” perform a task or function may be configured (e.g., programmed or structurally designed) at a time of manufacturing by a manufacturer to perform the function and/or may be configurable (or re-configurable) by a user after manufacturing to perform the function and/or other additional or alternative functions. The configuring may be through firmware and/or software programming of the device, through a construction and/or layout of hardware components and interconnections of the device, or a combination thereof. Additionally, uses of the phrases “ground” or similar in the foregoing discussion are intended to include a chassis ground, an Earth ground, a floating ground, a virtual ground, a digital ground, a common ground, and/or any other form of ground connection applicable to, or suitable for, the teachings of the present disclosure. Unless otherwise stated, “about,” “approximately,” or “substantially” preceding a value means +/- 10 percent of the stated value.

[0053] The above discussion is meant to be illustrative of the principles and various embodiments of the present disclosure. Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

CLAIMS

What is claimed is:

1. A system comprising a DC-to-DC voltage converter, the DC-to-DC voltage converter comprising:
 - a high-side Field-Effect Transistor (FET) comprising a gate, a source, and a drain;
 - a node coupled to the source of the high-side FET;
 - a low-side FET comprising a gate, a source, and a drain coupled to the node; and
 - a controller coupled to the gate of the high-side FET to switch on and off the high-side FET, and coupled to the gate of the low-side FET to switch on and off the low-side FET, the controller configured to switch on the low-side FET for a time interval before switching on the high-side FET and to switch off the low-side FET before switching on the high-side FET.
2. The system of claim 1, the controller further configured to operate the DC-to-DC voltage converter in an asynchronous mode when configured to switch on the low-side FET for a time interval before switching on the high-side FET and to switch off the low-side FET before switching on the high-side FET.
3. The system of claim 2, further comprising:
 - an inductor coupled to the node.
4. The system of claim 3, further comprising:
 - a power source coupled to the drain of the high-side FET.
5. The system of claim 4, further comprising:
 - a ground coupled to the source of the low-side FET.
6. The system of claim 1, further comprising:
 - an inductor coupled to the node.
7. The system of claim 6, further comprising:
 - a power source coupled to the drain of the high-side FET.
8. The system of claim 7, further comprising:
 - a ground coupled to the source of the low-side FET.
9. The system of claim 1, the DC-to-DC converter further comprising:
 - a gate driver coupled to the gate of the high-side FET and coupled to the gate of the low-side FET, the controller coupled to the gate driver to switch on and off the high-side FET and to switch on and off the low-side FET.

10. The system of claim 1, the DC-to-DC converter further comprising:
 - a diode comprising an anode coupled to the source of the low-side FET, and comprising a cathode coupled to the node.
11. A system comprising:
 - an inductor;
 - a first Field-Effect Transistor (FET) to conduct current to the inductor when switched on;
 - a diode coupled to the inductor to conduct current to the inductor when the first FET is switched off;
 - a second FET coupled in parallel with the diode; and
 - a controller to switch on the second FET for a time interval before switching on the first FET and to switch off the second FET before switching on the first FET.
12. The system of claim 11, wherein the second FET includes the diode.
13. The system of claim 12, further comprising:
 - a power source, the first FET to conduct current from the power source to the inductor when switched on.
14. The system of claim 11, further comprising:
 - a power source, the first FET to conduct current from the power source to the inductor when switched on.
15. The system of claim 11, further comprising:
 - a load coupled to the diode and to the inductor.
16. The system of claim 15, wherein the second FET includes the diode.
17. The system of claim 15, further comprising:
 - a power source, the first FET to conduct current from the power source to the inductor when switched on.
18. A method to operate a DC-to-DC voltage converter, the method comprising:
 - switching on and off a high-side Field-Effect Transistor (FET) and a low-side FET in the DC-to-DC voltage converter to regulate a voltage at a node in the DC-to-DC voltage converter;
 - during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for a time interval before switching on the high-side FET; and

during asynchronous operation of the DC-to-DC voltage converter, switching off the low-side FET before switching on the high-side FET.

19. The method of claim 18, further comprising:

during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for the time interval to discharge a space region in a diode developed during forward conduction of the diode, wherein the diode is coupled in parallel with the low-side FET.

20. The method of claim 18, further comprising:

during asynchronous operation of the DC-to-DC voltage converter, switching on the low-side FET for the time interval to discharge a space region in the low-side FET developed during forward conduction of the low-side FET when the DC-to-DC voltage converter is in asynchronous operation.

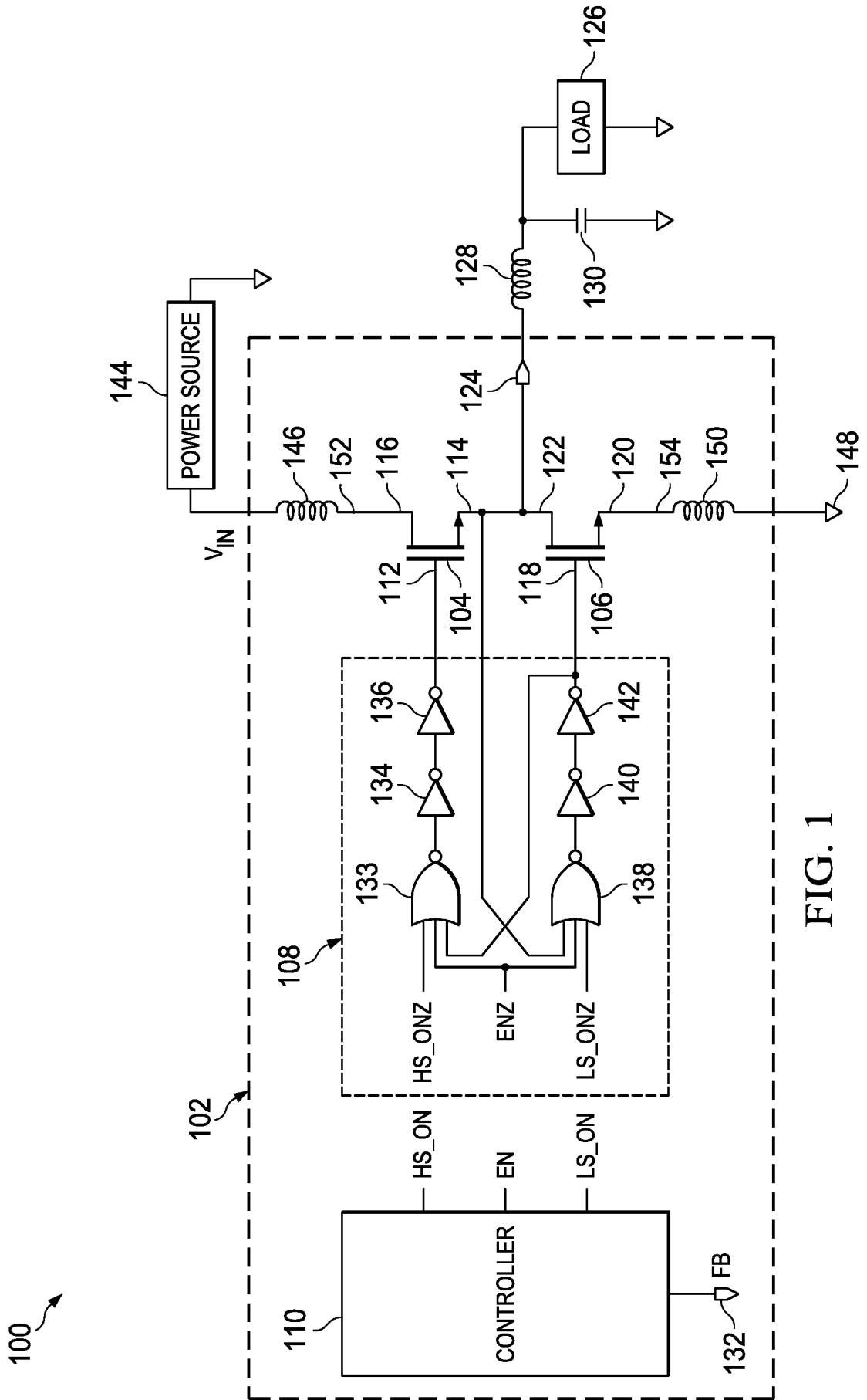


FIG. 1

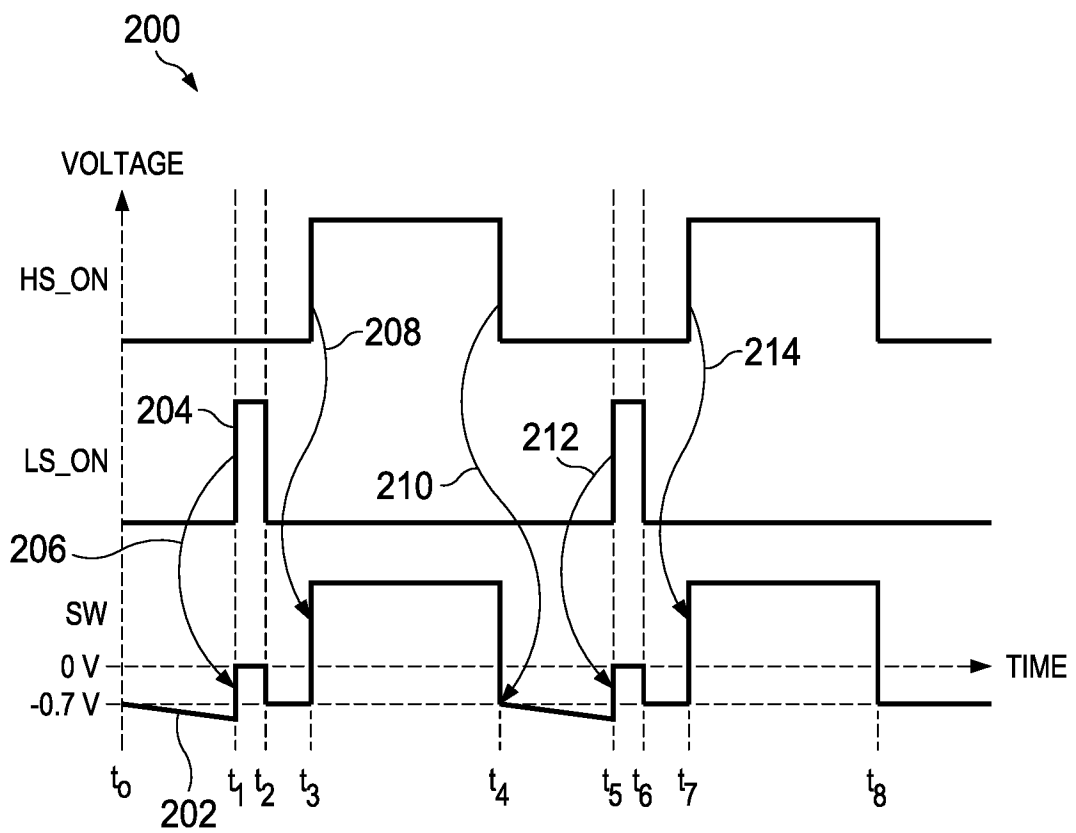


FIG. 2

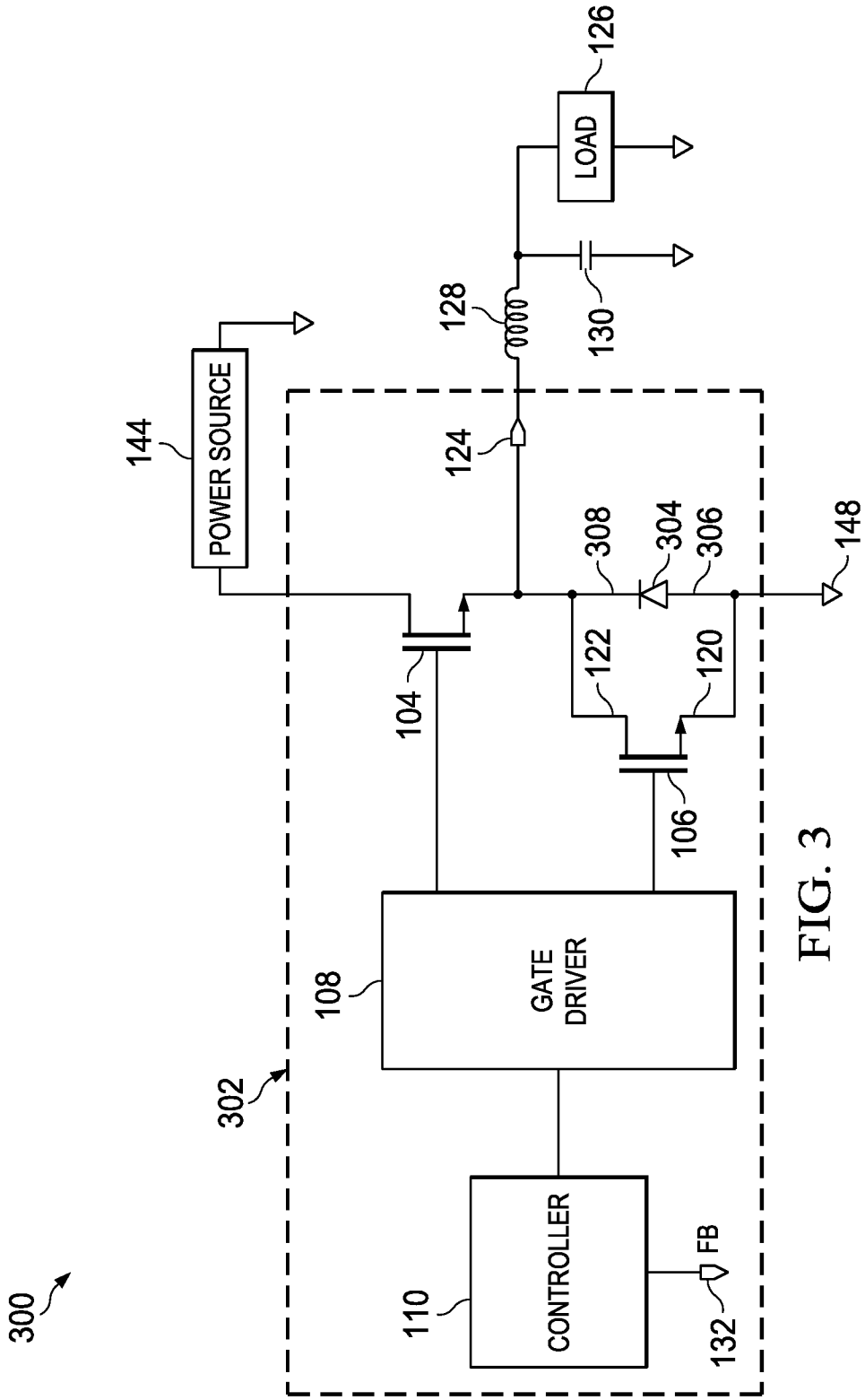


FIG. 3

4/8

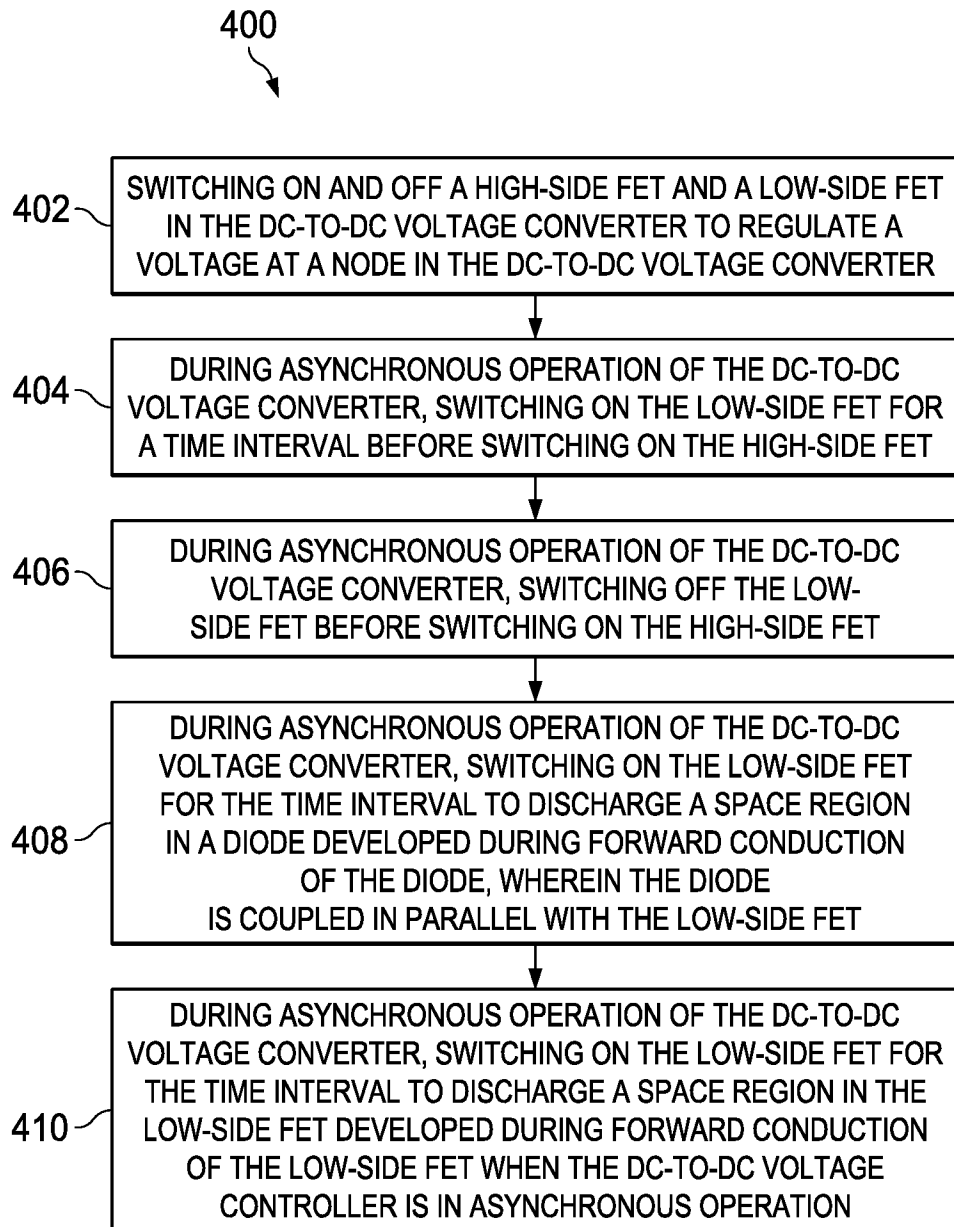


FIG. 4

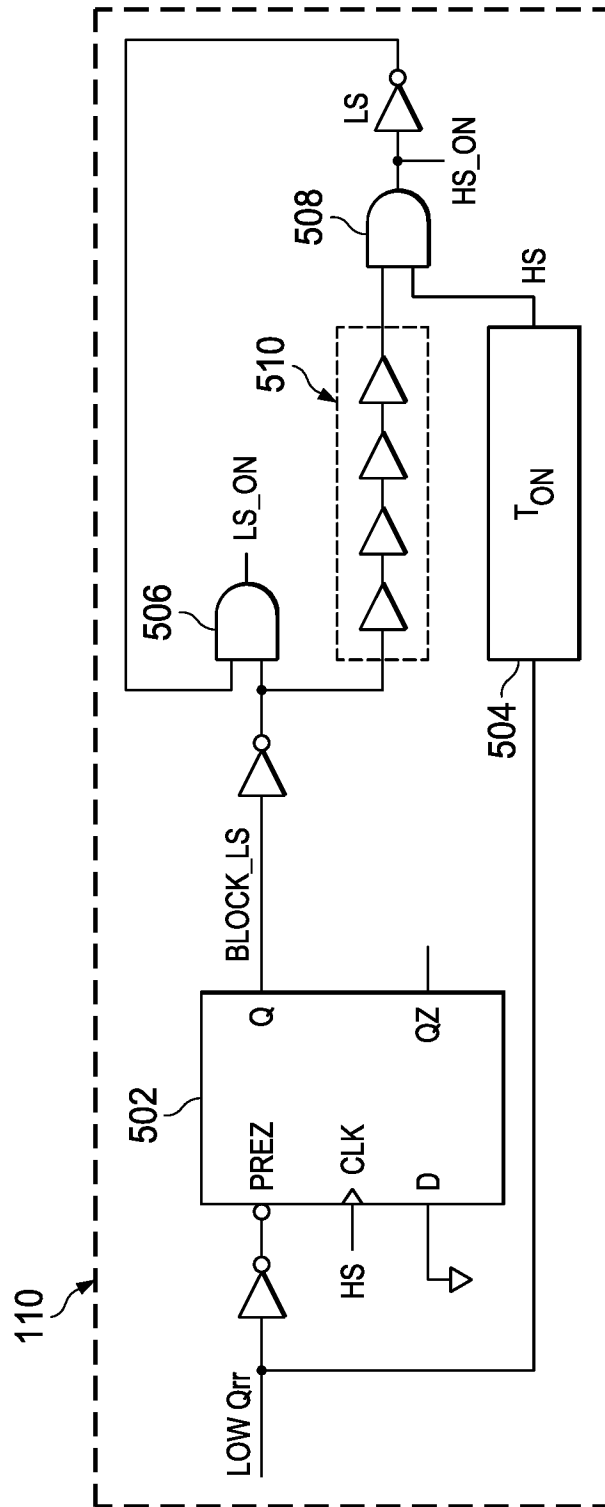


FIG. 5

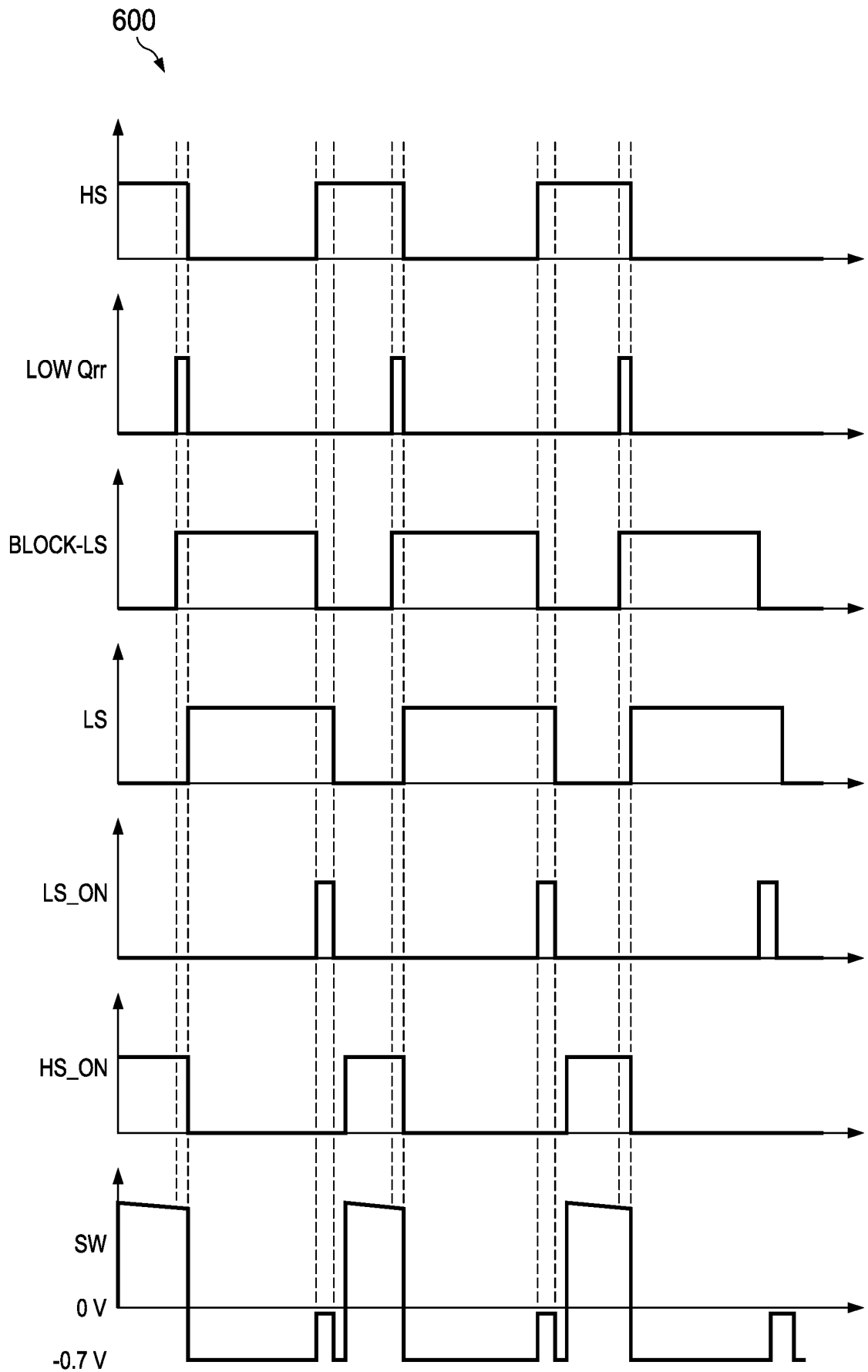


FIG. 6

700 ↗

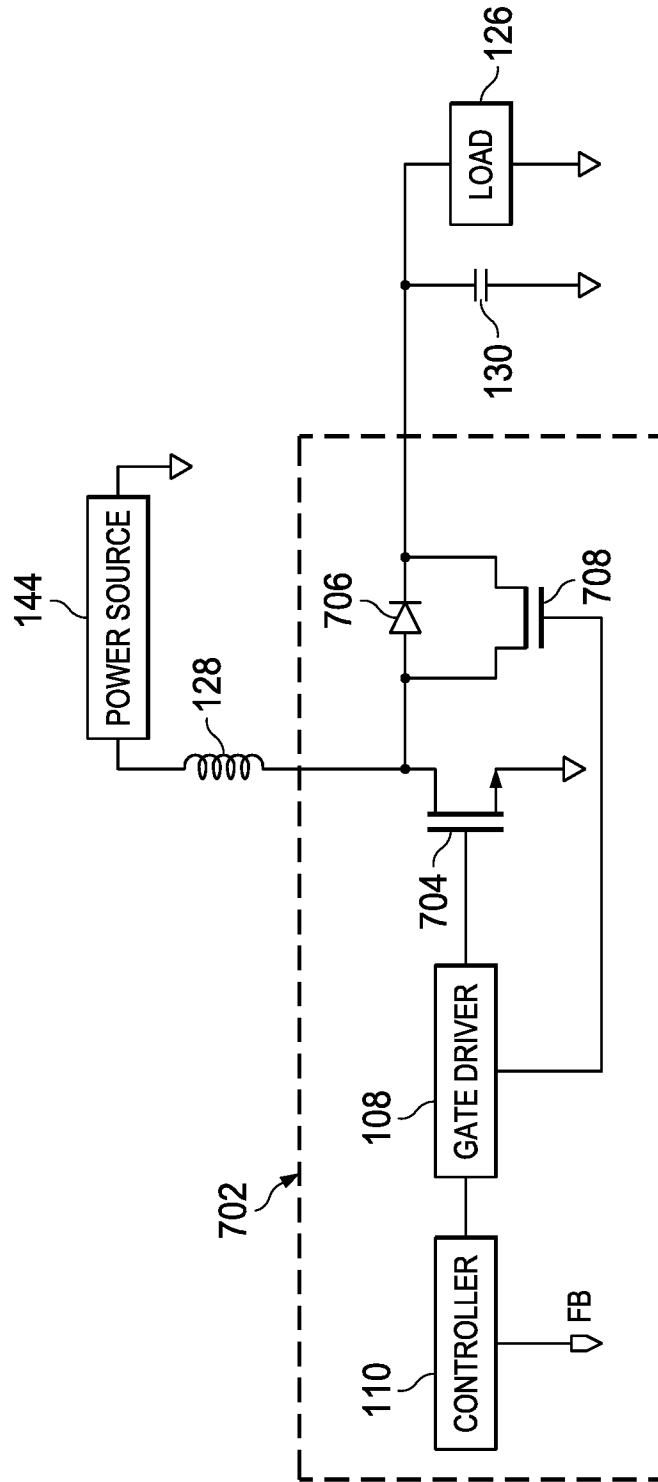


FIG. 7

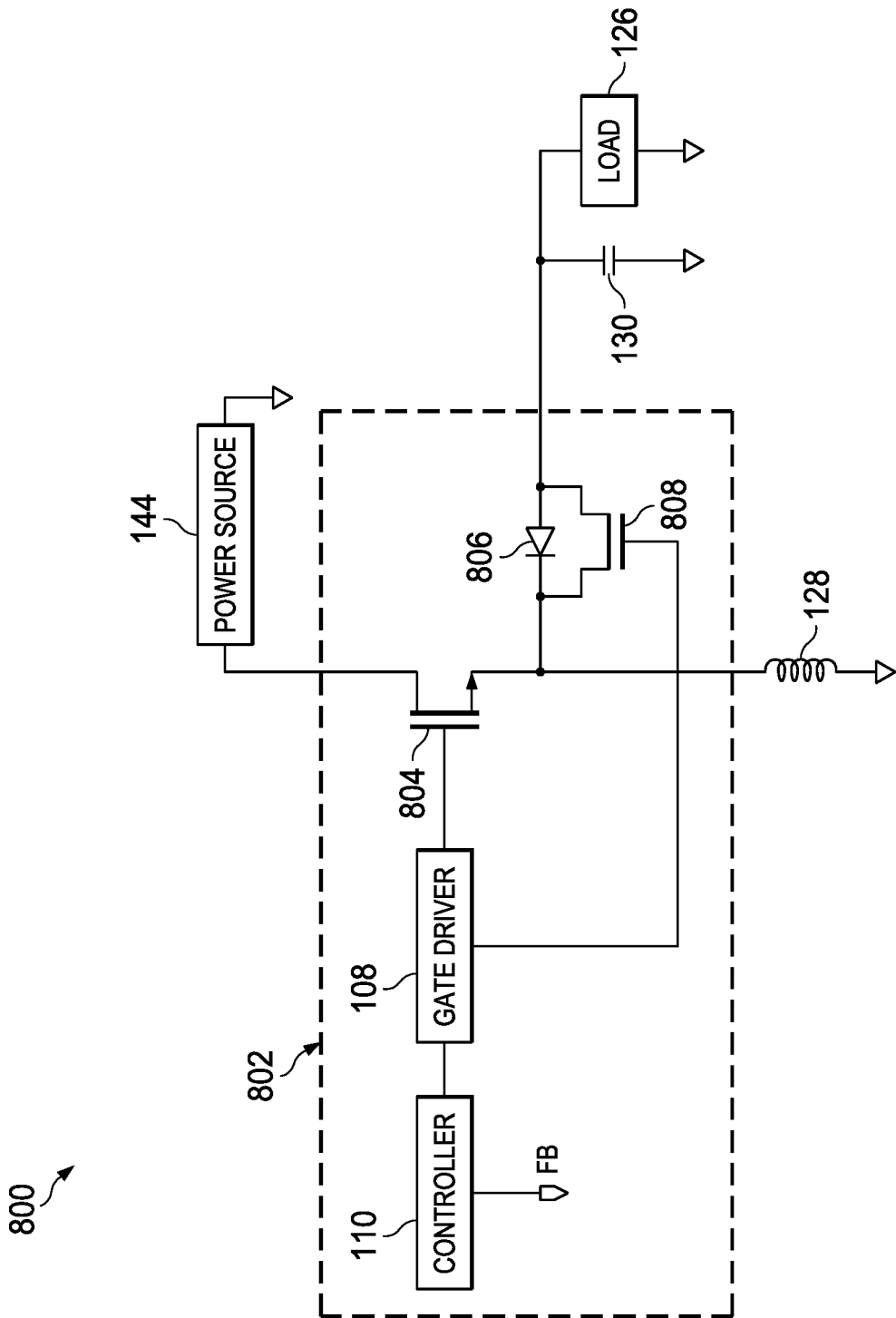


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/039814

A. CLASSIFICATION OF SUBJECT MATTER		
<i>H02M 1/088 (2006.01)</i> <i>H02M 3/145 (2006.01)</i> <i>H02M 3/157 (2006.01)</i> <i>H02M 3/158 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H02M 3/02-3/158, 7/033, G05F 1/565		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5428713 B2 (SANKEN ELECTRIC CO LTD) 26.02.2014	1-20
A	US 5414341 A (BENCHMARQ MICROELECT INC) 09.05.1995	1-20
A	WO 2002/063770 A2 (KONINKLIJKE PHILIPS ELECTRONICS N.V.) 15.08.2002	1-20
A	EP 2704301 B1 (STICHTING IMEC NEDERLAND) 27.07.2016	1-20
A	JP 2010200554 A (FUJI ELECTRIC SYSTEMS CO LTD) 09.09.2010	1-20
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents:		
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
Date of the actual completion of the international search		Date of mailing of the international search report
18 September 2019 (18.09.2019)		26 September 2019 (26.09.2019)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer A. Golovchenko Telephone No. (495) 531-64-81