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13/834,362 15 March 2013 (15.03.2013) US(71) Applicant: **CONVEY COMPUTER** [US/US]; 1302 E. Collins Blvd., Richardson, TX 75081 (US).(72) Inventors: **LEIDEL, John, D.**; 3600 Lindale Dr., McKinney, TX 75070 (US). **WADLEIGH, Kevin, R.**; 2901 Valley Spring Drive, Plano, TX 75025 (US). **BOLDING, Joe**; 803 Holly Circle, Allen, TX 75002 (US). **BREWER, Tony**; 5225 Mariners Drive, Plano, TX 75093 (US). **WALKER, Dean, E.**; 1829 Chattam Ct., Plano, TX 75025 (US).(74) Agent: **VIGUET, R., Ross**; Fulbright & Jaworski L.L.P., 2200 Ross Avenue, Suite 2800, Dallas, TX 75201-2784 (US).

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[Continued on next page]

(54) Title: SCHEDULING CONCURRENT APPLICATIONS IN MULTITHREADED PROCESSORS

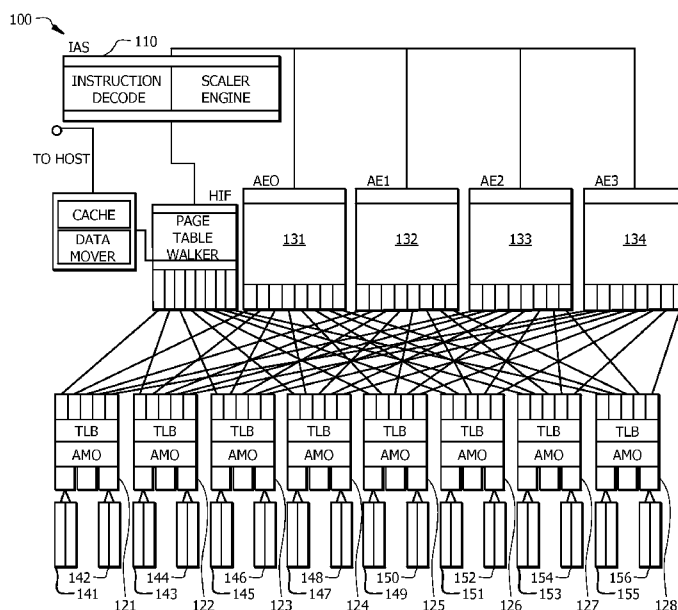


FIG. 1

(57) Abstract: Systems and methods which provide a modular processor framework and instruction set architecture designed to efficiently execute applications whose memory access patterns are irregular or non-unit stride as disclosed. A hybrid multithreading framework (HMTF) of embodiments provides a framework for constructing tightly coupled, chip-multithreading (CMT) processors that contain specific features well-suited to hiding latency to main memory and executing highly concurrent applications. The HMTF of embodiments includes an instruction set designed specifically to exploit the high degree of parallelism and concurrency control mechanisms present in the HMTF hardware modules. The instruction format implemented by a HMTF of embodiments is designed to give the architecture, the runtime libraries, and/or the application ultimate control over how and when concurrency between thread cache units is initiated. For example, one or more bit of the instruction payload may be designated as a context switch bit (CTX) for expressly controlling context switching.



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INTERNATIONAL SEARCH REPORT

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PCT/US13/42439

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 9/46 (2013.01)

USPC - 712/228

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8): G06F 9/46; G06F 9/44; G06F 15/173 (2013.01)

USPC: 712/228, 220, 235; 718/104; 709/224, 225, 226

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patent; USPTO; IEEE; ProQuest; Google Scholar; KEYWORDS: Multithread, processor, schedule, context switch, applications

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2012/0042121 A1 (KIM, D et al.) 16 February 2012; paragraphs [0052], [0055], [0056], [0059].	1, 9, 12, 13 ----- 2-8, 10, 11, 14-19
X --- Y	US 7237088 B2 (BARRY, E et al.) 26 June, 2007; column 2, lines 6-12, column 6, lines 37-48.	20 ----- 5-8, 17, 21, 22
Y	US 2012/0036514 A1 (MASTER, P et al.) 9 February 2012; paragraphs [0052], [0059], [0059], [0089].	2-4, 10, 11, 14-16, 18, 19, 22
Y	US 2012/0131309 A1 (JOHNSON, W et al.) 24 May 2012; paragraphs [1252], [1253], [1255].	3, 15
Y	US 8095778 B1 (GOLLA, R) 10 January 2012; column 10, lines 33-53, column 6, lines 4-8.	11, 19, 21

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