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(54) Title: WIDEBAND BIAS CIRCUITS AND METHODS

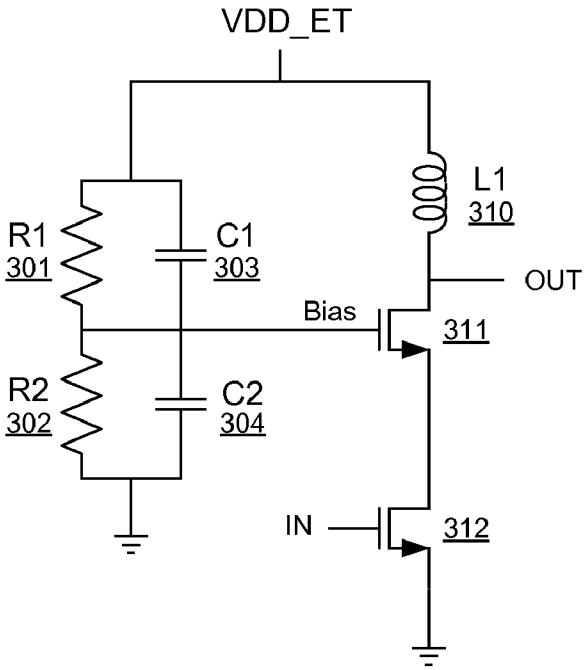

Fig. 3A

(57) Abstract: The present disclosure includes circuits and methods for wideband biasing. In one embodiment, an amplifiers includes a cascode transistor (311) between an input and an output of the amplifier. The cascode transistor (311) receives a bias from a bias circuit comprising a resistor (301) between the power supply (VDD ET) and a first node, a resistor (302) between the first node and a reference voltage, and a capacitor (303) between the power supply (VDD ET) and the first node. The power supply (VDD ET) may be a modulated power supply, which is coupled through the bias circuit to a capacitance (303) at the control terminal of the cascode transistor (311). An inductor (310) is configured between a terminal of the cascode transistor (311) and the power supply (VDD ET). The inductor (310) may isolate the output from the modulated supply signal (VDD ET).

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PATENT APPLICATION
WIDEBAND BIAS CIRCUITS AND METHODS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure claims priority to U.S. App. No. 14/172,150 filed February 4, 2014, the content of which is incorporated herein by reference in its entirety for all purposes. The present disclosure claims priority to U.S. Provisional App. No. 61/876,347 filed September 11, 2013, the content of which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND

[0002] The present disclosure relates to electronic circuits and methods, and in particular, to wideband bias circuits and methods.

[0003] CMOS transistors are occasionally stacked in order to split the voltage swing across multiple devices for reliability purposes. Fig. 1 illustrates a typical amplifier stage. An input signal is applied to the gate of a bottom MOS device 101 (e.g., in common source (CS) configuration). The top cascode device 102 (in common gate (CG) configuration) is commonly biased using a resistive element (e.g., resistor ladder including resistors 103 and 104) between the supply and ground. The cascode device has a gate capacitance 105 that holds a bias voltage. Traditional approaches for biasing nodes in a circuit from a supply voltage using resistive element are satisfactory if the supply voltage maintains a constant (or nearly constant) value. However, in applications where the supply voltage changes, the resistances and capacitances may impair the operation of the circuit.

SUMMARY

[0004] The present disclosure includes circuits and methods for wideband bias circuits. In one example embodiment, an amplifiers includes a cascode transistor between an input and an output of the amplifier. The cascode transistor receives a bias from a bias circuit comprising a resistor between the power supply and a first node, a resistor between the first node and a reference voltage (e.g., ground), and a capacitor

between the power supply and the first node. The power supply may be a modulated power supply, which is coupled through the bias circuit to a capacitance at the control terminal of the cascode transistor. An inductor is configured between a terminal of the cascode transistor and the power supply. The inductor may isolate the output from the modulated power supply signal.

[0005] In one embodiment, the present disclosure includes an amplifier circuit comprising a first transistor having a control terminal, a first terminal, and a second terminal, the control terminal configured to receive an input signal, a cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the second terminal of the cascode transistor is coupled to the first terminal of the first transistor, an inductor having a first terminal coupled to the first terminal of the cascode transistor and a second terminal coupled to a modulated power supply terminal, a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a first node, a second resistor having a first terminal coupled to the first node and a second terminal coupled to a reference voltage, and a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the first node, wherein the first node is coupled to the control terminal of the cascode transistor, and wherein the modulated power supply terminal produces a time varying power supply signal corresponding to the input signal.

[0006] In one embodiment, the control terminal of the cascode transistor comprises a capacitance.

[0007] In one embodiment, the first resistor, the second resistor, and the capacitor are configured to couple the time varying power supply signal to the control terminal of the cascode device across a first range of frequencies greater than a second range of frequencies of the input signal.

[0008] In one embodiment, a first product of a resistance of the first resistor and a capacitance of the capacitor is approximately equal to a second product of a resistance of the second resistor and a capacitance at the control terminal of the cascode transistor.

[0009] In one embodiment, the cascode transistor is a first cascode transistor, the amplifier circuit further comprising a second cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the first terminal of the second

cascode transistor is coupled to the second terminal of the first cascode transistor, and wherein the second terminal of the second cascode transistor is coupled to the first terminal of the first transistor, a third resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a second node, a fourth resistor having a first terminal coupled to the second node and a second terminal coupled to the reference voltage, and a second capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the second node, wherein the second node is coupled to the control terminal of the second cascode transistor.

[0010] In one embodiment, the circuit further comprises a third resistor coupled between the first node and the control terminal of the cascode transistor.

[0011] In one embodiment, the inductor isolates the first terminal of the cascode transistor from the time varying power supply signal on the second terminal of the inductor.

[0012] In one embodiment, a bandwidth of the input signal is less than a bandwidth of the time varying power supply signal.

[0013] In another embodiment, the present disclosure includes a method of amplifying a signal comprising receiving an input signal on a control terminal of a first transistor, the first transistor having a control terminal, a first terminal, and a second terminal, coupling the input signal through the first transistor and a cascode transistor to produce an output signal on a second terminal of the cascode transistor, the cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the second terminal of the cascode transistor is coupled to the first terminal of the first transistor, receiving a time varying power supply voltage from a modulated power supply on a terminal of a bias circuit, the bias circuit comprising a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a first node, a second resistor having a first terminal coupled to the first node and a second terminal coupled to a reference voltage, and a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the first node, wherein the first node is coupled to the control terminal of the cascode transistor, coupling the time varying power supply voltage to the control terminal of the

cascode transistor, and generating an impedance in an inductor having a first terminal coupled to the first terminal of the cascode transistor and a second terminal coupled to a modulated power supply terminal to isolate the first terminal of the cascode transistor from the time varying power supply voltage.

[0014] In one embodiment, the first resistor, the second resistor, and the capacitor are configured to couple the time varying power supply signal to the control terminal of the cascode device across a first range of frequencies greater than a second range of frequencies of the input signal.

[0015] In one embodiment, the bias circuit is a first bias circuit and the cascode transistor is a first cascode transistor, the method further comprising receiving the time varying power supply voltage from the modulated power supply on a terminal of a second bias circuit, the second bias circuit comprising a third resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a second node, a fourth resistor having a first terminal coupled to the second node and a second terminal coupled to the reference voltage, and a second capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the second node, wherein the second node is coupled to the control terminal of the second cascode transistor, and coupling the time varying power supply voltage to the control terminal of the second cascode transistor.

[0016] In one embodiment, the method further comprises coupling the time varying power supply voltage through a third resistor coupled between the first node and the control terminal of the cascode transistor.

[0017] In another embodiment, the present disclosure includes an amplifier circuit comprising a first transistor having a control terminal, a first terminal, and a second terminal, the control terminal configured to receive an input signal, a cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the second terminal is coupled to the first terminal of the first transistor, an inductor having a first terminal coupled to the first terminal of the cascode transistor and a second terminal coupled to receive a modulated power supply terminal, and means for coupling a maximum frequency of a time varying power supply signal corresponding to the input

signal from the modulated power supply terminal to the control terminal of the cascode transistor to bias the cascode transistor.

[0018] In one embodiment, the means for coupling a maximum frequency of the time varying power supply signal comprising a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a control terminal of the cascode transistor, a second resistor having a first terminal coupled to the control terminal of the cascode transistor and a second terminal coupled to a reference voltage, a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the control terminal of the cascode transistor, and a capacitance coupled to the control terminal of the cascode transistor.

[0019] In one embodiment, the means for coupling a maximum frequency of the time varying power supply signal comprising a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a first node, a second resistor having a first terminal coupled to the first node and a second terminal coupled to a reference voltage, a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the first node, a third resistor coupled between the first node and control terminal of the cascode transistor, and a capacitance coupled to the control terminal of the cascode transistor.

[0020] The following detailed description and accompanying drawings provide a better understanding of the nature and advantages of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] Fig. 1 illustrates a traditional bias circuit including resistive and capacitive elements.

[0022] Fig. 2A illustrates an example wideband bias circuit according to one embodiment.

[0023] Fig. 2B illustrates an example wideband bias circuit according to another embodiment.

[0024] Fig. 3A illustrates an example wideband bias circuit in an amplifier circuit according to one embodiment.

[0025] Fig. 3B illustrates frequency response of the example wideband bias circuit in Fig. 3A.

[0026] Fig. 4 illustrates another example of wideband bias circuits according to another embodiment.

[0027] Fig. 5 illustrates another example of wideband bias circuits according to another embodiment.

[0028] Fig. 6 illustrates an example spectrum of an envelope and input signal according to one embodiment.

[0029] Fig. 7A illustrates an example signal according to one embodiment.

[0030] Fig. 7B illustrates an example envelope according to one embodiment.

DETAILED DESCRIPTION

[0031] The present disclosure pertains to wideband bias circuits. In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be evident, however, to one skilled in the art that the present disclosure as expressed in the claims may include some or all of the features in these examples alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0032] Some embodiments of the present disclosure may pertain to envelope tracking applications. In an envelope tracking application, a power supply voltage Vdd may be varied over time to reduce the power consumption of a circuit. The time varying power supply voltage may correspond to an input signal so that the input signal may be processed using less power. One example system using envelope tracking (ET) is a power amplifier in a wireless system (e.g., a power amplifier in a transmission path that drives signals to an antenna).

[0033] In some ET applications, the bandwidth of the envelope signal may be considerably higher than the bandwidth of the signal being processed. For example, a power amplifier supply voltage (VDD_ET) may be modulated at envelope frequencies that can extend up to 5-10 times the bandwidth of a signal being transmitted. In the

long term evolution wireless protocol (LTE) at 20 MHz, for instance, the bandwidth of the power supply may extend up to 200MHz.

[0034] The combination of the bias resistors and the gate capacitance of prior art bias circuits as shown in Fig. 1 produce a low pass frequency response. For common values of gate capacitance, resistors would need to be very small (in the few hundred ohms range) to achieve the desired bandwidth resulting in a very significant power amplifier efficiency (PAE) degradation (around 3-5% for typical Universal Mobile Telecommunications System (UMTS) maximum power conditions).

[0035] Fig. 2A illustrates an example wideband bias circuit according to one embodiment. In this example, a circuit 210 may receive an input signal (IN) and produce an output signal (OUT). Output signal (OUT) may be an RF single coupled to an antenna (not shown) for transmission over the airwaves, for example. Circuit 210 may include one or more internal nodes that are biased to particular values. In this example, circuit 210 may receive a power supply voltage VDD_ET that may vary over time from a modulated power supply 230. For example, in some applications a preprocessing block 240 may receive a signal to be transmitted, S, and produce input signal IN and modulation control signal Se to control envelop tracking, for example. For instance, circuit 210 may perform envelope tracking (ET) using a time varying power supply VDD_ET. Features and advantages of the present disclosure include a wideband bias circuit that may generate a bias for a circuit node that varies with VDD. The output OUT may be isolated from the power supply signal using an inductor L1 220, for example, which may also isolate the bias circuit from the output signal. The circuit node may provide a bias voltage to a circuit in the signal path of the input signal, and accordingly may be biased using the time varying power supply voltage to reduce power consumption, for example. In this example, a capacitor (C1) 203 is added in parallel with the top resistor (R1) 201 of the resistor ladder to perform a zero-pole cancellation with the existing pole established by the bottom resistor ladder resistor (R2) 202 and a capacitance (C2) 204 resulting in a significant bandwidth extension. Capacitance C2 204 may be the total capacitance at the transistor bias node, for example, and may include intrinsic device capacitance, any further capacitance added to the node (e.g., MIM or MOS capacitances) as well as parasitic capacitances. The addition of capacitor C1 allows use of significantly larger values of resistors R1 and R2,

which may result in a higher PAE, for example. C1 may be added to the bias circuit, and by setting the values of the resistors and capacitors as follows, the following transfer function may be achieved between VDD_ET and the bias node:

Vbias/Vdd_et = R2/(R1+R2); where jwRC for R1C1 and R2C2 cancel.

Accordingly, a time varying power supply voltage (e.g., an envelope signal) may be coupled to a bias node of a circuit to bias the node without unduly eliminating high frequencies from the power supply signal, for example. In one embodiment, one or more of the capacitances or resistances may be programmable. Adding programming and tuning may allow independent control of the circuit bandwidth and bias voltage, for example.

[0036] Fig. 2B illustrates an example wideband bias circuit according to another embodiment. In this example, a resistor (R3) 205 is configured between terminals of R1, R2, and C1 and the bias node including parasitic node capacitance C2. This example configuration may reduce loading at particular frequencies (e.g., RF frequencies), but may limit the high frequency bandwidth of the circuit. The following transfer function may be achieved between VDD_ET and the bias node using the configuration shown in Fig. 2B:

Vbias/Vdd_et = R2/(R1+R2(1+jwC2R3)); where R1C1=R2C2 and R2>>R3

[0037] Fig. 3A illustrates an example wideband bias circuit in an amplifier circuit according to one embodiment. This example illustrates the application of a wideband bias circuit to generated a bias voltage on the gate of a cascode transistor 311 in an amplifier circuit. In this example, an input signal (IN) is received on the gate of NMOS transistor 312. Transistor 312 has a drain coupled to the source of transistor 311. A drain of transistor 311 is coupled to a time varying power supply voltage VDD_ET through an inductor (L1) 310. An output signal (OUT) is produced on the drain of transistor 311 and a terminal of inductor L1. VDD_ET may implement envelope tracking, for example. The modulated power supply voltage is converted to an appropriate bias voltage at the gate of transistor 311 by wideband bias circuit including resistor (R1) 301, resistor (R2) 302, capacitor (C1) 303, and gate capacitance (C2) 304. Inductor 310 may isolate the output at the drain of transistor 311 from the power supply signal and isolate the bias circuit from the output signal, for example. Fig. 3B illustrates

frequency response of the example wideband bias circuit in Fig. 3A. Response 350 illustrates that the response without capacitor C1 drops at high frequencies. Responses 351-355 illustrate that the responses for different values of C1 stay approximately flat at higher frequencies and do not drop off.

[0038] Fig. 4 illustrates another example of wideband bias circuits according to another embodiment. This example illustrates a driver amplifier and a power amplifier including wideband bias circuits according to one embodiment. The driver amplifier includes NMOS transistors 410-412 arranged in a cascode configuration and coupled to a power supply through inductor L1 413. An input signal (IN1) is received on the gate of transistor 410 and a time varying power supply voltage, VDD-ET, corresponding to the input signal is received at the power supply terminal. A first wideband bias circuit comprising resistors 401-402 and capacitors 403-404 generates a bias voltage on the gate of transistor 411, where capacitance 404 includes a gate capacitance of transistor 411 (e.g., device capacitance, additional added capacitance, and parasitic capacitance). A second wideband bias circuit comprising resistors 405-406 and capacitors 407-408 generates a bias voltage on the gate of transistor 412, where capacitance 408 also includes to a gate capacitance of transistor 412. The output signal of the driver circuit (OUT1) is from a node between L1 and the drain of transistor 412. OUT1 is provided to an input of the power amplifier through a matching network 490, for example.

[0039] Similarly, the power amplifier includes NMOS transistors 430-432 arranged in a cascode configuration and coupled to a power supply through inductor L2 433. An input signal (IN2) is received on the gate of transistor 430 from matching network 490 and a time varying power supply voltage, VDD-ET, corresponding to the input signal is received at the power supply terminal. A third wideband bias circuit comprising resistors 421-422 and capacitors 423-424 generates a bias voltage on the gate of transistor 431, where capacitance 424 includes to a gate capacitance of transistor 431 (e.g., device capacitance, additional added capacitance, and parasitic capacitance). A fourth wideband bias circuit comprising resistors 425-426 and capacitors 427-428 generates a bias voltage on the gate of transistor 432, where capacitance 428 also includes to a gate capacitance of transistor 432. The output signal of the power amplifier is from a node between L2 and the drain of transistor 432. The output signal is provided to an antenna, for example, through a matching network 491 (OUT2).

[0040] Fig. 5 illustrates another example of wideband bias circuits according to another embodiment. This example is the same as shown in Fig. 4, except each wideband bias circuit includes a resistor between the gate capacitance of each cascode transistor and the other elements of the wideband bias circuit.

[0041] Fig. 6 illustrates an example spectrum of an envelope and input signal according to one embodiment. This example illustrates that the frequency range of the time varying power supply voltage may be greater than the frequency range of the input signal being amplified, for example. The example shown in Fig. 6 illustrates an LTE signal and an LTE envelope. Fig. 7A illustrates an example signal according to one embodiment. Fig. 7A shows both the in-phase and quadrature components of an input signal. Fig. 7B illustrates an example envelope according to one embodiment. Fig. 7B shows a signal envelope for the input signal in Fig. 7A.

[0042] The above description illustrates various embodiments of the present disclosure along with examples of how aspects of the particular embodiments may be implemented. For example, while the above examples are described in terms of NMOS transistors, other transistor types could also be used. The above examples should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the particular embodiments as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations and equivalents may be employed without departing from the scope of the present disclosure as defined by the claims.

WHAT IS CLAIMED IS:

CLAIMS

1. An amplifier circuit comprising:

a first transistor having a control terminal, a first terminal, and a second terminal, the control terminal configured to receive an input signal;

a cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the second terminal of the cascode transistor is coupled to the first terminal of the first transistor;

an inductor having a first terminal coupled to the first terminal of the cascode transistor and a second terminal coupled to a modulated power supply terminal;

a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a first node;

a second resistor having a first terminal coupled to the first node and a second terminal coupled to a reference voltage; and

a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the first node,

wherein the first node is coupled to the control terminal of the cascode transistor, and wherein the modulated power supply terminal produces a time varying power supply signal corresponding to the input signal.

2. The circuit of claim 1 wherein the control terminal of the cascode transistor comprises a capacitance.

3. The circuit of claim 2 wherein the first resistor, the second resistor, and the capacitor are configured to couple the time varying power supply signal to the control terminal of the cascode device across a first range of frequencies greater than a second range of frequencies of the input signal.

4. The circuit of claim 1 wherein a first product of a resistance of the first resistor and a capacitance of the capacitor is approximately equal to a second product of a resistance of the second resistor and a capacitance at the control terminal of the cascode transistor.

5. The circuit of claim 1 wherein the cascode transistor is a first cascode transistor, the amplifier circuit further comprising:

a second cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the first terminal of the second cascode transistor is coupled to the second terminal of the first cascode transistor, and wherein the second terminal of the second cascode transistor is coupled to the first terminal of the first transistor;

a third resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a second node;

a fourth resistor having a first terminal coupled to the second node and a second terminal coupled to the reference voltage; and

a second capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the second node;

wherein the second node is coupled to the control terminal of the second cascode transistor.

6. The circuit of claim 1 further comprising a third resistor coupled between the first node and the control terminal of the cascode transistor.

7. The circuit of claim 1 wherein the inductor isolates the first terminal of the cascode transistor from the time varying power supply signal on the second terminal of the inductor.

8. The circuit of claim 1 wherein a bandwidth of the input signal is less than a bandwidth of the time varying power supply signal.

9. The circuit of claim 1 wherein at least one of the first resistor, the second resistor, and the capacitor are programmable.

10. A method of amplifying a signal comprising:

receiving an input signal on a control terminal of a first transistor, the first transistor having a control terminal, a first terminal, and a second terminal;

coupling the input signal through the first transistor and a cascode transistor to produce an output signal on a second terminal of the cascode transistor, the cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the second terminal of the cascode transistor is coupled to the first terminal of the first transistor;

receiving a time varying power supply voltage from a modulated power supply on a terminal of a bias circuit, the bias circuit comprising a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a first node, a second resistor having a first terminal coupled to the first node and a second terminal coupled to a reference voltage, and a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the first node, wherein the first node is coupled to the control terminal of the cascode transistor;

coupling the time varying power supply voltage to the control terminal of the cascode transistor; and

generating an impedance in an inductor having a first terminal coupled to the first terminal of the cascode transistor and a second terminal coupled to a modulated power supply terminal to isolate the first terminal of the cascode transistor from the time varying power supply voltage.

11. The method of claim 10 wherein the control terminal of the cascode transistor comprises a capacitance.

12. The method of claim 11 wherein the first resistor, the second resistor, and the capacitor are configured to couple the time varying power supply signal to the control terminal of the cascode device across a first range of frequencies greater than a second range of frequencies of the input signal.

13. The method of claim 10 wherein a first product of a resistance of the first resistor and a capacitance of the capacitor is approximately equal to a second product of a resistance of the second resistor and a capacitance at the control terminal of the cascode transistor.

14. The method of claim 10 wherein the bias circuit is a first bias circuit and the cascode transistor is a first cascode transistor, the method further comprising:

receiving the time varying power supply voltage from the modulated power supply on a terminal of a second bias circuit, the second bias circuit comprising a third resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a second node, a fourth resistor having a first terminal

coupled to the second node and a second terminal coupled to the reference voltage, and a second capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the second node, wherein the second node is coupled to the control terminal of the second cascode transistor; and

coupling the time varying power supply voltage to the control terminal of the second cascode transistor.

15. The method of claim 10 further comprising coupling the time varying power supply voltage through a third resistor coupled between the first node and the control terminal of the cascode transistor.

16. The method of claim 10 wherein a bandwidth of the input signal is less than a bandwidth of the time varying power supply signal.

17. The method of claim 10 wherein at least one of the first resistor, the second resistor, and the capacitor are programmable.

18. An amplifier circuit comprising:

a first transistor having a control terminal, a first terminal, and a second terminal, the control terminal configured to receive an input signal;

a cascode transistor having a control terminal, a first terminal, and a second terminal, wherein the second terminal is coupled to the first terminal of the first transistor;

an inductor having a first terminal coupled to the first terminal of the cascode transistor and a second terminal coupled to receive a modulated power supply terminal; and

means for coupling a maximum frequency of a time varying power supply signal corresponding to the input signal from the modulated power supply terminal to the control terminal of the cascode transistor to bias the cascode transistor.

19. The circuit of claim 18, said means for coupling a maximum frequency of the time varying power supply signal comprising:

a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a control terminal of the cascode transistor;

a second resistor having a first terminal coupled to the control terminal of the cascode transistor and a second terminal coupled to a reference voltage;

a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the control terminal of the cascode transistor; and

a capacitance coupled to the control terminal of the cascode transistor.

20. The circuit of claim 18, said means for coupling a maximum frequency of the time varying power supply signal comprising:

a first resistor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to a first node;

a second resistor having a first terminal coupled to the first node and a second terminal coupled to a reference voltage;

a capacitor having a first terminal coupled to the modulated power supply terminal and a second terminal coupled to the first node;

a third resistor coupled between the first node and control terminal of the cascode transistor; and

a capacitance coupled to the control terminal of the cascode transistor.

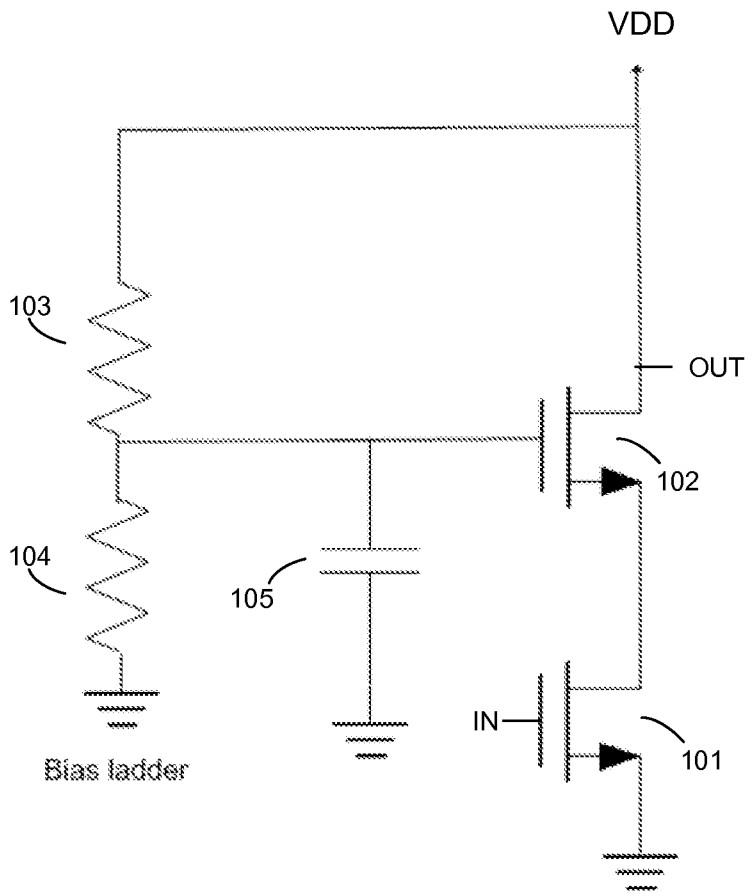
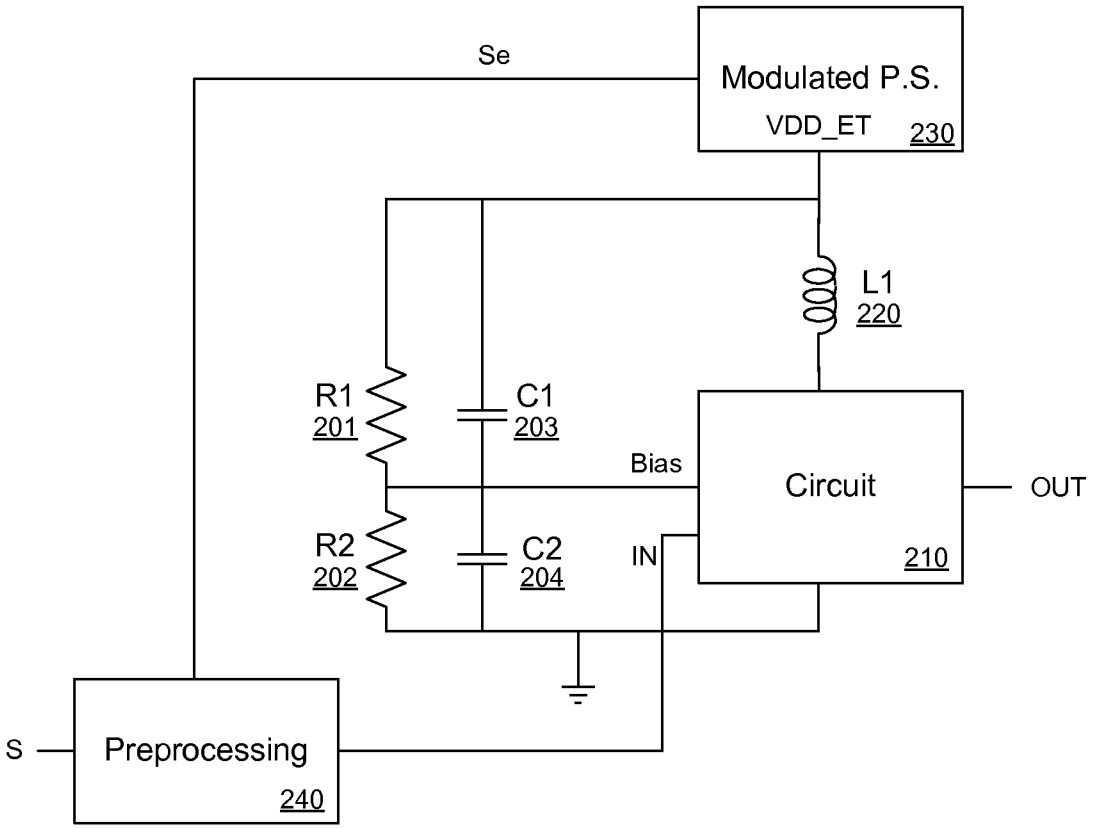


Fig. 1
(Prior Art)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201
C1
203
Bias
Circuit
OUT
R2
202
C2
204
IN
210
S
Preprocessing
240

Fig. 2A

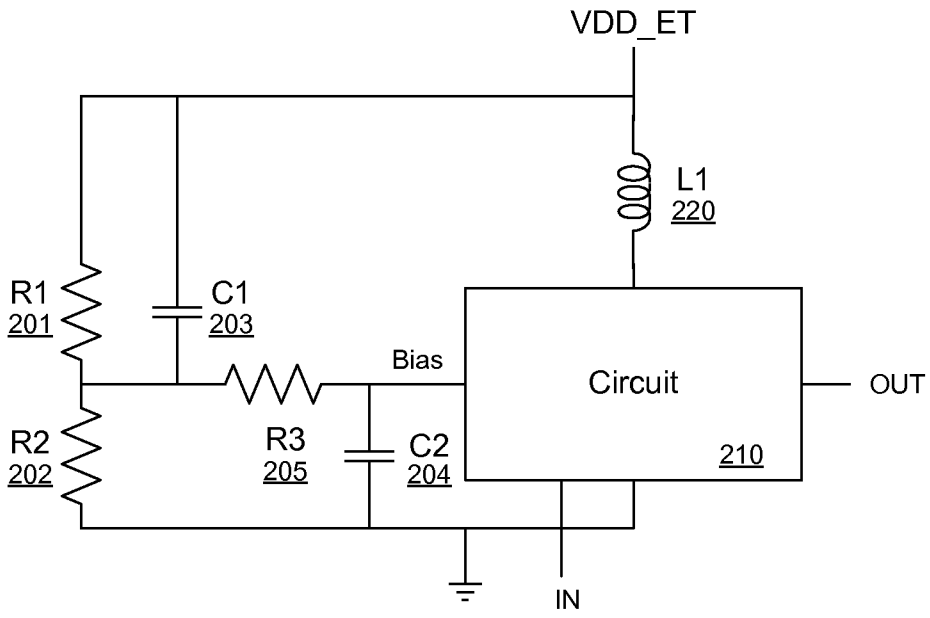
VDD_ET
L1
220
R1
201
C1
203
Bias
Circuit
OUT
R2
202
R3
205
C2
204
210
IN

Fig. 2B

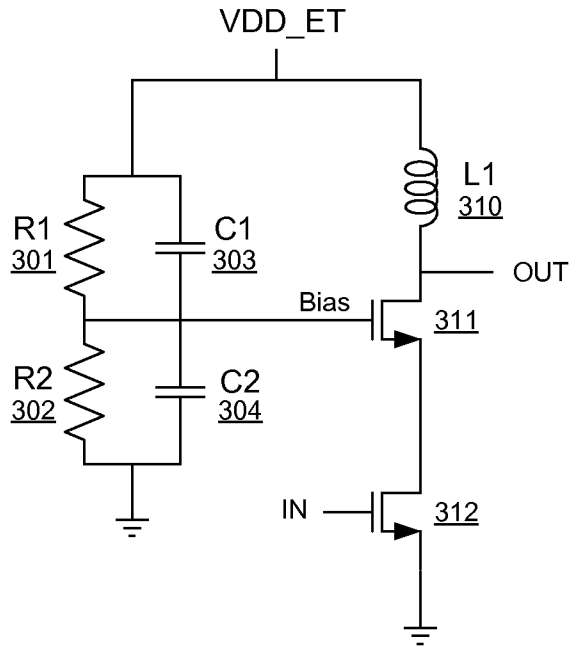
VDD_ET
L1
310
R1
301
C1
303
OUT
Bias
311
R2
302
C2
304
IN
312

Fig. 3A

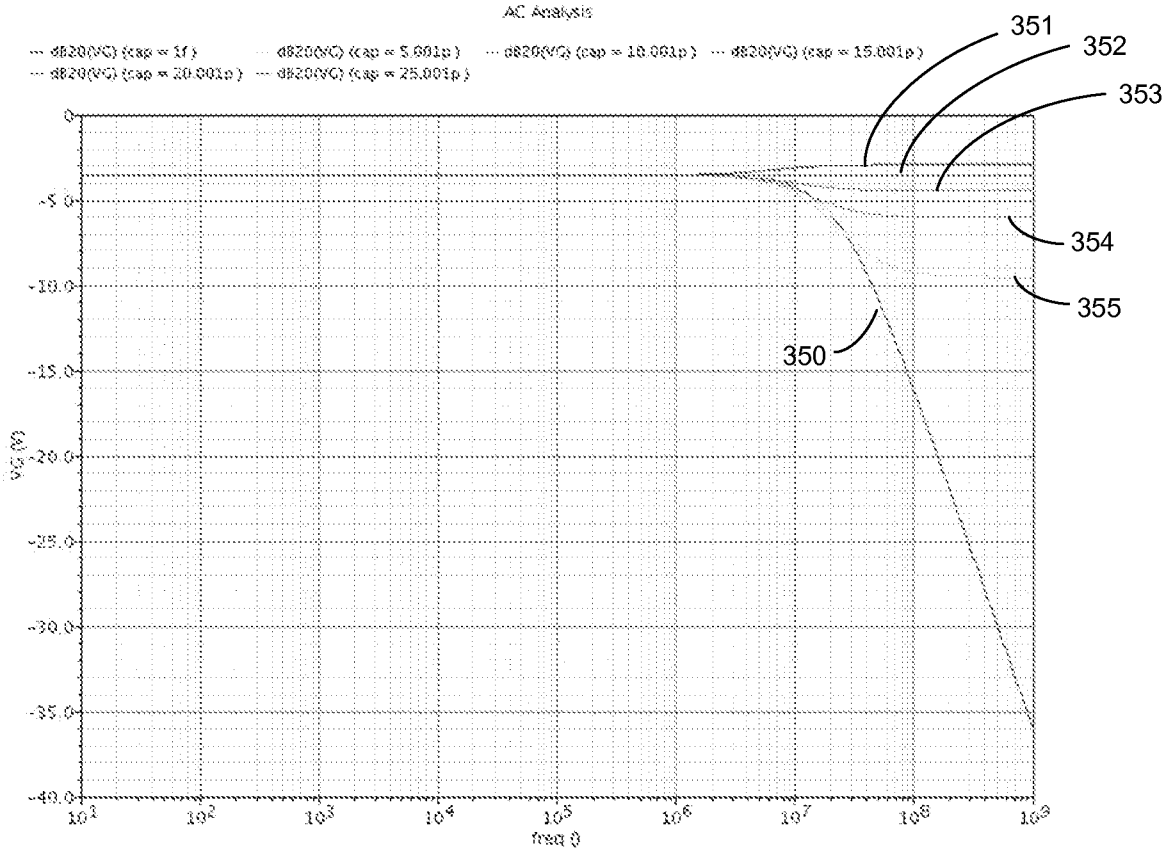
AC Analysis
351
352
353
354
355
350
freq ()

Fig. 3B

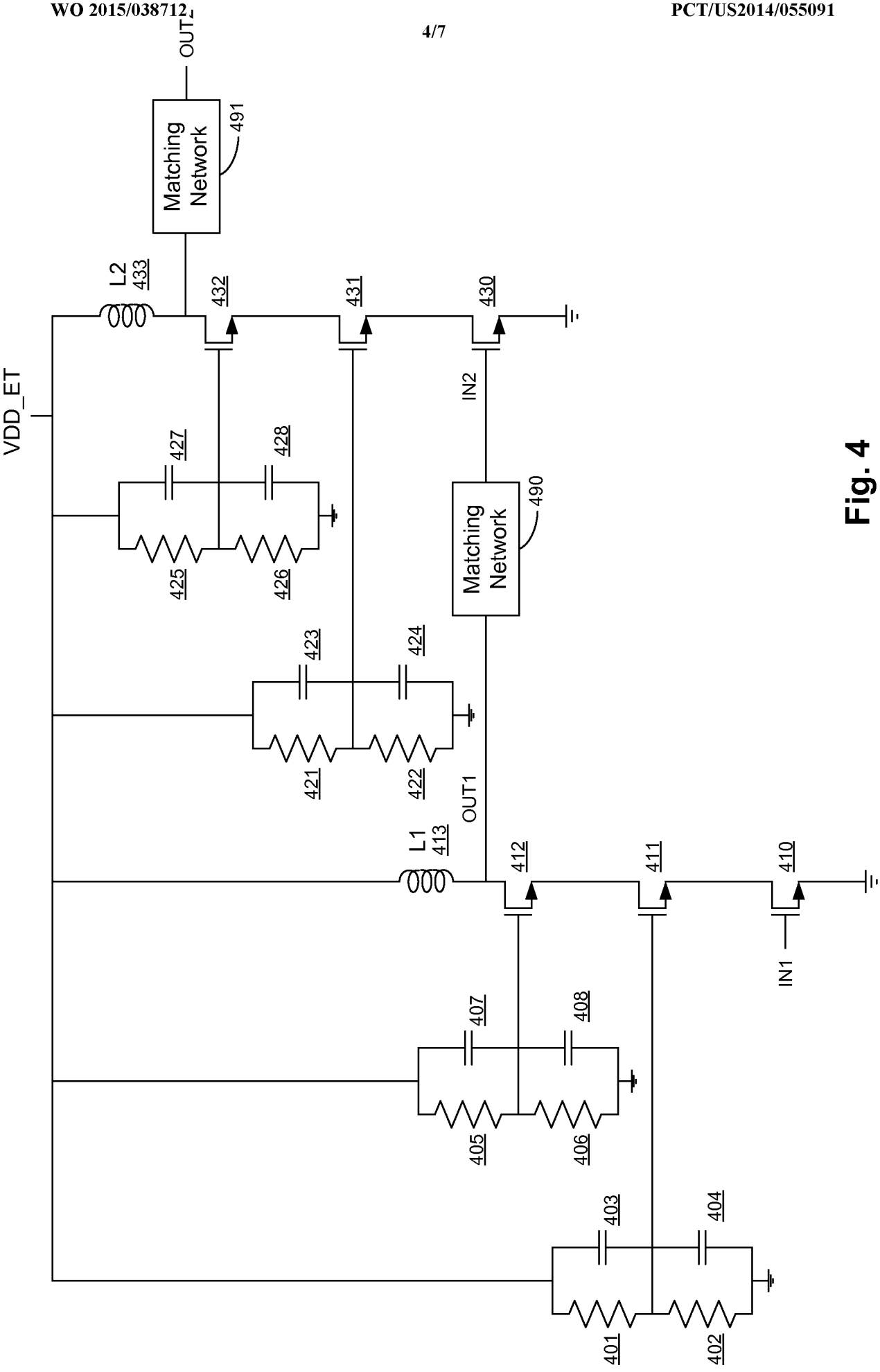
OUT
Matching Network
491
L2
433
432
431
430
VDD_ET
IN2
427
428
425
426
Matching Network
490
423
424
421
422
OUT1
L1
413
412
411
410
IN1
407
408
405
406
403
404
401
402

Fig. 4

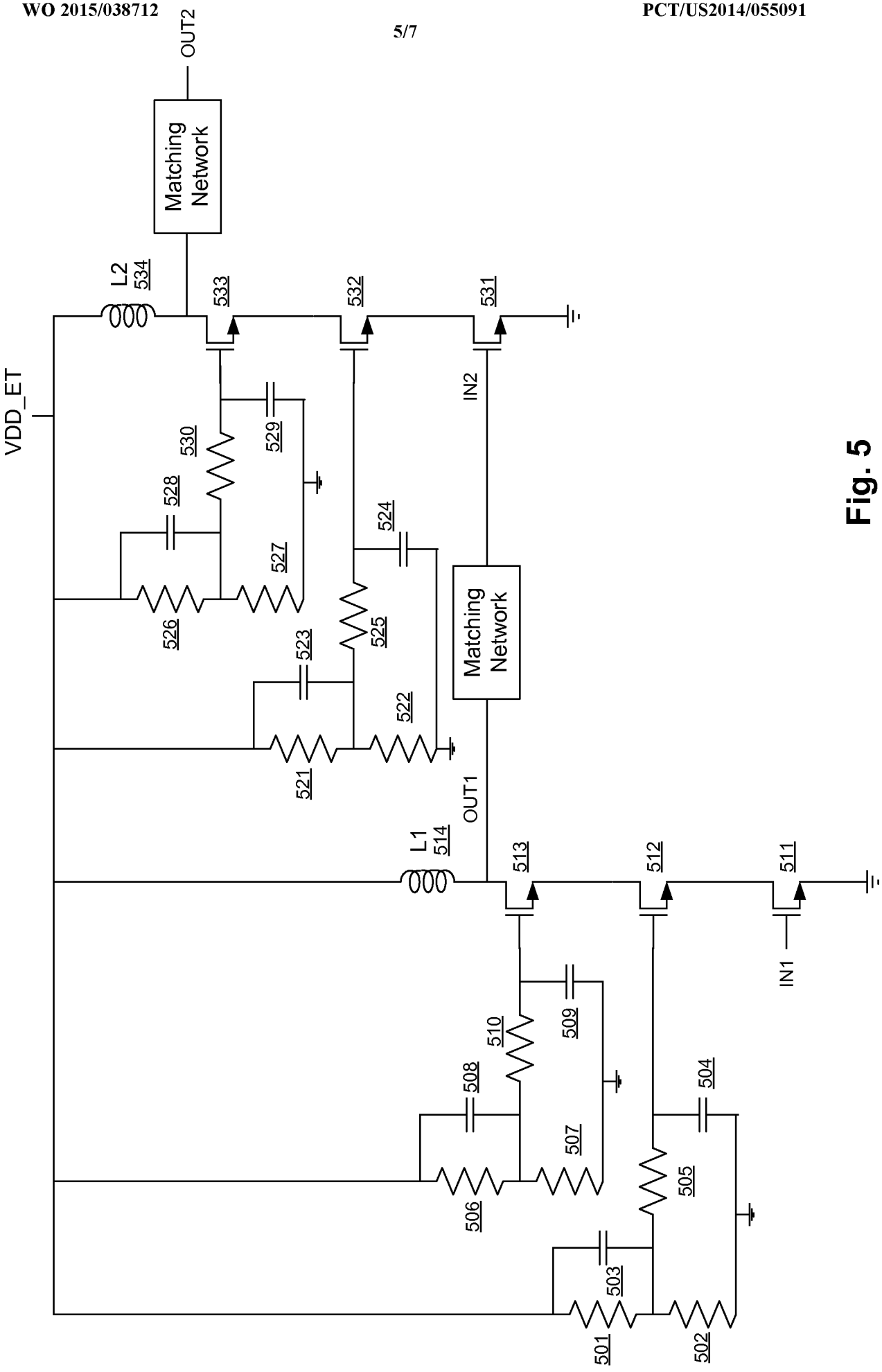
OUT2
Matching Network
L2
534
533
532
531
VDD_ET
IN2
530
529
528
527
524
526
525
523
522
Matching Network
521
OUT1
L1
514
513
512
511
IN1
510
509
508
507
504
506
505
503
501
502

Fig. 5

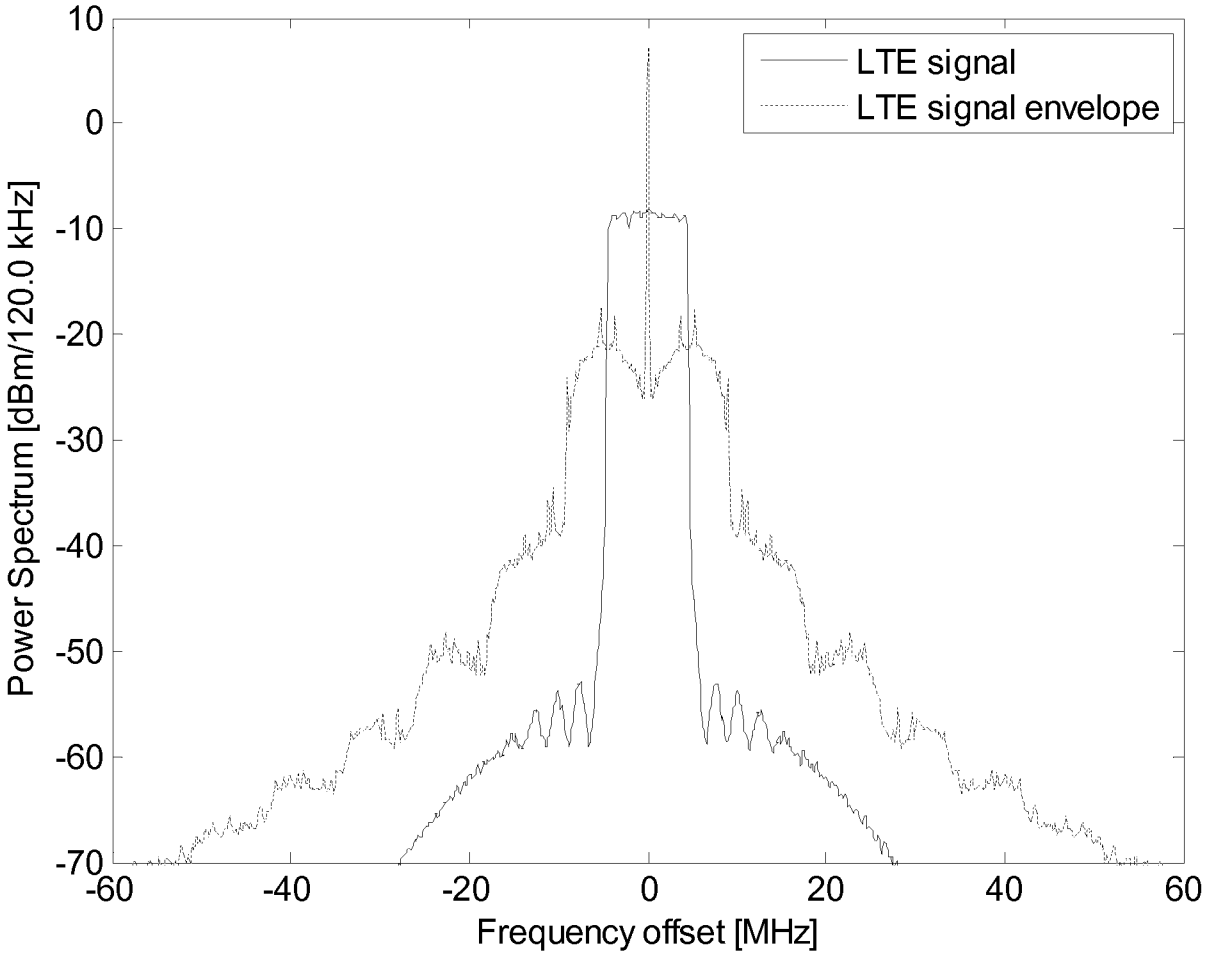
LTE signal
LTE signal envelope
Power Spectrum [dBm/120.0 kHz]
Frequency offset [MHz]
10
0
-10
-20
-30
-40
-50
-60
-70
-60
-40
-20
0
20
40
60

Fig. 6

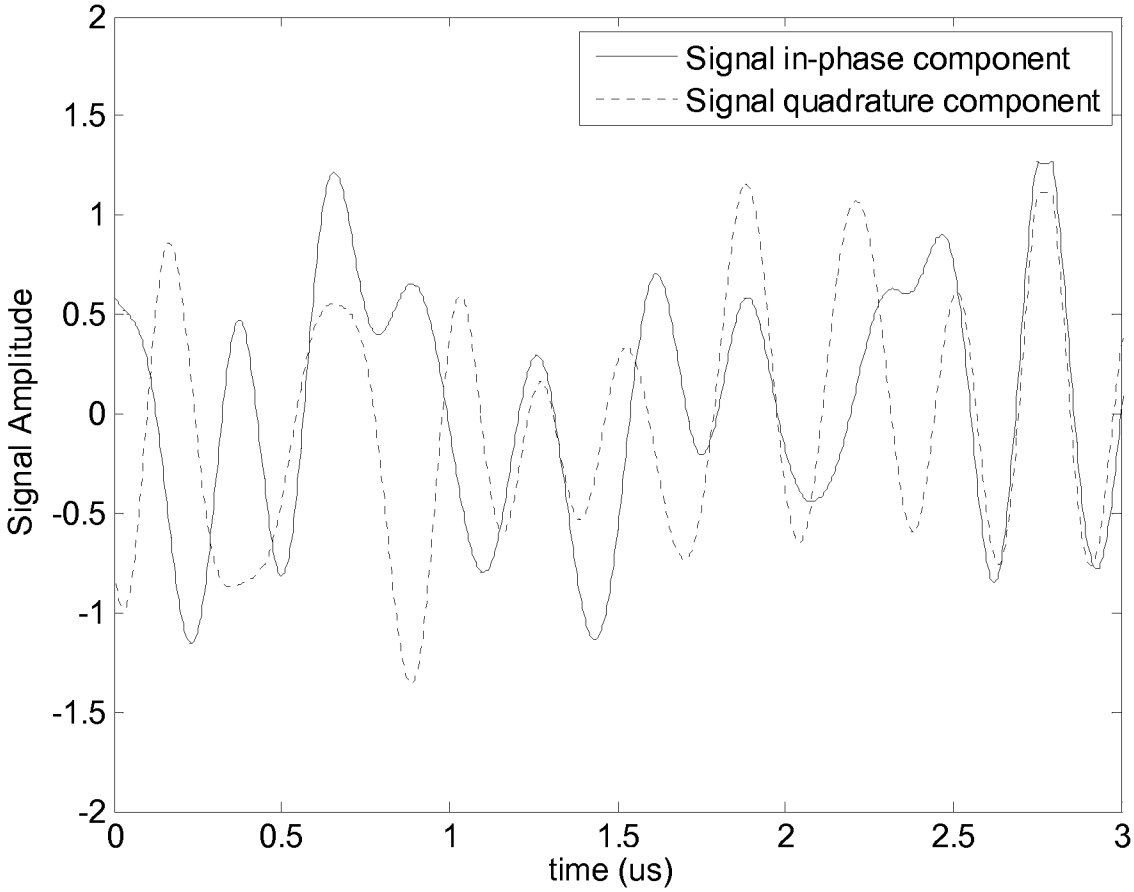
Signal in-phase component
Signal quadrature component
Signal Amplitude
time (us)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
0
0.5
1
1.5
2
2.5
3

Fig. 7A

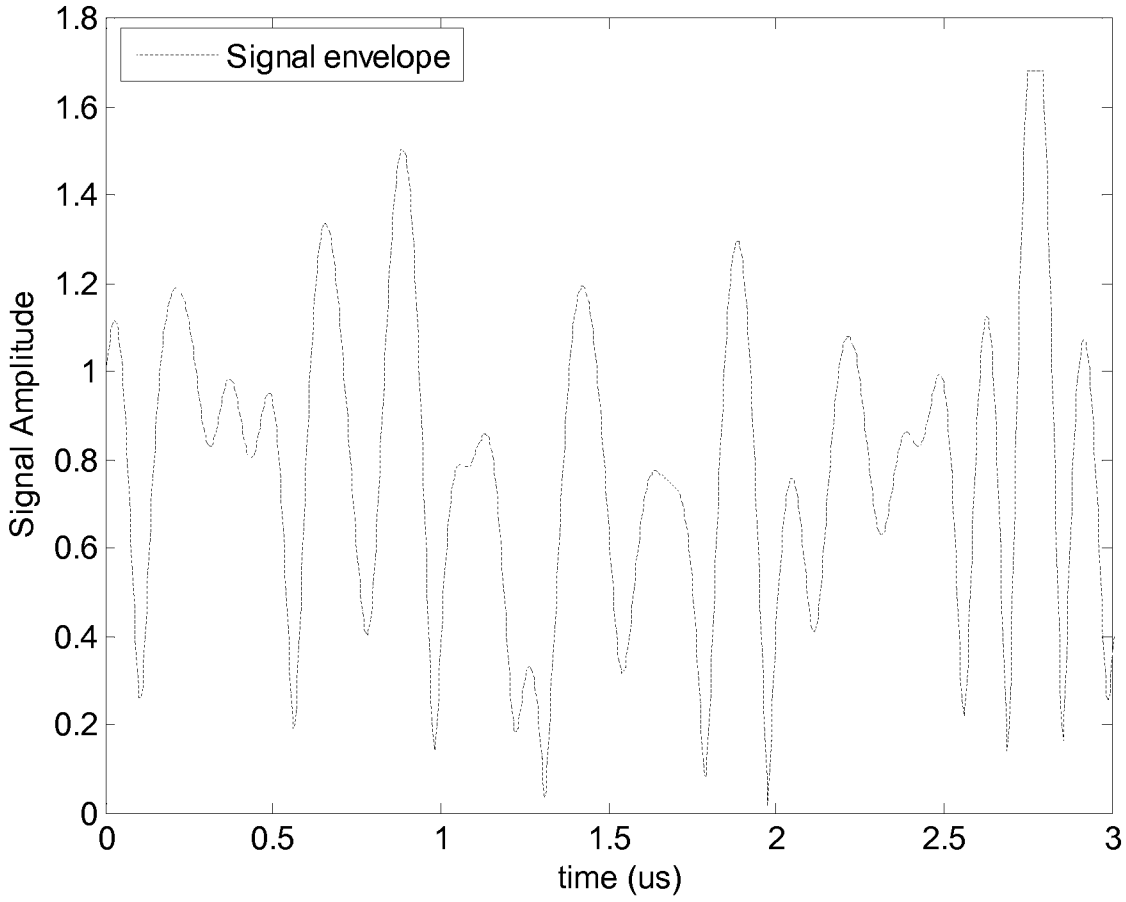
Signal envelope
Signal Amplitude
time (us)
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
0.5
1
1.5
2
2.5
3

Fig. 7B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/055091

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/02 H03F1/22 H03F3/193 H03F1/48
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2009/060095 A1 (NXP BV [NL]; HEIJDEN MARK PIETER [NL]; LEENAERTS DOMINICUS [NL]; APOST) 14 May 2009 (2009-05-14) page 3, line 18 - page 7, line 20; figures 2,3,4	1-20
A	US 4 394 590 A (HONDA AKIRA [JP]) 19 July 1983 (1983-07-19) column 1, line 47 - column 8, line 11; figures 2,3,6,7	1-20

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2014	24/11/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Fedi, Giulio

2

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/055091

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JOOSEUNG KIM ET AL: "Envelope-Tracking Two-Stage Power Amplifier With Dual-Mode Supply Modulator for LTE Applications", IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 61, no. 1, 17 January 2013 (2013-01-17), pages 543-552, XP011488011, ISSN: 0018-9480, DOI: 10.1109/TMTT.2012.2225532 page 543, right-hand column, line 3 - page 548, right-hand column, line 7; figures 7,12	1-20
A	US 2011/181364 A1 (AHADIAN JOSEPH F [US] ET AL) 28 July 2011 (2011-07-28) paragraphs [0026] - [0047]; figures 2,3,4,5	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/055091

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2009060095 A1	14-05-2009	EP 2220762 A1	25-08-2010
		US 2011012682 A1	20-01-2011
		WO 2009060095 A1	14-05-2009
US 4394590 A	19-07-1983	DE 2967520 D1	31-10-1985
		EP 0048758 A1	07-04-1982
		JP S6151810 B1	11-11-1986
		US 4394590 A	19-07-1983
		WO 8101924 A1	09-07-1981
US 2011181364 A1	28-07-2011	NONE	