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(54) Title: RF SWITCH STRUCTURE DESIGN IN STACKED RFSOI WAFERS FOR REDUCED DIE SIZE

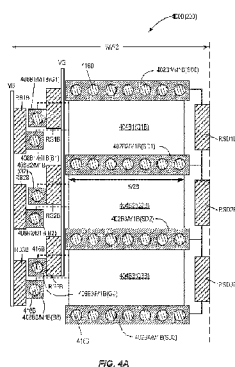


FIG. 4A

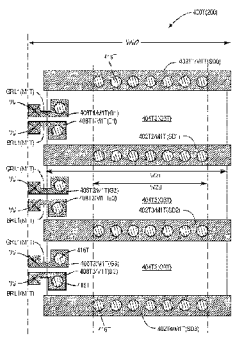


FIG. 4B

(57) Abstract: The present disclosure relates to implementation of a radio frequency (RF) switch structure including a bottom wafer and a top wafer over the bottom wafer. The bottom wafer includes a bottom active switch region providing a bottom field-effect transistor (FET), bias resistors surrounding the bottom active switch region, and bottom hybrid bond (HB) vias connected to the bottom FET and exposed on top of the bottom wafer. The top wafer includes a top active switch region providing a top FET, and top HB vias connected to the top FET and exposed on a bottom of the top wafer. Each top HB via is directly coupled to a corresponding bottom HB via, so that the top FET is electrically parallel to the bottom FET. The top active switch region is larger than the bottom active switch region, and at least partially covers areas of the bias resistors within the bottom wafer.



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***RF SWITCH STRUCTURE DESIGN IN STACKED RFSOI WAFERS FOR
REDUCED DIE SIZE***

Related Applications

5 **[0001]** This application claims the benefit of U.S. provisional patent application serial number 63/610,139, filed on December 14, 2023, and U.S. provisional patent application serial number 63/663,787, filed on June 25, 2024, the disclosures of which are hereby incorporated herein by reference in their entireties.

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Field of the Disclosure

[0002] The present disclosure relates to an implementation of a radio frequency (RF) switch structure, and in particular to an implementation of an RF switch structure with a stacked configuration to achieve a reduced die size and enhanced RF performance.

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Background

[0003] There is continuous demand for improvement in device size and performance for radio frequency (RF) products. Smaller die size allows for smaller devices, faster processing speeds, and lower power consumption of RF products. Previously, RF silicon-on-insulator (RFSOI) technology has enabled die size and performance improvement by using more advanced complementary metal oxide semiconductor factories, processes, and tools.

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[0004] However, reducing the die size of RF products causes several challenges. As the size of the die is reduced, parasitic capacitance and resistance become more prominent because the components are now closer together. This can negatively affect the signal integrity, frequency response, and noise of the RF products. Reduced die size also suffers from less effective thermal management because there is less area for the heat generated by the RF components to be dissipated. Reduced die size requires smaller or tighter tolerances, which require more sophisticated control of the manufacturing

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processes. These and other impacts of reducing die size alone thus typically increase the complexity and cost of RF products.

[0005] An alternative solution to providing more compact and higher performance RF circuits, especially for RF switches, is to utilize a stacked configuration. However, electronic components in a top portion of the stacked
5 configuration will have a larger vertical distance to a silicon handle wafer, such that the thermal performance might be downgraded, and in consequence the reliability of the die might be affected.

[0006] Accordingly, there remains a need for improved implementations of RF
10 switch structure designs, which utilize the stacked configuration to reduce the die size and ensure reliable RF operation. In addition, there is also a need to effectively utilize both top and bottom areas in the stacked configuration.

Summary

[0007] The present disclosure relates to an implementation of a radio
15 frequency (RF) switch structure with a stacked configuration to achieve a reduced die size and enhanced RF performance. The disclosed RF switch structure includes a bottom wafer and a top wafer stacked over the bottom wafer. The bottom wafer includes a first bottom active switch region configured to
20 provide a first bottom field-effect transistor (FET), a number of first bias resistors surrounding the first bottom active switch region, and a number of bottom hybrid bond (HB) vias. Certain ones of the bottom HB vias are electrically connected to the first bottom FET and exposed at a top surface of the bottom wafer. The top wafer includes a first top active switch region configured to provide a first top FET
25 and a number of top HB vias. Certain ones of the top HB vias are electrically connected to the first top FET, exposed at a bottom surface of the top wafer, and aligned with and directly connected to the certain ones of the bottom HB vias, respectively. As such, the first top FET and the first bottom FET are electrically parallel to each other. The first bias resistors are configured to provide direct
30 current (DC) voltage biasing to both the first top FET and the first bottom FET. The first top active switch region is formed over and larger than the first bottom

active switch region, and at least partially covers areas of the number of first bias resistors within the bottom wafer.

[0008] In one embodiment of the RF switch structure, the first bottom FET and the first top FET are multi-finger transistors.

5 **[0009]** In one embodiment of the RF switch structure, the first bottom FET and the first top FET are each a bilateral device, in which a source and a drain are interchangeable.

[0010] In one embodiment of the RF switch structure, the bottom wafer further includes a first bottom source/drain connection region, a second bottom
10 source/drain connection region, and a first bottom gate connection region, while the top wafer further includes a first top source/drain connection region, a second top source/drain connection region, and a first top gate connection region. Herein, the first bottom source/drain connection region is connected to a drain of the first bottom FET, the second bottom source/drain connection region is
15 connected to a source of the first bottom FET, and the first bottom gate connection region is connected to a gate of the first bottom FET. The first top source/drain connection region is connected to a drain of the first top FET, the second top source/drain connection region is connected to a source of the first top FET, and the first top gate connection region is connected to a gate of the
20 first top FET. One or more of the bottom HB vias are confined within and connected to the first bottom source/drain connection region, the second bottom source/drain connection region, and the first bottom gate connection region, respectively. One or more of the top HB vias are confined within and connected to the first top source/drain connection region, the second top source/drain
25 connection region, and the first top gate connection region, respectively.

[0011] In one embodiment of the RF switch structure, the bottom wafer further includes a first bottom body connection region, which is connected to a body of the first bottom FET, while the top wafer further includes a first top body
connection region, which is connected to a body of the first top FET. One or more
30 of the bottom HB vias are confined within and connected to the first bottom body

connection region, and one or more of the top HB vias are confined within and connected to the first top body connection.

[0012] In one embodiment of the RF switch structure, the first bottom source/drain connection region, the second bottom source/drain connection region, the first bottom gate connection region, and the first bottom body connection region are formed from a same first bottom metal layer, which is at a higher vertical level than the first bottom active switch region. The first top source/drain connection region, the second top source/drain connection region, the first top gate connection region, and the first top body connection region are formed from a same first top metal layer, which is at a lower vertical level than the first top active switch region.

[0013] In one embodiment of the RF switch structure, the first bottom active switch region is located between the first bottom source/drain connection region and the second bottom source/drain connection region in the horizontal plane.

The first top active switch region is located between the first top source/drain connection region and the second top source/drain connection region in the horizontal plane. The first top gate connection region and the first top body connection region are below and confined in the first top active switch region.

[0014] In one embodiment of the RF switch structure, the top wafer further includes a first gate route line, a first body route line, a first gate vertical via, and a first body vertical via. The first gate route line is formed from the first top metal layer and provides an electrical connection from the first top gate connection region towards a location horizontally outside of the first top active switch region. The first body route line is formed from the first top metal layer and provides an electrical connection from the first top body connection region towards a location horizontally outside of the first top active switch region. The first gate vertical via and the first body vertical via are horizontally outside the first top active switch region. The first gate vertical via extends vertically from the first gate route line towards a metal layer over the first top metal layer, while the first body vertical via extends vertically from the first body route line towards the metal layer over the first top metal layer. Herein, the first top gate connection region is connected to

the gate of the first top FET at least through the first gate route line and the first gate vertical via, and the first top body connection region is connected to the body of the first top FET at least through the first body route line and the first body vertical via.

5 **[0015]** In one embodiment of the RF switch structure, the first bottom gate connection region and the first bottom body connection region are horizontally outside the first bottom active switch region.

10 **[0016]** In one embodiment of the RF switch structure, a width of each of the first top source/drain connection region and the second top source/drain connection region is greater than a width of each of the first bottom source/drain connection region and the second bottom source/drain connection region.

15 **[0017]** In one embodiment of the RF switch structure, the first bottom source/drain connection region and the second bottom source/drain connection region have a same first connection width, and the first top source/drain connection region and the second top source/drain connection region have a same second connection width. The second connection width is greater than the first connection width.

20 **[0018]** In one embodiment of the RF switch structure, the first bias resistors include at least a first gate bias resistor and a first source-drain bias resistor. The first gate bias resistor is electrically coupled between the gate of the first bottom FET and a gate terminal providing a gate voltage signal, and the first source-drain bias resistor is electrically coupled between the drain of the first bottom FET and the source of the first bottom FET.

25 **[0019]** In one embodiment of the RF switch structure, the first bias resistors further include a first body bias resistor, which is electrically coupled between the body of the first bottom FET and a body terminal providing a body voltage signal.

30 **[0020]** In one embodiment of the RF switch structure, the first bias resistors are placed around the bottom active switch region along a device width direction. The first top active switch region is over the first bottom active switch region and extends in the device width direction to at least partially cover the areas of the

first bias resistors within the bottom wafer, such that the first top active switch region has a larger device width than the first bottom active switch region.

[0021] In one embodiment of the RF switch structure, the bottom wafer includes a number of bottom active switch regions, in which the first bottom

5 active switch region is included. The top wafer includes a number of top active switch regions, in which the first top active switch region is included. The bottom active switch regions are configured to provide a number of bottom FETs, respectively, and the top active switch regions are configured to provide a number of top FETs, respectively. The bottom FETs are electrically coupled in series within the bottom wafer, and the top FETs are electrically coupled in series within the top wafer. Each bottom HB via is exposed at the top surface of the bottom wafer, and electrically connected to a corresponding one of the bottom FETs. Each top HB via is exposed at the bottom surface of the top wafer, electrically connected to a corresponding one of the top FETs, and aligned with
10 and directly connected to a corresponding one of the bottom HB vias, such that each of the bottom FETs is electrically parallel to a corresponding one of the top FETs.

[0022] In one embodiment of the RF switch structure, the bottom HB vias and the top HB vias have the same number.

20 **[0023]** In one embodiment of the RF switch structure, the bottom wafer includes a number of bias resistors, in which the first bias resistors are included. Each bottom active switch region is surrounded by corresponding ones of the bias resistors in the horizontal plane. The bias resistors are configured to provide DC voltage biasing to each bottom FET and each top FET. Each top active
25 switch region is formed over and larger than a corresponding one of the bottom active switch regions, and at least partially covers areas of the corresponding ones of the bias resistors within the bottom wafer.

[0024] In one embodiment of the RF switch structure, the bottom wafer further includes a number of bottom source/drain connection regions and a number of
30 bottom gate connection regions. Each bottom source/drain connection region is connected to a drain or a source of a corresponding one of the bottom FETs, or

connected to a drain and a source of two adjacent ones of the bottom FETs.

Each bottom gate connection region is connected to a gate of the corresponding one of the bottom FETs. The top wafer further includes a number of top source/drain connection regions and a number of top gate connection regions.

- 5 Each top source/drain connection region is connected to a drain or a source of a corresponding one of the top FETs, or connected to a drain and a source of two adjacent ones of the top FETs. Each top gate connection region is connected to a gate of the corresponding one of the top FETs. One or more of the bottom HB vias are confined within and connected to each bottom source/drain connection
10 region and each bottom gate connection region, respectively. One or more of the top HB vias are confined within and connected to each top source/drain connection region and each top gate connection region, respectively.

[0025] In one embodiment of the RF switch structure, the bottom wafer further includes a number of bottom body connection regions, each of which is

- 15 connected to a body of the corresponding one of the bottom FETs. The top wafer further includes a number of top body connection regions, each of which is connected to a body of the corresponding one of the top FETs. One or more of the bottom HB vias are confined within and connected to each of the bottom body connection regions. One or more of the top HB vias are confined within and
20 connected to each of the top body connection regions.

[0026] In one embodiment of the RF switch structure, the bottom source/drain connection regions, the bottom gate connection regions, and the bottom body connection regions are formed from a same first bottom metal layer, which is at a higher vertical level than the bottom active switch regions. The top source/drain
25 connection regions, the top gate connection regions, and the top body connection regions are formed from a same first top metal layer, which is at a lower vertical level than the top active switch regions.

- [0027]** In one embodiment of the RF switch structure, each bottom active switch region is located between two of the bottom source/drain connection
30 regions in the horizontal plane. Each top active switch region is located between two of the top source/drain connection regions in the horizontal plane. Each top

gate connection region and each top body connection region are confined in a corresponding one of the top active switch regions.

[0028] In one embodiment of the RF switch structure, each bottom gate connection region and each bottom body connection region are horizontally
5 outside a corresponding one of the bottom active switch regions.

[0029] In one embodiment of the RF switch structure, the bias resistors are placed around the bottom active switch regions along a device width direction. Each top active switch region is over a corresponding one of the bottom active switch regions and extends in the device width direction to at least partially cover
10 the areas of the bias resistors within the bottom wafer, such that each top active switch region has a larger device width than the corresponding one of the bottom active switch regions.

[0030] According to one embodiment, a communication device includes receive circuitry, transmit circuitry, and antenna switching circuitry, which is
15 configured to transmit radio frequency signals between antennas and the receive circuitry and/or between the antennas and the transmit circuitry. Herein, at least the antenna switching circuitry includes an RF switch structure, which includes a bottom wafer and a top wafer stacked over the bottom wafer. The bottom wafer includes a first bottom active switch region configured to provide a first bottom
20 field-effect transistor (FET), a number of first bias resistors surrounding the first bottom active switch region, and a number of bottom hybrid bond (HB) vias. Certain ones of the bottom HB vias are electrically connected to the first bottom FET and exposed at a top surface of the bottom wafer. The top wafer includes a first top active switch region configured to provide a first top FET and a number
25 of top HB vias. Certain ones of the top HB vias are electrically connected to the first top FET, exposed at a bottom surface of the top wafer, and are aligned with and directly connected to the certain ones of the bottom HB vias, respectively. As such, the first top FET and the first bottom FET are electrically parallel to each other. The first bias resistors are configured to provide DC voltage biasing to both
30 the first top FET and the first bottom FET. The first top active switch region is

formed over and larger than the first bottom active switch region, and at least partially covers areas of the number of first bias resistors within the bottom wafer.

[0031] According to one embodiment, a method of implementing an RF switch structure starts with forming a bottom wafer that includes a first bottom active

5 switch region, a number of first bias resistors, and a number of bottom HB vias.

The first bottom active switch region is configured to provide a first bottom FET, which is surrounded by the first bias resistors in a horizontal plane. Each bottom HB via is electrically connected to the first bottom FET and exposed at a top surface of the bottom wafer. Next, a top wafer is formed, which includes a first

10 top active switch region and a number of top HB vias. The first top active switch region is configured to provide a first top FET, and each top HB via is electrically connected to the first top FET and exposed at a bottom surface of the top wafer.

The top wafer is then bonded to the bottom wafer. Herein, each top HB via exposed at the bottom surface of the top wafer is aligned with and directly

15 connected to a corresponding one of the bottom HB vias exposed at the top surface of the bottom wafer, such that the first top FET and the first bottom FET are electrically parallel to each other. The first bias resistors are configured to provide DC voltage biasing to both the first top FET and the first bottom FET. The first top active switch region is located over and larger than the first bottom active switch region, and at least partially covers areas of the first bias resistors within the bottom wafer.

[0032] In another aspect, any of the foregoing aspects individually or together, and/or various separate aspects and features as described herein, may be

combined for additional advantage. Any of the various features and elements as disclosed herein may be combined with one or more other disclosed features and elements unless indicated to the contrary herein.

[0033] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

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Brief Description of the Drawing Figures

[0034] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

5 **[0035]** Figures 1A and 1B illustrate schematics of a typical radio frequency (RF) switch structure with a stacked configuration.

[0036] Figures 2A and 2B illustrate schematics of an exemplary RF switch structure for better thermal performance.

10 **[0037]** Figures 3A-3D illustrate a typical implementation of the RF switch structure shown in Figures 2A and 2B.

[0038] Figures 4A-4D illustrate an exemplary implementation of the RF switch structure according to some embodiments of the present disclosure.

15 **[0039]** Figure 5 illustrates a flowchart of an exemplary implementation process of the RF switch structure according to some embodiments of the present disclosure.

[0040] Figure 6 illustrates a block diagram of an exemplary communication device that includes at least one RF switch structure with the exemplary implementation.

20 **[0041]** It will be understood that for clear illustrations, Figures 1A-6 may not be drawn to scale.

Detailed Description

25 **[0042]** The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the
30 accompanying claims.

[0043] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, 5 similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0044] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can 10 be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or 15 extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or 20 "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0045] Relative terms such as "below" or "above" or "upper" or "lower" or 25 "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0046] The terminology used herein is for the purpose of describing particular 30 embodiments only and is not intended to be limiting of the disclosure. As used

herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0047] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0048] Embodiments are described herein with reference to schematic illustrations of embodiments of the disclosure. As such, the actual dimensions of the layers and elements can be different, and variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are expected. For example, a region illustrated or described as square or rectangular can have rounded or curved features, and regions shown as straight lines may have some irregularity. Thus, the regions illustrated in the figures are schematic and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the disclosure. Additionally, sizes of structures or regions may be exaggerated relative to other structures or regions for illustrative purposes and, thus, are provided to illustrate the general structures of the present subject matter and may or may not be drawn to scale. Common elements between figures may be shown herein with common element numbers and may not be subsequently re-described.

[0049] To provide compact and high-performance radio frequency (RF) circuits, a vertically stacked configuration may be utilized in die fabrication. For

an RF switch structure, a portion of the RF switch structure can be implemented in a top wafer, while the reminder portion of the RF switch structure can be implemented in a bottom wafer. The top wafer is bonded to and positioned over the bottom wafer, which is formed over a silicon handle wafer (see PCT Patent Application No. PCT/US2023/071309, entitled “WAFER-LEVEL HYBRID BONDED RADIO FREQUENCY CIRCUIT” the disclosure of which is incorporated herein by reference in its entirety). Figures 1A and 1B illustrate schematics of a typical RF switch structure 100 with a stacked configuration. Figure 1A shows a schematic of a bottom switch portion 100B of the RF switch structure 100 intended to be implemented in a bottom wafer, while Figure 1B shows a schematic of a top switch portion 100T of the RF switch structure 100 intended to be implemented in a top wafer.

[0050] To minimize parasitic capacitances associated with the bottom switch portion 100B and the top switch portion 100T, and to avoid metal conductors of significant lengths as part of a fabrication process, the bottom switch portion 100B and the top switch portion 100T are designed to be mirror copies of one another. In this manner, the bottom and top switch portions 100B and 100T are connected in parallel to form the RF switch structure 100.

[0051] In detail, RF_INPUT terminals of the bottom switch portion 100B and the top switch portion 100T are connected to one another to form a single RF_INPUT terminal. Similarly, RF_OUTPUT terminals of the bottom switch portion 100B and the top switch portion 100T are connected to one another to form a single RF_OUTPUT terminal. As shown, each of the bottom switch portion 100B and the top switch portion 100T includes a set of the bottom field-effect transistors (FETs) QxB (e.g., Q1B, Q2B, and Q3B) and a set of the top FETs QxT (e.g., Q1T, Q2T, and Q3T), respectively. The set of the bottom FETs Q1B, Q2B, and Q3B are coupled in series between the RF_INPUT terminal and the RF_OUTPUT terminal. Herein, a drain node of the bottom FET Q1B is coupled to an input node SD0, a source node of the bottom FET Q1B is coupled to a drain node of the bottom FET Q2B at a first node SD1, a source node of the bottom FET Q2B is coupled to a drain node of the bottom FET Q3B at a second node

SD2, and a source node of the bottom FET Q3B is coupled to an output node SD3. The input node SD0 is coupled to the RF_INPUT terminal, while the output node SD3 is coupled to the RF_OUTPUT terminal. Similarly, the set of the top FETs Q1T, Q2T, and Q3T are also coupled in series between the RF_INPUT terminal and the RF_OUTPUT terminal, and share the same nodes SD0, SD1, SD2, and SD3 with the set of the bottom FETs Q1B, Q2B, and Q3B. A drain node of the top FET Q1T is coupled to the input node SD0, a source node of the top FET Q1T is coupled to a drain node of the top FET Q2T at the first node SD1, a source node of the top FET Q2T is coupled to a drain node of the top FET Q3T at the second node SD2, and a source node of the top FET Q3T is coupled to the output node SD3. Note that each top/bottom FET QxB/QxT is a bilateral device (e.g., symmetrical device), in which a source and a drain are interchangeable. Each top FET QxT is parallel to a corresponding bottom FET QxB. As such, by fabricating FETs on both top and bottom wafers, a total device width associated with all FETs can be twice that achieved with a non-stacked configuration (i.e., one wafer) in substantially the same footprint.

[0052] In order to direct current (DC) bias the RF switch structure 100, each of the bottom switch portion 100B and the top switch portion 100T may also include gate, body, and/or source-drain bias resistors. For a non-limited example, the bottom switch portion 100B may include three gate bias resistors RG1B, RG2B, and RG3B coupled between a gate terminal VG (e.g., providing a gate voltage signal) and gate terminals G1, G2, and G3 of the bottom FETs Q1B, Q2B, and Q3B, respectively; three body bias resistors RB1B, RB2B, and RB3B coupled between a body terminal VB (e.g., providing a body voltage signal, like ground) and body terminals B1, B2, and B3 of the bottom FETs Q1B, Q2B, and Q3B, respectively; and three source-drain bias resistors RSD1B, RSD2B, and RSD3B coupled between the source node and the drain node of the bottom FETs Q1B, Q2B, and Q3B, respectively. Similarly, gate, body, and source-drain resistors RG1T, RG2T, RG3T, RB1T, RB2T, RB3T, RSD1T, RSD2T, and RSD3T of the top switch portion 100T may be coupled as illustrated and described in the bottom switch portion 100B. Herein, the nodes RF_INPUT, RF_OUTPUT, VG,

VB, SD0, SD1, SD2, SD3, G1, G2, G3, B1, B2, and B3 are common in the bottom switch portion 100B and the top switch portion 100T. In implementations, to ensure that the top wafer and the bottom wafer share these common nodes RF_INPUT, RF_OUTPUT, VG, VB, SD0, SD1, SD2, SD3, G1, G2, G3, B1, B2, and B3, a number of hybrid bond (HB) vias are needed (more details are in the following description).

[0053] Under RF operations, the gate, body and source-drain bias resistors within the RF switch structure 100 may have significant current density. However, the gate, body, and source-drain bias resistors RG1T, RG2T, RG3T, RB1T, RB2T, RB3T, RSD1T, RSD2T, and RSD3T of the top switch portion 100T, which are intended to be fabricated in the top wafer, will have larger vertical distances to the silicon handle wafer, potentially resulting in thermal performance degradation. As such, the reliability of the RF switch structure 100 might be affected. It is therefore preferable to keep the gate, body and source-drain bias resistors of the RF switch structure 100 only in the bottom wafer to maintain lower resistor temperature and ensure reliable operation.

[0054] Figures 2A and 2B illustrate schematics of an exemplary RF switch structure 200 for better thermal performance. Figure 2A shows a schematic of a bottom switch portion 200B of the RF switch structure 200 intended to be implemented in a bottom wafer, while Figure 2B shows a schematic of a top switch portion 200T of the RF switch structure 200 intended to be implemented in a top wafer. The bottom switch portion 200B and the top switch portion 200T illustrated in Figures 2A and 2B are substantially similar to the bottom switch portion 100B and the top switch portion 100T illustrated in Figures 1A and 1B with the exception that the gate, body, and source-drain bias resistors RG1T, RG2T, RG3T, RB1T, RB2T, RB3T, RSD1T, RSD2T, and RSD3T shown in Figure 1B are omitted in the top switch portion 200T. Since the nodes RF_INPUT, RF_OUTPUT, VG, VB, SD0, SD1, SD2, SD3, G1, G2, G3, B1, B2, and B3 are shared by the set of the bottom FETs Q1B, Q2B, and Q3B and the set of the top FETs Q1T, Q2T, and Q3T, the gate, body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and

RSD3B implemented in the bottom wafer can also be utilized by the set of the top FETs Q1T, Q2T, and Q3T for DC voltage biasing. The resistance values of these bias resistors may be adjusted due to their utilization by both the set of the bottom FETs Q1B, Q2B, and Q3B and the set of the top FETs Q1T, Q2T, and Q3T. In some applications, the body bias resistors RB1B, RB2B, RB3B might be omitted, the bodies of the bottom FETs Q1B, Q2B, and Q3B might be biased locally (e.g., utilizing corresponding gate voltages of the bottom FETs Q1B, Q2B, and Q3B, respectively, not shown). The bodies of the top FETs Q1T, Q2T, and Q3T might also be biased locally (e.g., utilizing corresponding gate voltages of the top FETs Q1T, Q2T, and Q3T, respectively, or utilizing corresponding gate voltages of the bottom FETs Q1B, Q2B, and Q3B, respectively, not shown).

[0055] Because the top FETs QxT intended to be implemented in the top wafer will have larger vertical distances to the silicon handle wafer compared to the bottom FETs QxB intended to be implemented in the bottom wafer (the silicon handle wafer is placed underneath the bottom wafer), the top FETs QxT intended to be implemented in the top wafer have a greater thermal resistance in comparison to the bottom FETs QxB intended to be implemented in the bottom wafer. On the other hand, only the bottom switch portion 200B includes gate, body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B that may have significant current density under RF operations. Absent gate, body, and source-drain bias resistors in the top switch portion 200T, the top switch portion 200T may take advantage of the greater bulk in the top wafer. Accordingly, an asymmetric RF circuit formed by the bottom switch portion 200B and the top switch portion 200T may benefit from the difference in thermal performance, which may result in a lower resistor temperature and may ensure more reliable operation of the bottom switch portion 200B and the top switch portion 200T as coupled to one another.

[0056] In different applications, the top switch portion 200T may include fewer or more top FETs coupled in series between the RF_INPUT terminal and the RF_OUTPUT terminal, and the bottom switch portion 200B correspondingly may include fewer or more bottom FETs coupled in series between the RF_INPUT

terminal and the RF_OUTPUT terminal, and fewer or more corresponding bias resistors. Each top FET and its corresponding top FET may still be connected and parallel to each other, and utilize the same gate, body, and source-drain bias resistors implemented in the bottom wafer.

5 **[0057]** Figures 3A and 3B illustrate a typical implementation 300 of the RF switch structure 200 shown in Figures 2A and 2B. Figure 3A illustrates a top perspective view of a layout of a bottom wafer 300B, within which the bottom switch portion 200B is implemented, and Figure 3B illustrates a bottom perspective view of a layout of a top wafer 300T, within which the top switch portion 200T is implemented. The top wafer 300T is bonded to and placed over the bottom wafer 300B, such that the set of the top FETs QxT in the top wafer 300T are opposite to the set of the bottom FETs QxB in the bottom wafer 300B, respectively.

15 **[0058]** Typically, the bottom wafer 300B and the top wafer 300T may each include multiple metal layers and different vertical vias VV between the metal layers to achieve electrical connections, as illustrated in Figure 3C. Herein, Figure 3C only shows a small portion of the bottom wafer 300B and a small portion of the top wafer 300T for simplicity. For the purpose of this illustration, the bottom wafer 300B includes a first bottom metal layer M1B as the topmost bottom metal layer, a second bottom metal layer M2B underneath the first bottom metal layer M1B, and a third bottom metal layer M3B underneath the second bottom metal layer M2B, while the top wafer 300T includes a first top metal layer M1T as the bottommost top metal layer, a second top metal layer M2T over the first top metal layer M1T, and a third top metal layer M3T over the second top metal layer M2T. In different applications, the bottom wafer 300B and the top wafer 300T may each include fewer or more metal layers. In addition, the metal layers in the bottom wafer 300B and the top wafer 300T may also constitute certain portions of the bottom FETs QxB and the top FETs QxT, respectively (e.g., source/drain fingers connected to source/drain implants of the FETs QxB/QxT, more details are described below).

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[0059] From horizontal layout aspects, the bottom wafer 300B includes four bottom source/drain connection regions 302B (e.g., a first bottom source/drain connection region 302B1, a second bottom source/drain connection region 302B2, a third bottom source/drain connection region 302B3, and a fourth bottom source/drain connection region 302B4), three bottom active switch regions 304B (e.g., a first bottom active switch region 304B1, a second bottom active switch region 304B2, and a third bottom active switch region 304B3), three bottom gate connection regions 306B (e.g., a first bottom gate connection region 306B1, a second bottom gate connection region 306B2, and a third bottom gate connection region 306B3), and three bottom body connection regions 308B (e.g., a first bottom body connection region 308B1, a second bottom body connection region 308B2, and a third bottom body connection region 308B3). Herein, each bottom active switch region 304B is configured to provide a corresponding bottom FET QxB, while the bottom source/drain connection regions 302B, the bottom gate connection regions 306B, and the bottom body connection regions 308B are configured to provide connection from the bottom active switch regions 304B (i.e., from the bottom FETs QxB) towards the top wafer 300T. The bottom source/drain connection regions 302B, the bottom gate connection regions 306B, and the bottom body connection regions 308B are formed from the topmost metal layer (e.g., the first bottom metal layer M1B) in the bottom wafer 300B, which is at a higher vertical level than the bottom active switch regions 304B.

[0060] Similarly, the top wafer 300T includes four top source/drain connection regions 302T (e.g., a first top source/drain connection region 302T1, a second top source/drain connection region 302T2, a third top source/drain connection region 302T3, and a fourth top source/drain connection region 302T4), three top active switch regions 304T (e.g., a first top active switch region 304T1, a second top active switch region 304T2, and a third top active switch region 304T3), three top gate connection regions 306T (e.g., a first top gate connection region 306T1, a second top gate connection region 306T2, and a third top gate connection region 306T3), and three top body connection regions 308T (e.g., a first top body connection region 308T1, a second top body connection region 308T2, and a

third top body connection region 308T3). Herein, each top active switch region 304T is configured to provide a corresponding top FET QxT, while the top source/drain connection regions 302T, the top gate connection regions 306T, and the top body connection regions 308T are configured to provide connection from the top active switch regions 304T (i.e., from the top FETs QxT) towards the bottom wafer 300B. The top source/drain connection regions 302T, the top gate connection regions 306T, and the top body connection regions 308T are formed from the bottommost metal layer (e.g., the first top metal layer M1T) in the top wafer 300T, which is at a lower vertical level than the top active switch regions 304T.

[0061] For a non-limited example, each FET QxB/QxT in the bottom wafer 300B or in the top wafer 300T might be a multi-finger transistor as illustrated in Figure 3D. Each bottom/top active switch region 304B/304T substantially indicates a horizontal position where a multi-finger gate G (e.g., an H-shape gate), a channel CH, a multi-finger drain S/D1 (e.g., a comb structure), a multi-finger source S/D2 (e.g., a comb structure), and a body B of a corresponding FET QxB/QxT are located. The multi-finger gate G, the channel CH, the multi-finger drain S/D1, the multi-finger source S/D2, and the body B of each FET QxB/QxT might be formed at different vertical levels within the bottom/top wafer 300B/300T using metals, polysilicon, dielectrics, or any combination thereof. For instance, the multi-finger drain S/D1 and the multi-finger source S/D2 may be formed from a metal layer in the bottom wafer 300B or in the top wafer 300T (e.g., the second bottom metal layer M2B or the third bottom metal layer M3B in the bottom wafer 300B, the second top metal layer M2T or the third top metal layer M3T in the top wafer 300T, see Figure 3C) and electrically connected (through vertical vias) to source/drain implants (not shown) in the device layer. The multi-finger gate G may be formed of polysilicon underneath the bottommost bottom metal layer M3B or above the topmost top metal layer M3T. The body B is provided in the device layer underneath the bottommost bottom metal layer M3B or above the topmost top metal layer M3T. Note that each top/bottom FET

QxB/QxT is a symmetrical device and therefore the multi-finger drain and source S/D1 and S/D2 of one FET are interchangeable.

[0062] In the bottom wafer 300B, the multi-finger gate G, the channel CH, the multi-finger drain S/D1, the multi-finger source S/D2, and the body B of each bottom FET QxB are at lower vertical levels than the topmost bottom metal layer (e.g., the first bottom metal layer M1B). In the top wafer 300T, the multi-finger gate G, the channel CH, the multi-finger drain S/D1, the multi-finger source S/D2, and the body B of each top FET QxT are at higher vertical levels than the bottom most top metal layer (e.g., the first top metal layer M1T).

[0063] Each bottom gate connection region 306B may be electrically connected to the multi-finger gate G of the corresponding bottom FET QxB through one or more gate routing lines GRL (e.g., formed from the second bottom metal layer M2B and the third bottom metal layer M3B that are lower than the first bottom metal layer M1B) and one or more vertical vias VV (e.g., vertical vias between the first bottom metal layer M1B and the second bottom metal layer M2B, between the second bottom metal layer M2B and the third bottom metal layer M3B, and between the third bottom metal layer M3B and the multi-finger gate G). Each bottom body connection region 308B may be electrically connected to the body B of the corresponding bottom FET QxB through one or more body routing lines BRL (e.g., formed from the second bottom metal layer M2B and the third bottom metal layer M3B that are lower than the first bottom metal layer M1B) and one or more vertical vias VV (e.g., vertical vias between the first bottom metal layer M1B and the second bottom metal layer M2B, between the second bottom metal layer M2B and the third bottom metal layer M3B, and between the third bottom metal layer M3B and the body B). In this illustration, the bottom gate connection regions 306B and the bottom body connection regions 308B are located horizontally outside the bottom active switch regions 304B. Herein, each bottom gate connection region 306B is connected to the corresponding multi-finger gate G by both the vertical vias VV and the gate routing lines GRL rather than only by vertical vias VV within the corresponding bottom active switch region 304B, so as to avoid unintended short

circuits in the bottom active switch regions 304B. Each bottom body connection region 308B is connected to the corresponding body B by both the vertical vias VV and the body routing lines BRL rather than only by vertical vias VV within the corresponding bottom active switch region 304B, so as to avoid unintended short circuits in the bottom active switch regions 304B.

[0064] In addition, each bottom source/drain connection region 302B may be electrically connected to a corresponding multi-finger drain and/or a corresponding multi-finger source (e.g., formed from the second bottom metal layer M2B or the third bottom metal layer M3B in the bottom wafer 300B) through multiple vertical vias VV (e.g., vertical vias between the first bottom metal layer M1B and the second bottom metal layer M2B and optionally between the second bottom metal layer M2B and the third bottom metal layer M3B) and optional routing lines (e.g., formed from the second bottom metal layer M2B if the corresponding multi-finger drain S/D is formed from the third bottom metal layer M3B in the bottom wafer 300B). Herein, the second bottom source/drain connection region 302B2 is electrically connected to both the source of the first bottom FET Q1B and the drain of the second bottom FET Q2B, while the third bottom source/drain connection region 302B3 is electrically connected to both the source of the second bottom FET Q2B and the drain of the third bottom FET Q3B. In a horizontal plane, the first bottom active switch region 304B1 is located between the first and second bottom source/drain regions 302B1 and 302B2, the second bottom active switch region 304B2 is located between the second and third bottom source/drain regions 302B2 and 302B3, and the third bottom active switch region 304B3 is located between the third and fourth bottom source/drain regions 302B3 and 302B4.

[0065] Similar concepts apply to the top wafer 300T. Each top gate connection region 306T may be electrically connected to the multi-finger gate G of the corresponding top FET QxT through one or more gate routing lines GRL (e.g., formed from the second top metal layer M2T and the third top metal layer M3T that are located higher than the first top metal layer M1T) and one or more vertical vias VV (e.g., vertical vias between the first top metal layer M1T and the

second top metal layer M2T, between the second top metal layer M2T and the third top metal layer M3T, and between the third top metal layer M3T and the multi-finger gate G). Each top body connection region 308T is electrically connected to the body B of the corresponding top FET QxT through one or more body routing lines BRL (e.g., formed from the second top metal layer M2T and the third top metal layer M3T that are located higher than the first top metal layer M1T) and one or more vertical vias VV (e.g., vertical vias between the first top metal layer M1T and the second top metal layer M2T, between the second top metal layer M2T and the third top metal layer M3T, and between the third top metal layer M3T and the body B). In this illustration, the top gate connection regions 306T and the top body connection regions 308T are located horizontally outside the top active switch regions 304T. Herein, each top gate connection region 306T is connected to the corresponding multi-finger gate G by both the vertical vias VV and the gate routing lines GRL rather than only by vertical vias VV within the corresponding top active switch region 304T, so as to avoid unintended short circuits in the top active switch regions 304T. Each top body connection region 308T is connected to the corresponding body B by both the vertical vias VV and the body routing lines BRL rather than only by vertical vias VV within the corresponding top active switch region 304T, so as to avoid unintended short circuits in the top active switch regions 304T.

[0066] In addition, each top source/drain connection region 302T may be electrically connected to a corresponding multi-finger drain and/or a corresponding multi-finger source (e.g., formed from the second top metal layer M2T or the third top metal layer M3T in the top wafer 300T) through multiple vertical vias VV (e.g., vertical vias between the first top metal layer M1T and the second top metal layer M2T and optionally between the second top metal layer M2T and the third top metal layer M3T) and optional routing lines (e.g., formed from the second top metal layer M2T if the corresponding multi-finger drain/source is formed from the third top metal layer M3T in the top wafer 300T). Herein, the second top source/drain connection region 302T2 is electrically connected to both the source of the first top FET Q1T and the drain of the

second top FET Q2T, while the third top source/drain connection region 302T3 is electrically connected to both the source of the second top FET Q2T and the drain of the third top FET Q3T. In the horizontal plane, the first top active switch region 304T1 is located between the first and second top source/drain regions 302T1 and 302T2, the second top active switch region 304T2 is located between the second and third top source/drain regions 302T2 and 302T3, and the third top active switch region 304T3 is located between the third and fourth top source/drain regions 302T3 and 302T4.

[0067] Furthermore, the bottom wafer 300B also includes one or more bottom HB vias 316B connected to and confined within the bottom source/drain connection regions 302B, the bottom gate connection regions 306B, and the bottom body connection regions 308B (only certain bottom HB vias are labeled with reference numbers for clarity, see Figures 3C and 3D), respectively. Each bottom HB via 316B is exposed at a top surface of the bottom wafer 300B. The top wafer 300T includes one or more top HB vias 316T connected to and confined within the top source/drain regions 302T, the top gate connection regions 306T, and the top body connection regions 308T (only certain top HB vias are labeled with reference numbers for clarity, see Figures 3C and 3D), respectively. Each top HB via 316T is exposed at a bottom surface of the top wafer 300T. The bottom HB vias 316B and the top HB vias 316T are configured to electrically connect the top wafer 300T to the bottom wafer 300B.

[0068] Herein, the bottom HB vias 316B in the bottom wafer 300B and the top HB vias 316T in the top wafer 300T have a same number and are positioned at same relative locations in the horizontal plane. Once the top wafer 300T is placed over the bottom wafer 300B, each top HB via 316T is vertically aligned with and directly connected to a corresponding bottom HB via 316B. In detail, the bottom HB vias 316B confined within the bottom source/drain regions 302B are directly coupled to the top HB vias 316T confined within the top source/drain regions 302T, respectively. As such, the first bottom source/drain region 302B1 and the first top source/drain region 302T1 are connected (i.e., having a same voltage level as the input node SD0 shown in Figures 2A and 2B), the second

bottom source/drain region 302B2 and the second top source/drain region 302T2 are connected (i.e., having a same voltage level as the first node SD1 shown in Figures 2A and 2B), the third bottom source/drain region 302B3 and the third top source/drain region 302T3 are connected (i.e., having a same voltage level as the second node SD2 shown in Figures 2A and 2B), and the fourth bottom source/drain region 302B4 and the fourth top source/drain region 302T4 are connected (i.e., having a same voltage level as the output node SD3 shown in Figures 2A and 2B). In addition, the bottom HB vias 316B confined within the bottom gate connection regions 306B are directly coupled to the top HB vias 316T confined within the top gate connections region 306T, respectively. As such, the first bottom gate connection region 306B1 and the first top gate connection region 306T1 are connected (i.e., having a same voltage level as the first gate terminals G1 shown in Figures 2A and 2B), the second bottom gate connection region 306B2 and the second top gate connection region 306T2 are connected (i.e., having a same voltage level as the first gate terminals G2 shown in Figures 2A and 2B), and the third bottom gate connection region 306B3 and the third top gate connection region 306T3 are connected (i.e., having a same voltage level as the third gate terminals G3 shown in Figures 2A and 2B). The bottom HB vias 316B confined within the bottom body connection regions 308B are directly coupled to the top HB vias 316T confined within the top body connection regions 308T, respectively. As such, the first bottom body connection region 308B1 and the first top body connection region 308T1 are connected (i.e., having a same voltage level as the first body terminals B1 shown in Figures 2A and 2B), the second bottom body connection region 308B2 and the second top body connection region 308T2 are connected (i.e., having a same voltage level as the first body terminals B2 shown in Figures 2A and 2B), and the third bottom body connection region 308B3 and the third top body connection region 308T3 are connected (i.e., having a same voltage level as the third body terminals B3 shown in Figures 2A and 2B).

[0069] In this illustration, each top FET QxT is electrically parallel to a corresponding bottom FET QxB. If each bottom active switch region 304B has a

same device width $W1B$ and each top active switch region 304B has a same device width $W1T=W1B$, a total device width of FETs in both the top and bottom wafers 300T and 300B (i.e. the RF switch structure 200 with the stacked configuration) will be $W_{total1} = W1B + W1T$, which might be twice that of which can be achieved by a non-stacked configuration (i.e. one wafer configuration) in substantially the same footprint. By duplicating the top FETs Q1T, Q2T, and Q3T in the top wafer 300T to the bottom FETs Q1B, Q2B, and Q3B in the bottom wafer 300B, the RF switch structure 200 allows a device width of each FET (Q1T/ Q2T/Q3T/ Q1B/Q2B/Q3B) to be reduced by 30%, 40%, or 50% while maintaining a same overall electrical performance as a conventional RF switch structure with a non-stacked confirmation. For each bottom FET QxB and each top FET QxT, the current density is concentrated at the drain and source. In one embodiment, a width of each bottom source/drain connection region 302B may be substantially equal to (e.g., about 10% tolerance) the device width $W1B$ of the bottom active switch region 304B, and a width of each top source/drain connection region 302T may be substantially equal to (about 10% tolerance) the device width $W1T$ of the top active switch region 304T for good thermal dissipation.

[0070] To provide DC voltage biasing to the bottom FETs Q1B, Q2B, and Q3B, the bottom wafer 300B may also include the three bottom gate bias resistors RG1B, RG2B, and RG3B, the three bottom body bias resistors RB1B, RB2B, and RB3B, and the three bottom source-drain bias resistors RSD1B, RSD2B, and RSD3B. These bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B are typically formed from polysilicon underneath the bottommost bottom metal layer M3B (see Figure 3C). To avoid shorting the bottom FETs Q1B, Q2B, and Q3B, to ensure a relatively good RF performance, and to achieve a small footprint and a relatively thin profile, the first bottom gate bias resistor RG1B, the first bottom body bias resistor RB1B, and the first bottom source-drain bias resistor RSD1B may be placed to surround the first bottom active switch region 304B1 without overlap in the horizontal plane. The second bottom gate bias resistor RG2B, the second bottom body bias

resistor RB2B, and the second bottom source-drain bias resistor RSD2B may surround the second bottom active switch region 304B2 without overlap in the horizontal plane. The third bottom gate bias resistor RG3B, the third bottom body bias resistor RB3B, and the third bottom source-drain bias resistor RSD3B may surround the third bottom active switch region 304B3 without overlap in the horizontal plane.

[0071] The first, second, and third bottom gate bias resistors RG1B, RG2B, and RG3B are electrically coupled between the gate terminal VG and the first, second, and third gate terminals G1, G2, and G3, respectively (i.e., between the gate terminal VG and the first, second, and third bottom gate connection regions 306B1, 306B2, and 306B3, respectively) through routing lines (e.g., formed from the second bottom metal layer M2B and/or the third bottom metal layer M3B, not shown) and optionally through vertical vias VV (e.g., vertical vias between the third bottom metal layer M3B and the polysilicon gate bias resistors RGxB, between the second bottom metal layer M2B and the third bottom metal layer M3B, and/or between the first bottom metal layer M1B and the second bottom metal layer M2B, not shown). The first, second, and third bottom body bias resistors RB1B, RB2B, and RB3B are electrically coupled between the body terminal VB and the first, second, and third body terminals B1, B2, and B3, respectively (i.e., between the body terminal VB and the first, second, and third bottom body connection regions 308B1, 308B2, and 308B3, respectively) through routing lines (e.g., formed from the second bottom metal layer M2B and/or the third bottom metal layer M3B, not shown) and optionally through vertical vias VV (e.g., vertical vias between the third bottom metal layer M3B and the polysilicon body bias resistors RBxB, between the second bottom metal layer M2B and the third bottom metal layer M3B, and/or between the first bottom metal layer M1B and the second bottom metal layer M2B, not shown).

[0072] The first source-drain bias resistor RSD1B is electrically coupled between the drain (the input node SD0) of the first bottom FET Q1B and the source (the first node SD1) of the first bottom FET Q1B (i.e., between the first bottom source/drain region 302B1 and the second bottom source/drain region

302B2) through routing lines (e.g., formed from the second bottom metal layer M2B and/or the third bottom metal layer M3B, not shown) and optionally through vertical vias VV (e.g., vertical vias between the third bottom metal layer M3B and the polysilicon first source-drain bias resistor RSD1B, between the second
5 bottom metal layer M2B and the third bottom metal layer M3B, and/or between the first bottom metal layer M1B and the second bottom metal layer M2B, not shown). The second source-drain bias resistor RSD2B is electrically coupled between the drain (the first node SD1) of the second bottom FET Q2B and the source (the second node SD2) of the second bottom FET Q2B (i.e., between the
10 second bottom source/drain region 302B2 and the third bottom source/drain region 302B3) through routing lines (e.g., formed from the second bottom metal layer M2B and/or the third bottom metal layer M3B, not shown) and optionally through vertical vias VV (e.g., vertical vias between the third bottom metal layer M3B and the polysilicon second bottom source/drain region 302B2, between the
15 second bottom metal layer M2B and the third bottom metal layer M3B, and/or between the first bottom metal layer M1B and the second bottom metal layer M2B, not shown). The third source-drain bias resistor RSD3B is electrically coupled between the drain (the second node SD2) of the third bottom FET Q3B and the source (the output node SD3) of the third bottom FET Q3B (i.e., the third
20 bottom source/drain region 302B3 and the fourth bottom source/drain region 302B4) through routing lines (e.g., formed from the second bottom metal layer M2B and/or the third bottom metal layer M3B, not shown) and optionally through vertical vias VV (e.g., vertical vias between the third bottom metal layer M3B and the polysilicon third source-drain bias resistor RSD3B, between the second
25 bottom metal layer M2B and the third bottom metal layer M3B, and/or between the first bottom metal layer M1B and the second bottom metal layer M2B, not shown).

[0073] Since the top HB vias 316T and the bottom HB vias 316B provide connections between the top wafer 300T and the bottom wafer 300B as
30 described above, the DC voltage biasing to the top FETs Q1T, Q2T, and Q3T are also provided through the bottom gate, body, and source-drain bias resistors

RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B, which are located on the bottom wafer 300B.

[0074] As shown and described above, the bottom wafer 300B includes the set of the bottom FETs QxB (with the device width W1B) as well as the gate,

5 body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B, which might be needed to bias the RF switch structure 200. Compared to the bottom wafer 300B, the top wafer 300T only includes the set of the top FETs QxT (with the device width W1T) without any gate, body, and source-drain bias resistors. If the top wafer 300T contributes a
10 same amount to the total device width W_{total1} as the bottom wafer 300B (i.e., $W1B = W1T$, half of the total device width W_{total1} would be placed on the bottom wafer 300B and half of the total device width W_{total1} would be placed on the top wafer 300T) and has a same footprint as the bottom wafer 300B (i.e., the bottom wafer 300B and the top wafer 300B have a same wafer width WW1), there will be
15 an unutilized area around the set of the top FETs QxT in the top wafer 300T. For RF switch applications, which have a relatively small active device width (such as high throw count antenna switches), the area (footprint) for gate, body, and source-drain bias resistors can be a significant part compared to the area for the active switch regions, resulting in underutilization of the top wafer 300T.

20 Therefore, even if the stacked configuration shown in Figures 3A and 3B offers significant die size shrink, there is additional room for improvement to further utilize the area of the top wafer 300T.

[0075] Figures 4A and 4B illustrate an improved implementation 400 of the RF switch structure 200 according to some embodiments of the present disclosure.

25 Figure 4A illustrates a top perspective view of a layout of a bottom wafer 400B, within which the bottom switch portion 200B is implemented, and Figure 4B illustrates a bottom perspective view of a layout of a top wafer 400T, within which the top switch portion 200T is implemented. The top wafer 400T is bonded to and placed over the bottom wafer 400B, such that the set of the top FETs QxT in the
30 top wafer 400T are opposed to the set of the bottom FETs QxB in the bottom wafer 400B, respectively.

[0076] The bottom wafer 400B and the top wafer 400T may each include multiple metal layers and different vertical vias VV between the metal layers to achieve electrical connections (similar to the illustration shown in Figure 3C). For a non-limited example, the bottom wafer 400B also includes the first bottom metal layer M1B as the topmost bottom metal layer, the second bottom metal layer M2B underneath the first bottom metal layer M1B, and the third bottom metal layer M3B underneath the second bottom metal layer M2B, while the top wafer 300T also includes the first top metal layer M1T as the bottommost top metal layer, the second top metal layer M2T over the first top metal layer M1T, and the third top metal layer M3T over the second top metal layer M2T. In different applications, the bottom wafer 400B and the top wafer 400T may each include fewer or more metal layers. In addition, the metal layers in the bottom wafer 400B and the top wafer 400T may also constitute certain portions of the bottom FETs QxB and the top FETs QxT, respectively.

[0077] Herein, the bottom wafer 400B shown in Figure 4A has a similar layout and configuration as the bottom wafer 300B shown in Figures 3A and 3D (FET device size reduction can be achieved in the bottom wafer 400B, more details are in the following description). The bottom wafer 400B includes four bottom source/drain connection regions 402B (e.g., a first bottom source/drain connection region 402B1, a second bottom source/drain connection region 402B2, a third bottom source/drain connection region 402B3, and a fourth bottom source/drain connection region 402B4), three bottom active switch regions 404B (e.g., a first bottom active switch region 404B1, a second bottom active switch region 404B2, and a third bottom active switch region 404B3), three bottom gate connection regions 406B (e.g., a first bottom gate connection region 406B1, a second bottom gate connection region 406B2, and a third bottom gate connection region 406B3), three bottom body connection regions 408B (e.g., a first bottom body connection region 408B1, a second bottom body connection region 408B2, and a third bottom body connection region 408B3), three gate bias resistors RG1B, RG2B, RG3B, three body bias resistors RB1B, RB2B, RB3B, and three source-drain bias resistors RSD1B, RSD2B, and RSD3B.

[0078] Each bottom active switch region 404B is configured to provide a corresponding bottom FET QxB, which might be a multi-finger transistor, while the bottom source/drain connection regions 402B, the bottom gate connection regions 406B, and the bottom body connection regions 408B are configured to provide connection from the bottom active switch regions 404B (i.e., from the bottom FETs QxB) towards the top wafer 400T (similar to illustration and description of Figure 3D). The bottom source/drain connection regions 402B, the bottom gate connection regions 406B, and the bottom body connection regions 408B are formed from the topmost metal layer (e.g., the first bottom metal layer M1B) in the bottom wafer 400B, which is at a higher vertical level than the bottom active switch regions 404B. In different applications, the bottom wafer 400B might include fewer or more bottom active switch regions 404B (if the RF switch structure 200 includes fewer or more bottom FET QxB), and corresponding fewer or more bottom source/drain connection regions 402B, fewer or more bottom gate connection regions 406B, fewer or more bottom body connection regions 408B, fewer or more gate bias resistors, fewer or more body bias resistors, and fewer or more source-drain bias resistors.

[0079] In the horizontal plane, the first bottom active switch region 404B1 is located between the first and second bottom source/drain regions 402B1 and 402B2, the second bottom active switch region 404B2 is located between the second and third bottom source/drain regions 402B2 and 402B3, and the third bottom active switch region 404B3 is located between the third and fourth bottom source/drain regions 402B3 and 402B4. To avoid shorting the bottom active switch regions 404B, the bottom gate connection regions 406B, the bottom body connection regions 408B, the gate bias resistors RG1B, RG2B, and RG3B, the body bias resistors RB1B, RB2B, and RB3B, and the source-drain bias resistors RSD1B, RSD2B, and RSD3B may be located horizontally outside and are surrounding the bottom active switch regions 404B. The bias resistors RBxB/RGxB/ RSDxB may be formed from polysilicon underneath the bottommost bottom metal layer M3B (more details are as described above). In one embodiment, each bias resistor RBxB/RGxB/ RSDxB (e.g., RG1B, RG2B, RG3B,

RB1B, RB2B, RB3B, RG1B, RG2B, and RG3B) is segmented. Segmented schematics of the bias resistors RBxB, RGxB, and RSDxB are shown in Figure 4C.

[0080] The bottom wafer 400B also includes one or more bottom HB vias 416B confined within the bottom source/drain connection regions 402B, the bottom gate connection regions 406B, and the bottom body connection regions 408B (only certain bottom HB vias are labeled with reference numbers for clarity), respectively. Each bottom HB via 416B is exposed at a top surface of the bottom wafer 400B.

[0081] To effectively utilize the top wafer 400T, areas in the top wafer 400T, which are above the gate, body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B of the bottom wafer 400B, can be used to grow the top FETs QxT. In detail, the top wafer 400T includes four top source/drain connection regions 402T (e.g., a first top source/drain connection region 402T1, a second top source/drain connection region 402T2, a third top source/drain connection region 402T3, and a fourth top source/drain connection region 402T4), three top active switch regions 404T (e.g., a first top active switch region 404T1, a second top active switch region 404T2, and a third top active switch region 404T3), three top gate connection regions 406T (e.g., a first top gate connection region 406T1, a second top gate connection region 406T2, and a third top gate connection region 406T3), and three top body connection regions 408T (e.g., a first top body connection region 408T1, a second top body connection region 408T2, and a third top body connection region 408T3). For good connection/bonding, the top wafer 400T and the bottom wafer 400B are designed, such that once the top wafer 400T is placed over the bottom wafer 400B, each of the top source/drain connection regions 402T, the top active switch regions 404T, the top gate connection regions 406T, and the top body connection regions 408T in the top wafer 400T is aligned over a corresponding one of the bottom source/drain connection regions 402B, the bottom active switch regions 404B, the bottom gate connection regions 406B, and the bottom body connection regions 408B in the bottom wafer 400B.

[0082] Herein, each top active switch region 404T is configured to provide a corresponding top FET QxT, while the top source/drain connection regions 402T, the top gate connection regions 406T, and the top body connection regions 408T are configured to provide connection from the top active switch regions 404T (i.e., from the top FETs QxT) to the bottom wafer 400B. The top source/drain connection regions 402T, the top gate connection regions 406T, and the top body connection regions 408T are formed from the bottommost top metal layer (e.g., the first top metal layer M1T), which is at a lower vertical level than the top active switch regions 404T. In different applications, the top wafer 400T might include fewer or more top active switch regions 404T (if the RF switch structure 200 includes fewer or more top FET QxT), and corresponding fewer or more top source/drain connection regions 402T, fewer or more top gate connection regions 406T, and fewer or more top body connection regions 408T.

[0083] In some cases, when the bodies of the bottom FETs Q1B, Q2B, and Q3B and the bodies of the top FETs Q1T, Q2T, and Q3T are biased locally, the body bias resistors RB1B, RB2B, RB3B can be omitted in the bottom wafer 400B. If the bodies of the top FETs Q1T, Q2T, and Q3T are biased by utilizing corresponding gate voltages of the top FETs Q1T, Q2T, and Q3T, respectively, the bottom body connection regions 408B and associated bottom HB vias 416B in the bottom wafer 400B, and the top body connection regions 408T and associated top HB vias 416T in the top wafer 400T can also be omitted. If the bodies of the top FETs Q1T, Q2T, and Q3T are biased by utilizing corresponding gate voltages of the bottom FETs Q1B, Q2B, and Q3B, respectively, the bottom body connection regions 408B and the associated bottom HB vias 416B in the bottom wafer 400B, and the top body connection regions 408T and the associated top HB vias 416T in the top wafer 400T are still needed for electrical connection.

[0084] In one embodiment, each top FET QxT might be a multi-finger transistor, as illustrated in Figure 4D. Each top active switch region 404T substantially indicates a horizontal position where a multi-finger gate G (e.g., an H-shape gate), a channel CH, a multi-finger drain S/D1 (e.g., a comb structure),

a multi-finger source S/D2 (e.g., a comb structure), and a body B of a corresponding top FET QxT are located. The multi-finger gate G, the channel CH, the multi-finger drain S/D1, the multi-finger source S/D2, and the body B of each top FET QxT might be formed at different vertical levels higher than the first top metal layer M1T within the top wafer 400T, using metals, polysilicon, dielectrics, or any combination thereof. For instance, the multi-finger drain S/D1 and the multi-finger source S/D2 may be formed from a top metal layer in the top wafer 400T (e.g., the second top metal layer M2T or the third top metal layer M3T in the top wafer 400T) and electrically connected (through vertical vias) to source/drain implants in the device layer over the third top metal layer M3T (similar to the illustration shown in Figure 3C). The multi-finger gate G may be formed of polysilicon above the topmost top metal layer M3T (e.g., similar to the illustration in Figure 3C). The body B is provided in the device layer above the topmost top metal layer M3T. Each top FET QxT is a symmetrical device and therefore the multi-finger drain and source S/D1 and S/D2 of one top FET QxT are interchangeable.

[0085] Within the top wafer 400T, each top active switch region 404T extends in the direction of a device width (e.g., along a device width W2T) to at least partially cover the areas of the gate, body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B that surround the corresponding bottom active switch region 404B within the bottom wafer 400B. As such, the device width W2T of each top active switch region 404T is larger than a device width W2B of the corresponding bottom active switch region 404B. As described above, after the wafer bonding, the top gate connection regions 406T and the top body connection regions 408T in the top wafer 400T are designed to be vertically aligned with the corresponding bottom gate connection regions 406B and the corresponding bottom body connection regions 408B in the bottom wafer 400B, respectively, (i.e., the top gate connection regions 406T and the top body connection regions 408T in the top wafer 400T have the same relative locations as the corresponding bottom gate connection regions 406B and the corresponding bottom body connection regions 408B in the

bottom wafer 400B). As such, each top gate connection region 406T and each top body connection region 408T may overlap (e.g., confined in) a corresponding top active switch region 404T rather than being horizontally outside the corresponding top active switch region 404T. As such, each top gate connection region 406T and each top body connection region 408T (formed from the first top metal layer M1T) may overlap the multi-finger drain S/D1 and the multi-finger drain S/D2 (e.g., formed from the second/third top metal layer M2T/M3T) of the corresponding top active switch region 404T.

[0086] In order to electrically connect each top gate connection region 406T to the multi-finger gate G of a corresponding top FET QxT (within the corresponding top active switch region 404T) without shorting circuits, the top wafer 400T may include multiple first gate route lines GRL1 formed from the first top metal layer M1T to provide an electrical connection from the top gate connection region 406T towards a location horizontally outside of the corresponding top active switch region 404T. In addition, the top wafer 400T also includes other gate route lines GRL formed from the second top metal layer M2T and the third top metal layer M3T (located higher than the first top metal layer M1T) and multiple vertical vias VV (e.g., vertical vias between the first gate route lines GRL1 and the other gate route lines GRL, vertical vias between the other gate route lines GRL, and vertical vias between the other gate route lines GRL and the multi-finger gate G) to connect each top gate connection region 406T to the multi-finger gate G within the corresponding top active switch region 404T. Herein, if there is no first gate route line GRL1 (formed from the first top metal layer M1T and extending outside the top active switch region 404T) and each top gate connection region 406T is directly connected to the second top metal layer M2T through vertical vias, it may cause short circuits in the top active switch regions 404T. It is because the top gate connection region 406T overlaps the multi-finger drain S/D1 and the multi-finger drain S/D2, which may be formed from the second top metal layer M2T, and thus the vertical vias directly from the top gate connection region 406T to the second top metal layer M2T may accidentally cause short circuits of the multi-finger drain S/D1 and the multi-finger drain S/D2.

[0087] Similarly, to electrically connect each top body connection region 408T to the body B of a corresponding top FET QxT (within the corresponding top active switch region 404T) without shorting circuits, the top wafer 400T may include multiple first body route lines BRL1 formed from the first top metal layer M1T to provide an electrical connection from the top body connection region 408T towards a location horizontally outside of the corresponding top active switch region 404T. In addition, the top wafer 400T also includes other body route lines BRL formed from the second top metal layer M2T and the third top metal layer M3T (located higher than the first top metal layer M1T) and multiple vertical vias VV (e.g., vertical vias between the first body route lines BRL1 and the other body route lines BRL, vertical vias between the other body route lines BRL, and vertical vias between the other body route lines BRL and the body B) to connect each top body connection region 406T to the body B within the corresponding top active switch region 404T. Herein, if there is no first body route line BRL1 (formed from the first top metal layer M1T and extending outside the top active switch region 404T) and each top body connection region 408T is directly connected to the second top metal layer M2T through vertical vias, it may cause short circuits in the top active switch regions 404T. It is because the top body connection region 408T overlaps the multi-finger drain S/D1 and the multi-finger drain S/D2, which may be formed from the second top metal layer M2T, and thus the vertical vias directly from the top body connection region 408T to the second top metal layer M2T may accidentally cause short circuits of the multi-finger drain S/D1 and the multi-finger drain S/D2.

[0088] Each top source/drain connection region 402T is electrically connected to a corresponding multi-finger drain and/or a corresponding multi-finger source (e.g., formed from the second top metal layer M2T or the third top metal layer M3T in the top wafer 400T) through multiple vertical vias VV (e.g., vertical vias between the first top metal layer M1T and the second top metal layer M2T and optionally between the second top metal layer M2T and the third top metal layer M3T) and optional routing lines (e.g., formed from the second top metal layer M2T if the corresponding multi-finger drain/source is formed from the third top

metal layer M3T in the top wafer 400T). Herein, the second top source/drain connection region 402T2 is electrically connected to both the source of the first top FET Q1T and the drain of the second top FET Q2T, while the third top source/drain connection region 402T3 is electrically connected to both the source of the second top FET Q2T and the drain of the third top FET Q3T. In the horizontal plane, the first top active switch region 404T1 is located between the first and second top source/drain regions 402T1 and 402T2, the second top active switch region 404T2 is located between the second and third top source/drain regions 402T2 and 402T3, and the third top active switch region 404T3 is located between the third and fourth top source/drain regions 402T3 and 402T4.

[0089] The top wafer 400T further includes one or more top HB vias 416T, which are electrically connected to and confined within the top source/drain regions 402T, the top gate connection regions 406T, and the top body connection regions 408T (only certain top HB vias are labeled with reference numbers for clarity), respectively. Each top HB via 416T is exposed at a bottom surface of the top wafer 400T. The bottom HB vias 416B in the bottom wafer 400B and the top HB vias 416T in the top wafer 400T are configured to connect the top wafer 400T to the bottom wafer 400B. The bottom HB vias 416B and the top HB vias 416T not only transmit control voltages (e.g., voltages at SD0-SD3, G1-G3, and B1-B3) from the bottom wafer 400B to the top wafer 400T but are also important to be included for thermal relief.

[0090] Herein, the bottom HB vias 416B in the bottom wafer 400B and the top HB vias 416T in the top wafer 400T have a same number and are positioned in same relative locations in the horizontal plane. Once the top wafer 400T is placed over the bottom wafer 400B, each bottom HB via 416B is vertically aligned with and directly connected to a corresponding top HB via 416T. In detail, the bottom HB vias 416B confined within the bottom source/drain regions 402B are directly coupled to the top HB vias 416T confined within the top source/drain regions 402T, respectively. As such, the first bottom source/drain region 402B1 and the first top source/drain region 402T1 are connected (i.e., having a same

voltage level as the input node SD0 shown in Figures 2A and 2B), the second bottom source/drain region 402B2 and the second top source/drain region 402T2 are connected (i.e., having a same voltage level as the first node SD1 shown in Figures 2A and 2B), the third bottom source/drain region 402B3 and the third top source/drain region 402T3 are connected (i.e., having a same voltage level as the second node SD2 shown in Figures 2A and 2B), and the fourth bottom source/drain region 402B4 and the fourth top source/drain region 402T4 are connected (i.e., having a same voltage level as the output node SD3 shown in Figures 2A and 2B). Although the bottom HB vias 416B confined in the bottom source/drain regions 402B have the same number of the top HB vias 416T confined in the top source/drain regions 402T, each top source/drain region 402T may have an extended device width greater than a corresponding bottom source/drain region 402B. A connection width of each bottom source/drain connection region 402B may be smaller than, equal to, or greater than the device width W2B of the bottom active switch region 404B. A connection width of each top source/drain connection region 402T may be smaller than, equal to, or greater than the device width W2T of the top active switch region 404T. Note that the extra usage of the first top metal layer M1T (e.g., the first gate route lines GRL1, the first body route lines BRL1, and the extended connection width of the top source/drain regions 402T) will help the top HB vias 416T to dissipate heat generated in the top wafer 400T.

[0091] The bottom HB vias 416B confined within the bottom gate connection regions 406B are directly coupled to the top HB vias 416T confined within the top gate connections region 406T, respectively. As such, the first bottom gate connection region 406B1 and the first top gate connection region 406T1 are connected (i.e., having a same voltage level as the first gate terminals G1 shown in Figures 2A and 2B), the second bottom gate connection region 406B2 and the second top gate connection region 406T2 are connected (i.e., having a same voltage level as the first gate terminals G2 shown in Figures 2A and 2B), and the third bottom gate connection region 406B3 and the third top gate connection region 406T3 are connected (i.e., having a same voltage level as the third gate

terminals G3 shown in Figures 2A and 2B). The bottom HB vias 416B confined within the bottom body connection regions 408B are directly coupled to the top HB vias 416T confined within the top body connection regions 408T, respectively. As such, the first bottom body connection region 408B1 and the first
 5 top body connection region 408T1 are connected (i.e., having a same voltage level as the first body terminals B1 shown in Figures 2A and 2B), the second bottom body connection region 408B2 and the second top body connection region 408T2 are connected (i.e., having a same voltage level as the first body terminals B2 shown in Figures 2A and 2B), and the third bottom body connection
 10 region 408B3 and the third top body connection region 408T3 are connected (i.e., having a same voltage level as the third body terminals B3 shown in Figures 2A and 2B).

[0092] In this illustration, the DC voltage biasing to the top FETs Q1T, Q2T, and Q3T in the top wafer 400 are also provided through the bottom gate, body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B, which are located on the bottom wafer 400B. The
 15 resistance values of these bias resistors may be adjusted due to their utilization by both the set of the bottom FETs Q1B, Q2B, and Q3B and the set of the top FETs Q1T, Q2T, and Q3T. In addition, each top FET QxT with the device width W2T in the top wafer 400T is electrically parallel to a corresponding bottom FET QxB with the device width W2B in the bottom wafer 400B. A total device width of the FETs in both the top and bottom wafers 400T and 400B will be $W_{total2} = W2B + W2T$ (where $W2T > W2B$). With the same footprint, the total device width W_{total2} of the FETs in both top and bottom wafers 400T and 400B can be larger
 20 than the total device width W_{total1} of the FETs in both top and bottom wafers 300T and 300B. It is because the areas in the top wafer 400T, which are above the gate, body, and source-drain bias resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B of the bottom wafer 400B, may also be partially or completely utilized to form the top active switch regions 404T. The increased total device
 25 width W_{total2} of the FETs in both top and bottom wafers 400T and 400B may enhance the overall electrical performance (e.g., reduced turn-on resistance) of
 30

the RF switch structure 200. Alternatively, to maintain the same overall electrical performance (e.g., maintain the same turn-on resistance, where $W_{total2} = W_{total1}$), a footprint of the implementation 400 can be smaller than a footprint of the implementation 300 (e.g., a wafer width $WW2$ of the top/bottom wafer 400T/400B is smaller than the wafer width $WW1$ of the top/bottom wafer 300T/300B). In a non-limited example, to achieve the same total device width, the device width $W2B$ of the bottom wafer 400B may be reduced by approximately 25% compared to the device width $W1B$ of the bottom wafer 300B, while the device width $W2T$ of the bottom wafer 400T may be increased by approximately 25% compared to the device width $W1T$ of the top wafer 300T ($W2B \approx 75\% W1B$ and $W2T \approx 125\% W1T$). When the gate, body, and source-drain resistors $RG1B$, $RG2B$, $RG3B$, $RB1B$, $RB2B$, $RB3B$, $RSD1B$, $RSD2B$, and $RSD3B$ are factored in, the wafer width $WW2$ of the top/bottom wafer 400T/400B is about 85% of the wafer width $WW1$ of the top/bottom wafer 300T/300B. An area ratio between the bottom FETs QxB and the bias resistors (the gate, body, and source-drain resistors $RG1B$, $RG2B$, $RG3B$, $RB1B$, $RB2B$, $RB3B$, $RSD1B$, $RSD2B$, and $RSD3B$) will determine the total area/footprint reduction for the implementation 400. The higher that area ratio is, the larger the potential total area/footprint shrink is.

[0093] Note that the concepts of this disclosure are not limited to the device width reduction. Reductions in device length (orthogonal to the device width) as well as reductions in both the device width and device length are possible, depending on where the gate, body, and source-drain resistors $RG1B$, $RG2B$, $RG3B$, $RB1B$, $RB2B$, $RB3B$, $RSD1B$, $RSD2B$, and $RSD3B$ are located in the bottom wafer 400B. When the gate, body, and source-drain resistors $RG1B$, $RG2B$, $RG3B$, $RB1B$, $RB2B$, $RB3B$, $RSD1B$, $RSD2B$, and $RSD3B$ reside only along the device width direction of the bottom active switch regions 404B (as illustrated in Figure 4A), the reductions can be achieved in the device width. When the gate, body, and source-drain resistors $RG1B$, $RG2B$, $RG3B$, $RB1B$, $RB2B$, $RB3B$, $RSD1B$, $RSD2B$, and $RSD3B$ reside only along the length direction of the bottom active switch regions 404B (orthogonal to the device width, not

shown), the reductions can be achieved in the device length. When the gate, body, and source-drain resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B reside along both the device width and the length directions of the bottom active switch regions 404B (not shown), the reductions
5 can be achieved in both the device width and the device length.

[0094] Figure 5 illustrates a flowchart of an exemplary method of providing the implementation 400 of the RF switch structure 200 according to some embodiments of the present disclosure. Although the process steps are illustrated in a series, the process steps are not necessarily order dependent.
10 Some steps may be taken in a different order than that presented. Further, processes within the scope of this disclosure may include fewer or more steps than those illustrated in Figure 5.

[0095] Initially, a bottom wafer (e.g., the bottom wafer 400B) is formed (step 502), which includes a number of bottom active switch regions (e.g., the bottom active switch regions 404B), a number of bias resistors (e.g., the bottom gate, body, and source-drain resistors RG1B, RG2B, RG3B, RB1B, RB2B, RB3B, RSD1B, RSD2B, and RSD3B), and a number of bottom HB vias (e.g., the bottom HB vias 416B). Herein, the bottom active switch regions are configured to provide a number of bottom FETs (e.g., the bottom FETs QxB), respectively,
15 each of which is surrounded by certain ones of the bias resistors in a horizontal plane. The bottom FETs are electrically coupled in series. Each bottom HB via is electrically connected to a corresponding bottom FET and exposed at a top surface of the bottom wafer. The bottom wafer formed herein may also include other components and features as the bottom wafer 400B.

[0096] In addition, a top wafer (e.g., the top wafer 400T) is also formed (step 504), which includes a number of top active switch regions (e.g., the top active switch regions 404T) and a number of top HB vias (e.g., the top HB vias 416T). Herein, the top active switch regions are configured to provide a number of top FETs (e.g., the top FETs QxT), respectively. The top FETs are electrically
20 coupled in series. The top HB vias have a same number as the bottom HB vias and have the same relative positions as the bottom HB vias in the horizontal
30

plane. Each top HB via is electrically connected to a corresponding top FET and exposed at a bottom surface of the top wafer. The top wafer formed herein may also include other components and features as the top wafer 400T.

[0097] Once the bottom wafer and the top wafer are formed, the top wafer is bonded to the bottom wafer (step 506). Herein, each top HB via exposed at the bottom surface of the top wafer is aligned with and directly connected to a corresponding bottom HB via exposed at the top surface of the bottom wafer, such that each top FET and a corresponding bottom FET are electrically parallel to each other. The bias resistors are configured to provide the DC voltage biasing to each top FET and each bottom FET. Each top active switch region is formed over and larger than a corresponding bottom active switch region, and at least partially covers areas of the corresponding ones of the bias resistors within the bottom wafer.

[0098] Figure 6 illustrates a block diagram of an exemplary communication device 600, in which at least one RF switch structure implemented as the implementation 400 shown in Figures 4A-4D can be provided. Herein, the communication device 600 can be any type of communication device, such as mobile terminals, smart watches, tablets, computers, navigation devices, access points, base stations (e.g., eNB or gNB), and any other type of wireless communication devices that support wireless communications, such as cellular, wireless local area network (WLAN), Bluetooth, Ultra-wideband (UWB), and near field communications. The communication device 600 will generally include a control system 602, a baseband processor 604, transmit circuitry 606, receive circuitry 608, antenna switching circuitry 610, multiple antennas 612, and user interface circuitry 614. In a non-limiting example, the control system 602 can be a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC), as an example. In this regard, the control system 602 can include at least a microprocessor(s), an embedded memory circuit(s), and a communication bus interface(s). The receive circuitry 608 receives radio frequency signals via the antennas 612 and through the antenna switching circuitry 610 from one or more base stations. A low noise amplifier and a filter of

the receive circuitry 608 cooperate to amplify and remove broadband interference from the received signal for processing. Down conversion and digitization circuitry (not shown) will then down convert the filtered, received signal to an intermediate or baseband frequency signal, which is then digitized into one or more digital streams using an analog-to-digital converter(s) (ADC).

[0099] The baseband processor 604 processes the digitized received signal to extract the information or data bits conveyed in the received signal. This processing typically comprises demodulation, decoding, and error correction operations, as will be discussed in greater detail below. The baseband processor 604 is generally implemented in one or more digital signal processors (DSPs) and ASICs.

[00100] For transmission, the baseband processor 604 receives digitized data, which may represent voice, data, or control information, from the control system 602, which it encodes for transmission. The encoded data is output to the transmit circuitry 606, where a digital-to-analog converter(s) (DAC) converts the digitally encoded data into an analog signal and a modulator modulates the analog signal onto a carrier signal that is at a desired transmit frequency or frequencies. A power amplifier will amplify the modulated carrier signal to a level appropriate for transmission and deliver the modulated carrier signal to the antennas 612 through the antenna switching circuitry 610 to the antennas 612. The multiple antennas 612 and the replicated transmit and receive circuitries 606, 608 may provide spatial diversity. Modulation and processing details will be understood by those skilled in the art. In some embodiments, the at least one RF switch structure implemented as the implementation 400 shown in Figures 4A-4D may be provided in any one or more of the circuitries in the communication device 600, such as the antenna switching circuitry 610.

[00101] It is contemplated that any of the foregoing aspects, and/or various separate aspects and features as described herein, may be combined for additional advantage. Any of the various embodiments as disclosed herein may be combined with one or more other disclosed embodiments unless indicated to the contrary herein.

[00102] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A radio frequency (RF) switch structure comprising:

5 a bottom wafer including a first bottom active switch region, a plurality of first bias resistors, and a plurality of bottom hybrid bond (HB) vias, wherein:

the first bottom active switch region is configured to provide a first bottom field-effect transistor (FET), which is surrounded by the plurality of first bias resistors in a horizontal plane; and

10 certain ones of the plurality of bottom HB vias are electrically connected to the first bottom FET and exposed at a top surface of the bottom wafer; and

a top wafer formed over the bottom wafer and including a first top active switch region and a plurality of top HB vias, wherein:

15 the first top active switch region is configured to provide a first top FET and is formed over the first bottom active switch region;

certain ones of the plurality of top HB vias are electrically connected to the first top FET, exposed at a bottom surface of the top wafer, and are aligned with and directly connected to the certain ones of the plurality of bottom HB vias, respectively, such that the first top FET and the first bottom FET are electrically parallel to each other;

20 the plurality of first bias resistors is configured to provide direct current (DC) voltage biasing to both the first top FET and the first bottom FET; and

25 the first top active switch region is larger than the first bottom active switch region, and at least partially covers areas of the plurality of first bias resistors within the bottom wafer.

2. The RF switch structure of claim 1 wherein the first bottom FET and the first top FET are multi-finger transistors.

30

3. The RF switch structure of claim 1 wherein each of the first bottom FET and the first top FET is a bilateral device, in which a source and a drain are interchangeable.

5 4. The RF switch structure of claim 3 wherein:

the bottom wafer further includes a first bottom source/drain connection region, a second bottom source/drain connection region, and a first bottom gate connection region;

10 the first bottom source/drain connection region is connected to a drain of the first bottom FET, the second bottom source/drain connection region is connected to a source of the first bottom FET, and the first bottom gate connection region is connected to a gate of the first bottom FET;

15 the top wafer further includes a first top source/drain connection region, a second top source/drain connection region, and a first top gate connection region;

the first top source/drain connection region is connected to a drain of the first top FET, the second top source/drain connection region is connected to a source of the first top FET, and the first top gate connection region is connected to a gate of the first top FET;

20 one or more of the plurality of bottom HB vias are confined within and connected to the first bottom source/drain connection region, the second bottom source/drain connection region, and the first bottom gate connection region, respectively; and

25 one or more of the plurality of top HB vias are confined within and connected to the first top source/drain connection region, the second top source/drain connection region, and the first top gate connection region, respectively.

5. The RF switch structure of claim 4 wherein:

30 the bottom wafer further includes a first bottom body connection region, which is connected to a body of the first bottom FET;

one or more of the plurality of bottom HB vias are confined within and connected to the first bottom body connection region;

the top wafer further includes a first top body connection region, which is connected to a body of the first top FET; and

5 one or more of the plurality of top HB vias are confined within and connected to the first top body connection region.

6. The RF switch structure of claim 5 wherein:

the first bottom source/drain connection region, the second bottom
10 source/drain connection region, the first bottom gate connection region, and the first bottom body connection region are formed from a same first bottom metal layer, which is at a higher vertical level than the first bottom active switch region; and

the first top source/drain connection region, the second top source/drain
15 connection region, the first top gate connection region, and the first top body connection region are formed from a same first top metal layer, which is at a lower vertical level than the first top active switch region.

7. The RF switch structure of claim 6 wherein:

20 the first bottom active switch region is located between the first bottom source/drain connection region and the second bottom source/drain connection region in the horizontal plane; and

the first top active switch region is located between the first top
source/drain connection region and the second top source/drain connection
25 region in the horizontal plane; and

the first top gate connection region and the first top body connection region are below and confined in the first top active switch region.

8. The RF switch structure of claim 7 wherein:

30 the top wafer further includes a first gate route line, a first body route line, a first gate vertical via, and a first body vertical via;

the first gate route line is formed from the first top metal layer and provides an electrical connection from the first top gate connection region towards a location horizontally outside of the first top active switch region;

the first body route line is formed from the first top metal layer and
5 provides an electrical connection from the first top body connection region towards a location horizontally outside of the first top active switch region;

the first gate vertical via and the first body vertical via are located horizontally outside of the first top active switch region; and

the first gate vertical via extends vertically from the first gate route line
10 towards a metal layer over the first top metal layer, while the first body vertical via extends vertically from the first body route line towards the metal layer over the first top metal layer, wherein the first top gate connection region is connected to the gate of the first top FET at least through the first gate route line and the first gate vertical via, and the first top body connection region is connected to the
15 body of the first top FET at least through the first body route line and the first body vertical via.

9. The RF switch structure of claim 6 wherein the first bottom gate connection region and the first bottom body connection region are horizontally
20 outside the first bottom active switch region.

10. The RF switch structure of claim 4 wherein:
a width of each of the first top source/drain connection region and the second top source/drain connection region is greater than a width of each of the
25 first bottom source/drain connection region and the second bottom source/drain connection region.

11. The RF switch structure of claim 10 wherein:
the first bottom source/drain connection region and the second bottom
30 source/drain connection region have a same first connection width, and the first

top source/drain connection region and the second top source/drain connection region have a same second connection width; and

the second connection width is greater than the first connection width.

5 12. The RF switch structure of claim 1 wherein:

the plurality of first bias resistors includes at least a first gate bias resistor and a first source-drain bias resistor; and

the first gate bias resistor is electrically coupled between a gate of the first bottom FET and a gate terminal providing a gate voltage signal, and the first
10 source-drain bias resistor is electrically coupled between a drain of the first bottom FET and a source of the first bottom FET.

13. The RF switch structure of claim 12 wherein:

the bottom wafer further includes a first bottom source/drain connection
15 region, a second bottom source/drain connection region, and a first bottom gate connection region;

the first bottom source/drain connection region is connected to the drain of the first bottom FET, the second bottom source/drain connection region is connected to the source of the first bottom FET, and the first bottom gate
20 connection region is connected to the gate of the first bottom FET;

the top wafer further includes a first top source/drain connection region, a second top source/drain connection region, and a first top gate connection region;

the first top source/drain connection region is connected to a drain of the
25 first top FET, the second top source/drain connection region is connected to a source of the first top FET, and the first top gate connection region is connected to a gate of the first top FET;

one or more of the plurality of bottom HB vias are confined within and connected to the first bottom source/drain connection region, the second bottom
30 source/drain connection region, and the first bottom gate connection region, respectively; and

one or more of the plurality of top HB vias are confined within and connected to the first top source/drain connection region, the second top source/drain connection region, and the first top gate connection region, respectively.

5

14. The RF switch structure of claim 12 wherein:

the plurality of first bias resistors further includes a first body bias resistor, which is electrically coupled between a body of the first bottom FET and a body terminal providing a body voltage signal.

10

15. The RF switch structure of claim 14 wherein:

the bottom wafer further includes a first bottom source/drain connection region, a second bottom source/drain connection region, a first bottom gate connection region, and a first bottom body connection region;

15

the first bottom source/drain connection region is connected to the drain of the first bottom FET, the second bottom source/drain connection region is connected to the source of the first bottom FET, the first bottom gate connection region is connected to the gate of the first bottom FET, and a first bottom body connection region is connected to the body of the first bottom FET;

20

the top wafer further includes a first top source/drain connection region, a second top source/drain connection region, a first top gate connection region, and a first top body connection region;

the first top source/drain connection region is connected to a drain of the first top FET, the second top source/drain connection region is connected to a source of the first top FET, the first top gate connection region is connected to a gate of the first top FET, and a first top body connection region is connected to a body of the first top FET;

25

one or more of the plurality of bottom HB vias are confined within and connected to the first bottom source/drain connection region, the second bottom source/drain connection region, the first bottom gate connection region, and the first bottom body connection region, respectively; and

30

one or more of the plurality of top HB vias are confined within and connected to the first top source/drain connection region, the second top source/drain connection region, the first top gate connection region, and the first top body connection region, respectively.

5

16. The RF switch structure of claim 1 wherein:

the plurality of first bias resistors is placed around the bottom active switch region along a device width direction; and

the first top active switch region is over the first bottom active switch region and extends in the device width direction to at least partially cover the areas of the plurality of first bias resistors within the bottom wafer, such that the first top active switch region has a larger device width than the first bottom active switch region.

15 17. The RF switch structure of claim 1 wherein:

the bottom wafer includes a plurality of bottom active switch regions, wherein the first bottom active switch region is included in the plurality of bottom active switch regions;

the top wafer includes a plurality of top active switch regions, wherein the first top active switch region is included in the plurality of top active switch regions;

the plurality of bottom active switch regions is configured to provide a plurality of bottom FETs, respectively, and the plurality of top active switch regions is configured to provide a plurality of top FETs, respectively;

the plurality of bottom FETs is electrically coupled in series within the bottom wafer, and the plurality of top FETs is electrically coupled in series within the top wafer;

each of the plurality of bottom HB vias is exposed at the top surface of the bottom wafer, and electrically connected to a corresponding one of the plurality of bottom FETs; and

30

each of the plurality of top HB vias is exposed at the bottom surface of the top wafer, electrically connected to a corresponding one of the plurality of top FETs, and aligned with and directly connected to a corresponding one of the plurality of bottom HB vias, such that each of the plurality of bottom FETs is
5 electrically parallel to a corresponding one of the plurality of top FETs.

18. The RF switch structure of claim 17 wherein a number of the plurality of bottom HB vias is the same as a number of the plurality of top HB vias.

10 19. The RF switch structure of claim 17 wherein:
the bottom wafer includes a plurality of bias resistors, wherein the plurality of first bias resistors is included in the plurality of bias resistors;
each of the plurality of bottom active switch regions is surrounded by
corresponding ones of the plurality of bias resistors in the horizontal plane;
15 the plurality of bias resistors is configured to provide DC voltage biasing to each of the plurality of bottom FETs and each of the plurality of top FETs; and
each of the plurality of top active switch regions is formed over and larger than a corresponding one of the plurality of bottom active switch regions, and at least partially covers areas of the corresponding ones of the plurality of bias
20 resistors within the bottom wafer.

20. The RF switch structure of claim 19 wherein:
the bottom wafer further includes a plurality of bottom source/drain connection regions and a plurality of bottom gate connection regions;
25 each of the plurality of bottom source/drain connection regions is connected to a drain or a source of a corresponding one of the plurality of bottom FETs, or connected to a drain and a source of two adjacent ones of the plurality of bottom FETs;
each of the plurality of bottom gate connection regions is connected to a
30 gate of the corresponding one of the plurality of bottom FETs;

the top wafer further includes a plurality of top source/drain connection regions and a plurality of top gate connection regions;

each of the plurality of top source/drain connection regions is connected to a drain or a source of a corresponding one of the plurality of top FETs, or
5 connected to a drain and a source of two adjacent ones of the plurality of top FETs;

each of the plurality of top gate connection regions is connected to a gate of the corresponding one of the plurality of top FETs;

one or more of the plurality of bottom HB vias are confined within and
10 connected to each of the plurality of bottom source/drain connection regions and each of the plurality of bottom gate connection regions, respectively; and

one or more of the plurality of top HB vias are confined within and connected to each of the plurality of top source/drain connection regions and each of the plurality of top gate connection regions, respectively.

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21. The RF switch structure of claim 20 wherein:

the bottom wafer further includes a plurality of bottom body connection regions, each of which is connected to a body of the corresponding one of the plurality of bottom FETs;

20 the top wafer further includes a plurality of top body connection regions, each of which is connected to a body of the corresponding one of the plurality of top FETs;

one or more of the plurality of bottom HB vias are confined within and connected to each of the plurality of bottom body connection regions; and

25 one or more of the plurality of top HB vias are confined within and connected to each of the plurality of top body connection regions.

22. The RF switch structure of claim 21 wherein:

30 the plurality of bottom source/drain connection regions, the plurality of bottom gate connection regions, and the plurality of bottom body connection

regions are formed from a same first bottom metal layer, which is at a higher vertical level than the plurality of bottom active switch regions; and

the plurality of top source/drain connection regions, the plurality of top gate connection regions, and the plurality of top body connection regions are
5 formed from a same first top metal layer, which is at a lower vertical level than the plurality of top active switch regions.

23. The RF switch structure of claim 22 wherein:

each of the plurality of bottom active switch regions is located between
10 two of the plurality of bottom source/drain connection regions in the horizontal plane;

each of the plurality of top active switch regions is located between two of the plurality of top source/drain connection regions in the horizontal plane; and

each of the plurality of top gate connection regions and each of the
15 plurality of top body connection regions are confined in a corresponding one of the plurality of top active switch regions.

24. The RF switch structure of claim 22 wherein each of the plurality of bottom gate connection regions and each of the plurality of bottom body connection
20 regions are horizontally outside a corresponding one of the plurality of bottom active switch regions.

25. The RF switch structure of claim 19 wherein:

the plurality of bias resistors is placed around the plurality of bottom active
25 switch regions along a device width direction; and

each of the plurality of top active switch regions is over a corresponding one of the plurality of bottom active switch regions and extends in the device width direction to at least partially cover the areas of the plurality of bias resistors within the bottom wafer, such that each of the plurality of top active switch
30 regions has a larger device width than the corresponding one of the plurality of bottom active switch regions.

26. A communication device comprising:

receive circuitry;

transmit circuitry; and

5 antenna switching circuitry, which is configured to transmit radio frequency signals between antennas and the receive circuitry and/or between the antennas and the transmit circuitry, wherein at least the antenna switching circuitry includes an RF switch structure comprising:

10 a bottom wafer including a first bottom active switch region, a plurality of first bias resistors, and a plurality of bottom hybrid bond (HB) vias, wherein:

the first bottom active switch region is configured to provide a first bottom field-effect transistor (FET), which is surrounded by the plurality of first bias resistors in a horizontal plane; and

15 certain ones of the plurality of bottom HB vias are electrically connected to the first bottom FET and exposed at a top surface of the bottom wafer; and

a top wafer formed over the bottom wafer and including a first top active switch region and a plurality of top HB vias, wherein:

20 the first top active switch region is configured to provide a first top FET and is formed over the first bottom active switch region;

25 certain ones of the plurality of top HB vias are electrically connected to the first top FET, exposed at a bottom surface of the top wafer, and are aligned with and directly connected to the certain ones of the plurality of bottom HB vias, respectively, such that the first top FET and the first bottom FET are electrically parallel to each other;

30 the plurality of first bias resistors is configured to provide direct current (DC) voltage biasing to both the first top FET and the first bottom FET; and

the first top active switch region is larger than the first bottom active switch region, and at least partially covers areas of the plurality of first bias resistors within the bottom wafer.

- 5 27. A method of implementing a radio frequency (RF) switch structure comprising:

forming a bottom wafer that includes a first bottom active switch region, a plurality of first bias resistors, and a plurality of bottom hybrid bond (HB) vias, wherein:

- 10 the first bottom active switch region is configured to provide a first bottom field-effect transistor (FET), which is surrounded by the plurality of first bias resistors in a horizontal plane; and

each of the plurality of bottom HB vias is electrically connected to the first bottom FET and exposed at a top surface of the bottom wafer;

- 15 forming a top wafer that includes a first top active switch region and a plurality of top HB vias, wherein:

the first top active switch region is configured to provide a first top FET; and

- 20 each of the plurality of top HB vias is electrically connected to the first top FET, and exposed at a bottom surface of the top wafer; and bonding the top wafer to the bottom wafer, wherein:

- 25 each of the plurality of top HB vias exposed at the bottom surface of the top wafer is aligned with and directly connected to a corresponding one of the plurality of bottom HB vias exposed at the top surface of the bottom wafer, such that the first top FET and the first bottom FET are electrically parallel to each other;

the plurality of first bias resistors is configured to provide direct current (DC) voltage biasing to both the first top FET and the first bottom FET; and

the first top active switch region is located over and larger than the first bottom active switch region, and at least partially covers areas of the plurality of first bias resistors within the bottom wafer.

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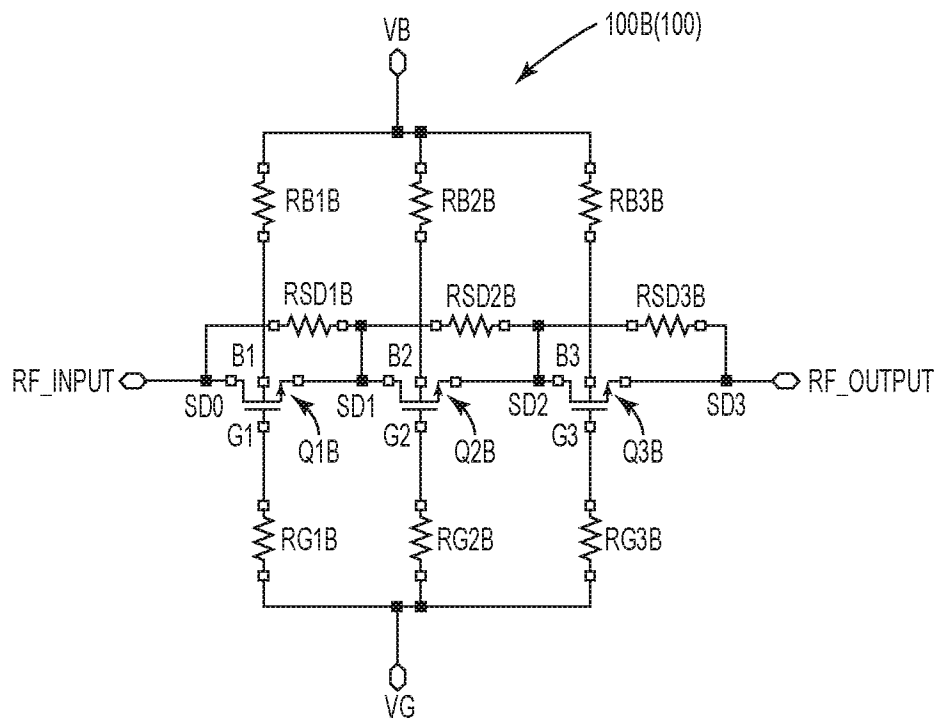


FIG. 1A

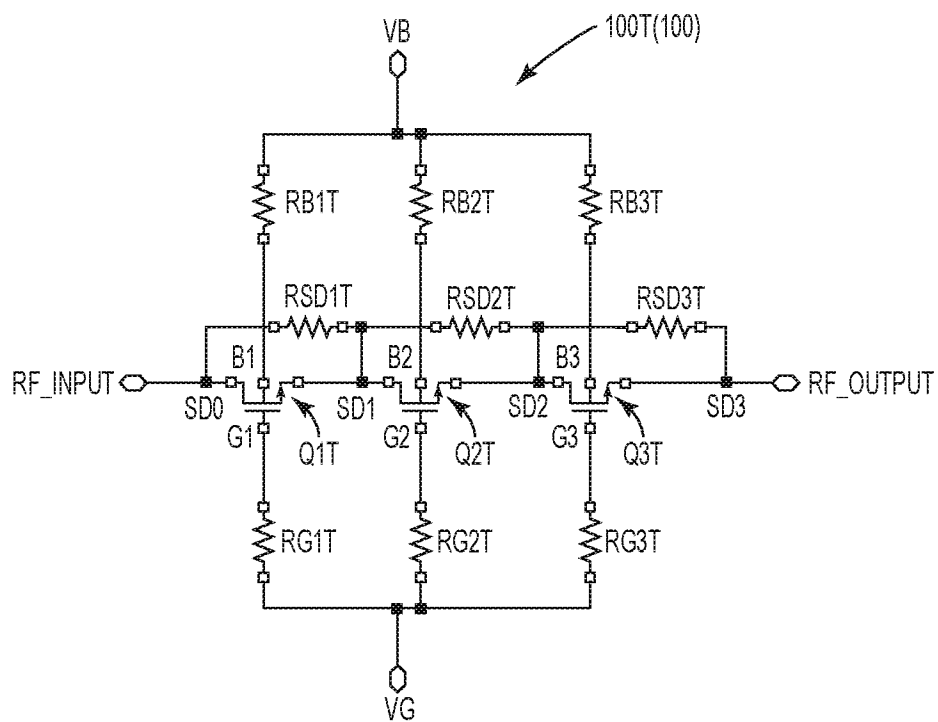


FIG. 1B

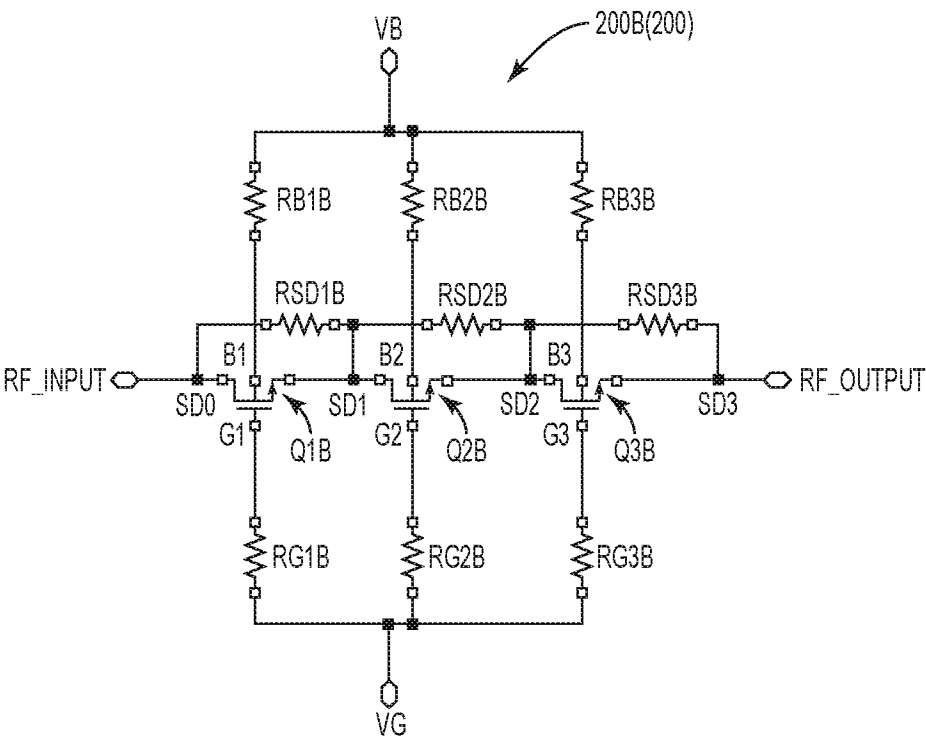


FIG. 2A

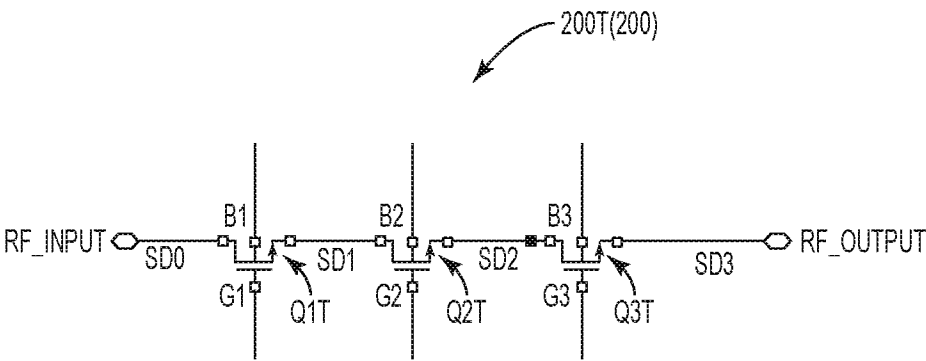


FIG. 2B

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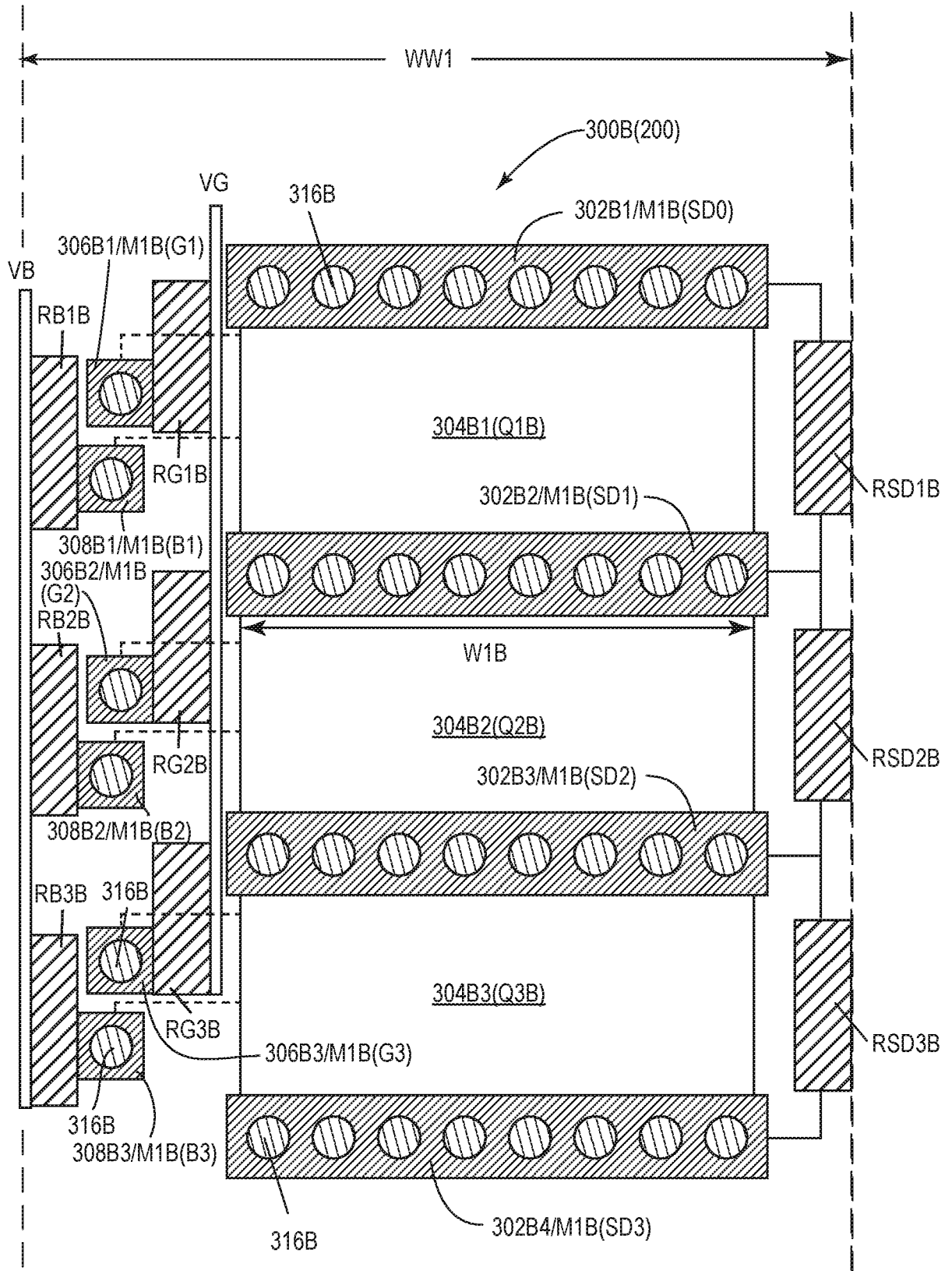


FIG. 3A

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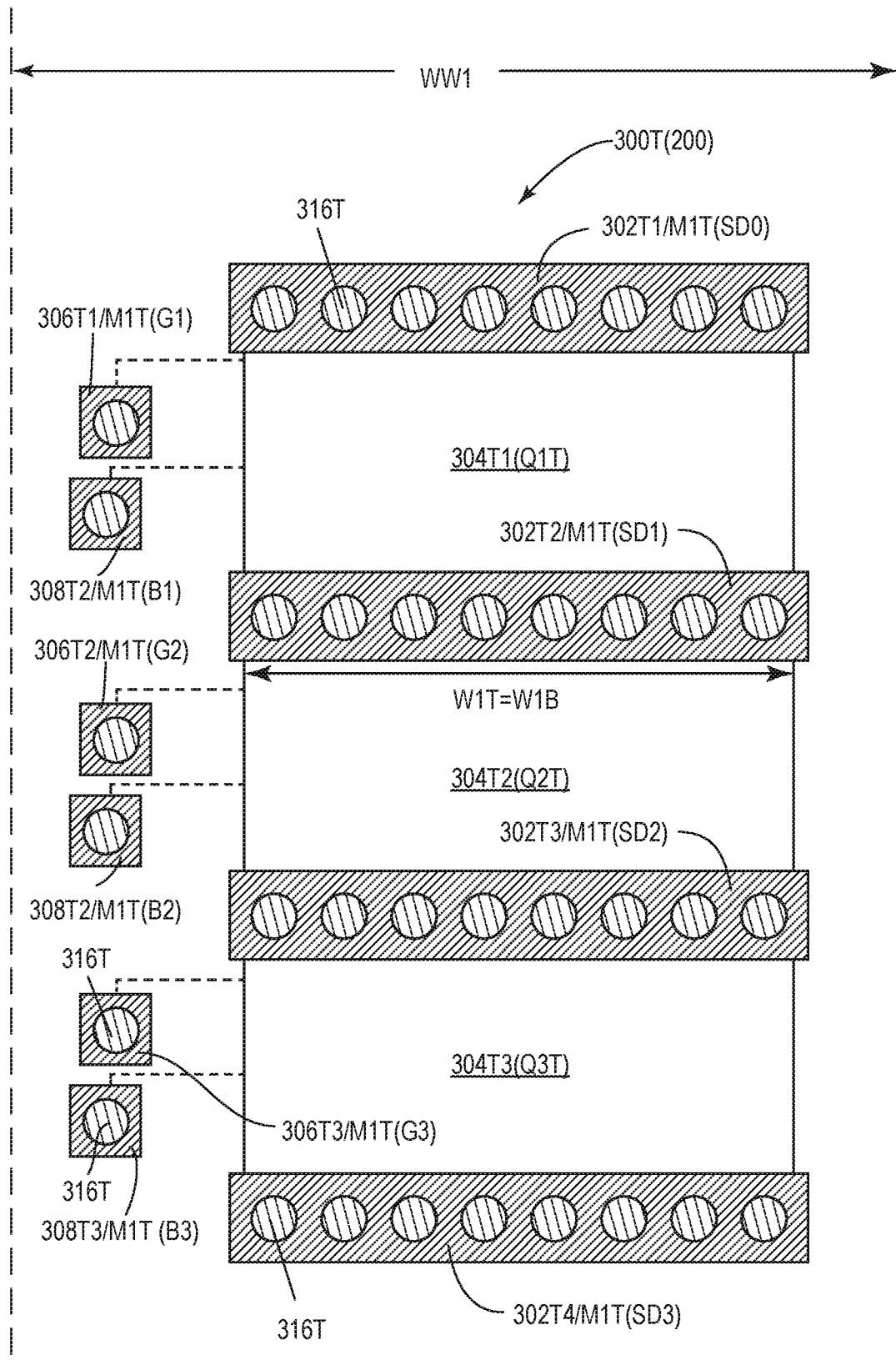


FIG. 3B

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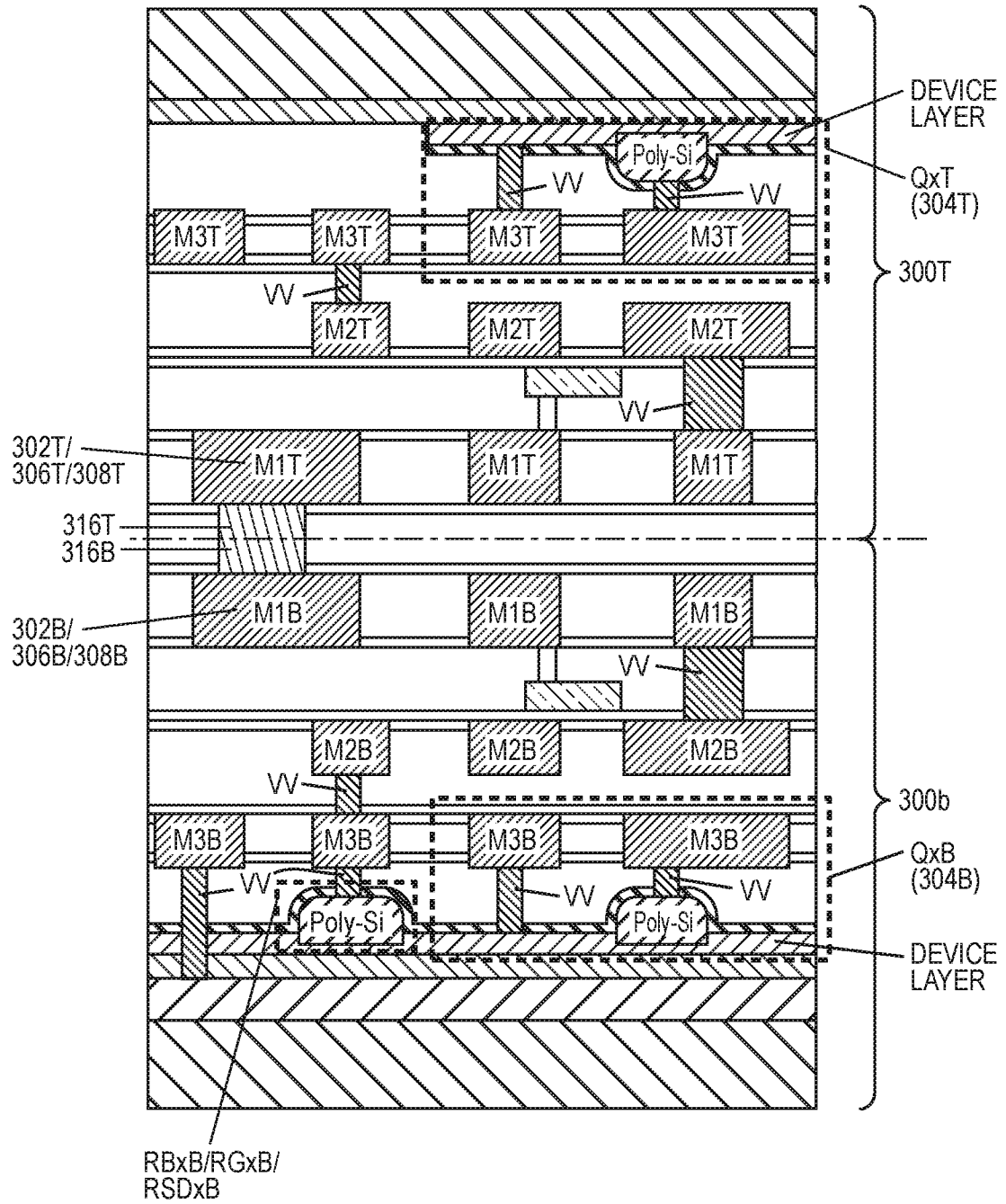


FIG. 3C

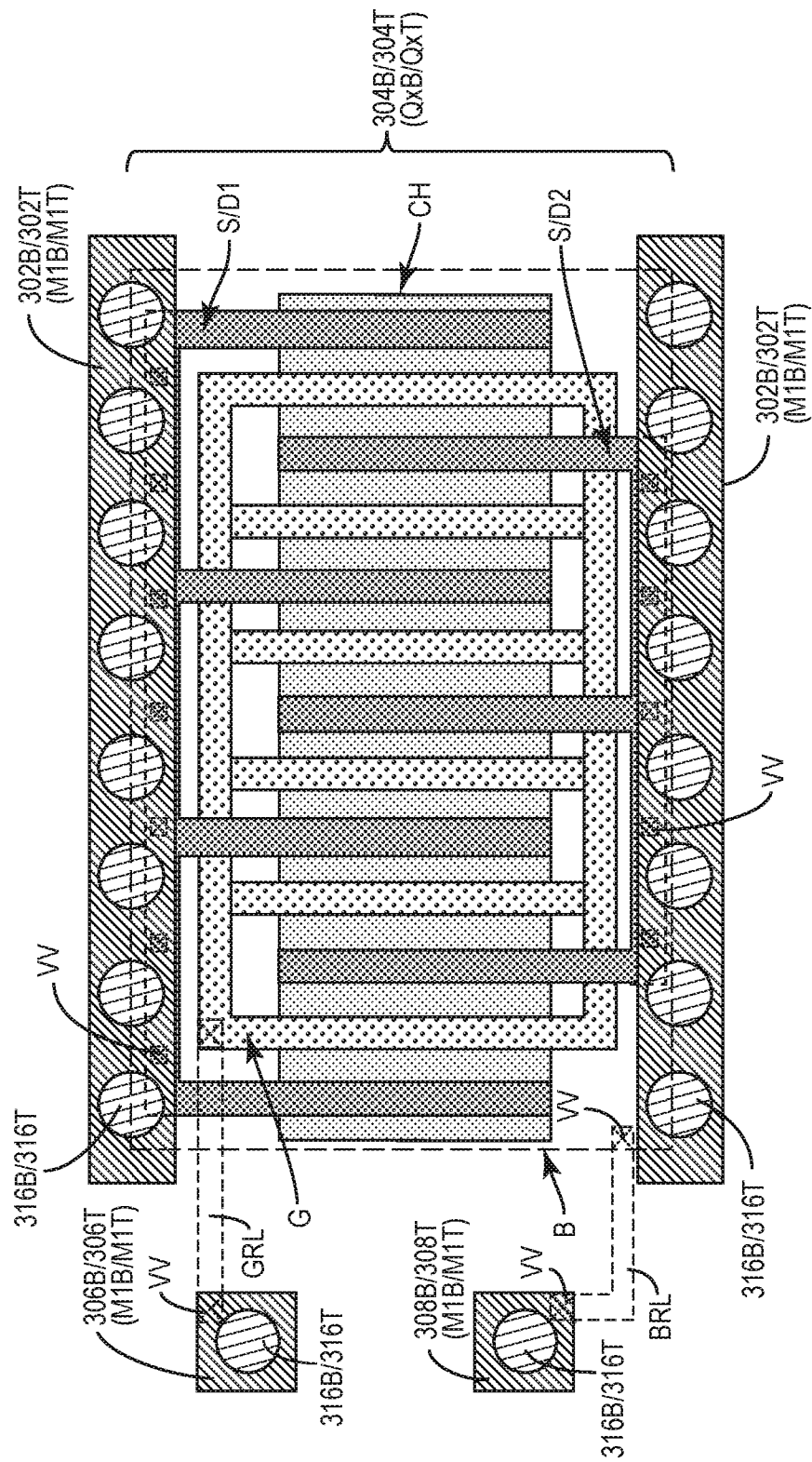


FIG. 3D

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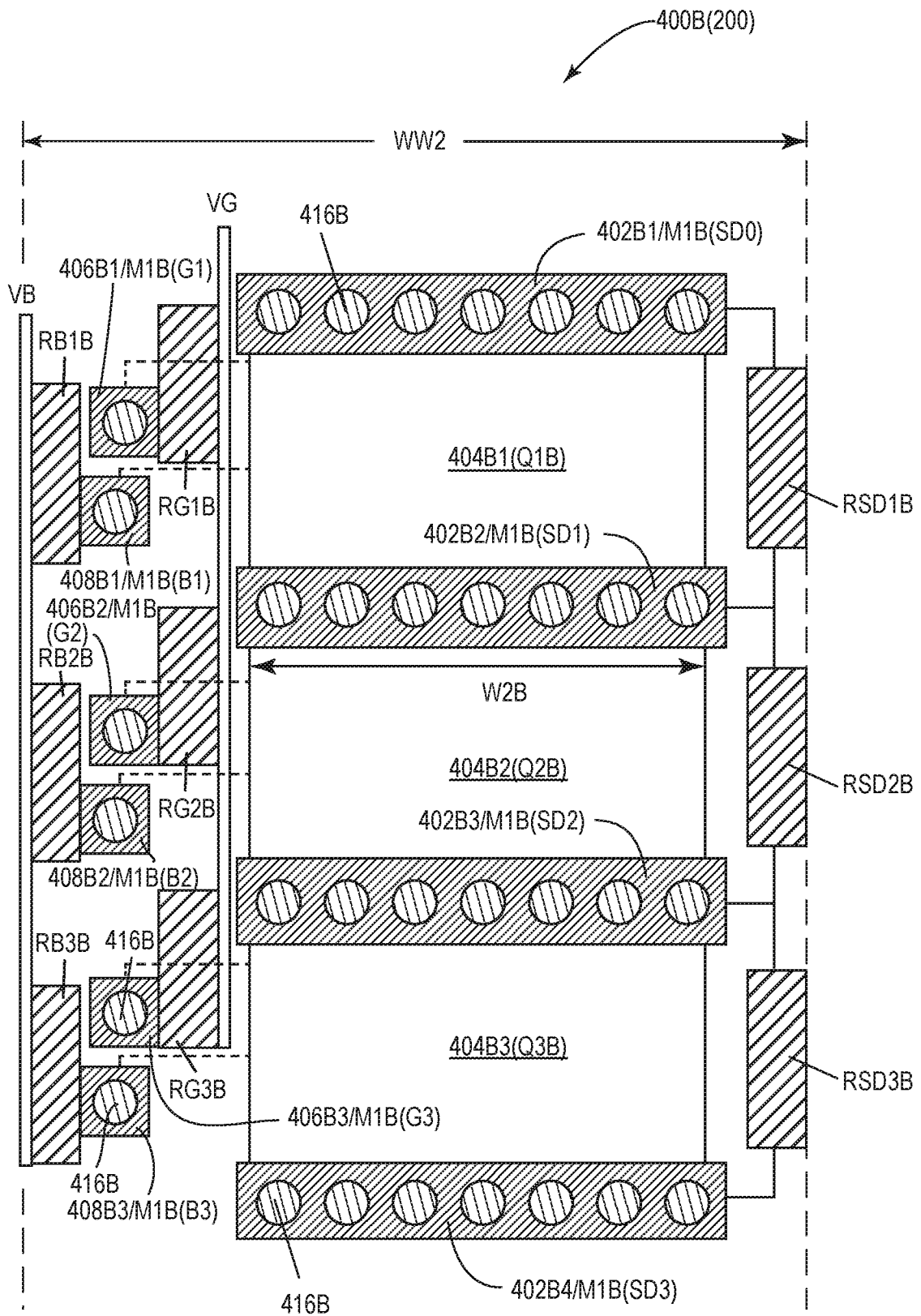


FIG. 4A

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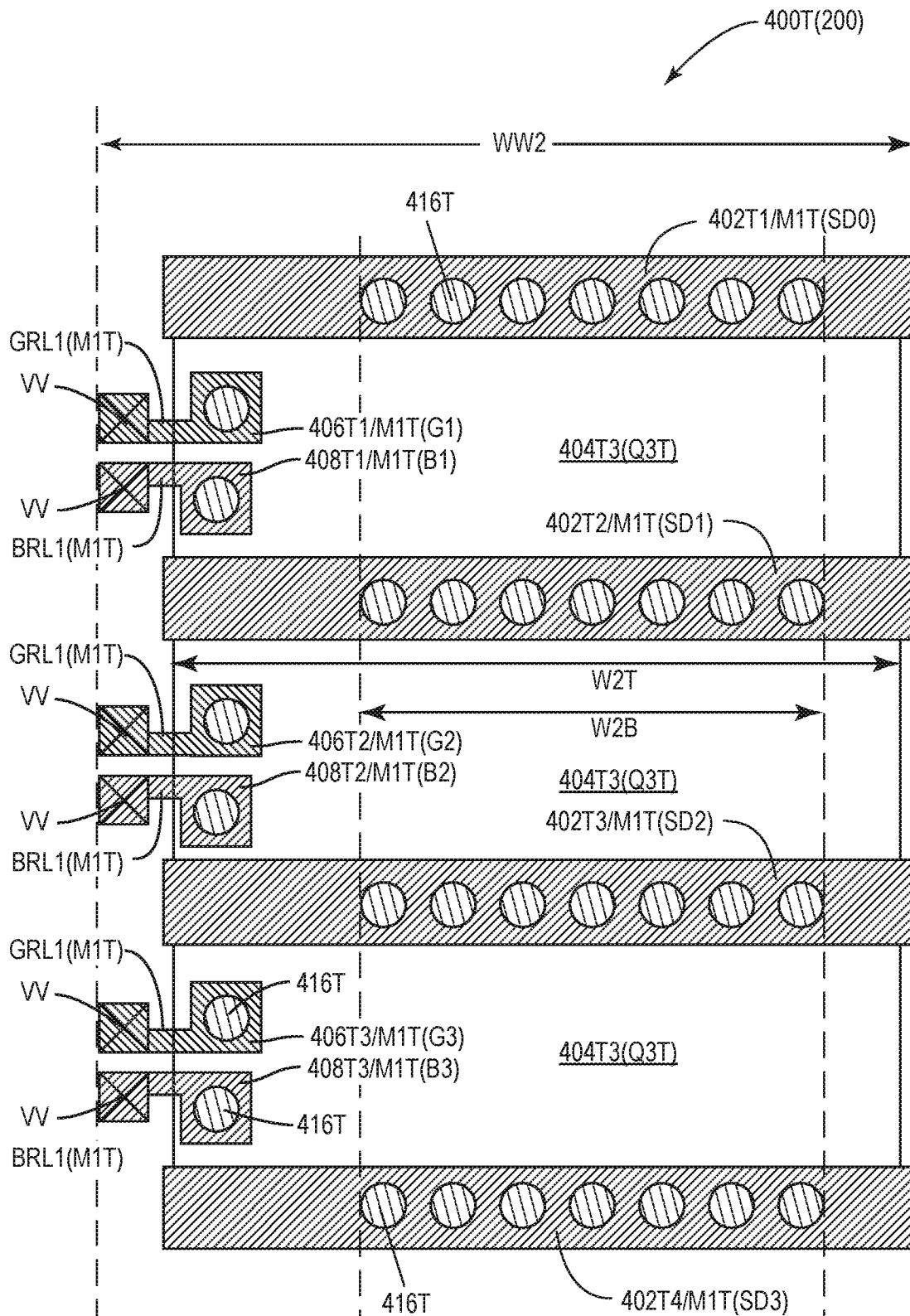


FIG. 4B

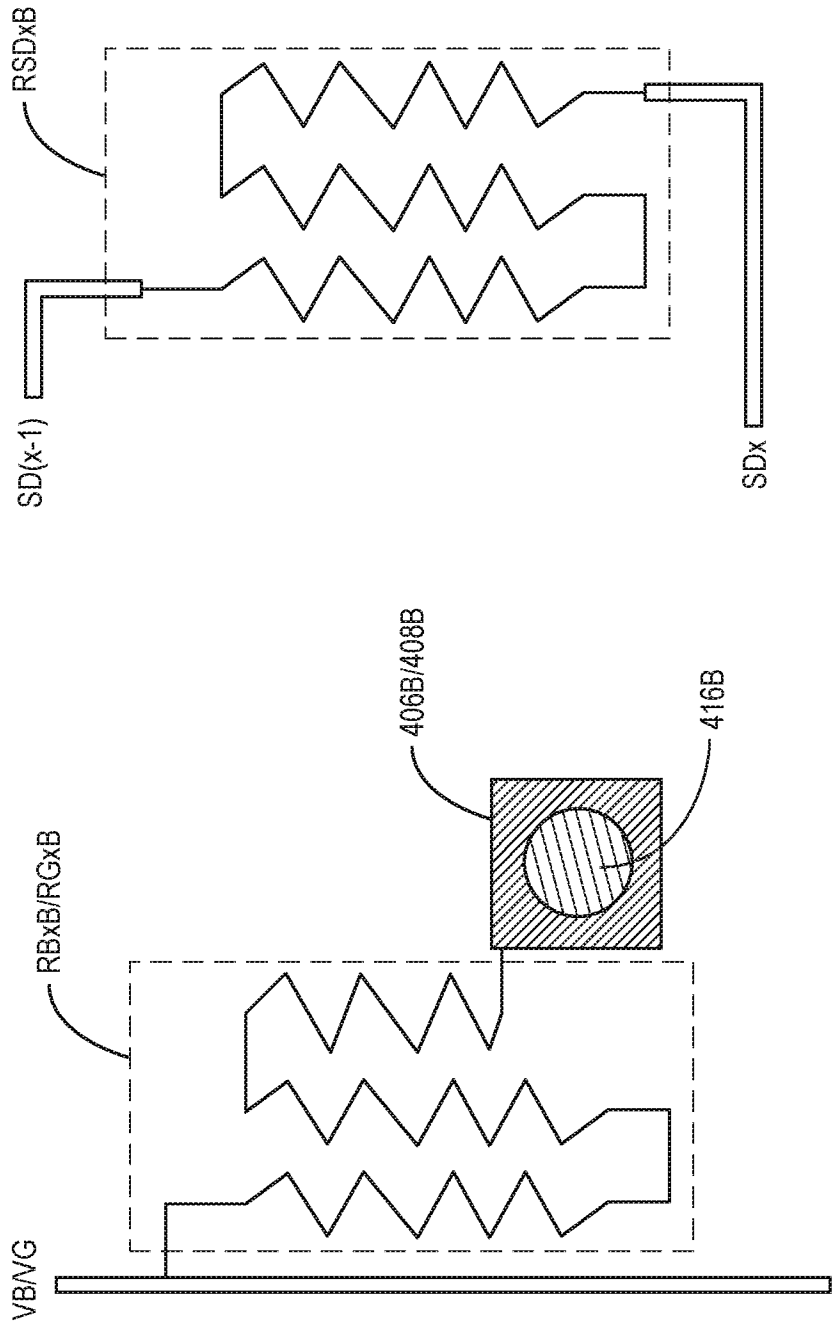


FIG. 4C

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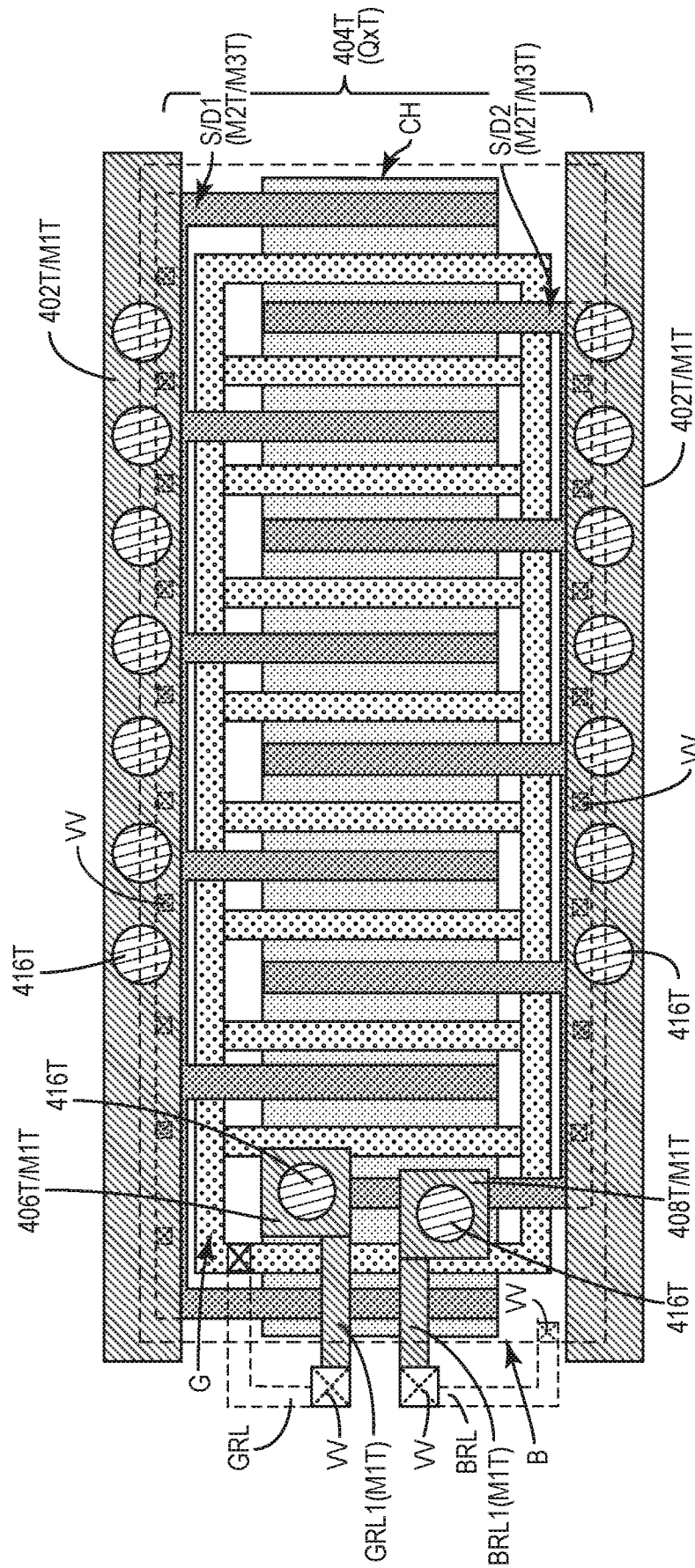
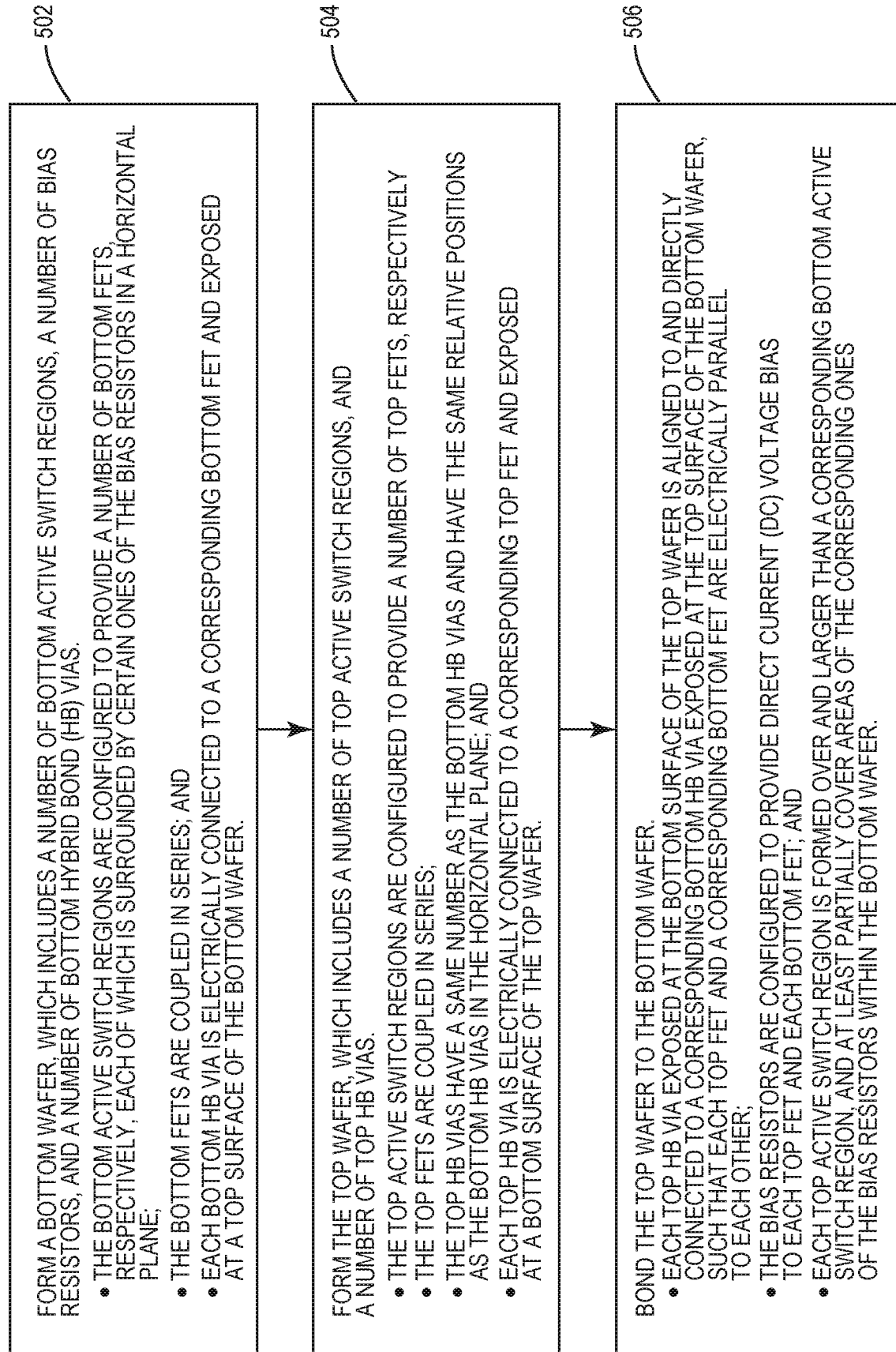


FIG. 4D

**FIG. 5**

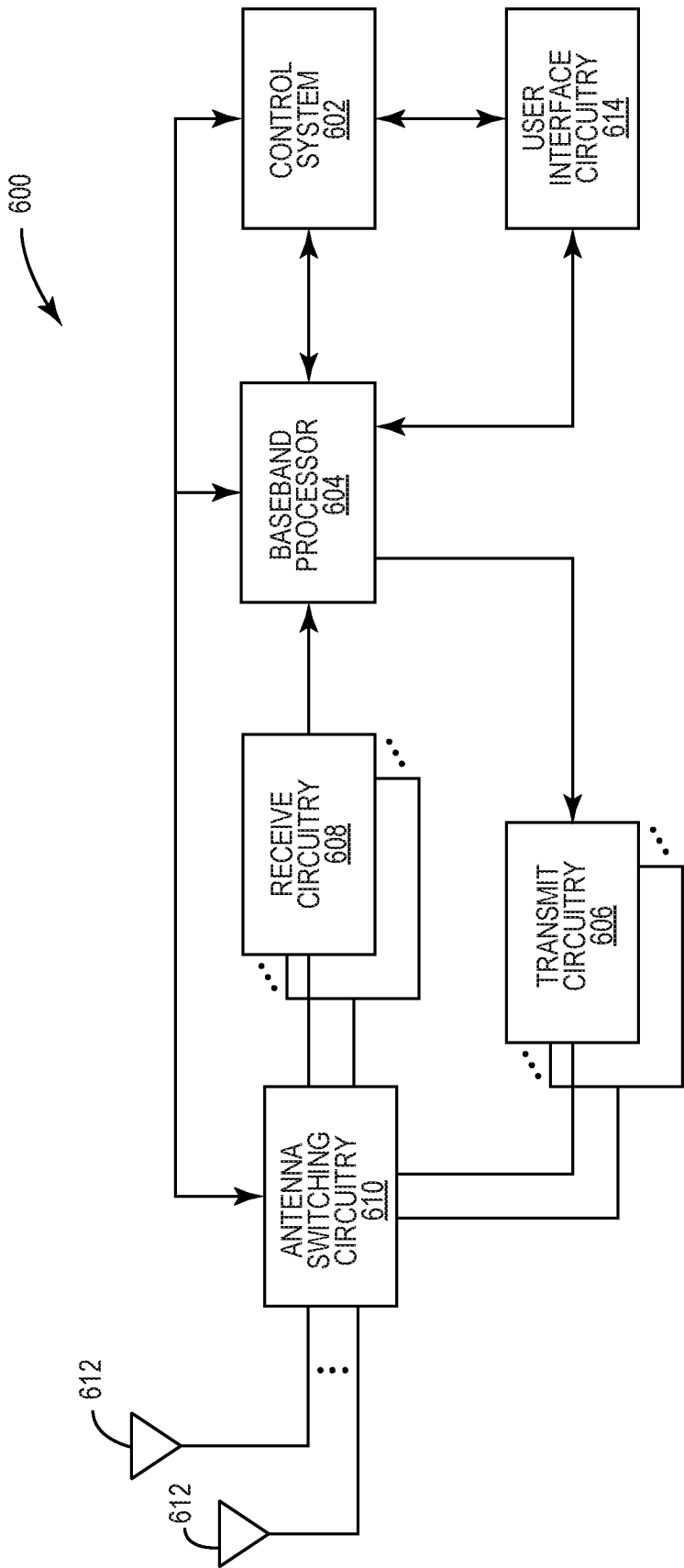


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/057669

A. CLASSIFICATION OF SUBJECT MATTER					
INV.	H03K17/10	H03K17/693	H10D80/00	H01L23/66	H01L23/00
	H01L25/065	H03F3/195	H03F3/21	H03F3/24	
ADD.					
According to International Patent Classification (IPC) or to both national classification and IPC					
B. FIELDS SEARCHED					
Minimum documentation searched (classification system followed by classification symbols)					
H03K H10D H01L					
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched					
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)					
EPO-Internal					
C. DOCUMENTS CONSIDERED TO BE RELEVANT					
Category*	Citation of document, with indication, where appropriate, of the relevant passages				Relevant to claim No.
A	WO 2023/200691 A1 (PSEMI CORP [US]) 19 October 2023 (2023-10-19) paragraphs [0071] - [0075]; figures 11A, 11B -----				1 - 27
A	US 2020/395936 A1 (BLIN GUILLAUME ALEXANDRE [US]) 17 December 2020 (2020-12-17) paragraphs [0058] - [0064]; figures 8,9 -----				1 - 27
A	US 2021/074730 A1 (STAMPER ANTHONY K [US] ET AL) 11 March 2021 (2021-03-11) paragraph [0029]; figures 1-19 -----				1 - 27
A	US 2021/013119 A1 (VERMA PURAKH RAJ [SG] ET AL) 14 January 2021 (2021-01-14) figure 18 -----				1 - 27
☐ Further documents are listed in the continuation of Box C.					
☒ See patent family annex.					
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"E" earlier application or patent but published on or after the international filing date			"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone		
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)			"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art		
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"P" document published prior to the international filing date but later than the priority date claimed					
Date of the actual completion of the international search			Date of mailing of the international search report		
5 March 2025			17/03/2025		
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016			Authorized officer Le Gallo, Thomas		

INTERNATIONAL SEARCH REPORT

Information on patent family members

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