



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<b>(51) International Patent Classification <sup>3</sup>:</b>  <b>H04J 15/00</b>	<b>A1</b>	<b>(11) International Publication Number:</b> WO 80/01228  <b>(43) International Publication Date:</b> 12 June 1980 (12.06.80)
<b>(21) International Application Number:</b> PCT/DK79/00054  <b>(22) International Filing Date:</b> 30 November 1979 (30.11.79)  <b>(31) Priority Application Number:</b> 5471/78  <b>(32) Priority Date:</b> 1 December 1978 (01.12.78)  <b>(33) Priority Country:</b> DK  <b>(71) Applicant (for all designated States except US):</b> FORSVA- RETS FORSKNINGSTJENESTE [DK/DK]; Øster- brogades Kaserne, DK-2100 København Ø, (DK).  <b>(72) Inventor; and</b> <b>(75) Inventor/Applicant (for US only):</b> BROCK-NANNE- STAD, Lars, Verner [DK/DK]; Bakketoppen 4, DK- 2830 Virum (DK).  <b>(74) Agent:</b> HOFMAN-BANG & BOUTARD; Adelgade 15, DK-1304 København K, (DK).		<b>(81) Designated States:</b> DE, DE (European patent), FR (Eu- ropean patent), GB, GB (European patent), JP, NL, NL (European patent), SE, SE (European patent), US.  <b>Published</b> <i>With international search report</i> <i>In English translation (filed in Danish)</i>
<b>(54) Title:</b> A PROCESS AND AN APPARATUS FOR TRANSFERRING INFORMATION REPRESENTING AT LEAST TWO PARAMETERS		
<b>(57) Abstract</b>  <p>A process and an apparatus for transferring information representing a plurality of parameters which are each indicated by a plurality of digits of different weight. The parameters may represent a plurality of measurable states of an arbitrary type, e.g. two coordinates on a display, the parameter value being a measure of the state. The most important digit is first transferred from all the parameters in a predetermined sequence, and then the digit next in importance from all the parameters in the same predetermined sequence, and so on, until a desired accuracy or resolutibility for the parameter values has been achieved, depending upon the state of operation, and transfer of information is then discontinued so that the row of digits is not necessarily transferred entirely. This is achieved by the connection, shown in fig. 1, between the registers (1, 2, 3, 4), the buffer register (6) and the main register (5), from which the information is read out serially.</p>		

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A process and an apparatus for transferring information representing at least two parameters

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The invention relates to a process for transferring information representing a plurality of parameters which are each defined by a plurality of measureable states of an arbitrary type, the parameter value being a  
5 measure of the state. The invention will be explained below substantially with respect to the case where there are two parameters which define their respective co-ordinates in a two-dimensional system of co-ordinates. If the system of co-ordinates e.g. belongs to a display,  
10 a great number of associated parameter values may define an image matrix used for optical reading of e.g. alphanumeric characters.

The resolubility of the parameters depends upon the number of digits each parameter contains in a given  
15 system of notation. As the time of information transfer is proportional to the total number of digits it will be appreciated that a known serial transfer of all the parameter digits will take an unnecessarily long time if, in a given case, a significantly lower resolubility will  
20 suffice, e.g. for representing an image of a number, than is needed to represent a more complicated pattern.

The object of the invention is to provide a process for transferring information from two or more data sources, in which the information is serially transferred in data  
25 groups each of which contains a single bit from each data source, said process permitting a variable resolubility to be achieved in a very simple manner so that the transfer of information may be adapted in particular to rate of transfer and sensivitivity to noise, depending  
30 upon the necessary and sufficient resolubility.



This object is achieved by arranging each data source so as to represent a parameter, such as a co-ordinate in a system of co-ordinates, so that the weight of each digit in a parameter represents a predetermined digit position in the corresponding data source and by interrupting the transfer of the row of digits thus produced when the transferred partial row represents each parameter with a predetermined accuracy. By combining the features of a front portion of the digit row representing with reduced resolubility all the parameters and of interrupting the transfer of the row, as stated, the resolubility and transmission time can be varied according to the number of digits in sequence which are included in the transfer of information.

- 15 As the weight of the digits in said row of digits thus gradually decreases it is, as stated in claim 2, expedient to have the digit of the greatest weight, which originates from the most important parameter to be transferred, in the front of the sequence.
- 20 As according to the invention the digits are arranged in groups of uniform weight, there will be empty places in the sequence of the digits if only one of the parameters contains fewer digits than the other parameters. These empty places may advantageously be used for digits for error detection or flag characters, as stated in claim 3.

The invention is not restricted to a specific system of notation since each digit may be represented by an electric voltage having a plurality of discrete voltage levels corresponding to the radix of the system of notation. Owing to modern technology developed for binary information, the invention is preferably carried out in the binary system of notation.



The invention also relates to an apparatus for carrying out the process, said apparatus being of the type described in the introductory portion of claim 4. The apparatus is characterized by the coupling of registers defined in the characterizing portion of claim 4, which in connection with said buffer register provides simple means for dynamic variation of resolubility, the buffer register being arranged to transfer its information to the main register when the plurality of digits necessary for the desired resolubility has been read from the last-mentioned register in the sequence, the remaining portion of the digits in the digit row being erased by parallel transfer of the information in the buffer register to the main register.

- 15 Claim 5 defines means which are particularly appropriate for carrying out the process of claim 3.

In addition to the examples already mentioned, the invention is a great value in many other applications. For process monitoring e.g., the invention allows a large number of parameters to be monitored rapidly in succession with a relatively rough resolubility corresponding to predetermined maximum and minimum values of the parameters, and permits an automatic increase in resolubility for accurate determination of a parameter value which in the rough resolubility should exceed the predetermined limits. Similar advantages can be achieved in connection with recognition of two or multidimensional patterns, e.g. in connection with radar images, aids for the partially sighted, detecting of the outline of objects on a conveyor belt, etc.

The invention will be explained in more detail in the following description of some embodiments with reference to the drawing, in which



fig. 1 shows a first embodiment of the apparatus of the invention,

fig. 2 shows another embodiment, and

fig. 3 shows still another embodiment in connection with  
5 a light-sensitive matrix for optical reading of two-dimensional patterns.

Fig. 1 shows a first embodiment of the apparatus of the invention, said embodiment comprising a plurality of registers 1, 2, 3 and 4, a main register 5 as well as  
10 a buffer register 6 for the main register 5. The registers 5 and 6 contain sixteen places numbered from top to bottom, while the other registers each contain four places, likewise numbered from top to bottom in the register concerned. The registers 1, 2, 3 and 4 thus  
15 contain the decimal numbers 9, 10, 3 and 4, respectively.

The registers 1, 2, 3 and 4 may contain values of measurement from a process monitoring system which it is desired to transmit serially to a central receiver via a lead L. The duration of this transfer of information will  
20 be proportional to the number of bits to be transferred, which in this case is 16, but in other instances where many more registers of the type 1, 2, 3 and 4 are present, the transfer of information may take an excessively long time, particularly when the system is in a monitoring  
25 state where only a rough indication of the many process parameters is desired.

It being assumed for the present purposes that information from the registers 1, 2, 3 and 4 is supplied directly through the buffer register 6 to the main register 5, the  
30 registers 1, 2, 3 and 4 are coupled to the main register 5, as appears from fig. 1 (for clarity the figure only

shows the connections to the first and the last places, the other connections being provided in fundamentally the same manner), and which entails that the first four places in the main register 5 contain the most important bits from each of the registers 1, 2, 3 and 4, respectively. The places 4-8 in the main register 5 contain the four bits of place No. 2 in each of the registers 1, 2, 3 and 4, and so on. This has the advantage that the row of digits read serially from the top of the main register 5 begins with the most important bits from each of the parameter registers and ends with the least important bits in each of the parameter registers. The receiver (not shown) may then be so arranged that it receives only a front fraction of the row of digits on the lead L, depending upon the resolubility which is desired in the given case. In addition to the example already mentioned, the resolubility may e.g. be diminished if, for a while, there is much noise in the system. It being well-known that the probability of errors in the reception of the sequence of the digits increases with the number of digits transferred, e.g. owing to errors of synchronization, the invention provides the additional advantage that such errors will with the greatest probability spread on the least important bits, while the most important bits from each parameter register will be transferred with less probability of errors.

Instead of the receiver being arranged to cut-off the last fraction of the digit sequence on the lead L, the buffer register 6 may according to the invention operate in the following manner. The buffer register 6 is a parallel-in/parallel-out register which serves as an intermediate store for information to the main register 5, and is arranged to transfer its information to the main register 5 when the desired front fraction of the preceding row of digits has been read to the lead L. This



means that only twelve bits are read to the lead L in the example shown in fig. 1; the last four bits (1001) are not read out, but are erased and replaced by the new row of digits from the buffer register 6. The timing of the transfer from the buffer register 6 to the main register 5 thus decides the number of bits which in the preceding digit sequence are read to the lead L. Each row of digits on the lead L can by the use of not shown means be enlarged so as to contain parity bits and flag characters so that error detection may be effected in the receiver.

Flag characters and digits for error correction may, in particular when the source registers do not contain equally many storage cells, be expediently input by means of the embodiment shown in fig. 2, where the main register 5 in fig. 1 is omitted for clarity. The embodiment shown in fig. 2 corresponds in principle to the embodiment shown in fig. 1, it being observed that the source registers 1A, 1B, 1C and 1D contain four, three, two and two storage cells, respectively, and that an additional logic circuit 8 is provided.

Fig. 2 shows all the connections between the source registers 1A, 1B, 1C and 1D and the buffer register 6A, and since the registers 3A and 4A only contain two storage cells each, it will appear that there are two vacant storage cell places (7A) in the third storage group of the buffer register 6A. Similarly, there are three vacant storage cells (7B) in the fourth storage group. The logic circuit 8 is arranged to receive information from all the buffer register cells which receive information from the source registers 1A, 1B, 1C and 1D and to produce auxiliary digits on the basis of this which are transferred to the buffer register cells 7A, 7B. Flag characters may e.g. be





transferred to the cells 7A, and error correcting digits may be introduced in the cells 7B.

This embodiment may e.g. be used in a process monitoring system with many source registers in which some registers (1A) may contain many digits for accurate parameter values, while other registers contain fewer digits, where e.g. two digits (the registers 3A, 4A) may indicate whether a valve is open or closed. If it is of great importance to know whether a valve is open or closed, high priority will be accorded to the associated source register, i.e. it is disposed at the front in the sequence 1A, 2A, 3A, 4A ....., and it will then be understood that, roughly, process monitoring may be effected by using a shortened row of digits in the buffer register and main register, respectively. If the predetermined parameter values deviate outside a relatively rough margin, a larger fraction of the row of digits, perhaps the entire row of digits may be included by using automatic control means (not described here) so as to provide more detailed and accurate information about the state of the process system.

Cutting off of a last part of the digit sequence on the lead L does not have to take place at a time when equally many bits from each of the parameter registers have been transferred, but may also be effected at a time when the bit last transferred is supplied by the parameter register 1 or 1A so that the parameter value in that register is transferred with greater accuracy than the parameter values in the other registers.

Fig. 3 shows a known light-sensitive matrix 10 with 256 image-plots and with associated scanning registers 11, 12. The co-ordinates of the image plots are indicated by binary numbers, as shown in fig. 3, and in a preferred scanning method of the registers 11, 12 the co-ordinates



of the matrix plots receiving a light intensity above a given threshold value will appear on the outputs thereof. In the figure the double-hatched areas indicate the number 2, the co-ordinates of the area stressed by a full line being 1001, 1010, which sets of co-ordinates will be followed below, it being remembered that the other co-ordinates, which together define the number 2, are read according to a predetermined pattern and treated in the same manner as will be described below for the arbitrarily selected area indicated by a full line in the matrix 10.

At a certain time during the scanning process the co-ordinates 1001, 1010 will thus be read from the registers 11 and 12, respectively, and be transferred in respective registers of co-ordinates 13 and 14, where the most important bit is at the top of the registers shown in the figure. The information in the registers 13, 14 is transferred, according to the invention, to a main register 15, as appears from the shown connections between the storage cells of the registers, which entails that a row of digits like the one on the lead L in fig. 1 will be produced on the serial output U from the main register 15.

In the operation described above the maximum resolvability of the matrix 10 is utilized, which may be useful in connection with complicated patterns, but transfer of an image of a number does not necessitate maximum resolvability. This appears from fig. 3 which shows that the number 2 may easily be recognized on the basis of the single- or double-hatched areas which in size correspond to 64 such areas in the matrix 10. The latter areas may be represented by co-ordinates each of which only contains three binary bits that may be transferred to the shown scanning registers 16 and 17 which for the purpose of reading out are arranged in the same manner as the

scanning registers 11 and 12. The shown converters 18 and 19 provide for conversion to a situation in which only three co-ordinate bits are transferred to the registers 13 and 14. The bit in the registers 13 and 14 which is not used may then be picked up by a parity bit for the co-ordinate information, and said parity bits may then be input by means of a circuit 20 and 21.

The embodiment in fig. 3 provides a digit sequence on the output U by means of the converters 18 and 19 where the resolubility of the respective co-ordinates differs. For example, in the transfer of information representing the image of number, information from the scanning registers 11 and 17 might be read so as to provide for the accommodation of a single parity bit in the digit sequence on the output U with good resolubility, the greatest resolubility being achieved in the width, and less resolubility in the height, corresponding to the fact that numbers are usually narrow and tall.

The embodiment shown in fig. 3 may of course be enlarged to transfer of co-ordinates for three- or multidimensional information where further co-ordinates might e.g. contain information about the intensity of the basic colours in a colour image. Similarly, there should be more co-ordinate registers with connections according to the invention to a longer main register. Each co-ordinate register and the main register may then have interposed between them a buffer register, as was explained in connection with figs. 1 and 2.



## P a t e n t   C l a i m s

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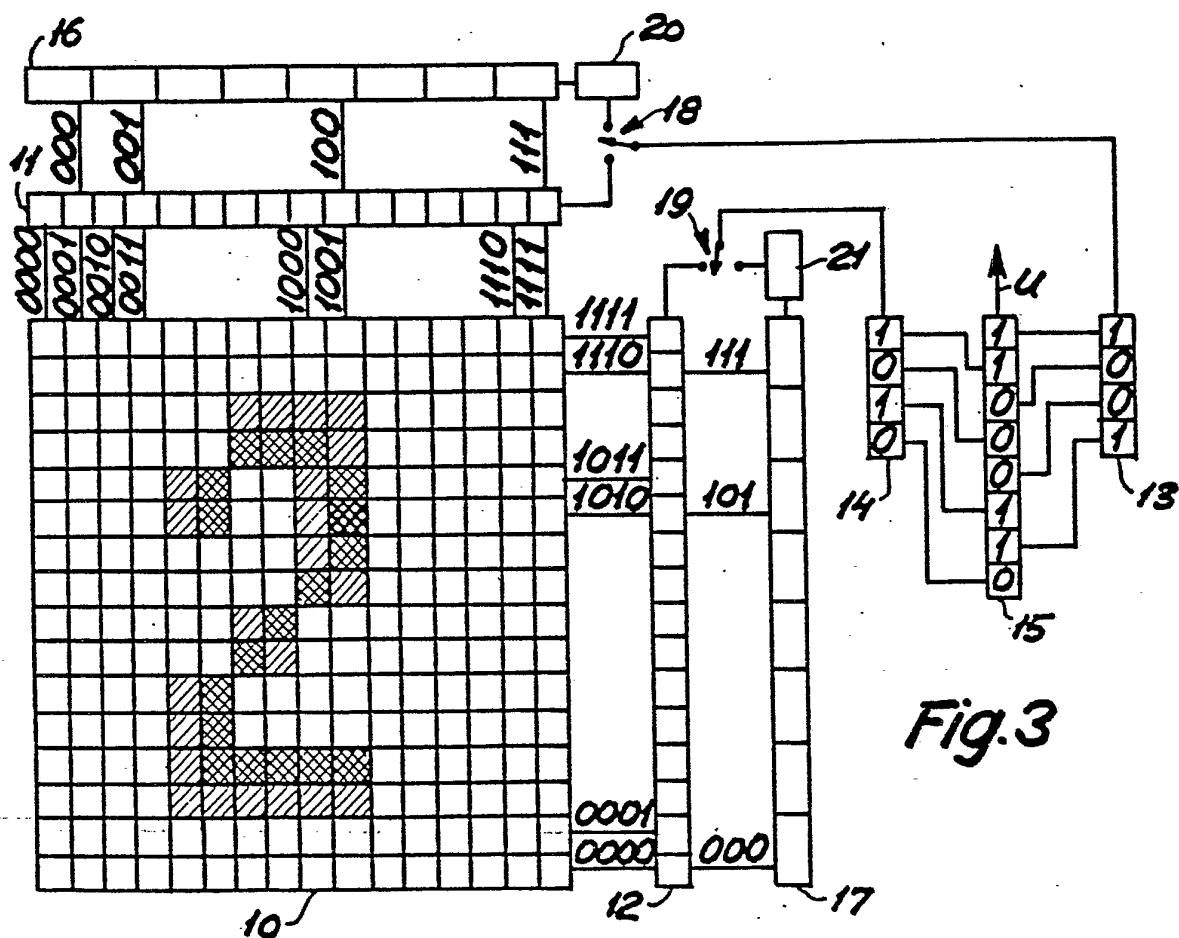
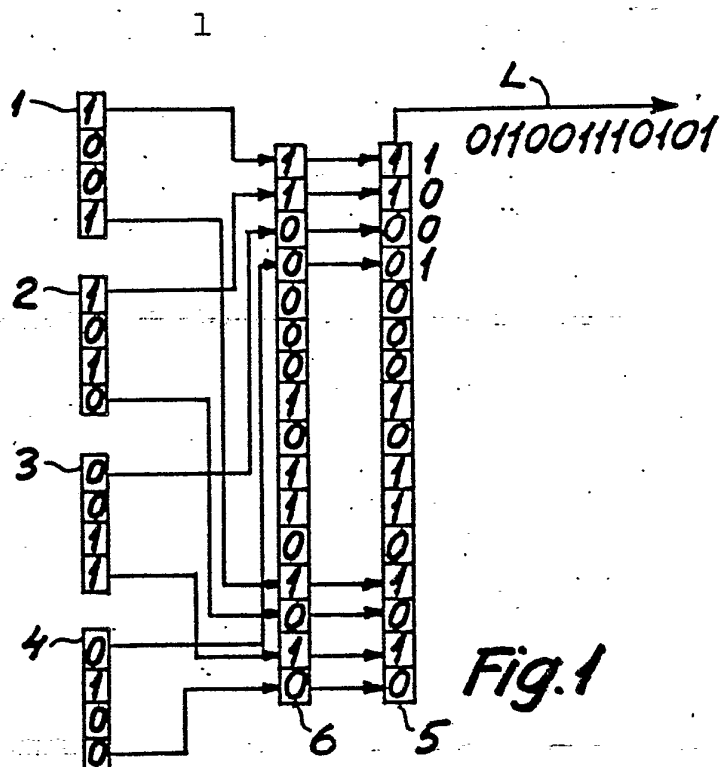
1. A process for transferring information from two or more data sources, in which the information is transferred serially in data groups each of which contains a single bit from each data source, c h a r a c t e r i z e d by  
5 arranging each data source (1, 2, 3, 4) to represent a parameter, such as a co-ordinate in a system of co-ordinates, so that the weight of each digit in a parameter represents a predetermined digit position in the corresponding data source, and by interrupting the  
10 transfer of information of the row of digits thus produced when the transferred partial row represents each parameter with a predetermined accuracy.
2. A process according to claim 1, c h a r a c t e r -  
i z e d by ranking the parameters in priority and intro-  
15 ducing them in the row of digits so that a bit in each data group originating from a first parameter is positioned in front of another bit in same data group originating from a second parameter, the first parameter having a higher priority than the second parameter.
- 20 3. A process according to claim 1 or 2, and where the parameters are represented by a different number of bits, c h a r a c t e r i z e d by introducing into each data group flag digits and/or error correcting digits on the place or places in the data group corresponding to the  
25 parameters represented by a relatively small number of bits.
4. An apparatus for carrying out the process according to claims 1-3 and comprising a plurality of source registers with a plurality of storage cells each of which  
30 being connected for transfer of binary information to the

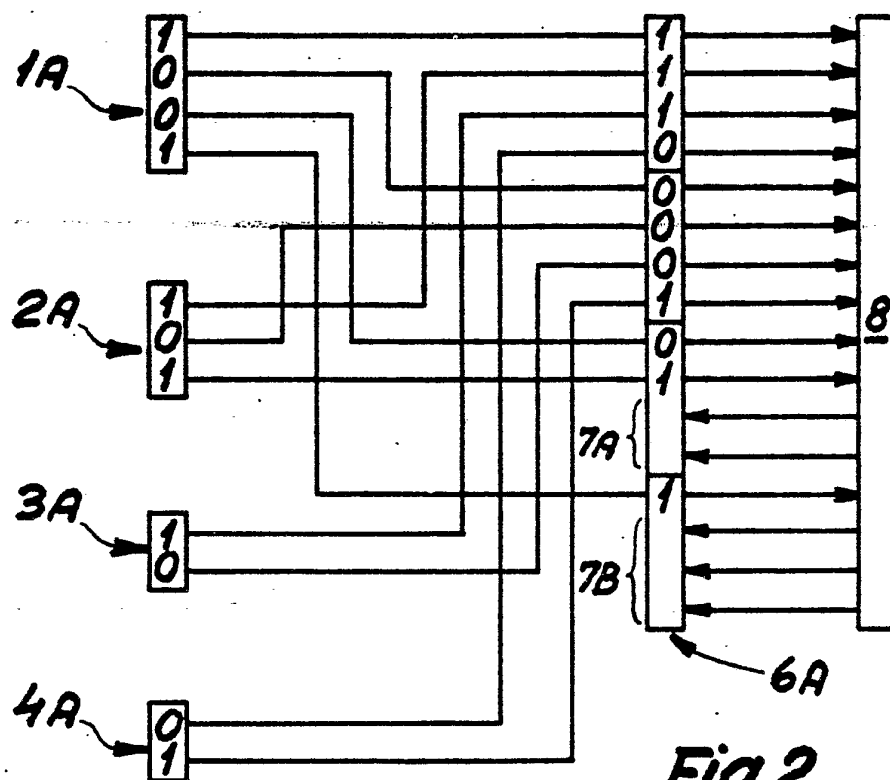


respective storage cells in a main register, c h a r a c -  
t e r i z e d in that the main register (5) is a  
parallel-in/serial-out register which has a plurality  
of storage groups corresponding to the largest amount of  
5 storage cells among the source registers (1, 2, 3, 4),  
each of said storage groups comprising main register  
cells with respective position numbers, and that the main  
memory (5) is arranged to receive source information over  
a corresponding parallel-in/parallel-out buffer register  
10 (6) when a predetermined number of the contents of the  
main storage cells has been read out so that a main  
storage cell receives a bit from a source register cell,  
the position and group numbers of the main memory cell  
corresponding to the source register number and storage  
15 cell position, respectively, in the source register.

5. An apparatus according to claim 4, c h a r a c t e r -  
i z e d in that buffer register cells (7A, 7B), which do  
not receive information from a source register (1A, 1B,  
1C, 1D), are coupled to logic circuits (8) arranged to  
20 produce distinguishing and/or error correcting information,  
depending upon the contents of the buffer register cells  
coupled to the source registers.





*Fig. 2*

## FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

II    **FIELDS SEARCHED**  
 Classification System Continuation  
 US Cl: 179-2, 179-15

V. ☐ **OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE <sup>10</sup>**

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers \_\_\_\_\_, because they relate to subject matter <sup>12</sup> not required to be searched by this Authority, namely:

2. ☐ Claim numbers \_\_\_\_\_, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out <sup>13</sup>, specifically:

VI. ☐ **OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING <sup>11</sup>**

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

## Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.



# INTERNATIONAL SEARCH REPORT

International Application No. PCT/DK79/00054

<b>I. CLASSIFICATION OF SUBJECT MATTER</b> (If several classification symbols apply, indicate all) <sup>3</sup> According to International Patent Classification (IPC) or to both National Classification and IPC <sup>3</sup>  <div style="text-align: center; font-family: monospace; font-size: 1.2em;">H 04 J 15/00</div>																				
<b>II. FIELDS SEARCHED</b>  <div style="text-align: center; font-size: 0.8em;">Minimum Documentation Searched <sup>4</sup></div> <table style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 30%; text-align: left; font-size: 0.8em;">Classification System</th> <th style="text-align: left; font-size: 0.8em;">Classification Symbols</th> </tr> <tr> <td style="vertical-align: top;">IPC <sup>3</sup></td> <td>H 04 J 3/00, 02, 04, 16; H 04 J 15/00; H 04 N 1/00, H 04 N 7/12; H 04 L 5/00, 22; G 01 D 5/00, 244, 245, 249; G 08 C 15/00; G 08 C 19/18</td> </tr> <tr> <td style="vertical-align: top;">Deutsche KI</td> <td>21a<sup>3</sup>:46/10 .../...</td> </tr> </table> <div style="text-align: center; font-size: 0.8em; margin-top: 5px;">Documentation Searched other than Minimum Documentation to the extent that such Documents are included in the Fields Searched <sup>5</sup></div>			Classification System	Classification Symbols	IPC <sup>3</sup>	H 04 J 3/00, 02, 04, 16; H 04 J 15/00; H 04 N 1/00, H 04 N 7/12; H 04 L 5/00, 22; G 01 D 5/00, 244, 245, 249; G 08 C 15/00; G 08 C 19/18	Deutsche KI	21a <sup>3</sup> :46/10 .../...												
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Deutsche KI	21a <sup>3</sup> :46/10 .../...																			
SE, NO, DK, FI classes as above																				
<b>III. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <sup>14</sup> <table style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 10%; text-align: left; font-size: 0.8em;">Category <sup>6</sup></th> <th style="text-align: left; font-size: 0.8em;">Citation of Document, <sup>16</sup> with indication, where appropriate, of the relevant passages <sup>17</sup></th> <th style="width: 15%; text-align: left; font-size: 0.8em;">Relevant to Claim No. <sup>18</sup></th> </tr> <tr> <td style="vertical-align: top;">X</td> <td>GB, A, 977 876 published 1964, December 16, General Electric Company Limited</td> <td>1-2, 4</td> </tr> <tr> <td style="vertical-align: top;">X</td> <td>GB, A, 1 377 374 published 1974, December 11, Plessey Company Limited</td> <td>1-2, 4</td> </tr> <tr> <td style="vertical-align: top;">A</td> <td>US, A, 3 842 206 published 1974, October 15, International Standard Electric Corporation</td> <td>4</td> </tr> <tr> <td style="vertical-align: top;">A</td> <td>US, A, 4 027 301 published 1977, May 31, Sun Oil Company of Pennsylvania</td> <td>4</td> </tr> <tr> <td style="vertical-align: top;">A</td> <td>J Martin, "Telecommunications and the Computer" published 1969 by Prentice-Hall Inc, see pages 384-390</td> <td>3, 5</td> </tr> </table>			Category <sup>6</sup>	Citation of Document, <sup>16</sup> with indication, where appropriate, of the relevant passages <sup>17</sup>	Relevant to Claim No. <sup>18</sup>	X	GB, A, 977 876 published 1964, December 16, General Electric Company Limited	1-2, 4	X	GB, A, 1 377 374 published 1974, December 11, Plessey Company Limited	1-2, 4	A	US, A, 3 842 206 published 1974, October 15, International Standard Electric Corporation	4	A	US, A, 4 027 301 published 1977, May 31, Sun Oil Company of Pennsylvania	4	A	J Martin, "Telecommunications and the Computer" published 1969 by Prentice-Hall Inc, see pages 384-390	3, 5
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<div style="font-size: 0.8em;"> <p>• Special categories of cited documents: <sup>15</sup></p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>"A" document defining the general state of the art</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document cited for special reason other than those referred to in the other categories</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> </div> <div style="width: 45%;"> <p>"P" document published prior to the international filing date but on or after the priority date claimed</p> <p>"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance</p> </div> </div> </div>																				
<b>IV. CERTIFICATION</b> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border-bottom: 1px solid black; padding: 5px;">           Date of the Actual Completion of the International Search <sup>2</sup>  <div style="font-family: monospace; font-size: 1.1em;">1980-01-25</div> </td> <td style="width: 50%; border-bottom: 1px solid black; padding: 5px;">           Date of Mailing of this International Search Report <sup>2</sup>  <div style="font-family: monospace; font-size: 1.1em;">1980-02-04</div> </td> </tr> <tr> <td style="border-bottom: 1px solid black; padding: 5px;">           International Searching Authority <sup>1</sup>  <div style="font-family: monospace; font-size: 1.1em;">Swedish Patent Office</div> </td> <td style="border-bottom: 1px solid black; padding: 5px;">           Signature of Authorized Officer <sup>20</sup>  <div style="font-family: cursive; font-size: 1.1em;">Sten-Ove Henningsson</div> <div style="font-family: monospace; font-size: 1.1em;">Sten-Ove Henningsson</div> </td> </tr> </table>			Date of the Actual Completion of the International Search <sup>2</sup> <div style="font-family: monospace; font-size: 1.1em;">1980-01-25</div>	Date of Mailing of this International Search Report <sup>2</sup> <div style="font-family: monospace; font-size: 1.1em;">1980-02-04</div>	International Searching Authority <sup>1</sup> <div style="font-family: monospace; font-size: 1.1em;">Swedish Patent Office</div>	Signature of Authorized Officer <sup>20</sup> <div style="font-family: cursive; font-size: 1.1em;">Sten-Ove Henningsson</div> <div style="font-family: monospace; font-size: 1.1em;">Sten-Ove Henningsson</div>														
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