

[54] **TWO-DIMENSIONAL IMAGE DATA COMPRESSION AND DECOMPRESSION SYSTEM**

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[52] U.S. Cl. **364/515; 358/260; 358/261; 364/200**

[57] **ABSTRACT**

A dual-mode encoding and decoding procedure enables image data to be compressed optionally in one-dimensional (1D) mode or two-dimensional (2D) mode. In 1D mode, color transitions in the image are encoded as run length features only. In 2D mode, the transitions are encoded as vertical correlation features wherever possible, and where this is not possible, the transitions are encoded as run length features. The compression

achieved by run length encoding in 2D mode may be enhanced in those instances where the "history line" which precedes the current scan line contains a transition located between points that are vertically aligned with the beginning and end points of the run currently being encoded. Run length counting is suspended for those pels in the current run that could have been referenced to the history transition if the run had ended with any of these pels, thereby enabling the run to be encoded as though it contained fewer pels than its actual length. Compression may be enhanced still further by dynamically interchanging the variable-length bit patterns respectively representing certain vertical correlation and run length prefix codes depending upon whether the preceding transition was encoded as a vertical correlation feature or a run length feature.

**20 Claims, 23 Sheets Drawing,
166 Pages Specification**

The file of this unexamined application may be inspected and copies thereof may be purchased (849 O.G. 1221, Apr. 9, 1968).

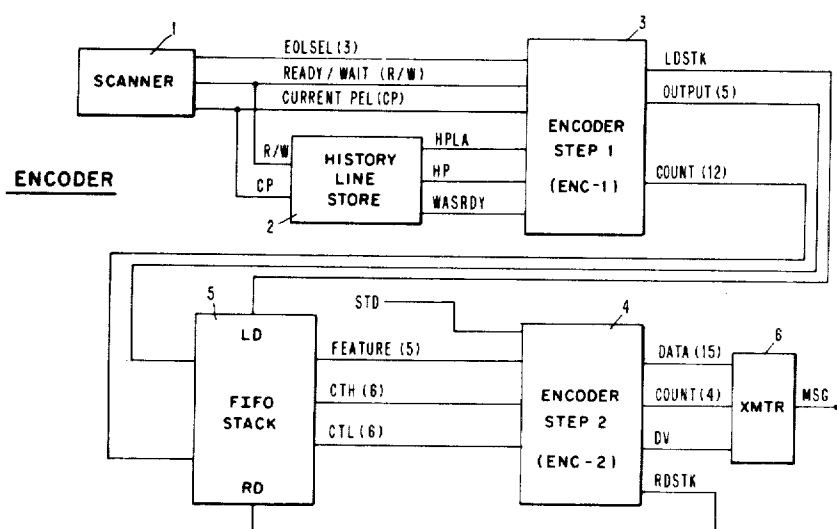


FIG. 1

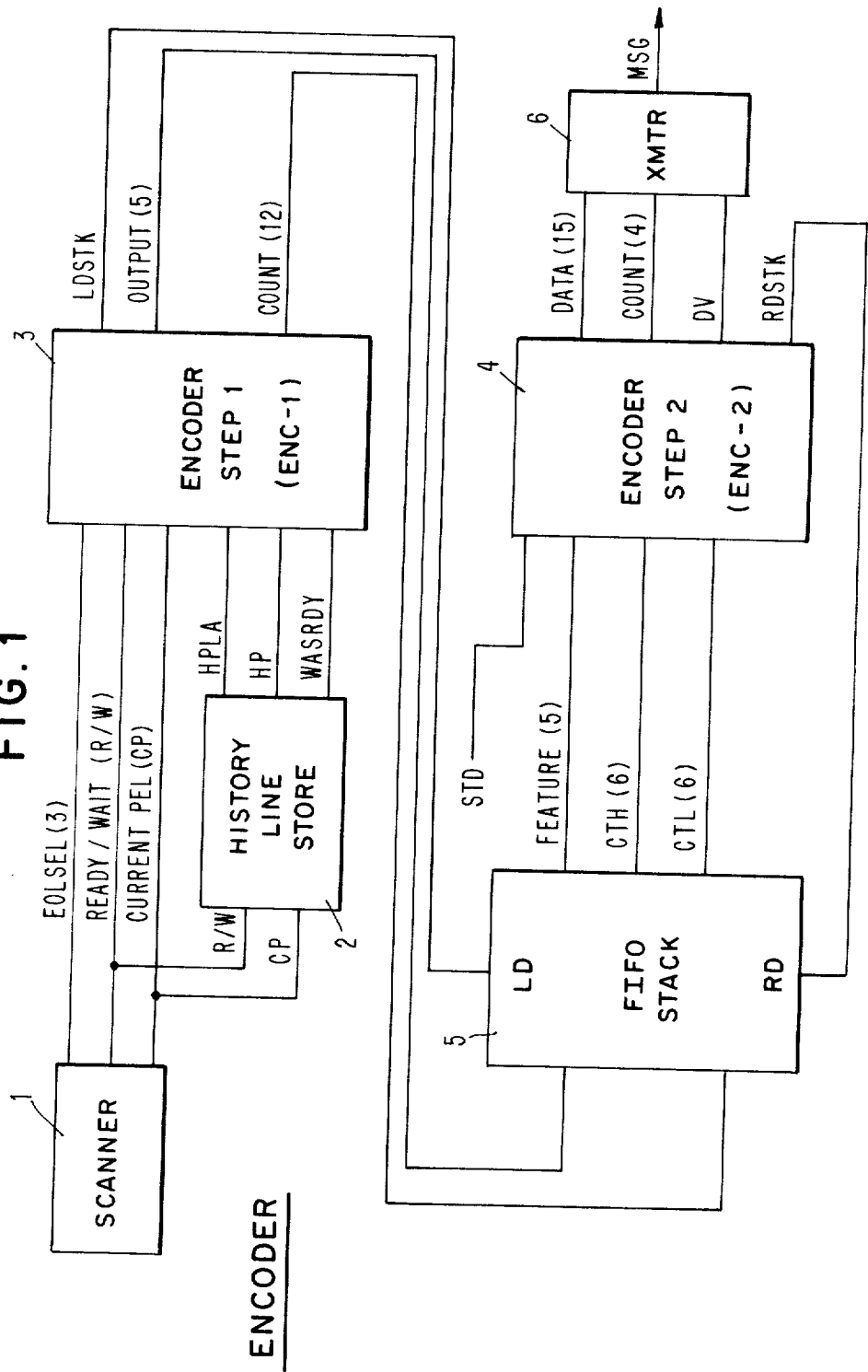
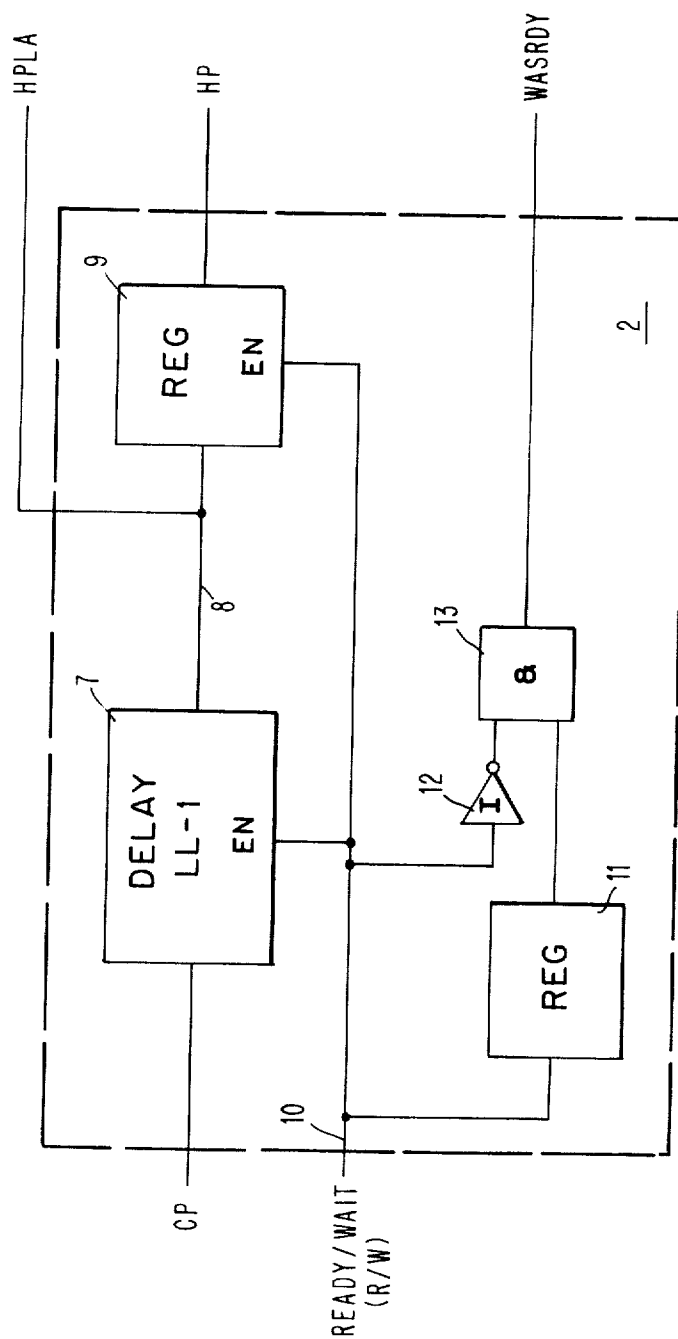


FIG. 2



ENCODER
HISTORY LINE STORE

FIG. 4
INPUTS TO ENCODER STEP 1

CONDITION	NEW INPUT			
READY	R	CP	HP	HPLA

READY	R	CP	HP	HPLA
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READY (LAST CYCLE)	R	CP	HP	HPLA
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WAIT (FIRST CYCLE) (OTHER CYCLES)	W	S1	HP	HPLA
	W	S1	S2	S3

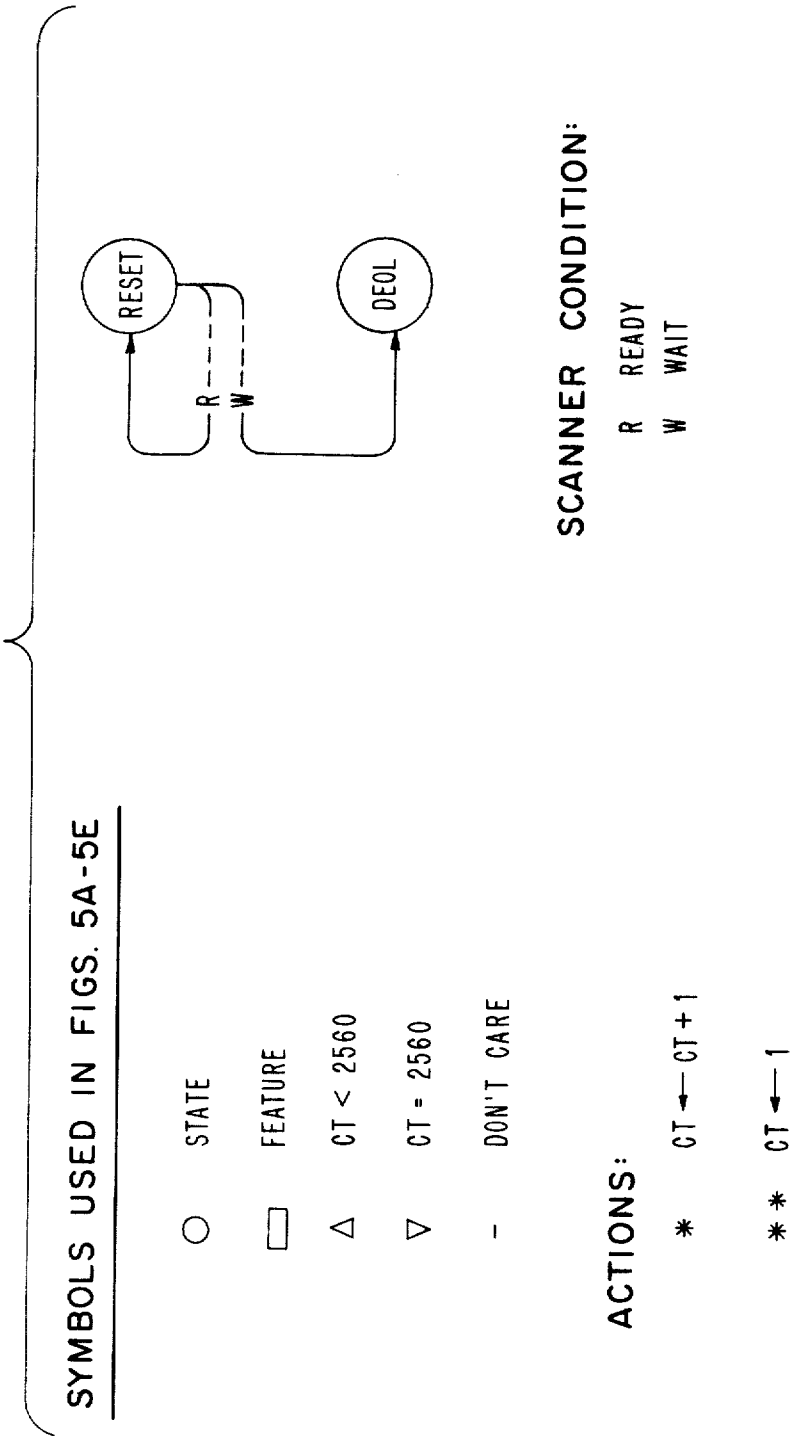
READY (FIRST CYCLE)	R	CP	HP	HPLA
------------------------	---	----	----	------

READY	R	CP	HP	HPLA
-------	---	----	----	------

FIG. 4A				
			HP	HPLA
			CP	
FIG. 4B				
			HP	HPLA
			CP	
FIG. 4C				
HPLA				HP
				CP
FIG. 4D				
HP	HPLA			
FIG. 4E				
HP	HPLA			
CP				
FIG. 4F				
			HP	HPLA
			CP	

FIG. 5A

STATE DIAGRAM FOR ENCODER STEP 1 (INITIALIZATION)



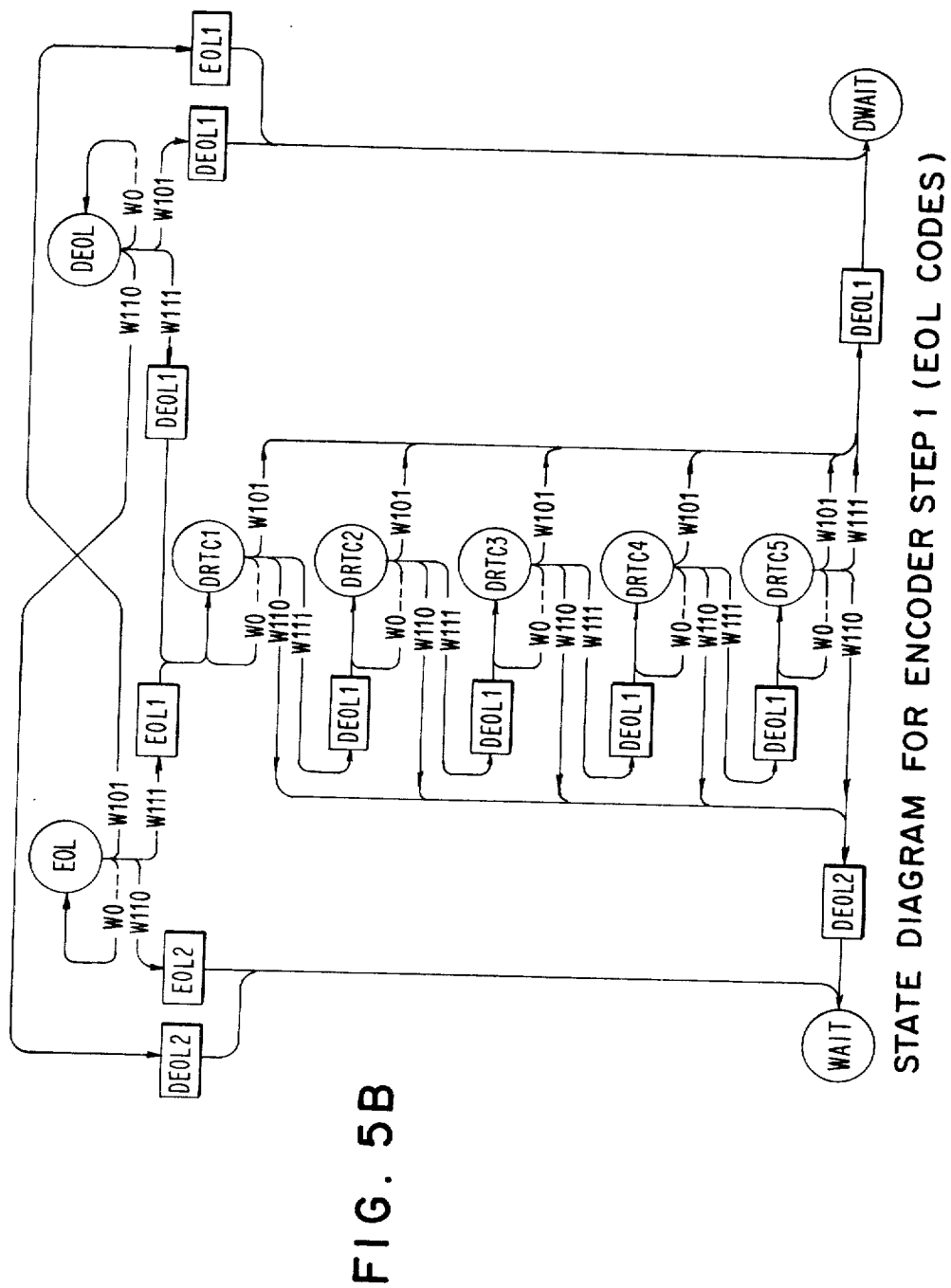


FIG. 5D

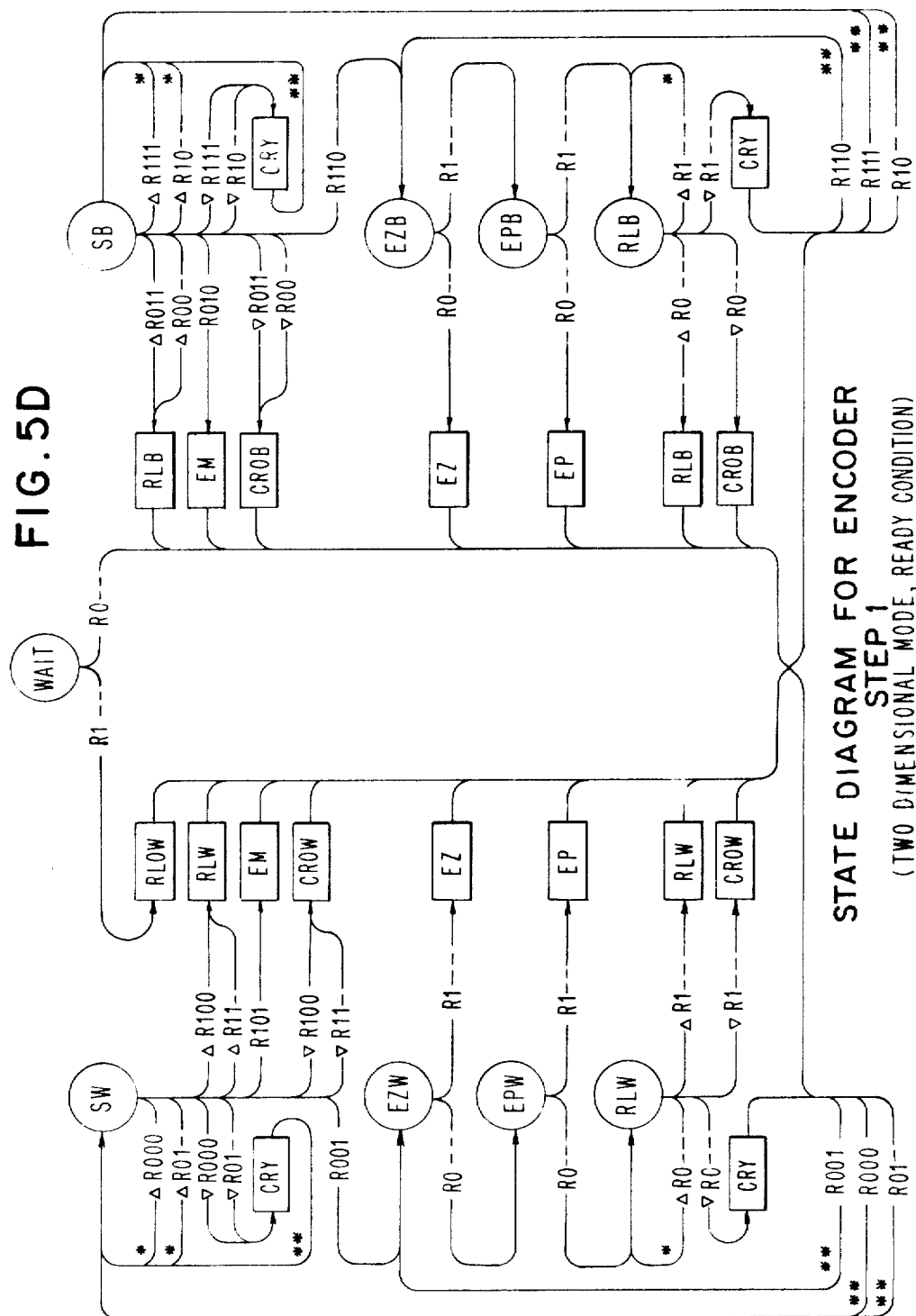
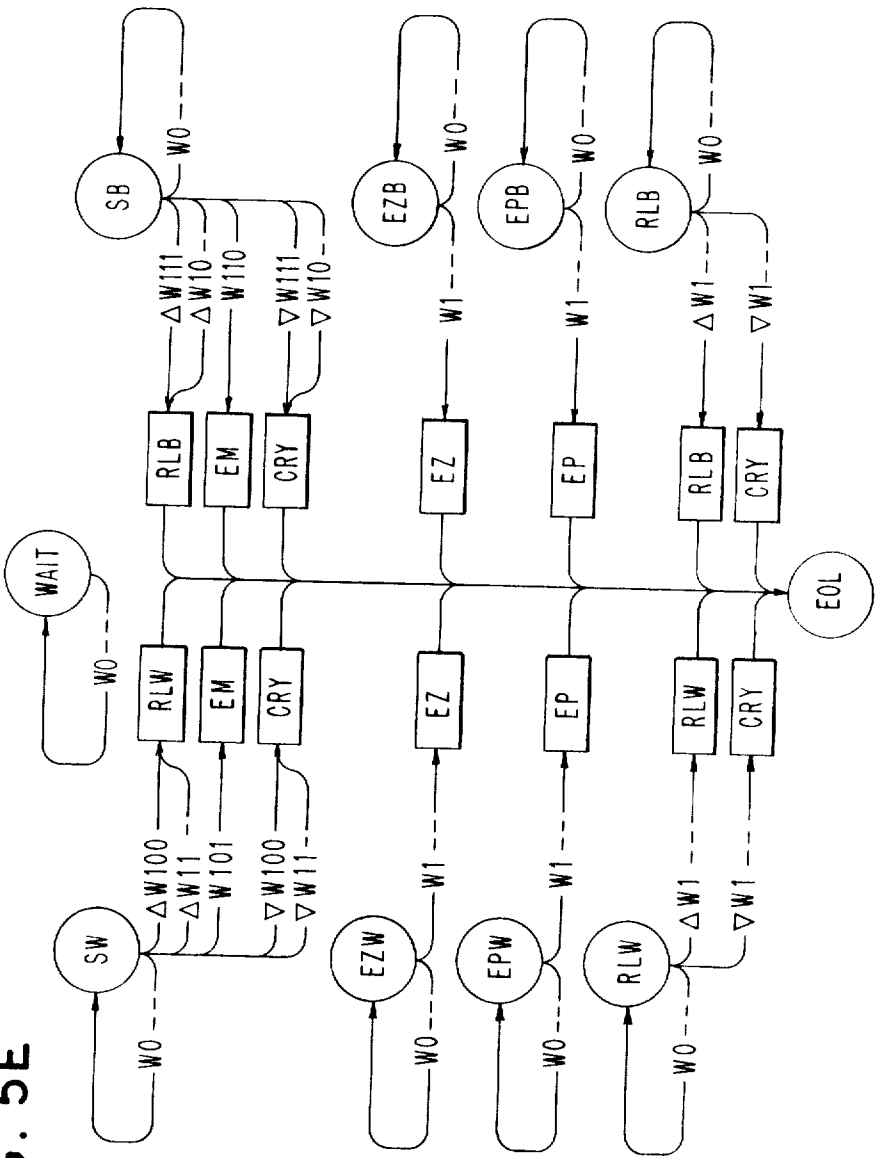
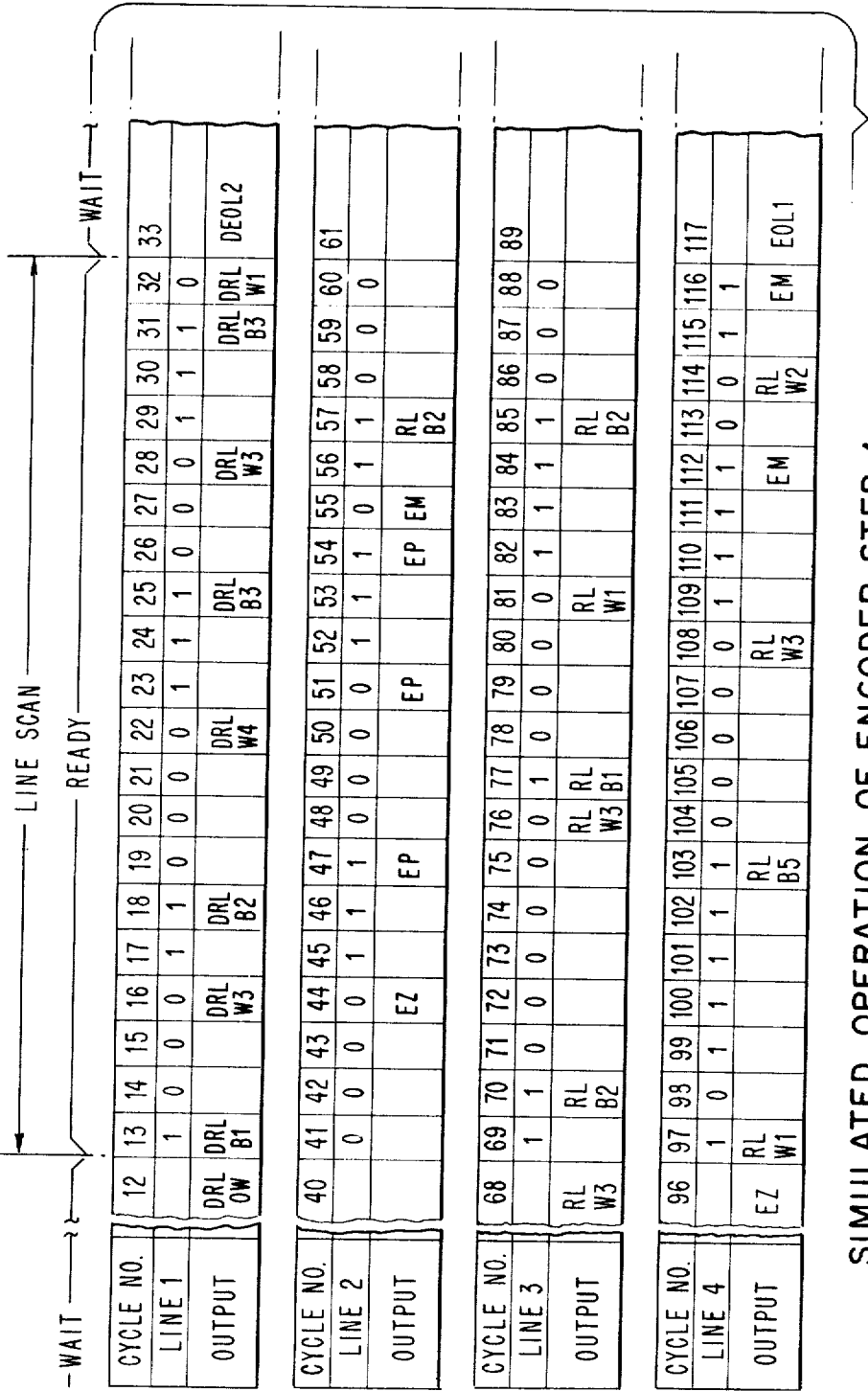


FIG. 5E



STATE DIAGRAM FOR ENCODER STEP 1 (TWO DIMENSIONAL MODE,
WAIT CONDITION)



SIMULATED OPERATION OF ENCODER STEP 1
USING EXAMPLE 4
(CERTAIN CYCLES ONLY)

FIG. 6

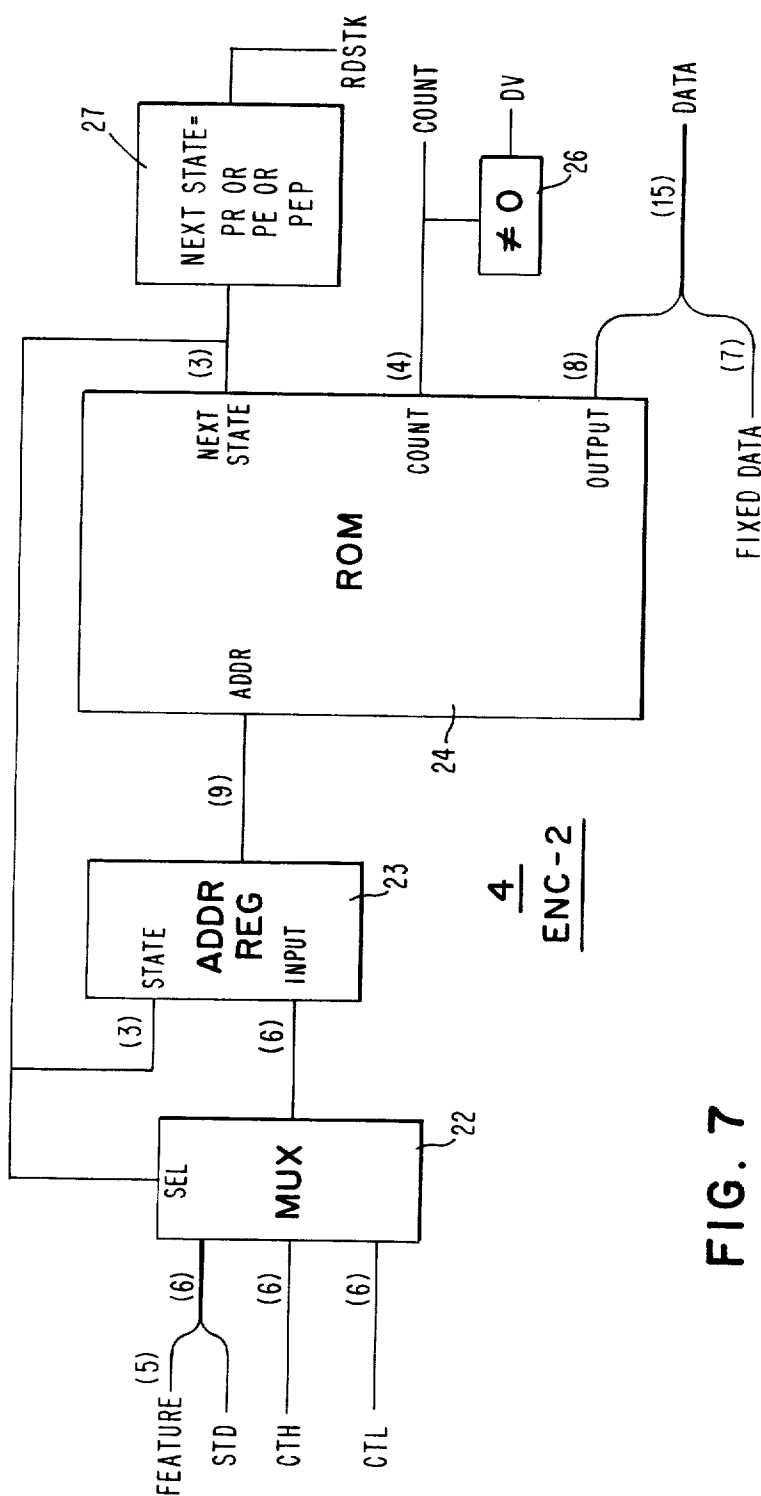
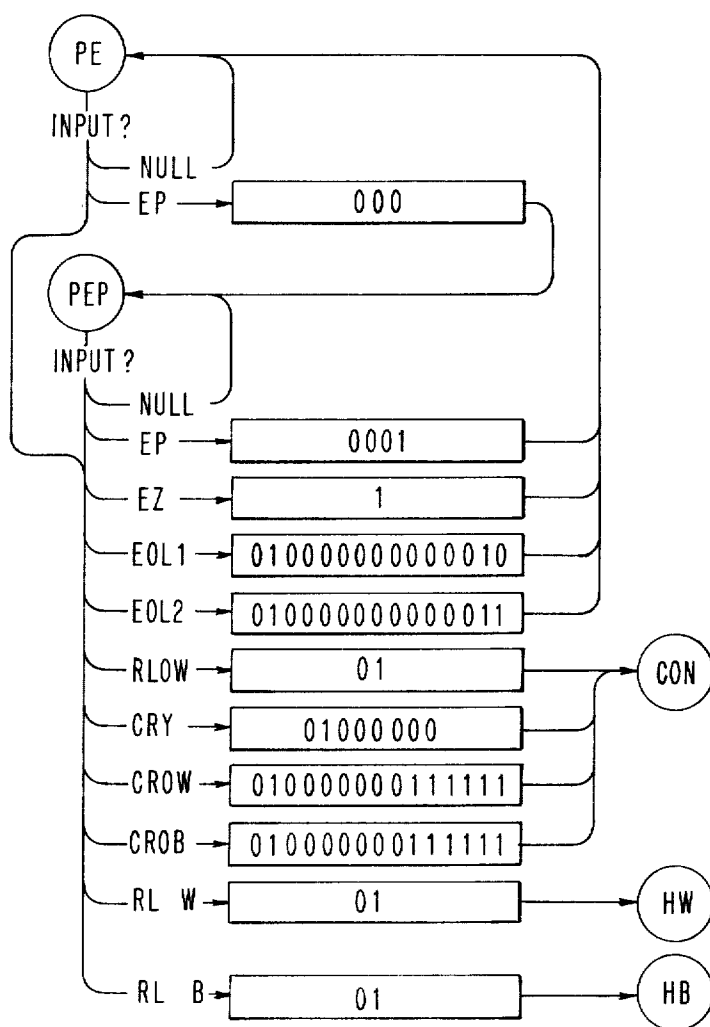


FIG. 8A

STATE DIAGRAM FOR ENCODER STEP 2



SYMBOLS USED IN FIGS. 8A-8E

□ OUTPUT
 ○ STATE

FIG. 8B
STATE DIAGRAM FOR ENCODER STEP 2
(CONTINUED)

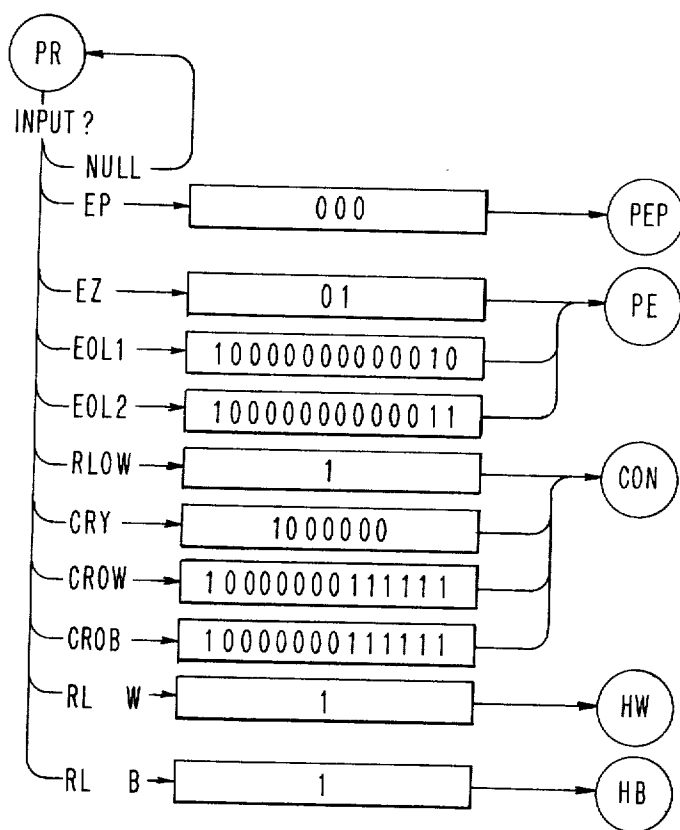


FIG. 8C

STATE DIAGRAM FOR ENCODER STEP 2 (CONTINUED)

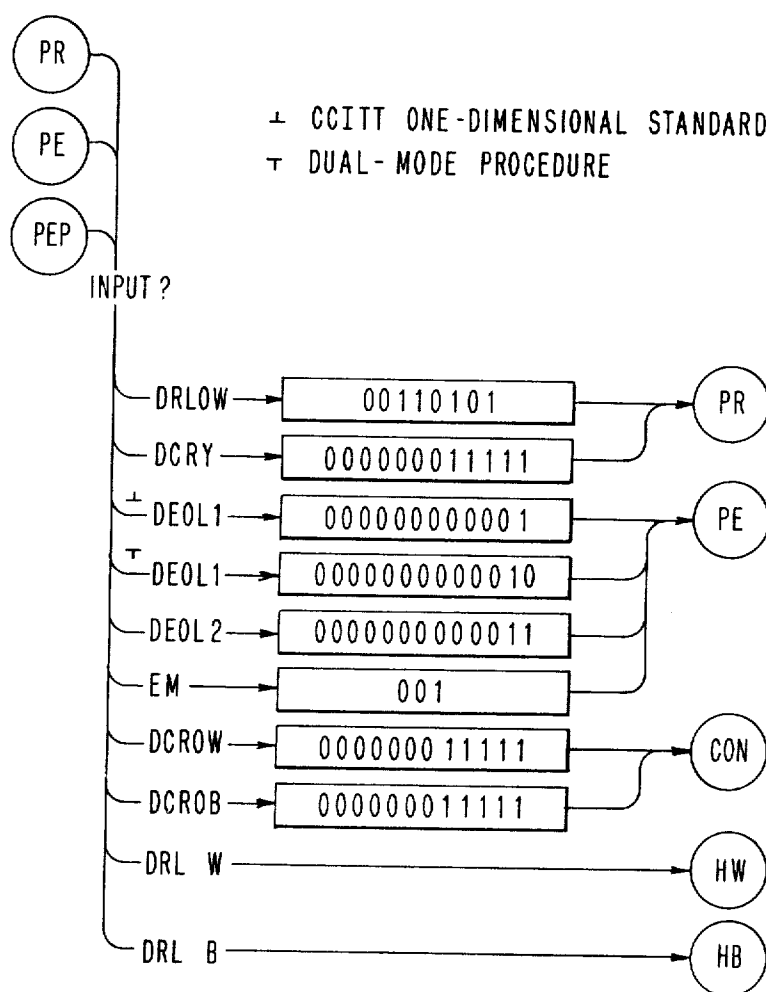
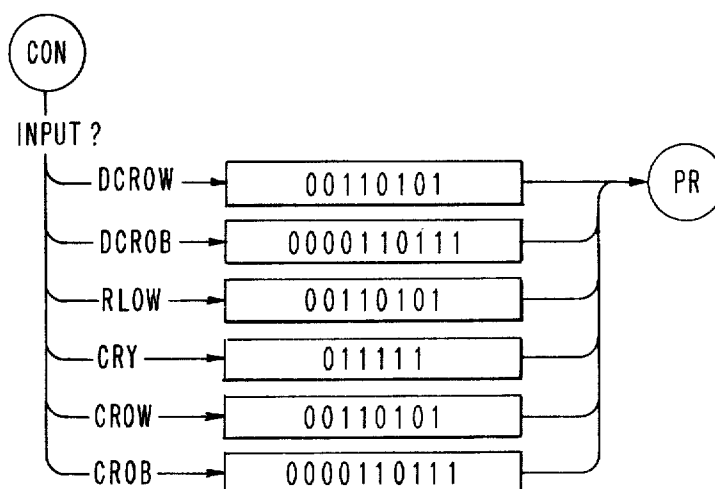


FIG. 8D

STATE DIAGRAM FOR ENCODER STEP 2
(CONTINUED)

**FIG. 8E**

STATE DIAGRAM FOR ENCODER STEP 2
(CONTINUED)

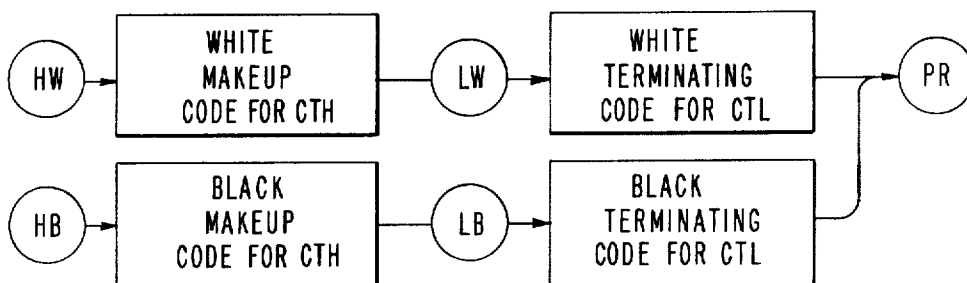


FIG. 9
DECODER

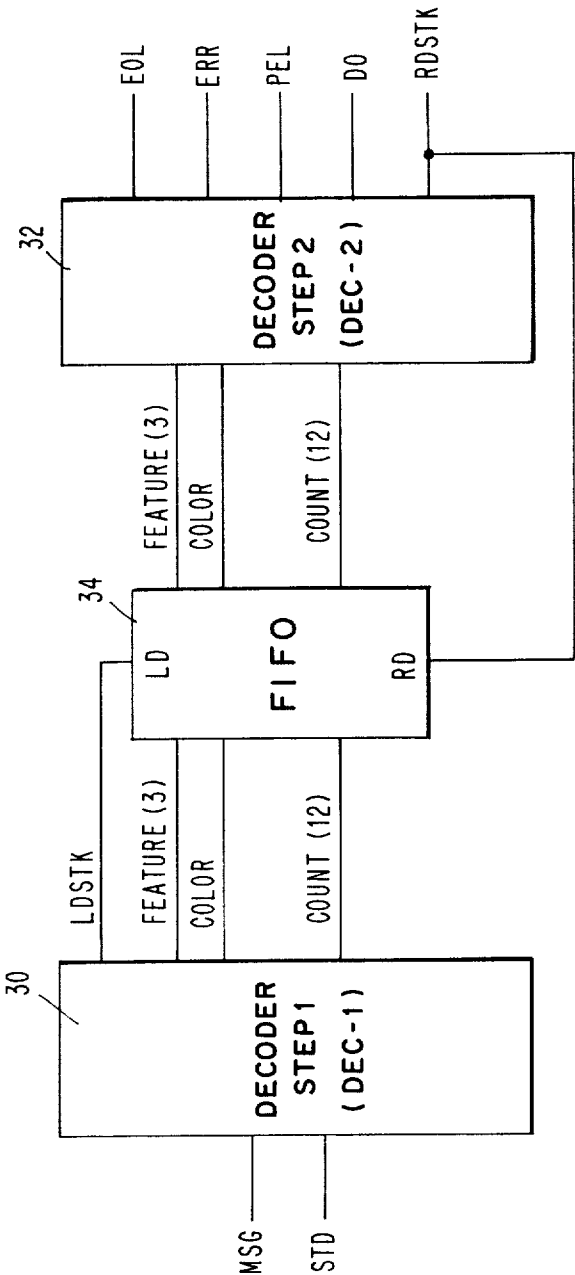
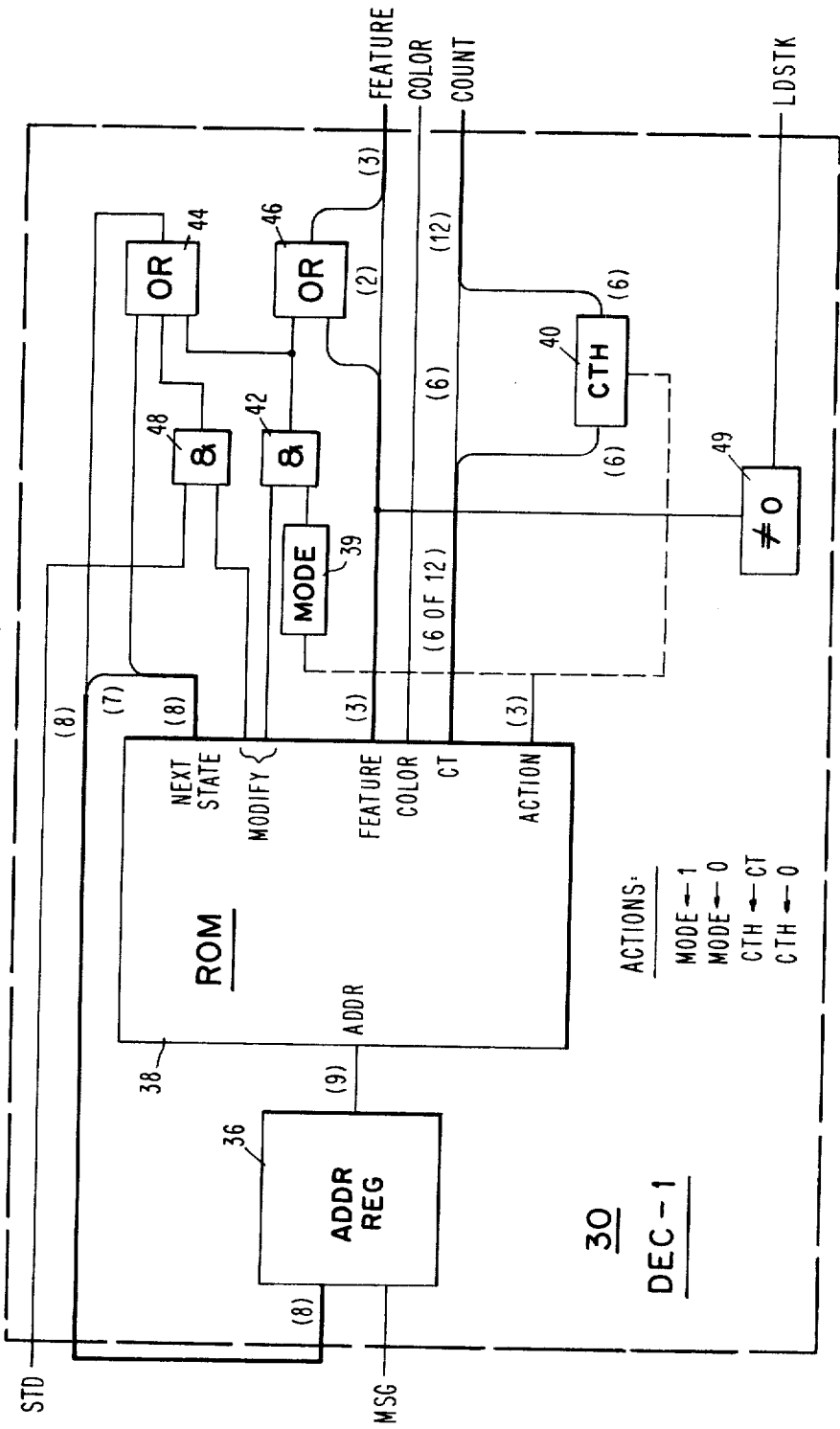
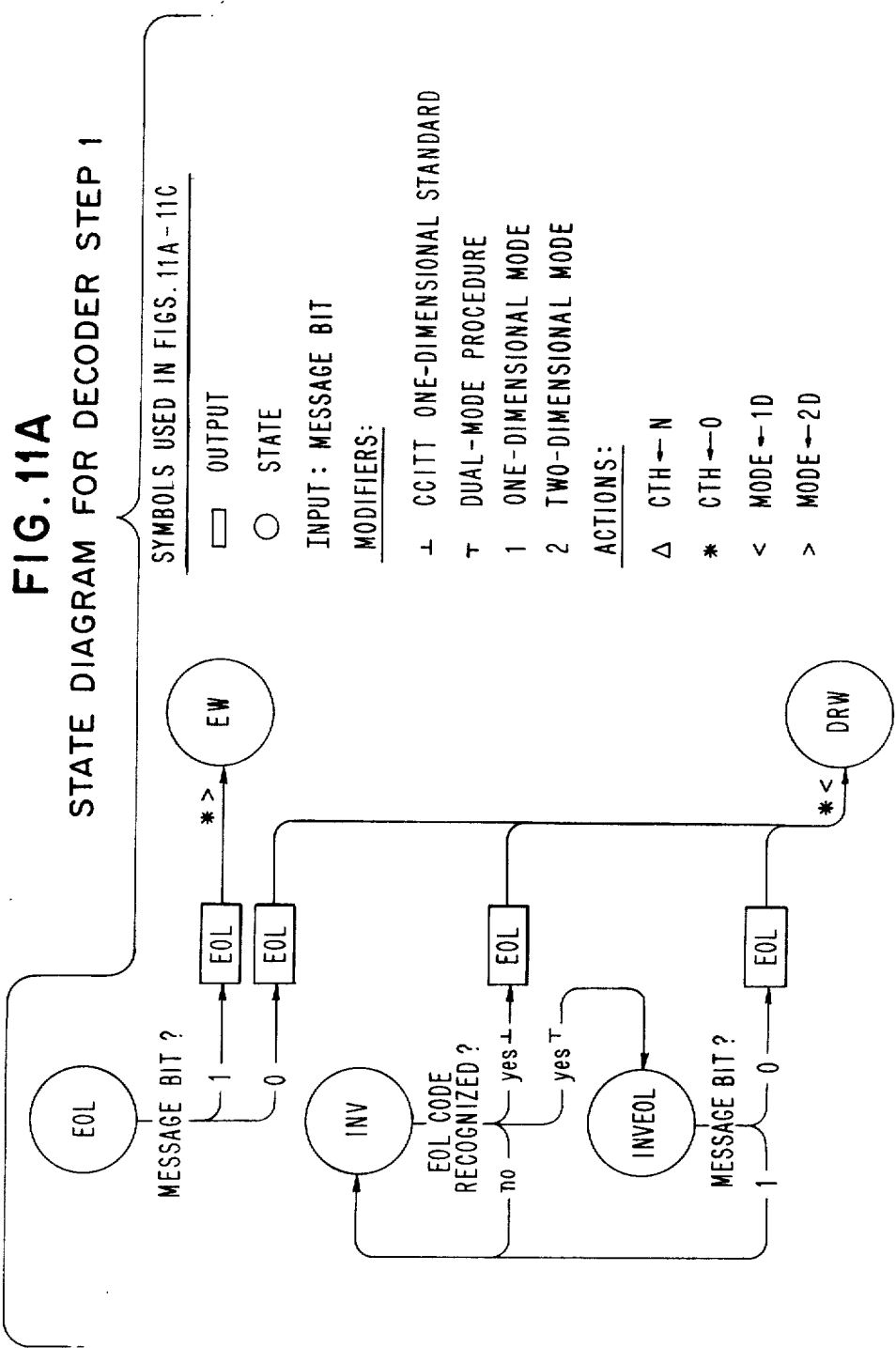
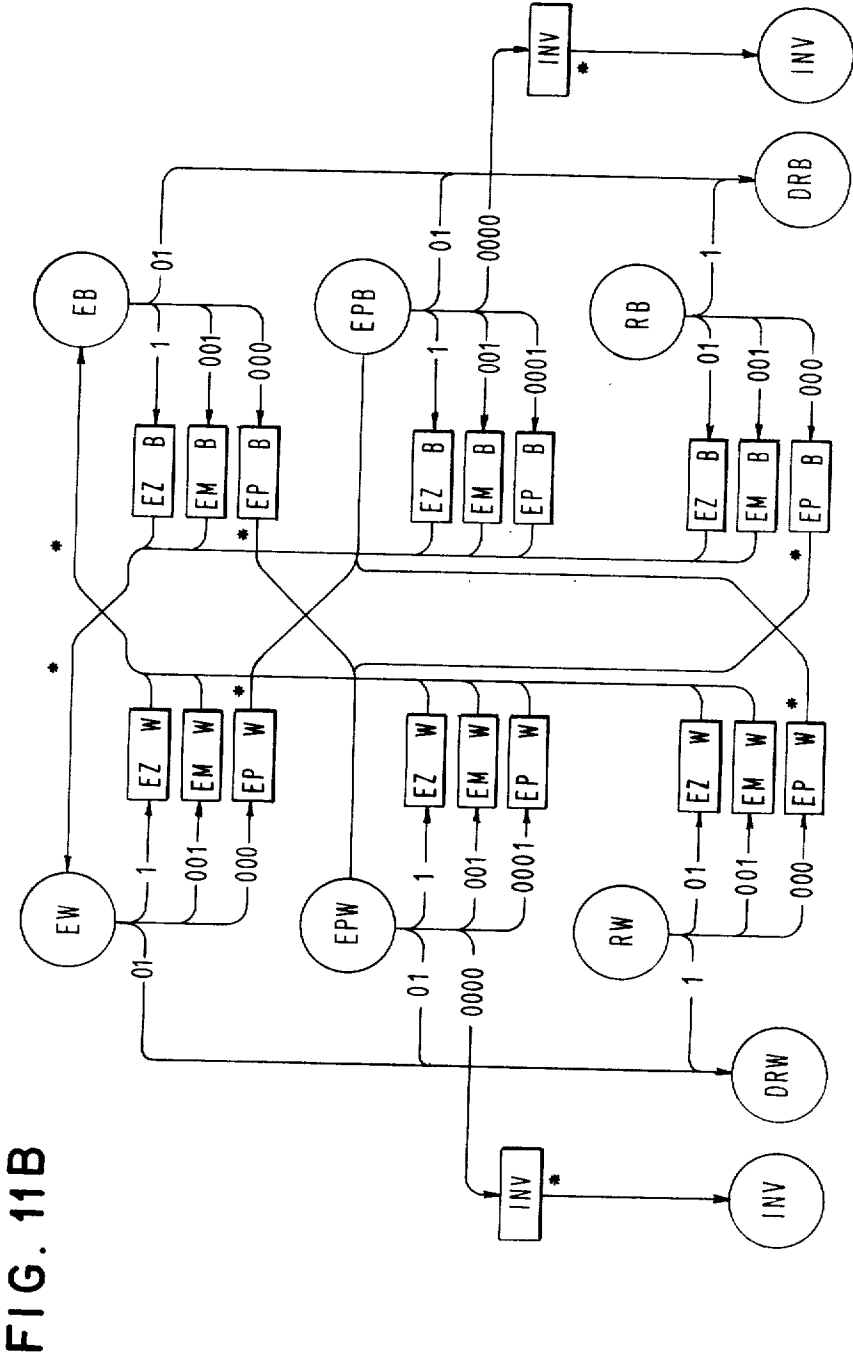


FIG. 10
DECODER STEP 1







STATE DIAGRAM FOR DECODER STEP 1
(CONTINUED)

FIG. 11B

FIG. 11C

STATE DIAGRAM FOR DECODER

STEP 1

(CONTINUED)

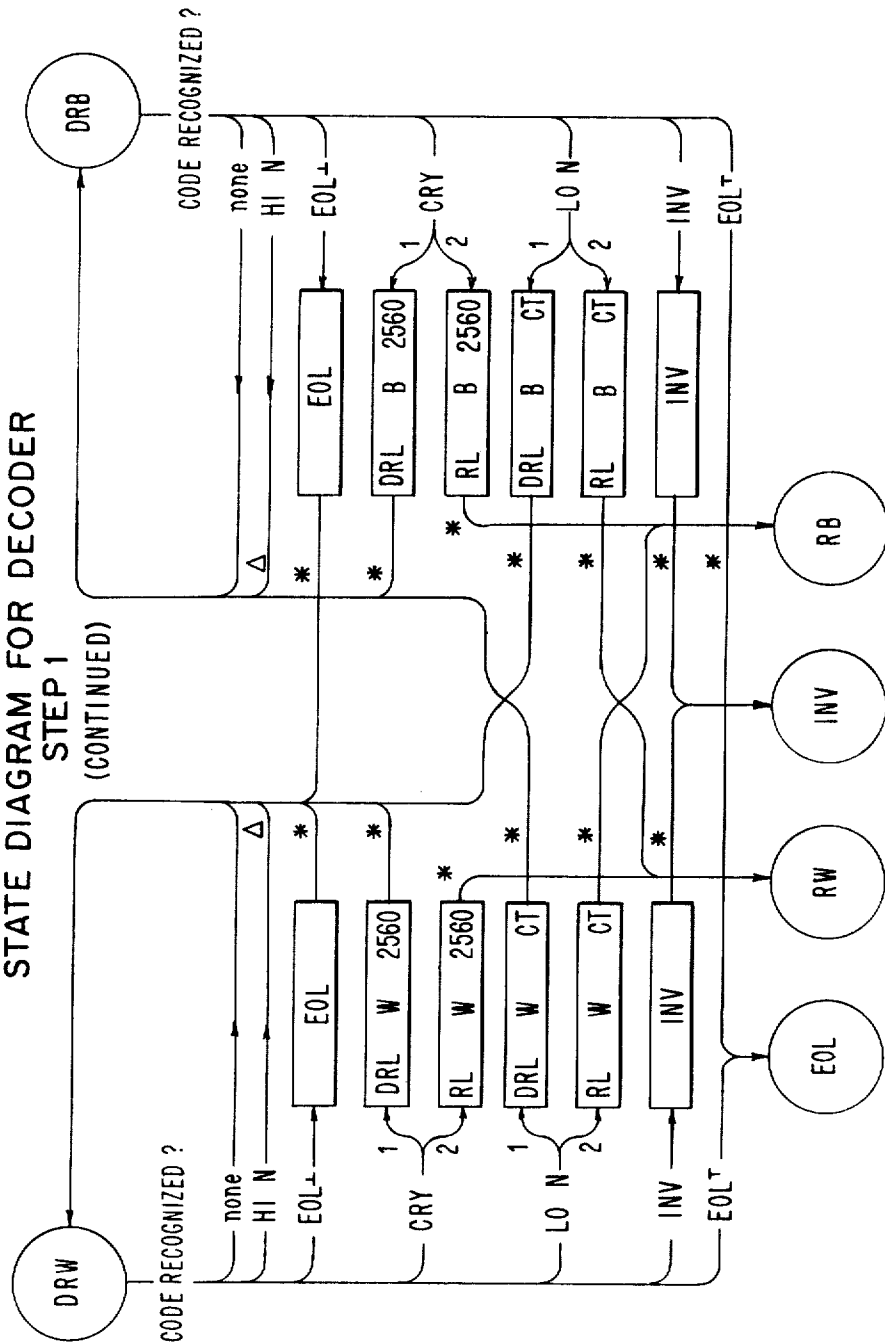
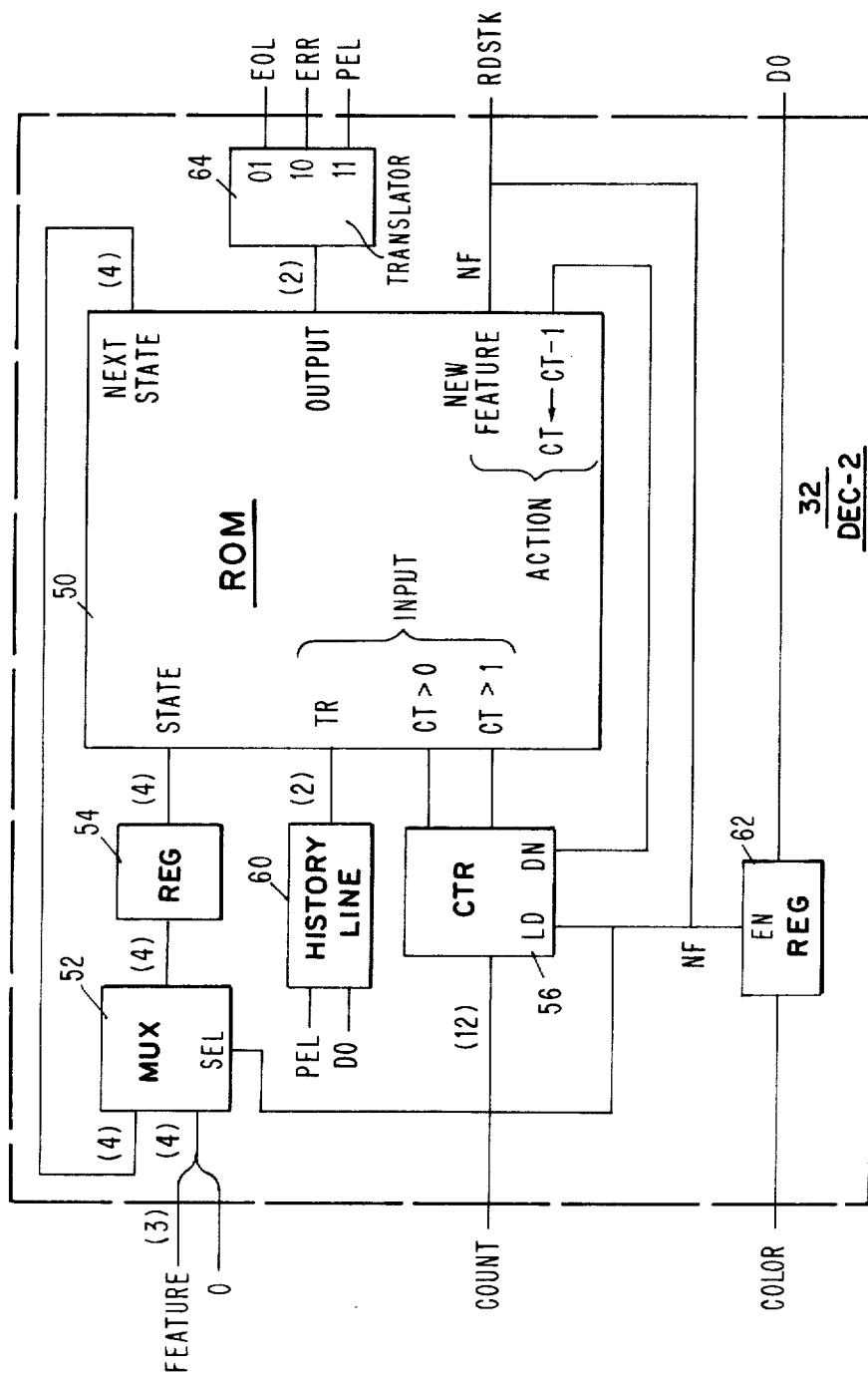


FIG. 12



DECODER STEP 2

