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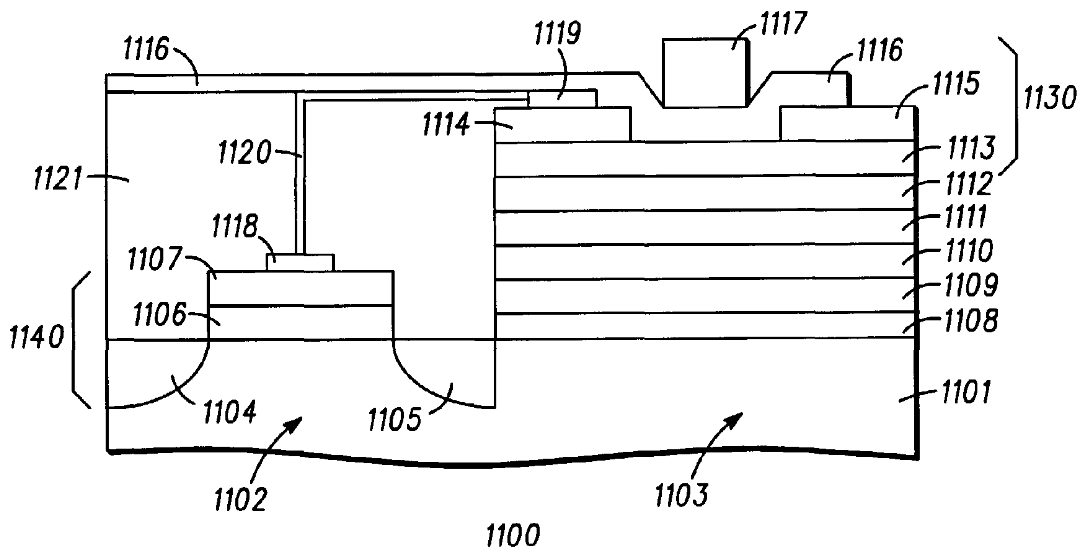

(57) Abstract: High quality epitaxial layers of compound semiconductor materials (1113) suitable for use in connection with Hall-effect devices can be grown overlying large silicon wafers (1101) by first growing an accommodating buffer layer (1110) on a silicon wafer. The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer (1109) of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer.

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COMPOUND SEMICONDUCTOR HALL SENSOR

FIELD OF THE INVENTION

5 This invention relates generally to semiconductor structures and devices and to a method for their fabrication, and more specifically to the fabrication and use of Hall sensors using compound semiconductor thin films, such as indium arsenide (InAs) and/or gallium arsenic antimonide (GaAsSb) thin films, grown on a monocrystalline semiconductor substrate.

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BACKGROUND OF THE INVENTION

The vast majority of semiconductor discrete devices and integrated circuits are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. Other semiconductor materials, such as the 15 so-called compound semiconductor materials, have physical attributes, including wider bandgap and/or higher mobility than silicon, or direct bandgaps that make these materials advantageous for certain types of semiconductor devices. Unfortunately, compound semiconductor materials are generally much more expensive than silicon and are not available in large wafers as is silicon. Gallium arsenide (GaAs), the most 20 readily available compound semiconductor material, is available in wafers only up to about 150 millimeters (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and are widely available at 200 mm. The 150 mm GaAs wafers are many times more expensive than are their silicon counterparts. Wafers of other compound semiconductor materials are even less available and are more expensive than 25 GaAs.

Because of the desirable characteristics of compound semiconductor materials, and because of their present generally high cost and low availability in bulk form, for many years attempts have been made to grow thin films of the compound semiconductor materials on a foreign substrate. To achieve optimal characteristics of 30 the compound semiconductor material, however, a monocrystalline film of high

crystalline quality is desired. Attempts have been made, for example, to grow layers of a monocrystalline compound semiconductor material on germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting
5 thin film of compound semiconductor material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline compound semiconductor material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in that film at a low cost compared to the cost of fabricating such devices on a bulk wafer of compound semiconductor material or in an
10 epitaxial film of such material on a bulk wafer of compound semiconductor material. In addition, if a thin film of high quality monocrystalline compound semiconductor material could be realized on a bulk wafer such as a silicon wafer, a monolithic integration of integrated devices, such as, for example, optoelectronic devices, such as laser diodes, light emitting diodes, photodiodes, or heterojunction tunnel devices, could
15 be achieved that took advantage of the best properties of both the silicon and the compound semiconductor material.

A Hall device, such as a Hall sensor, is normally a four-terminal device used for detecting a magnetic field. In a typical Hall sensor, a semiconductor layer has two electrodes for passing electrical current in a first direction through the semiconductor
20 layer, and two additional electrodes for detecting the voltage transverse to the electrical current at times when a magnetic field to be detected is passing through the semiconductor layer.

Hall sensors typically use n-type silicon when cost is of primary importance and GaAs for higher temperature capability due to its larger band gap. In addition, InAs,
25 indium antimonide (InSb), and other semiconductor materials are gaining popularity due to their high carrier mobilities that result in greater sensitivity and frequency response capabilities above the 10-20 kHz typical of silicon Hall sensors. For example, InAs Hall sensors have small temperature dependence of output voltage, good stability to pulse voltage noise, low offset drift and low noise properties for low
30 magnetic field sensing.

The demand for Hall sensors is rapidly growing due to the evolving electronics industry. As the demand increases, there is a need for materials that are highly sensitive, with a large electron mobility over a wide temperature range. Compatibility of the Hall sensor material with semiconductor substrates is important since Hall sensors are often used in integrated devices that include other semiconductor structures. InAs is a good material for use in Hall sensors due to its high electron mobility as compared with other III-V compound semiconductor materials. One difficulty in the past with InAs, however, is the lack of insulating substrates that are lattice matched with InAs to enable growth of high quality InAs thin films. For example, current InAs thin films grown by molecular beam epitaxy (MBE) on GaAs exhibit approximately 7% lattice mismatch, which creates many misfit dislocations at the InAs/GaAs interface, thus degrading the electronic properties of the InAs thin film, such as electron mobility.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline compound semiconductor film, such as InAs, over another monocrystalline material, such as GaAs or silicon, and for a process for making such a structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 - 3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer;

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer;

FIG. 9 illustrates schematically, in cross section, a monolithic integrated circuit in accordance with one embodiment of the invention; and

5 FIGS. 10-11 illustrate schematically, in cross section, device structures in accordance with further exemplary embodiments of the invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other 10 elements to help to improve understanding of embodiments of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention provides a template that reduces the lattice mismatch between InAs and an underlying insulating substrate to less than about 2% and provides 15 a method of growing the InAs over a semiconductor substrate or layer, thus allowing for monolithic integration of Hall sensors with complementary metal-oxide-silicon (CMOS) integrated circuits.

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor 20 structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall 25 include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes 30 an amorphous intermediate layer 28 positioned between substrate 22 and

accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous
5 intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material from Group
10 IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a
15 monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise
20 occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer.
25 Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with
30 the overlying compound semiconductor material. For example, the material could be an

oxide or nitride having a lattice structure substantially matched to the substrate and/or to the subsequently applied semiconductor material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 38 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG. 3,

which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or
5 orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For
10 example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials in the indium phosphide
15 (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-
20 arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of
25 zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice structure of the compound semiconductor material exhibits a 45 degree rotation with

respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

5 In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. 10 The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

15

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In 20 addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium 25 arsenide (InGaAs), an aluminum indium phosphide (AlInP), an indium gallium arsenide phosphide (InGaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, 30 wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case

may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as
5 those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this
10 embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is
15 especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated
20 in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer that is suitably formed of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as
25 described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1),which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application
30 and may depend on such factors as desired insulating properties of layer 36, type of

semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that
5 can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include
10 materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar
15 manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a
20 substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a
25 grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that tend to be polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host
30 crystal. As the mismatch in lattice constants increases, the thickness of achievable, high

quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

5 In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The
10 inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is
15 achievable.

Still referring to FIGS. 1 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate
20 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected
25 materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is

achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium
5 indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer
10 that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline
15 semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other
20 structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a
25 grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in

accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stoichiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the

strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of
5 oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in
10 lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material.
15 For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an
20 appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

25 FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed

which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using
5 accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is
10 formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of
15 either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and
20 growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now
25 amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and
30 semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of

about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26 may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration

enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, 5 and niobates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

10 Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by 15 the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to 20 react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to 25 react with the capping material to form a template for the deposition of a compound semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIG. 9 illustrates schematically, in cross section, a device structure 900 in accordance with a further embodiment of the invention. Device structure 900 includes 30 a monocrystalline semiconductor substrate 901, preferably a monocrystalline silicon

wafer. Monocrystalline semiconductor substrate 901 includes two regions, 902 and 903. An electrical semiconductor component generally indicated by the dashed line 911 is formed in region 902. Electrical component 911 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor, or an integrated circuit such as a MOS integrated circuit. For example, electrical component 911 can be a MOS circuit configured to perform digital signal processing or another function for which silicon integrated circuits are well suited. The electrical semiconductor component in region 902 can be formed by conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 904 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 911.

Insulating material 904 and any other layers that may have been formed or deposited during the processing of semiconductor component 911 in region 902 are removed from the surface of region 903 to provide a bare substrate surface in that region, for example, a bare silicon surface. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide layer can quickly form on the bare surface. Optionally, a layer of barium or barium and oxygen may be deposited onto the native oxide layer on the surface of region 903 and then reacted with the oxidized surface to form a template layer 907. In accordance with one embodiment of the invention, a monocrystalline oxide layer 906 is formed overlying the template layer by a process of molecular beam epitaxy (MBE). In one aspect of this exemplary embodiment, reactants including barium, titanium, and oxygen are deposited on the template layer to form the monocrystalline oxide layer. Initially during the deposition, the partial pressure of oxygen is kept near the minimum necessary to fully react with the barium and titanium to form a monocrystalline barium titanate layer 906. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the barium titanate reacts with silicon at the surface of region 903 to form an amorphous layer 905 at the interface between the silicon substrate and the monocrystalline oxide. Alternatively, an amorphous oxide layer comprising material from layer 905 and 906

can be formed by epitaxially forming a monocrystalline oxide layer 906 and subsequently heat treating the resulting structure to convert the monocrystalline oxide to an amorphous oxide, as discussed below.

In accordance with one embodiment of the invention, the step of depositing the monocrystalline oxide layer 906 is followed by depositing an intermediate oxide transition layer 908. Transition layer 908 generally comprises an ordered, crystalline metal oxide, such as magnesium oxide (MgO), tantalum oxide (TaO), or manganese oxide (MnO), and is preferably grown by an MBE process. The step of depositing the transition layer 908 is followed by depositing a second template layer 909, which can be, for example, 1-10 monolayers of gallium antimonide (GaSb), InMgO, or MgAsO. Template layer 909 serves as a "seed" layer to aid in formation of an overlying monocrystalline compound semiconductor layer 910. In a preferred embodiment, monocrystalline compound semiconductor layer 910 comprises a semiconductor material particularly suitable for use in the formation of highly reliable, sensitive Hall sensor devices, such as InAs or GaAsSb.

In accordance with one aspect of the present embodiment, after formation of layer 908, the monocrystalline titanate layer and the silicon oxide layer, which is interposed between substrate 901 and the titanate layer, are exposed to an anneal process such that the titanate and oxide layers form an amorphous oxide layer. An additional compound semiconductor layer 910 is then epitaxially grown over layers 908 and 909. Alternatively, the above described anneal process can be performed after formation of template layer 909 or compound semiconductor layer 910.

In accordance with a further embodiment of the invention, a semiconductor component, generally indicated by a dashed line 912, is formed in compound semiconductor layer 910. Semiconductor component 912 can be formed by processing steps conventionally used in the fabrication of indium arsenide or other III-V compound semiconductor material devices. Semiconductor component 912 may be any active or passive component, and preferably is a Hall sensor, tunnel diode, light emitting diode, semiconductor laser, photodetector, heterojunction bipolar transistor (HBT), high frequency MESFET, or other component that utilizes and takes advantage of the

physical properties of compound semiconductor materials. A metallic conductor schematically indicated by the line 913 can be formed to electrically couple device 912 and device 911, thus implementing an integrated device that includes at least one component formed in the silicon substrate and one device formed in the
5 monocrystalline compound semiconductor material layer. Although illustrative structure 900 has been described as a structure formed on a silicon substrate 901 and having a barium titanate layer 906 and an InAs or GaAsSb layer 910, similar devices can be fabricated using other monocrystalline substrates, monocrystalline oxide layers and other monocrystalline compound semiconductor layers as described elsewhere in
10 this disclosure.

FIG. 10 illustrates a semiconductor structure 1000 in accordance with a further embodiment of the invention. In this embodiment, structure 1000 is a Hall sensor formed of monocrystalline epitaxial layers of compound semiconductor material on a monocrystalline silicon substrate. Structure 1000 includes a monocrystalline
15 semiconductor substrate 1001, such as a monocrystalline silicon wafer. An amorphous oxide layer 1002 is preferably formed overlying substrate 1001, in accordance with the process described above. An accommodating buffer layer 1003 is formed overlying substrate 1001 and amorphous oxide layer 1002. As described above, amorphous oxide layer 1002 may be grown at the interface between substrate 1001 and the growing
20 accommodating buffer layer 1003 by the oxidation of substrate 1001 during the growing of layer 1003. Accommodating buffer layer 1003 is preferably a monocrystalline oxide material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. In this embodiment, wherein substrate 1001 is monocrystalline silicon and the overlying compound semiconductor
25 material layer is monocrystalline InAs, layer 1003 may comprise, for example, an alkali earth metal titanate such as barium titanate or strontium titanate, an alkali earth metal hafnate such as barium hafnate or strontium hafnate, or an alkali earth metal zirconate such as barium zirconate or strontium zirconate.

An intermediate oxide transition layer 1004 is preferably formed overlying layer
30 1003 to alleviate any strains that might result from a mismatch of the crystal lattice of

accommodating buffer layer 1003 and the lattice of the monocrystalline semiconductor material layer. Transition layer 1004 can comprise any suitable oxide material, such as manganese oxide (MnO), magnesium oxide (MgO), or tantalum oxide (TaO). In this exemplary embodiment, transition layer 1004 is a layer of MgO and can have a
5 thickness of about 10 to about 100 nm and preferably a thickness of about 50 nm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the indium arsenide on the monocrystalline oxide, a template layer 1005 may be formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ga-Sb, Ga-Mg-O-Sb, In-Mg-O, or Mg-As-O.

10 A monocrystalline compound semiconductor material layer 1006 is then formed overlying template layer 1005, preferably by MBE. Compound semiconductor material layer 1006 preferably comprises a material that is highly sensitive and has a large electron mobility over a wide temperature range, such as InAs or GaAsSb. In this preferred embodiment of the invention, layer 1006 comprises a layer of InAs having a
15 thickness of from about 10 to 1000 nm.

In accordance with the exemplary embodiment of the invention illustrated in FIG. 10, semiconductor device structure 1000 comprises an InAs Hall sensor device. Structures and methods of fabricating InAs Hall sensor devices are well known to those skilled in the art. As illustrated in FIG. 10, after formation of InAs layer 1006, spaced-
20 apart conductive electrodes 1007 and 1008 are formed overlying layer 1006 in accordance with well-known fabrication techniques. A passivation layer 1009 is formed overlying electrodes 1007 and 1008 and insulates the region between the electrodes. A floating semiconductor device 1010 is then formed on passivation layer 1009 and may comprises any suitable device known in the art, such as, for example, an
25 accelerometer. Electrical connections may then be made to the devices according to conventional techniques available to those skilled in the art. If device 1010 is desirably formed of monocrystalline material, then layer 1009 is preferably monocrystalline.

Referring now to FIG. 11, a monolithic integrated circuit is provided in accordance with one embodiment of the present invention. Monolithic integrated
30 circuit 1100 generally includes a MOS circuit 1140 electrically coupled to a Hall sensor.

In FIG. 11, for illustration purposes only, and without limitation, MOS circuit 1140 is electrically coupled to an InAs Hall sensor 1130, such as that exhibited in FIG. 10. In this embodiment, semiconductor substrate 1101 is a monocrystalline silicon substrate, such as a silicon wafer, and has two regions, 1102 and 1103.

5 In accordance with this embodiment of the invention, template layer 1108, amorphous oxide layer 1109, monocrystalline oxide layer 1110, intermediate oxide transition layer 1111, template layer 1112, monocrystalline compound semiconductor material layer 1113, and electrodes 1114 and 1115 are formed of the same materials and by the same processing steps as those described with reference to the fabrication of the

10 Hall sensor device of FIG. 10. For sake of brevity, formation of these components will not be discussed additionally with relation to FIG. 11.

In accordance with the present embodiment of the invention, MOS circuit 1140 is first formed in semiconductor substrate 1101 using conventional processing steps and techniques well known to those skilled in the art. MOS circuit 1140 generally

15 comprises a gate electrode 1107, a gate dielectric layer 1106, and n+ doped regions 1104 and 1105. Gate dielectric layer 1106 is formed in region 1102 of substrate 1101, and gate electrode 1107 is then formed over gate dielectric layer 1106. Selective n-type doping is performed to form n+ doped regions 1104 and 1105 within substrate 1101 along adjacent sides of gate electrode 1107 and are source, drain, or source/drain

20 regions for the MOS transistor. The n+ doped regions 1104 and 1105 have a doping concentration of at least about 1E18 atoms per cubic centimeter. After formation of MOS portion 1140 of the integrated circuit, all of the layers formed during processing are removed from the surface of substrate 1101 in region 1103 where Hall sensor 1130 will be formed. A bare silicon surface is thus provided for the subsequent processing of

25 Hall sensor 1130, for example in the manner set forth above.

After formation of both MOS circuit 1140 and Hall sensor 1130 on substrate 1101, processing continues to form a substantially completed integrated circuit 1100. Ohmic contacts 1118 and 1119 may be formed on gate electrode 1107 and electrode 1114, respectively, using standard processing techniques well known in the art. An

30 insulating layer 1121 is formed over substrate 1101, MOS circuit 1140, and Hall sensor

1130. Portions of insulating layer 1121 are then removed to define contact openings where the devices are to be interconnected. Interconnect trenches are formed within insulating layer 1121 to provide the lateral connections between the contacts. As illustrated in FIG. 11, interconnect 1120 connects the gate electrode of the MOS transistor to an electrode 1114 of Hall sensor 1130. A passivation layer 1116 is formed over the interconnect 1120 and insulating layer 1121. Following formation of passivation layer 1116, device 1117 may be formed on Hall sensor 1130 in the region defined by electrodes 1114 and 1115. Device 1117 may be any floating device suitable for use in connection with Hall sensor 1130, such as, for example, an accelerometer. Other electrical connections may be made to the devices and/or other electrical or electronic components within the integrated circuit 1100 but not illustrated in the figure according to conventional techniques available to those skilled in the art.

Clearly, these embodiments of integrated circuits having compound semiconductor portions and Group IV semiconductor portions are meant to illustrate embodiments of the present invention and do not limit the present invention. There are a multiplicity of other combinations of semiconductor devices and other embodiments of the present invention that come within the present disclosure. For example, the compound semiconductor portion may include light emitting diodes, photodetectors, diodes, or the like, and the Group IV semiconductor portions can include digital logic, memory arrays, and most structures that can be formed in conventional MOS integrated circuits. By using embodiments of the present invention, it is now simpler to integrate devices that work better in compound semiconductor materials with other components that work better or are easily and/or inexpensively formed within Group IV semiconductor materials. This allows the device size to decrease, the manufacturing costs to decrease, and yield and reliability to increase.

As contemplated in the above description, a monocrystalline Group IV wafer can also be used in forming only compound semiconductor electrical components over the wafer. In this manner, the wafer is essentially a "handle" wafer used during the fabrication of the compound semiconductor electrical components within a monocrystalline compound semiconductor layer overlying the wafer. Therefore,

electrical components can be formed within II-V or II-IV semiconductor materials over a wafer of at least approximately 200 millimeters in diameter and possibly at least approximately 300 millimeters.

By the use of this type of substrate, a relatively inexpensive "handle" wafer overcomes the fragile nature of the compound semiconductor wafers by placing them over a relatively more durable and easy to fabricate base material. Therefore, an integrated circuit can be formed such that all electrical components, and particularly all active electronic devices, can be formed within the compound semiconductor material even though the substrate itself may include a Group IV semiconductor material. Fabrication costs for compound semiconductor devices should decrease because larger substrates can be processed more economically and more readily compared to relatively smaller and more fragile conventional compound semiconductor wafers.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. For example, use of Sb-based materials, such as indium antimonide (InSb), aluminum antimonide (AlSb), indium aluminum antimonide (InAlSb), gallium antimonide (GaSb), indium gallium antimonide (InGaSb), and aluminum gallium antimonide (AlGaSb) for a Hall-effect active layer is possible in accordance with the present invention. As those skilled in the art will appreciate, the present invention may be applicable to any Hall effect device or other semiconductor device structures in any III-V or other compound semiconductor that can be lattice-matched to silicon using a perovskite or other appropriate oxide.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical,

required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other
5 elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A monolithic integrated circuit comprising:

a MOS circuit formed at least partially in a monocrystalline substrate;

a monocrystalline compound semiconductor layer overlying the monocrystalline
5 substrate; and

a Hall sensor formed at least partially in the monocrystalline compound semiconductor layer, the Hall sensor electrically coupled to the MOS circuit.

2. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises
10 a MOS transistor having a gate electrode and the Hall sensor is electrically coupled to the gate electrode.

3. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises a digital circuit.

15

4. The monolithic integrated circuit of claim 1 wherein the Hall sensor comprises an InAs layer.

5. The monolithic integrated circuit of claim 1 wherein the Hall sensor comprises a
20 GaAsSb layer.

6. A semiconductor device comprising:
a monocrystalline semiconductor substrate;
an oxide layer formed overlying the substrate;
a monocrystalline compound semiconductor layer formed overlying the oxide
5 layer; and
a Hall sensor formed at least partially in the monocrystalline compound semiconductor layer.

7. The semiconductor device of claim 6 further comprising an intermediate
10 crystalline oxide transition layer interposed between the oxide layer and the monocrystalline compound semiconductor layer.

8. The semiconductor device of claim 6 further comprising a template layer interposed between the transition layer and the monocrystalline compound
15 semiconductor layer.

9. The semiconductor device of claim 6 wherein the monocrystalline compound semiconductor layer comprises a material selected from the group consisting of InAs, GaAsSb, and InSb.

20

10. The semiconductor device of claim 7 wherein the intermediate crystalline oxide transition layer comprises a material selected from the group consisting of MgO, TaO, and MnO.

25 11. The semiconductor device of claim 8 wherein the template layer comprises a material selected from the group consisting of GaSb, InMgO, and MgAsO.

12. The semiconductor device of claim 6 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth
30 metal zirconates, and alkali earth metal hafnates.

13. The semiconductor device of claim 6 wherein the oxide layer comprises an oxide selected from the group consisting of $BaTiO_3$, $BaZrO_3$, $BaHfO_3$, $SrHfO_3$, and $SrZrO_3$.

5

14. The semiconductor device of claim 6 wherein the oxide layer comprises an amorphous oxide layer.

15. The semiconductor device of claim 14 wherein the oxide layer comprises an
10 amorphous oxide formed epitaxially as a monocrystalline oxide layer and subsequently heat treated to convert the monocrystalline oxide to an amorphous oxide.

16. The semiconductor device of claim 6 wherein the substrate comprises silicon.

15 17. The semiconductor device of claim 16 further comprising an amorphous silicon oxide formed underlying the oxide layer.

18. The semiconductor device of claim 6 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.

20

19. A process for fabricating a semiconductor device comprising the steps of:
providing a monocrystalline semiconductor substrate;
epitaxially growing a layer of monocrystalline oxide overlying the substrate;
growing a monocrystalline compound semiconductor structure overlying the
5 monocrystalline oxide, the monocrystalline compound semiconductor structure comprising an intermediate oxide transition layer, a template layer, and a monocrystalline compound semiconductor layer; and
forming a Hall sensor at least partially within the monocrystalline compound semiconductor structure.

10

20. The process of claim 19 further comprising the step of forming an amorphous oxide layer underlying the layer of monocrystalline oxide during the step of epitaxially growing.

15 21. The process of claim 20 further comprising the step of thermally annealing the layer of monocrystalline oxide to convert the monocrystalline oxide to a further layer of amorphous oxide.

22. The process of claim 19 wherein the step of growing a monocrystalline
20 compound semiconductor structure comprises the step of growing by a process selected from the group consisting of MBE, MOCVD, CVD, MEE, ALE, PVD, PLD, and CSD.

23. The process of claim 19 wherein the step of providing a semiconductor substrate comprises the step of providing a monocrystalline substrate comprising silicon.

25

24. The process of claim 23 further comprising the steps of:
forming a digital integrated circuit at least partially within the substrate; and
forming an interconnection electrically interconnecting the digital integrated circuit and the Hall sensor.

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25. The process of claim 24 wherein the step of forming a digital integrated circuit comprises the step of forming a MOS transistor having a gate electrode and the Hall sensor is electrically coupled to the gate electrode.

5 26. A process for fabricating a semiconductor device comprising the steps of:
providing a monocrystalline semiconductor substrate;
epitaxially growing a layer of monocrystalline oxide overlying the substrate;
growing a monocrystalline compound semiconductor structure overlying the monocrystalline oxide, the monocrystalline compound semiconductor structure
10 comprising an intermediate oxide transition layer, a template layer, and a monocrystalline compound semiconductor layer, wherein the monocrystalline compound semiconductor layer comprises InAs; and
forming a Hall sensor at least partially within the monocrystalline compound semiconductor structure.

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27. The process of claim 26 further comprising the step of forming an amorphous oxide layer underlying the layer of monocrystalline oxide during the step of epitaxially growing.

20 28. The process of claim 27 further comprising the step of thermally annealing the layer of monocrystalline oxide to convert the monocrystalline oxide to a further layer of amorphous oxide.

29. The process of claim 26 wherein the step of growing a monocrystalline
25 compound semiconductor structure comprises the step of growing by a process selected from the group consisting of MBE, MOCVD, CVD, MEE, ALE, PVD, PLD, and CSD.

30. The process of claim 26 further comprising the steps of:
forming a digital integrated circuit at least partially within the substrate; and

forming an interconnection electrically interconnecting the digital integrated circuit and the Hall sensor.

31. The process of claim 30 wherein the step of forming a digital integrated circuit
5 comprises the step of forming a MOS transistor having a gate electrode and the Hall sensor is electrically coupled to the gate electrode.

32. A process for fabricating a semiconductor device comprising the steps of:
providing a monocrystalline silicon substrate;
forming a CMOS circuit at least partially within the silicon substrate, the CMOS circuit comprising a MOS transistor having a gate electrode;
5 epitaxially growing a layer of monocrystalline oxide overlying the substrate;
forming an amorphous layer of silicon oxide underlying the layer of monocrystalline oxide during the step of epitaxially growing;
forming an intermediate oxide transition layer overlying the layer of monocrystalline oxide;
10 growing a monocrystalline compound semiconductor structure overlying the transition layer;
heat treating the layer of monocrystalline oxide to convert the monocrystalline oxide to an additional layer of amorphous oxide;
forming a Hall sensor at least partially from the monocrystalline compound
15 semiconductor structure; and
forming an electrical interconnection between the Hall sensor and the gate electrode.

33. The process of claim 32 wherein the step of epitaxially growing a layer of
20 monocrystalline oxide comprises the step of epitaxially growing a layer of oxide selected from the group consisting of: alkali earth metal titanates, alkali earth metal hafnates, and alkali earth metal zirconates.

34. The process of claim 33 wherein the step of epitaxially growing a layer of
25 monocrystalline oxide comprises the step of epitaxially growing a layer of $BaTiO_3$.

35. The process of claim 32 further comprising the step of forming a template layer interposed between the transition layer and the monocrystalline compound semiconductor structure.

30

36. The process of claim 35 wherein the step of forming a template layer comprises forming a template layer comprising a material selected from the group consisting of GaSb, InMgO, and MgAsO.

5 37. The process of claim 32 wherein the step of forming an intermediate oxide transition layer comprises forming a transition layer of oxide selected from the group consisting of MgO, MnO, and TaO.

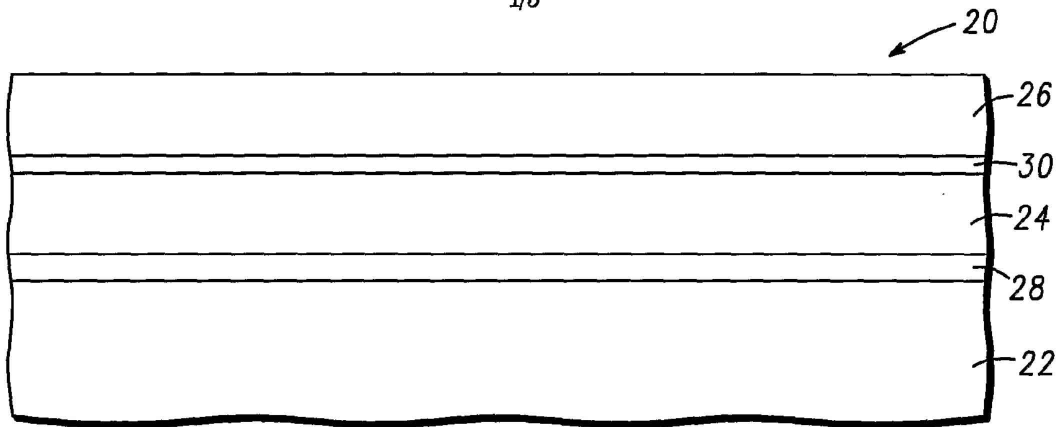

FIG. 1

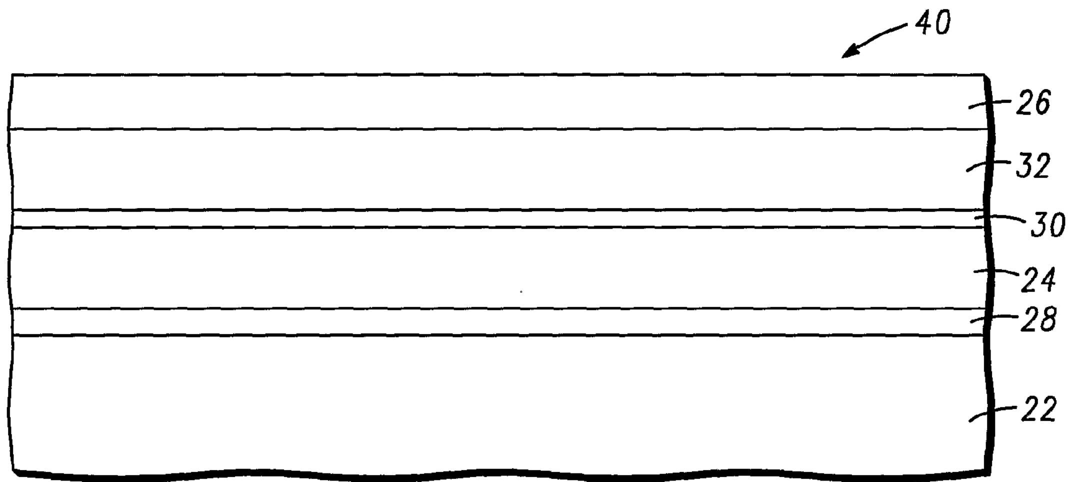

FIG. 2

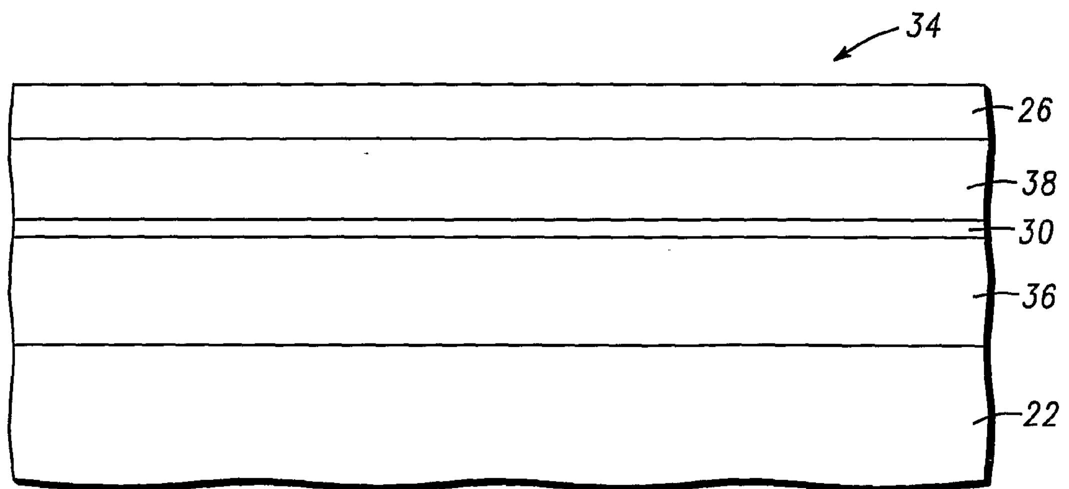

FIG. 3

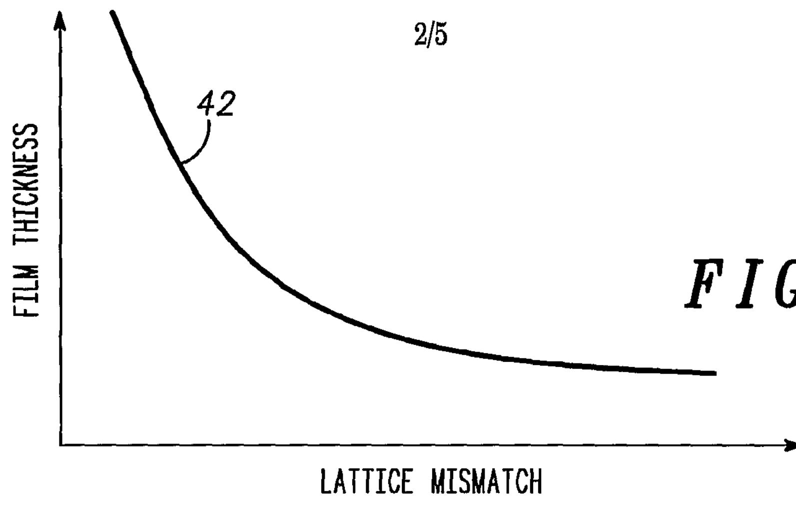

FIG. 4

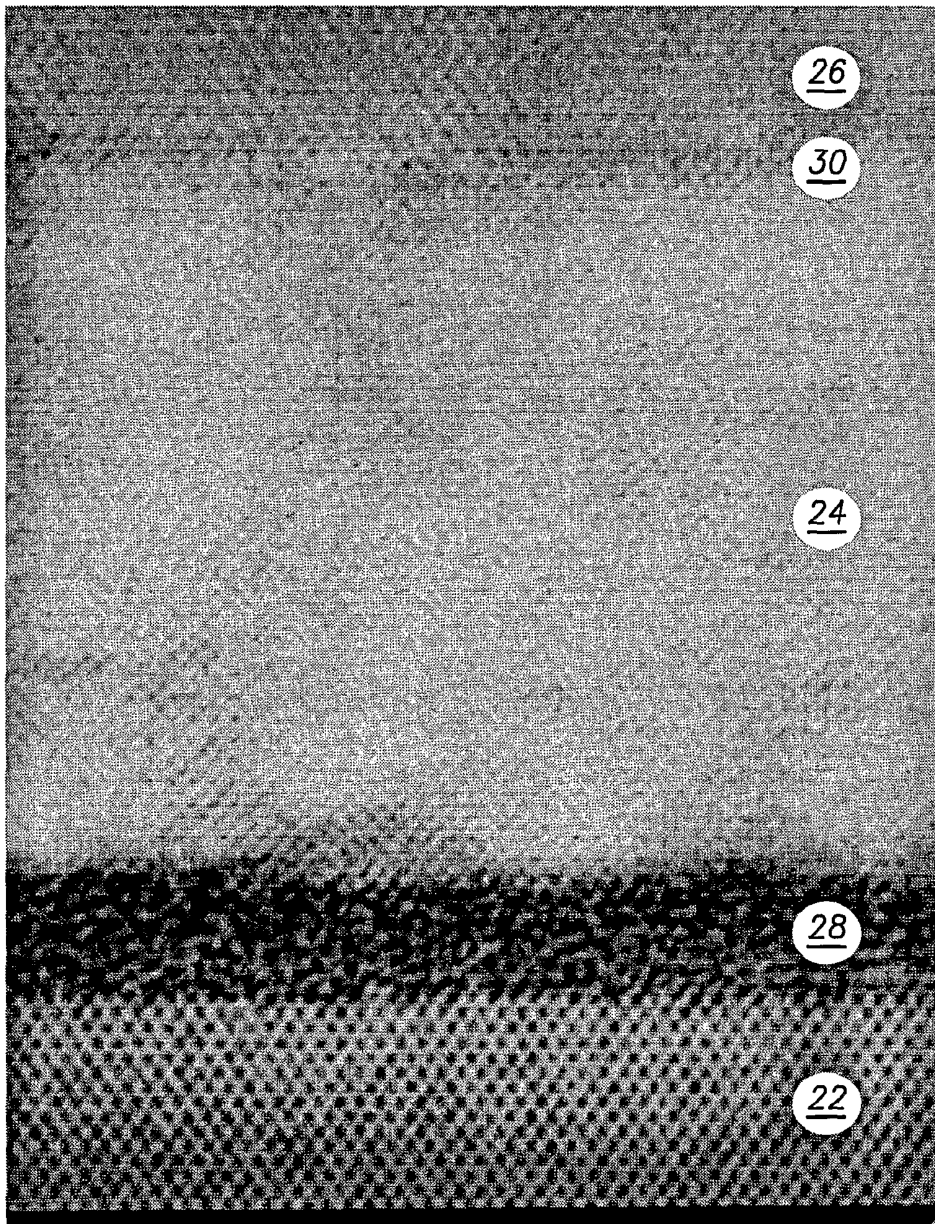

FIG. 5

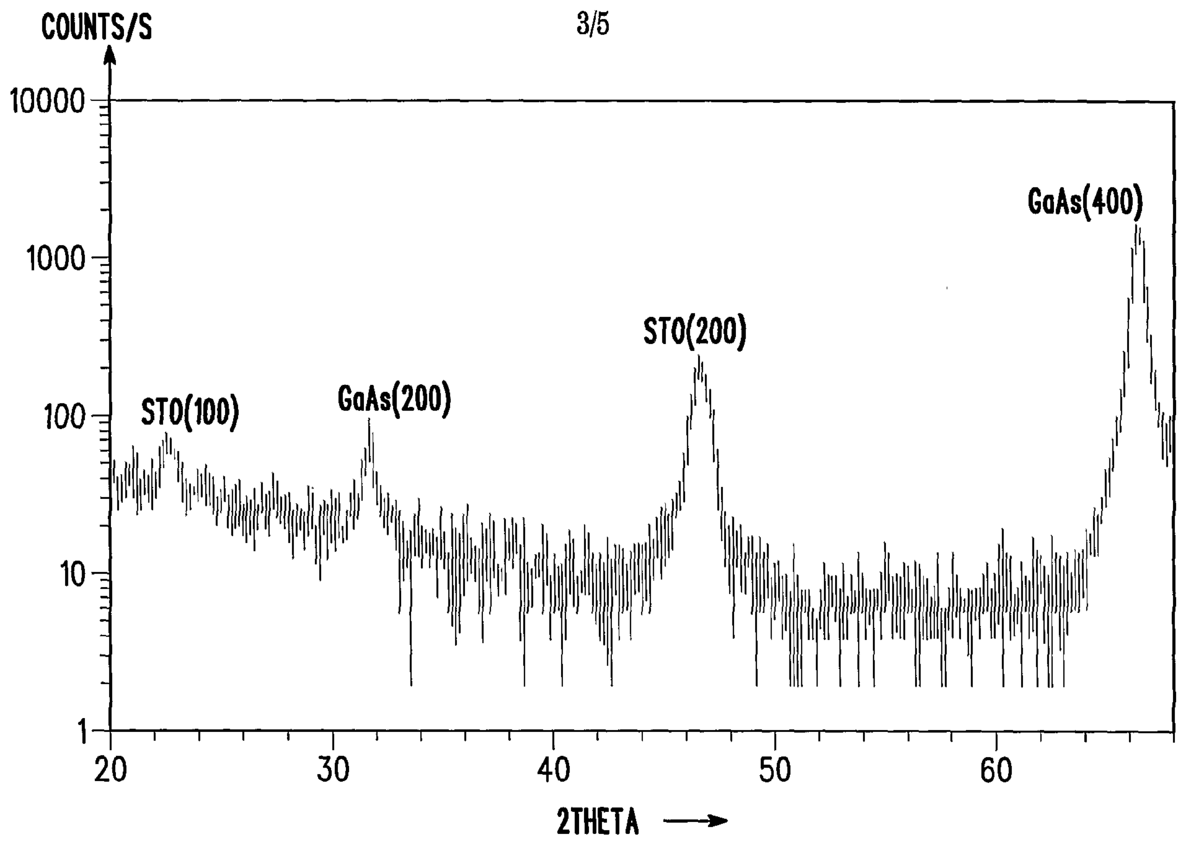

FIG. 6

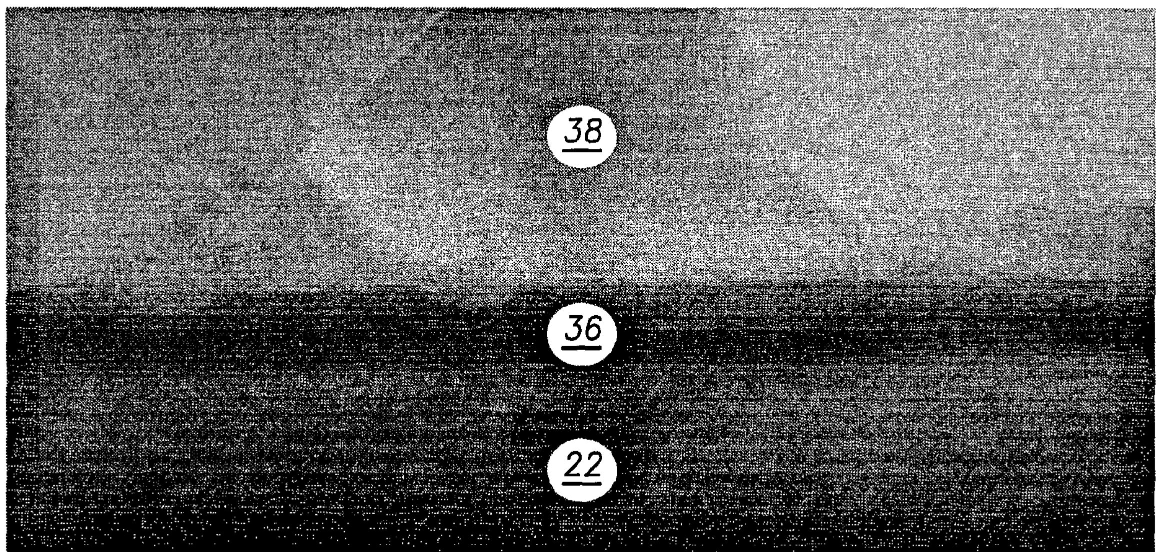

FIG. 7

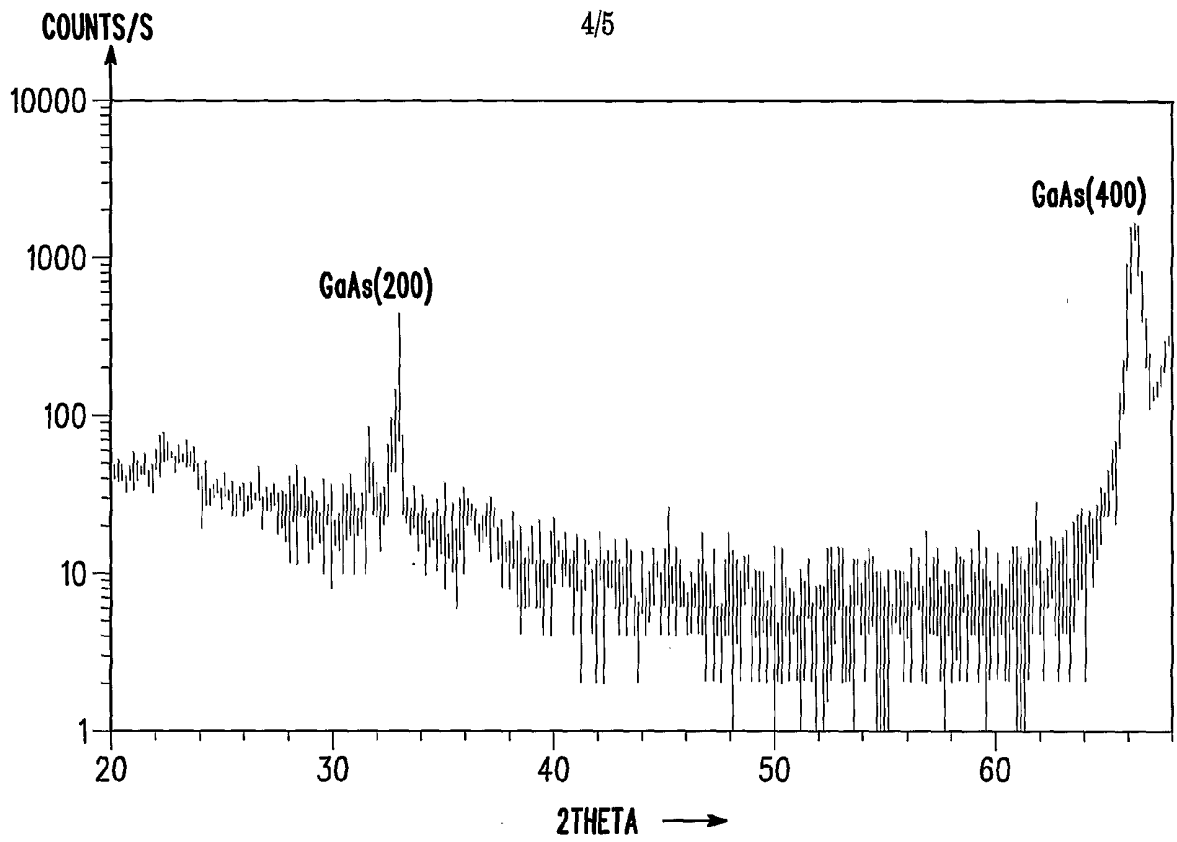

FIG. 8

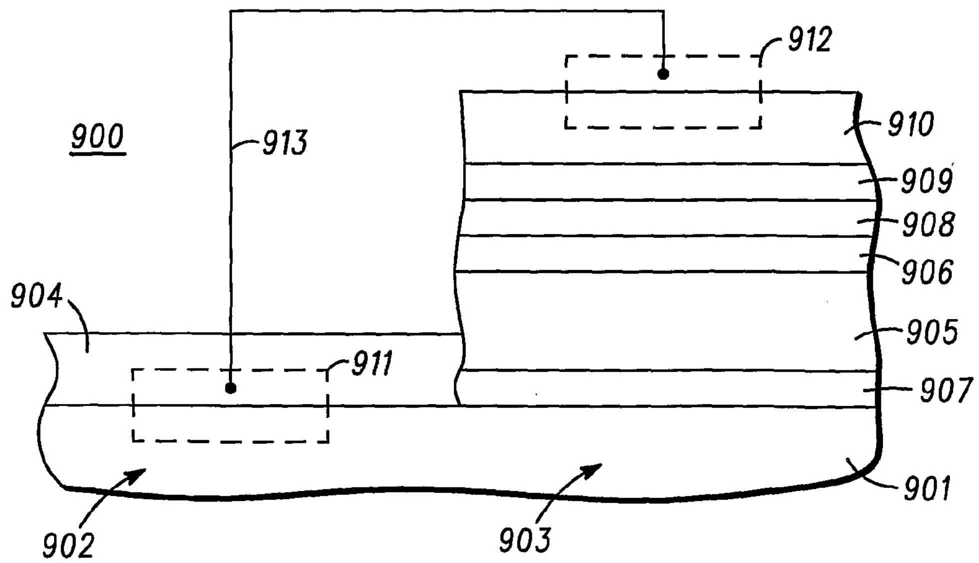

FIG. 9

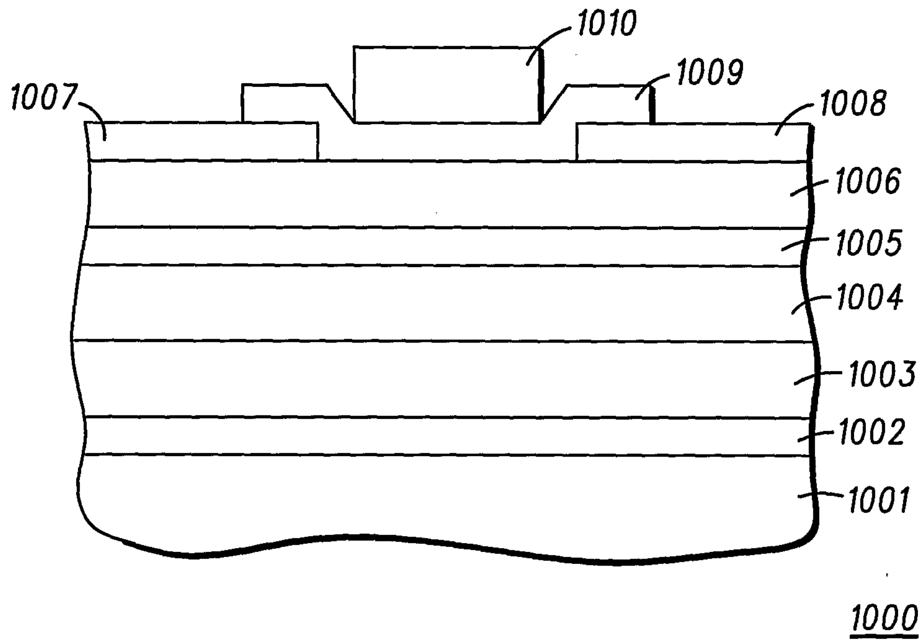

FIG. 10

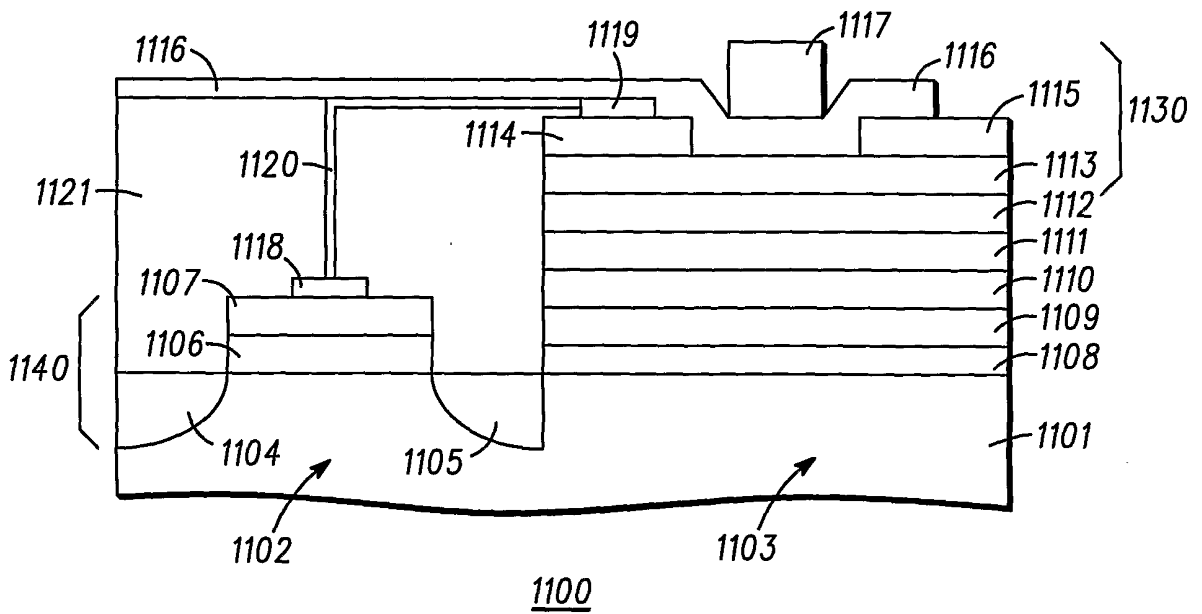

FIG. 11