July 8, 1969 G. W. KINZELMAN 3,454,926

DUAL-CHANNEL SYSTEM FOR SETTING DIGITAL ELECTRONIC TIMERS

Filed Dec. 22, 1965 Sheet 1 of 4

FIG. 1.

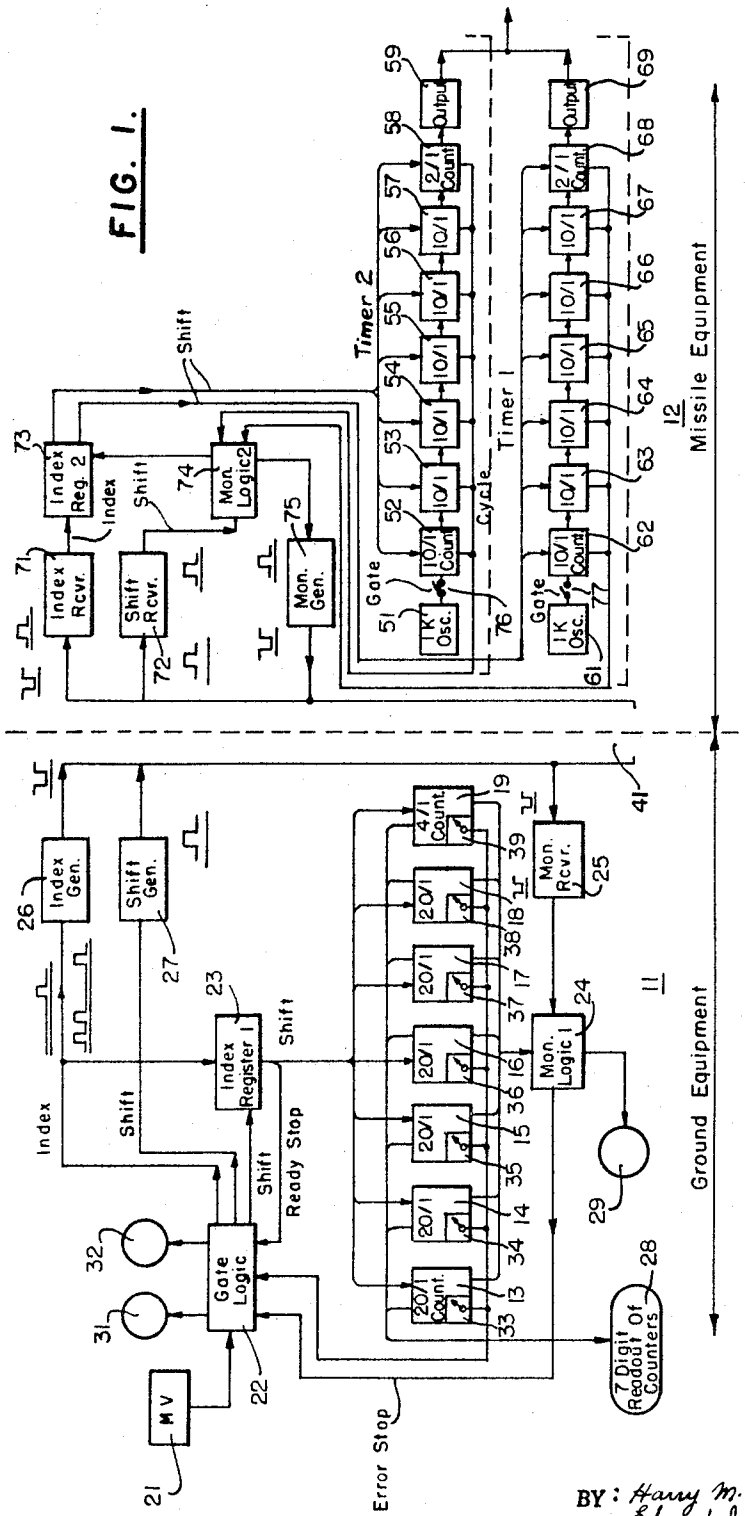



FIG. 2B.

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 9 | H | H | H | H | A E |
| 8 | L | H | H | H | A B C D E |
| 7 | L | L | H | H | B C D E |
| 6 | L | L | L | H | C D E |
| 5 | L | L | L | L | D E |
| 4 | L | L | L | L | A E |
| 3 | H | H | L | L | A B C D E |
| 2 | H | H | H | L | D E |
| 1 | H | H | H | H | A E |
| 0 | H | H | H | H | A B C D E |

FIG. 2A.

| | A | B | C | D |
|---|---|---|---|---|
| 1 | H | H | H | A D |
| 2 | L | H | H | H A B C D |
| 3 | L | L | H | H B C D |
| 4 | L | L | L | H C D |
| 5 | L | L | L | L A B C D |
| 6 | H | H | L | L A B C |
| 7 | H | H | H | L C |
| 8 | H | H | H | H |

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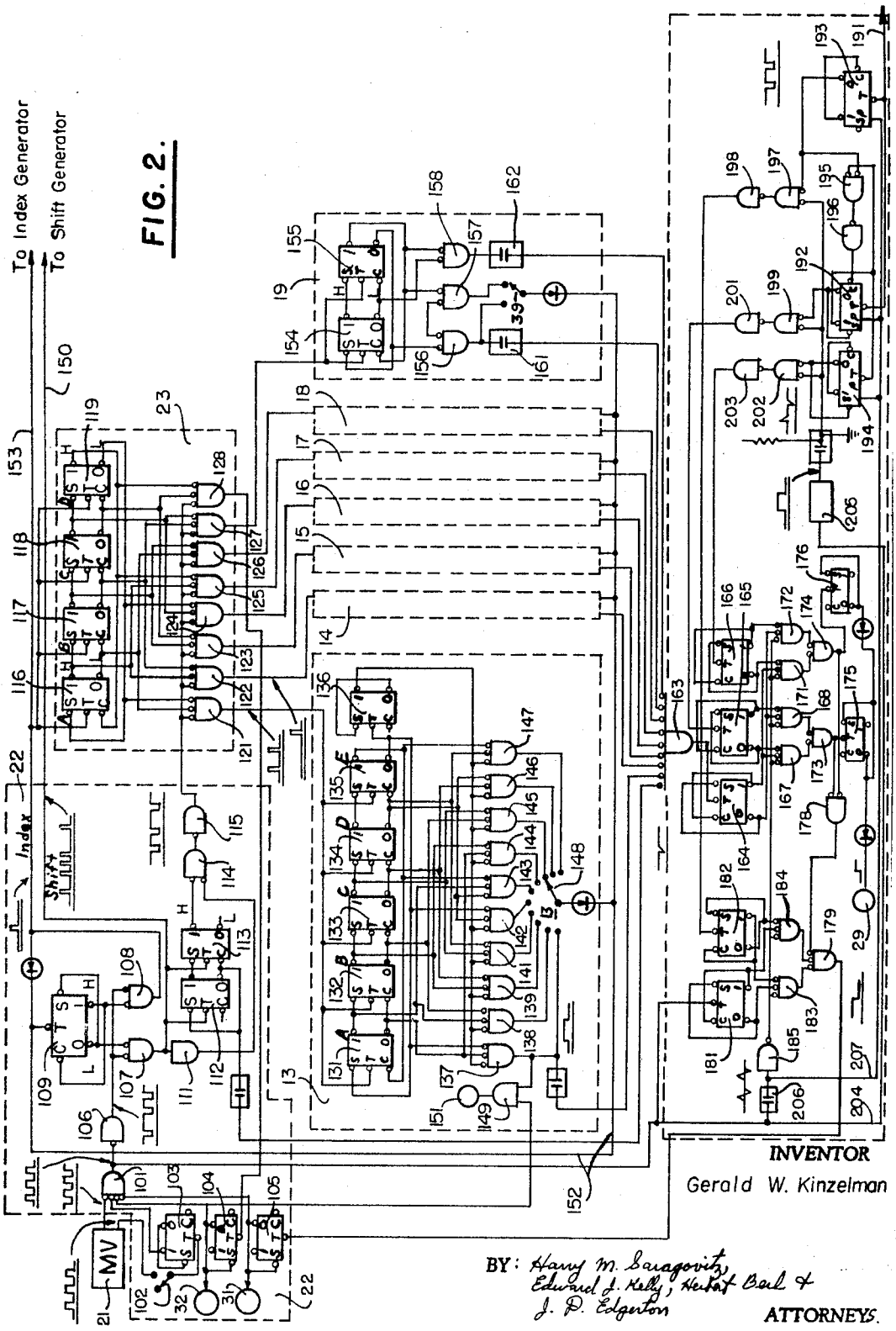
BY: Harry M. Saragovitz, Edward J. Kelly, Herbert Berl & J. D. Edgerton
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DUAL-CHANNEL SYSTEM FOR SETTING DIGITAL ELECTRONIC TIMERS

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FIG. 2.




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DUAL-CHANNEL SYSTEM FOR SETTING DIGITAL ELECTRONIC TIMERS

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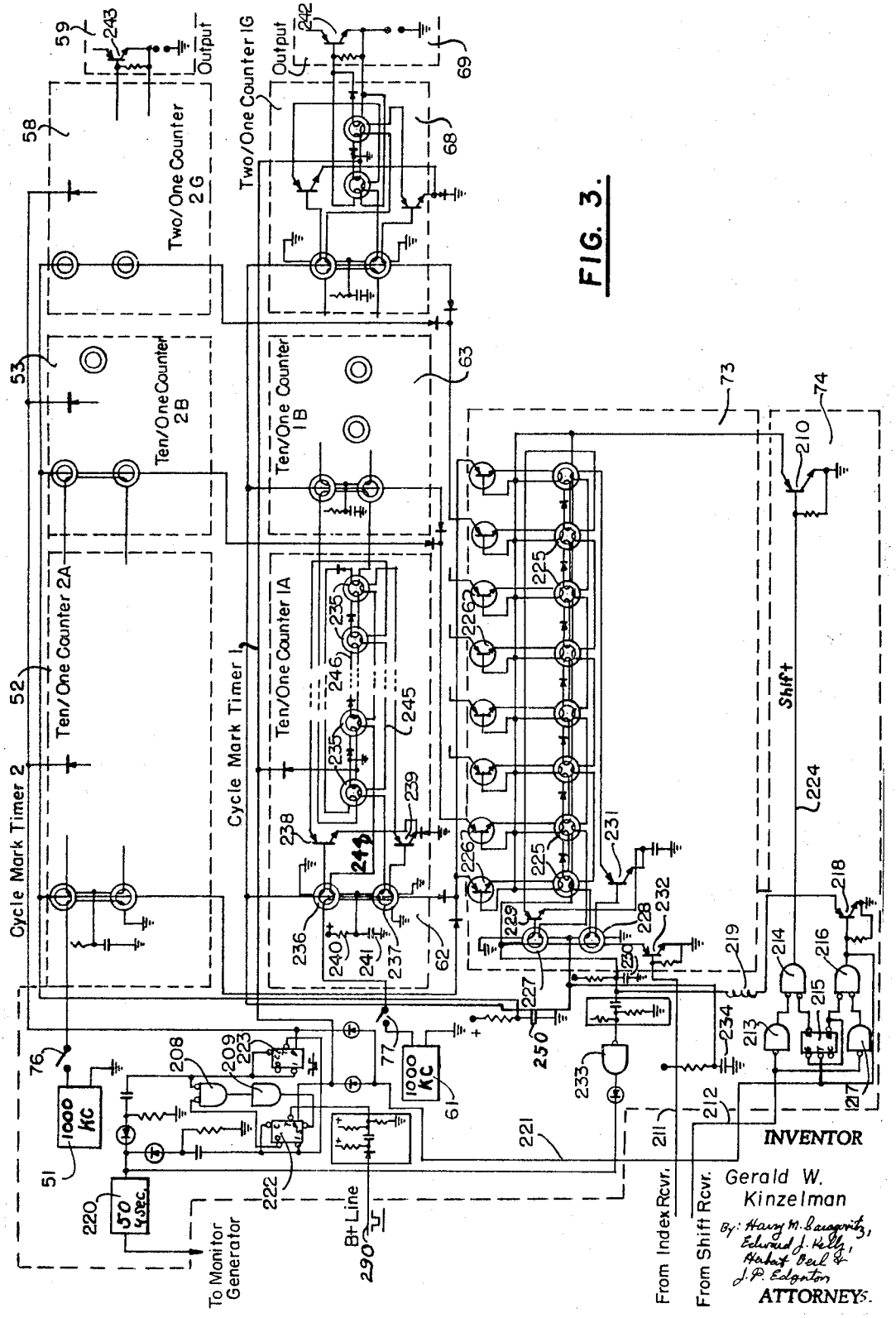



FIG. 3.

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DUAL-CHANNEL SYSTEM FOR SETTING DIGITAL ELECTRONIC TIMERS

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FIG. 5.

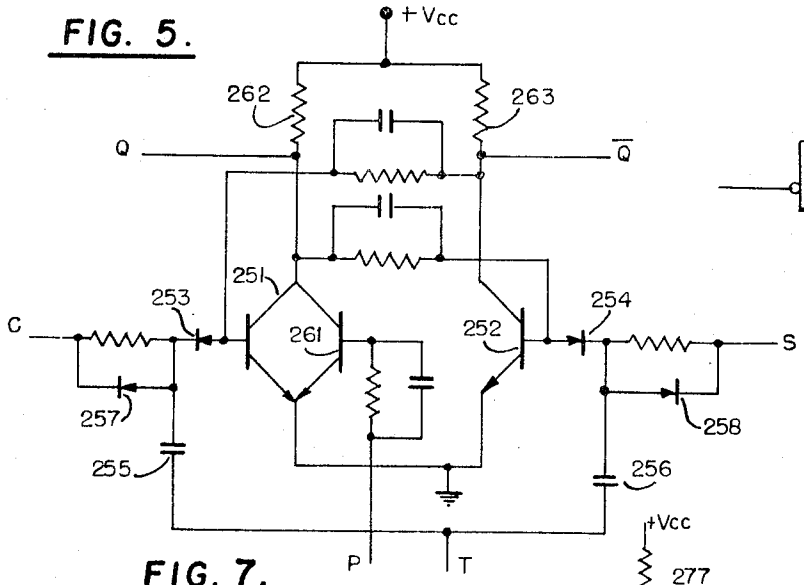



FIG. 4.

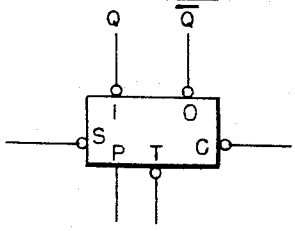



FIG. 7.

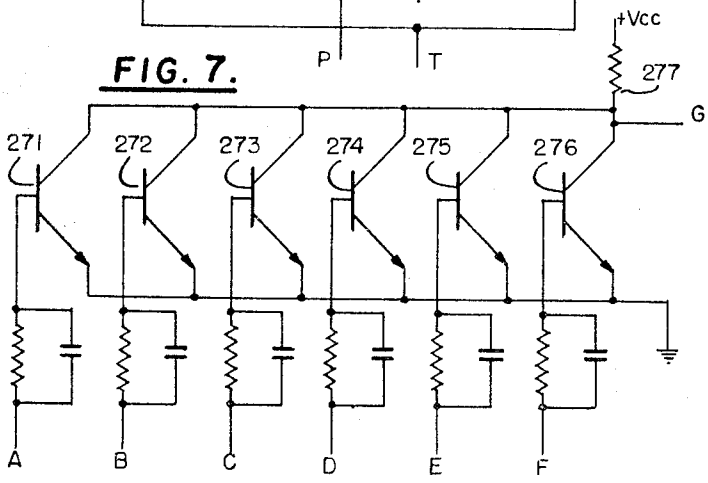



FIG. 6.

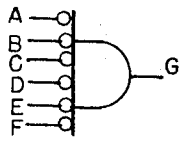
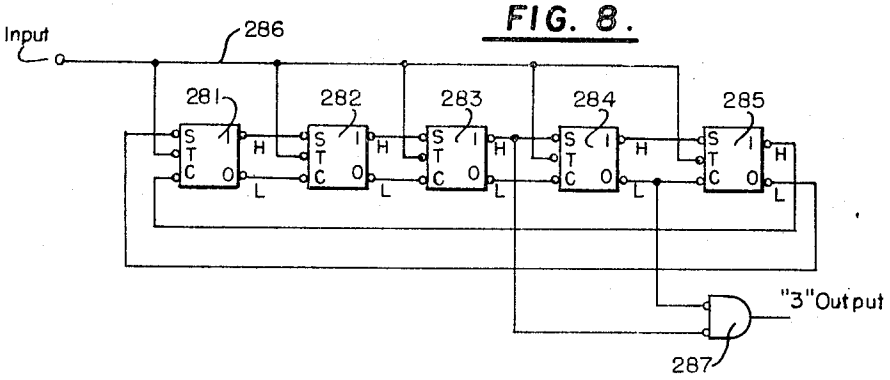



FIG. 8.




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United States Patent Office

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3,454,926

# DUAL-CHANNEL SYSTEM FOR SETTING DIGITAL ELECTRONIC TIMERS

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Int. Cl. G08c 9/00, 11/00

U.S. Cl. 340—146.1 14 Claims

## ABSTRACT OF THE DISCLOSURE

An electronic timer system is described having two independent timers for use in a missile, together with the ground equipment required for remote checking, setting, and monitoring the setting of the timers over two wires. Each decade is set individually and an electronic stepping switch switches the setter from decade to decade. Monitor pulses are returned to the setter to prove that the timers are in phase with the setter. Each decade is checked for proper operation, is set independently, and is monitored to insure that it has the desired setting.

This invention relates to counters, and more particularly to counters which may be used remotely and which may be controlled, set, and monitored from a distance.

Counters are used for many purposes. Counters have been used to maintain records of the number of operations or activities which occur during any specific event. Counters are used to keep score in sports events and other such activities. Counters are used in modern data processing equipment to accumulate numbers and to store information. And, counters are used as clocks, to measure time, to indicate intervals of time from the beginning of an event, and to measure or to indicate the passage of time. Counters are used in any of several ways. The counters may be used to count output pulses in standard or clock oscillators. When an interval of time is to be indicated, there are three ways in which the counter may be used. The counter may be so constructed that it counts forward, and when a particular count is reached, it generates an output pulse. Or a predetermined time may be preset in a backward-counting counter, and the counter operated to count pulses from a standard or clock source. In this way when the counter reaches zero, the preset interval of time has elapsed. The third way is to feed into the counter the complement of the time interval desired. Then when the counter counts the pulses forwardly, a pulse or a signal is generated when the capacity of the counter is reached to indicate the passage of the desired interval of time.

To construct a counter specifically to generate signals at several different counts is expensive. Therefore, when a counter is to be used as a general purpose elapsed time indicator, either a forwardly counting counter is used, in which case it generates its signal when its capacity is reached and the complement of the desired interval of time is preset in the counter, or a backwardly-counting counter is used and the interval of time desired is preset into the counter, the counter generating a signal when it has counted back to zero.

Probably the largest number of counters are used in modern data processing systems, and in such systems most of the equipment is located at a single location. In these systems there is little or no problem involved with setting or operating counters since the information is transferred over comparatively short distances. However, in some installations a setting and monitoring station may be a substantial distance from the point from where the clock is located and from where the timing is to take place. In this type of system a transmission link becomes important between the monitoring station and the remote operative station. The transmission link may be by means of wires or by means of radio, but in either case the more complex the signals to be transmitted, the more complicated the transmission link. In a system where the interval timer is remote from the monitoring station, there have been two common ways in which the counter was preset to a prescribed interval regardless of the type of counter used. The fastest way of presetting the counter was to provide each stage of the counter with a separate setting means and to simultaneously feed the signals to all of the stages of a multistaged counter, to set all stages of the counter to the proper count at the same time. This method requires a very complex transmission link since the link must carry either a single wire or a single channel for each of the counter stages which has to be set. The alternative which has been used in the past has been to supply to the counter, over a single transmission channel or a single pair of wires, a plurality of pulses in serial form which sets the counter from its zero or home count to the desired count. This system requires nothing more than a very limited or simple transmission link with only a single channel. Usually the counter has a very large capacity and, when a large number is to be inserted, it requires a long time to preset the counter to be desired interval.

It is, therefore, an object of this invention to provide a new and improved time measuring system which can be readily operated from a remote location.

It is another object of this invention to provide a new and improved time measuring system which can be preset from a remote location to measure any time interval within the capacity of the system readily and without complex transmission paths.

It is a further object of this invention to provide a new and improved time measuring system which may be remotely set and remotely monitored over a single pair of wires or over a single transmission channel.

It is still another object of this invention to provide a new and improved time measuring and counter system which may be preset and monitored from a distance with only a simple transmission line without requiring a substantial amount of time to accomplish the monitoring presetting.

Other objects and advantages of this invention will become apparent as the following description proceeds, which description should be considered together with the accompanying drawings in which:

FIG. 1 is a block diagram of an over-all system using this invention;

FIG. 2 is a block diagram of the control and monitoring equipment located at the home or ground station;

FIGURE 2A shows the manner in which the outputs from register **23** in FIGURE 1 are coded;

FIGURE 2B shows the manner in which the decoding of the counters **13–18** is accomplished;

FIG. 3 is a partial block and partial schematic circuit diagram of the remote time measuring equipment;

FIG. 4 is a symbol for a flip-flop as it is used in the block diagrams of FIGS. 2 and 3;

FIG. 5 is the schematic circuit diagram of a typical flip-flop as represented by the symbol of FIG. 4;

FIG. 6 is the symbol for a typcial gate used in the block diagrams of FIGS. 2 and 3;

FIG. 7 is a schematic circuit diagram of a typical gate circuit represented by the symbol of FIG. 6; and

FIG. 8 is a block diagram of a Johnson counter as used in this invention.

Referring now to the drawings in detail, and more particularly to FIG. 1, the reference character **11** designates the equipment in the monitoring or ground station. The ground station equipment comprises an over-all counter made up of counter stages **13**, **14**, **15**, **16**, **17** and **18**, each having a capacity of twenty counts and arranged in

sequence, and a counter **19** with a capacity of four. The clock generator is a multi-vibrator **21**, which generates signals continually at a fixed, known rate and feeds its output pulses to what can be called gate logic **22**. One output from the gate logic **22** is applied to an index register **23**, the output of which supplies the signals to the counters **13–19**. In addition, a second output from the gate logic **22** is applied to a shift generator **27**, and a third output is applied to an index generator **26**. The outputs from the index generator **26** and the shift generator **27** are applied to the remote or missile equipment **12**. The output from the counters **13** through **19** is applied to the monitor logic **24**, the output of which is applied to the gate logic **22**. In addition, the counters **13** through **19** contain setting switches **33, 34, 35, 36, 37, 38** and **39**, respectively, which are set to determine the count at which each counter stage generates an output signal and which are connected to the gate logic **22**, and an output from the index register is fed back to the gate logic **22**. A readout **28** is provided so that a visual display of the count in the counters **13** through **19** may be available. Error lamps **29** and **31** indicate if an error has been made and a ready lamp **32** indicates that the missile or vehicle equipment **12** has been properly preset and is in condition for operation.

The equipment in the missile or the remote station **12** comprises two separate timers, timer **1** and timer **2**, timer **2** having a one kilocycle oscillator **51** which feeds through a gate switch **76** into the several stages of a counter comprising ten-count counters **52, 53, 54, 55, 56** and **57** and a two-count counter **58**. The output from timer **2** is applied to an output stage **59**. Timer **1** comprises a one kilocycle oscillator **61**, the output of which is fed through a gate switch **77** to ten-count counters **62, 63, 64, 65, 66, 67** and a two-count counter **68**. The output from timer **1** is applied to an output stage **69** which joins the output from the output stage **59** at a common output. Information is transmitted along a single channel transmission path **41** from the home station **11** and is applied to the inputs of an index receiver **71** and a shift receiver **72**. The output of the index receiver **71** is applied to an input of an index register **73**. The output of the shift receiver **72** is applied to an input of a monitor logic **74**. There are two outputs from the index register **73**. One output is applied to the individual counters of timer **1** and the other is connected to the individual counters of timer **2**. The outputs of the individual counters are applied to the inputs to the monitor logic **74** together with the output from the shift receiver **72**, and the output from the monitor logic **74** is applied to a monitor generator **75** which applies an output signal to the transmission path **41** for transmission to the ground equipment **11**.

The electronic timer system comprises two independent timers for use in a remote installation such as, for example, a missile. Ground equipment **11** serves to preset the timers in the missile and to provide remote checking and monitoring facilities for the timer. The single transmission channel **41** may comprise a single pair of wires or a single radio channel. The maximum settable amount in the timers may be, for example, two million counts, with each count representing $10^{-3}$ seconds. The time required to set the timers of this capacity with serial pulses is entirely too long to be practical. The alternative method which comprises setting all of the individual counter stages simultaneously requires a substantial number of channels for setting and monitoring purposes. The approach used in this invention for accomplishing the desired result utilizes a single information channel and avoids large delays in stepping the counters through their individual counts. In this apparatus each state of the counter is individually set to its desired value, and when this is accomplished, the setting means is switched from that stage to the nex stage which is also set to the desired value. Thus, only about 60 to 70 pulses are required to set the timer to its desired count. In actual practice, however, about twice this number of pulses is utilized so that each counter stage can be completely cycled once to prove that it is operating reliably. In addition, monitor pulses are returned to the ground station as each stage cycles to indicate that the timers are in phase with the setting device.

When the ground station is prepared to operate, the multi-vibrator **21** is free-running, generating pulses at a rate of approximately one kilocycle per second. These pulses are fed through the gate logic **22**, and, as will be explained in greater detail when later figures are described, the first two pulses are applied directly to the missile equipment **12** to clear the flip-flops in that equipment to a desired condition and to place a count of one in the lower order stages of timers **1** and **2**. The first two pulses from the multi-vibrator **21** do not affect the ground equipment **11**.

Counter stages **13–19** and all flip-flops are first cleared to an initial desired condition by a clear signal, not shown, and the switches **33–39** are manually set to the value, as shown on the switches, which it is desired to set into the individual counter stages **62–68** and **52–58** of timers **1** and **2**. Once the desired setting is made on the individual switches **33–39**, pulses from the multi-vibrator **21** are fed into the counters **13–19**, with the index register **23** selecting the individual stages to which the pulses are directed, starting with the stage **13**. Since the stage **13**, which is the lowest order stage in the counter, has a count capacity of 20 counts, and it has been set to generate an output signal when the corresponding stages in the timers **1** and **2** reach a count less than 10, it requires the number of pulses to be set into the timers **1** and **2** plus ten additional pulses to reach the count at which it generates an output. In some installations, the individual counter stages are cleared to a count of one, or a carry is added at the start, and the total number of pulses required to reach an output signal from the stage **13** is modified by these conditions. The pulses which are applied to the counter stage **13** are also applied over the transmission path **41** to the lowest order stages **62** and **52** of timers **1** and **2**. Thus, the pulses applied to the stages **13, 52** and **62** cause the stages **52** and **62** to completely cycle once through ten counts and then proceed to the desired value. When the stage **13** has reached the amount set on the switch **33**, it generates an output pulse which is applied to the gate logic **22** to halt further operation of that stage. The gate logic **22** then causes the index register to switch the output of the multi-vibrator **21** to the next counter stage **14**. At the same time, the index generator **26** causes a pulse signal to be applied to the transmission line **41** and transmitted to the remote installation **12**, where it causes the index register **73** to switch the incoming pulses from the stages **52** and **62** to stages **53** and **63**. When the stages **52** and **62** had cycled and passed through their capacities, they emitted pulses which were applied to the transmission line **41** for transmission back to the ground station **11** and to the monitor receiver **25**. Monitor logic **24** receives the signal from monitor receiver **25** and indicates when the timers **1** and **2** are operating properly.

Some of the details of the operation of the ground equipment will become clearer with reference to FIG. 2 which is a detailed block diagram of the ground equipment. The multi-vibrator **21**, which is the clock for the ground equipment, has an output applied to one input of a gate **101** in the gate logic **22**. Another output from the multi-vibrator **21** is applied through a start switch **102** to an input of a flip-flop **103**, which is also in the gate logic **22**. The other two inputs to the gate **101** are outputs from flip-flops **104** and **105**. Flip-flop **104** is the ready stop flip-flop and flip-flop **105** is the error stop flip-flop. The output from the gate **101** is applied to the input of a gate **106**, which supplies output pulses to a pair of gates **107** and **108**. The other inputs to the gates **107** and **108** are applied from the two outputs of the flip-flop

109. Pulses passing through the gate 107 are applied to the input of a gate 111, to the shift line for application to the shift generator, and to the inputs to flip-flops 112 and 113. The output from the gate 111 is applied to one of the inputs to a gate 114, the other input of which comes from the flip-flop 113. The output from gate 114 feeds the input to gate 115, which applies pulses passing therethrough to the shift line and thereby to one input of each of the gates 121, 122, 123, 124, 125, 126, 127 and 128 of the index register 23. In addition, the index register comprises flip-flops 116, 117, 118, and 119 which are interconnected with the gates 121–128 to provide aa automatic electronic switching register which applies the pulses from the multi-vibrator 21 in sequence to each of the counter stages 13–19. Only counter 13 of the twenty-count capacity counters is shown in detail, and it comprises flip-flops 131, 132, 133, 134, 135 and 136, and gates 137, 138, 139, 141, 142, 143, 144, 145, 146 and 147. A switch 33, shown in FIG. 2 as having a rotary contact 148, is set at a position where it passes an output from one of the gates 137–147 of the counter stage 13. This effectively sets the count at which an output signal is generated by counter stage 13. Each switch terminal is also provided with a lamp 151 and a lamp gate 149, although the drawing shows only one such lamp and gate to avoid unnecessary clutter. The output from the counter stage 13 is applied to line 152 which applies a signal to the input of flip-flop 109 through gate 108 and thereby to the index register 23 to step that register one count. In addition, the same signal is applied to the line 153 for application to the index generator which supplies a similar pulse to the transmission line 41 for transmission to the missile equipment 12. The other counter stages 14–18 which have a capacity of 20 counts are the same as the stage 13 and are not shown in detail. The outputs from each of the stages 14–18 are connected to the line 152 just as the output from the stage 13. The counter stage 19 is one which has a capacity of only four, and it comprises flip-flops 144 and 155, the gates 156, 157 and 158. This counter stage 19, being the highest order of the counter, has three separate outputs. One output is applied through a diode in common with the outputs from all of the other counter stages 13–18 to supply an index signal through flip-flop 109 and gate 108 to the index register 23. Another output is connected through a capacitor 161 to an input to a gate 163, and a third through the capacitor 162 to another input of the same gate 163.

The output from the gate 163, which has inputs from all of the counter stages 13–19 and from the cycle mark generators including gate logic 22, is applied to a flip-flop 164 in the monitor logic 24. The monitor logic 24 in the ground equipment 11 comprises flip-flops 164, 165, 166, 175, 176, 181, 182, 192, 193 and 194 and gates 167, 168, 171, 172, 173, 174, 178, 179, 183, 184, 185, 195, 196, 197, 198, 199, 201 202 and 203. The shift and cycle marks from timers 1 and 2 are applied to the input of flip-flops 193 and 192 from the monitor receiver 25 through line 191. The output from flip-flop 193 is passed through gates 197 and 198 when gate 197 is opened by a sampling pulse from the one-shot multi-vibrator 205 to become a pulse mark which is applied to the input of a flip-flop 182 and the output of the flip-flop 192 is passed through gates 199 and 201 when gate 199 is opened to become timer 1 cycle mark. Timer 2 cycle mark originates as an output of flip-flop 194 which passes through gates 202 and 203. The output from the flip-flop 193 is also applied through gates 195 and 196 to a control input of flip-flop 192. In addition, the output pulses from gate 101 in the gate logic 22 are applied through the pulse mark line 204 and a delay one-shot multi-vibrator 205 to the inputs of the gates 197, 199 and 202, and through a differentiating capacitor 206 to the input to gate 185 and through line 207 to the clear inputs to flip-flops 194, 192 and 193. The timers 1 and 2 cycle marks are applied to the inputs of flip-flops 165 and 166 respectively. The cycle mark from the output of gate 163 is applied to the input of flip-flop 164. The outputs from flip-flops 154, 165 and 166 are combined in gates 167, 168, 171, 172, 173 and 174, and the result is applied to flip-flops 175 and 176 to indicate errors by lighting lamp 29 for a single error, or out-of-step, and to light lamp 31 for two such errors. The pulse mark from the monitor receiver is applied to an input of flip-flop 182 and the pulse mark from gate 101 in gate logic 22 is applied to an input of flip-flop 181. The outputs of the flip-flops 181 and 182 are combined in gates 179, 183 and 184 to indicate errors in lack of synchronism.

The system 12 which is incorporated into the vehicle or missile is illustrated in detailed form in FIG. 3. Some of the missile equipment has been omitted from FIG. 3 to avoid unnecessary clutter and to render the drawing more readily understandable. For example, the index and shift receivers 71 and 72 are not shown; only three stages of each of the timers 1 and 2 are shown since the remaining stages are identical to those shown; the monitor generator 75 is not shown. What is illustrated in FIG. 3 is sufficient to clearly describe the invention.

The input pulses transmitted over the transmission channel 41 and received by the index and shift receivers 71 and 72 are applied to lines 211 and 212, respectively. The shift pulses transmitted along line 212 to an input gate 213 shift the count of the individual counter stages whereas the index pulses transmitted along line 211 index the timers 1 and 2 from one stage to the next. The output of the gate 213 is applied to the input of a gate 214, the other input to which is applied from one output of a flip-flop 215. The other output from the flip-flop 215 is applied to one input to a gate 216 which supplies a clear signal through a silicon controlled rectifier 218 to clear windings 219. The output from the gate 216 is also applied to the input of flip-flop 215 and supplies a clear signal along line 221 to the input of a flip-flop 222 and to the input of another flip-flop 223. The outputs from the flip-flops 222 and 223 are applied through a one-shot multi-vibrator 220 to the monitor genetrator for transmission over the channel 41 as a cycle mark or pulse. All of this circuitry is in the monitor logic 74. The shift line 224 is the output from the gate 214 and applies the signal output from the gate 214 to the base of SCR 210, and, thereby, to the index register 73. The index register 73 comprises an eight stage magnetic core counter in which each stage comprises a core 225, input cores 227 and 228, input SCR's 229 and 231, and an output SCR 226 for each stage. Line 211 is connected through an SCR 232 to the cores 227 and 228, and supplies pulses for a gate 233. A capacitor 234 serves as an energy source for the SCR's 229 and 231. The output SCR 226 to the left, the lowest order, is connected to the inputs of the timers 1 and 2. Each of the timers 1 and 2 comprises a magnetic core counter similar to that of the index register 73. Although not all of them are shown in FIG. 3, the first stage of timer 1 comprises ten magnetic cores 235, each of which comprises a timer stage, input cores 236 and 237, input SCR's 238 and 239 and capacitor 241. Timer 2 is constructed the same as timer 1. What are shown in detail in FIG. 3 are, of course, only stages 62 and 68 of timer 1; stage 63 is shown as a block and the remainding stages are not shown at all. Similarly, of the seven counter stages of timer 2, only stages 52, 53 and 58 are shown even as blocks; the rest are merely indicated. Since the counter stages of the timers 1 and 2 are identical, showing one of them in detail is sufficient to present a complete description of all. The output stage from the timer 1 is an SCR 242 and the output stage 59 from timer 2 is an SCR 243.

The symbol for a flip-flop as it is shown in FIG. 2 is illustrated in FIG. 4 with the actual circuit represented by the symbol of FIG. 4 shown in FIG. 5. The symbol (FIG. 4) used for a flip-flop in this description represents a package which can be used in any of several ways.

The package comprises a plurality of input and output terminals. The output terminals, see FIG. 4, are represented by Q and $\overline{Q}$, one being the inverse of the other. The two basic input control terminals are C and S. The terminal P is a preset input terminal, and the terminal T is a trigger input terminal.

Referring to FIG. 5, the flip-flop itself comprises transistors **251** and **252** cross-connected with the base electrode of one transistor connected to the collector electrode of the other. The C input is connected to the base of the transistor **251** through a diode **253**. The S input is applied to the base of the transistor **252** through diode **254**. The T input is applied through a capacitor **255** to the base of the transistor **251** and through a capacitor **256** to the base of transistor **252**. A third transistor **261** has its collector and emitter circuits connected in parallel with the collector and emitter of the transistor **251**. The P input terminal is connected to the base of the transistor **261**. The Q output is taken across a load resistor **262** in the collector circuit of the transistors **251** and **261**, and the output $\overline{Q}$ is taken across a load resistor **263** in the collector circuit of the transistor **252**.

In operation, the flip-flop represents a "one" when the terminal Q is low, and "zero" when $\overline{Q}$ is low. The terminal Q is low when the transistors **251** or **261** are conductive. When transistor **251** or **261** is conductive, then transistor **252** is cut off. A high signal applied to P will drive transistor **252** into non-conduction and the flip-flop into the "one" state. The terminals S and C are control inputs and help determine what happens to the flip-flop when a trigger pulse is applied to the input T. Thus, when the potentials applied to C and S are both high and a downward-going pulse is applied to T, the flip-flop remains in the state it was. When the potential on C is high and the potential on S is low, a downward-going pulse on T places the flip-flop in the "one" state. When the potential on C is low, and the potential on S is high, a downward-going pulse on T places the flip-flop in the "zero" state. If the potentials on both S and C are low, then there is no positive way of predetermining the final condition of the flip-flop when a pulse is applied to T. The circuit of FIG. 5 is converted into a binary counter by connecting C to Q and S to $\overline{Q}$. Then, whenever a downwardly-going pulse is applied to T, the flip-flop will change its state.

FIG. 6 shows the symbol used for an "and" gate in this specification, the number of circles denoting the number of inputs. One form of circuitry for the gate is shown in FIG. 7 which shows a plurality of transistors **271, 272, 273, 274, 275** and **276** with their collectors and emitters connected in parallel and in series with a load resistor **277** which is connected at one end to B+ and at the other end to the gate output G. The individual base electrodes are connected to separate inputs A, B, C, D, E, and F. When any of the transistors **271–276** are conductive, the potential at G is low. It is only when all of the inputs A–F are low, and none of the transistors **271–276** are conducting, that the current flow through the resistor **277** is sufficiently low to render the output at G high.

Referring now to FIGS. 1 and 2, the operation of the over-all system is described. The time interval which the timers **1** and **2** are to measure in milliseconds before initiating a desired operation is determined. This amount is then set on the individual switches **33–39** so that the counter stages **13–19** produce output signals when the correct amount is reached. The switches **33–39** are so arranged that this operation is correct, taking into consideration the idiosyncrasies of the individual counter stages. Since the counter stages **13–19** are forward counting counters, the switches **33–39** are numbered so that the output from the counter stage actually occurs when the nines complement of the desired time is placed into the stage. The nines complement rather than the tens complement is used to avoid problems with carries. Thus, the counter stages **13–19** are not connected together in a ring and one stage does not carry to another. So, the nines complement is used and a single pulse is added at the end to convert the nines complement into the tens complement. In stages **13–18**, the output is generated from each stage when the count in that stage reaches a count of nine plus the amount to be set into the stage, in this case the nines complement of the desired time period. In stage **19**, which is a four count stage, the amount is one plus the amount set on the switch **39**. In FIG. 3, the switches **76** and **77** connecting the oscillators **51** and **61** to timers **1** and **2** are open at this time. Once the switches **33–39** have been set, the clock oscillator **21** in the ground equipment **11** (FIG. 2) is started, and the start switch **101** is closed. After the start switch **102** is closed, the first two pulses from the clock **21** are not sent to the index register **23**, but are sent, instead, to the missile equipment **12**. The first pulse clears the missile equipment **12** to a desired condition, and the second pulse inserts a count of one into the timers **1** and **2**. When the start switch **102** is closed, flip-flop **103** changes state when the potential of the lower output terminal from the clock **21** drops. At this time, the upper output terminal of the clock **21** rises in potential and maintains an input to gate **101** high. All of the other inputs to the gate **101** are low. Thus, when the clock **21** pulses, the output to gate **101** changes with the pulses and the pulses therethrough until such time as one of the flip-flops **104** or **105** changes its state and raises the potential on another input to gate **101**. The first pulse through the gate **101**, in addition to being applied to the missile equipment **12**, also is applied to the T input of the flip-flop **112** through gates **106** and **107** to change the state of the flip-flop **112**. The second pulse from the clock **21** changes the state of the flip-flop **113**. Until both flip-flops **112** and **113** are changed by the first two pulses, no pulses can pass through the gate **114**. So, the effect of the first two pulses on the ground equipment **11** is to prevent any action in the ground equipment **11** until the missile equipment has been cleared and the timers **1** and **2** set to the count of one. Pulse outputs from the clock **21** are now applied to the input of the index register **23**.

Single input gates such as the gates **106, 111** and **115** are readily used as pulse inverters. The output of a gate as it is shown in FIG. 7 is the inverse of its input. Thus, when the inputs to a gate are low, the gate output is high. Inverter gates are used in this equipment to ensure that signals have the proper polarity.

The index register **23** serves as a large stepping switch to determine to which of the counters **13–19** the pulses from the clock **21** are being applied at any time. Thus, the clock pulses are applied to the input to the index register **23**, and the output from the index register **23** upon which the pulses appear depends upon the register's state at any time. Initially, the first stage **121** is conductive, passing the pulses from the clock **21** to the input of counter **13**. When a pulse is applied to the input to counter **13**, it is applied to the flip-flops **131, 132, 133, 134** and **135** simultaneously. This pulse is applied to the T inputs of the flip-flops, and the state into which the flip-flops are driven depends upon the state of the flip-flop and the condition of the other two control input signals. Consider, for this explanation, FIG. 8. Five flip-flops **281, 282, 283, 284** and **285** are shown. These five flip-flops can represent any of ten digits, as depicted in the table below. As shown in FIG. 8, the one output from flip-flop **281** is connected to the S input of flip-flop **282**, and the 0 output from flip-flop **281** is connected to the C input of flip-flop **282**. This continues down the chain with the 1 and 0 outputs from the flip-flops **285** finally connected to the C and S inputs of flip-flop **281** to form a chain. Input pulses are applied through line **286** simultaneously to the T inputs of all the flip-flops. The first pulse to arrive on line **286** changes the condition of the flip-flop **281** so that it is placed in the 1 state. The next pulse places flip-flop **282** into the 1 state, etc. As can be seen from

the following table, each successive pulse changes the state of the next following flip-flop. After all five flip-flops **281–285** have been placed in the 1 state, the next pulse places flip-flop **281** into the 0 state. This continues until all of the flip-flops are again in the 0 condition. For decoding purposes, a gate, such as **287**, is connected to pairs of outputs. In FIG. 8, gate **287** has two inputs, one of which is connected to the 1 output of flip-flop **283**, and the other of which is connected to the 0 output of flip-flop **284**. When both of these outputs are low, the gate **287** has a high output. A high potential out of gate **287** represents a count of 3. For each digit to be represented by the state of the counter, a separate gate must be provided and its inputs may be connected in accordance with the following table:

| Digit | Flip-flop | | | | | Connections | |
|---|---|---|---|---|---|---|---|
| | 281 | 282 | 283 | 284 | 285 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | ---------- | 281, 285 |
| 1 | 1 | 0 | 0 | 0 | 0 | 281 | 282 |
| 2 | 1 | 1 | 0 | 0 | 0 | 282 | 283 |
| 3 | 1 | 1 | 1 | 0 | 0 | 283 | 284 |
| 4 | 1 | 1 | 1 | 1 | 0 | 284 | 285 |
| 5 | 1 | 1 | 1 | 1 | 1 | 281, 285 | ---------- |
| 6 | 0 | 1 | 1 | 1 | 1 | 282 | 281 |
| 7 | 0 | 0 | 1 | 1 | 1 | 283 | 282 |
| 8 | 0 | 0 | 0 | 1 | 1 | 284 | 283 |
| 9 | 0 | 0 | 0 | 0 | 1 | 285 | 284 |

In the above table, the pulse number and the amount represented by the counter have been considered the same. Thus, when the first pulse is received, flip-flop **281** is in the 1 state and the others remain in the 0 state. On the second pulse, **281** and **282** are in the 1 state and the others in the 0 state. A gate having two inputs is connected to the 0 outputs of flip-flops **281** and **285** to depict 0; another such gate has its inputs connected to the 1 output of the flip-flop **281** and the 0 output of flip-flop **282** to depict the count of 1, etc. The table thus presents a wiring guide as well as the conditions of the five flip-flops for each count of the counter.

In FIG. 2, the counter **13** is shown to be a counter similar to that of FIG. 8 with a flip-flop **136** added as a binary counter to double the number of possible combinations. In addition to the flip-flops and the gates as shown in FIG. 8, the switch **33** is connected to the outputs of the various gates. When the count of the counter **13** reaches nine plus the desired amount, a signal is passed through the appropriate gate to the contact of switch **33** to which that gate output is connected—in this case gate **145**—and the pulse passes to the index signal line **152** and is applied to the input of the flip-flop **109**. The condition of the flip-flop **109** is changed to open gate **108** and close gate **107**, and the next output pulse from the clock **21** passes through gate **108** and is applied to the input of flip-flop **109**. The condition of the flip-flop **109** is changed to open gate **108** and close gate **107**, and the next output pulse from the clock **21** passes through gate **108** and is applied to the input of the index register **23** to change the count of the register.

The counters **13–18** are 20-count counters and to accomplish this count, the flip-flop **136** has been added as a binary counter stage. Decoding of the counter **13–18** is in accordance with the table shown in FIG. 2B, with the second count of ten for the counter being a duplicate of that shown but with the flip-flop **136** in the opposite condition. The manner in which the outputs from the register **23** are coded is shown in FIG. 2A. Since the register **23** need switch only from one of the counters **13–19** to another, only eight counter positions are needed, the count of eight cutting off pulses to any of the counters **13–19**.

The shift pulses from the clock **21** are applied through gates **107**, **111**, **114** and **115** to the inputs of the gates **121–128** of the index register **23**. Whichever one of the gates **121–128** is opened passes the pulses to the input of the appropriate counter **13–19**. As mentioned, the counters **13–19** are cycled through their counts until the value in the counter reaches nine plus the nines complement of the amount set on the switch **148**. At this time, a pulse passes through the switch **148** to index the index register **23** to the next count. Subsequent pulses from the clock **21** are then applied to the next following counter **13–19**. The process continues until all of the counters have cycled, the last output from the counter **19** setting the index register **23** to eight and cutting off the flow of pulses to the counters. Thus, the counters are shifted automatically after the second pulse output from the clock **21** until the index register is set to eight, at which time further counting is terminated.

Each time a pulse from the clock **21** is applied to the shift line through gates **107**, **111**, **114** and **115**, a similar pulse is also applied to the shift line **150** and to the transmission path **41** for transmission to the missile equipment **12**. In the missile equipment **12**, shown in some detail in FIG. 3, the input pulses are applied from the shift receiver **72** to the shift line **212**. After passing through gate **213**, which inverts the signal, and through gate **214** when the flip-flop **215** is in the one state, the pulses are applied through line **224** to the control electrode of the silicon controlled rectifier **210**. The operation of the rectifier (SCR) **210** grounds capacitor **230** through all of the cores **225** simultaneously, and passes to one SCR **226** a pulse from the core **225** to which it is connected and which is in the one state. The outputs of the individual SCR's **226** are each applied to the input to one of the counters **52–58** and **62–68** and reapplied through the corresponding core **225** to reset it to the one state. Thus, depending upon the state of the index register **73**, the input shift pulses from the ground equipment **11** are applied to one or another of the counter stages in the two timers.

The index register **73** comprises a magnetic core counter with silicon controlled rectifiers serving as output gates. The core counter is also used in each of the counter stages of timer **1** and timer **2**. To explain the operation of the core counter, reference is made to counter **62** of timer **1** which is shown in detail in FIG. 3. It is assumed for this discussion that current flowing through the signal wires which pass through the cores **235**, **236** and **237** in a downward direction, as shown in FIG. 3, place the core in the zero state, and current passing upwardly places the core in the one state. Also, for this discussion, consider as the source of pulses the oscillator **61**, and the switch **77** as closed. When a pulse passes from the oscillator **61** through the switch **77** and is applied to the cores **236** and **237**, the current passes downward and places cores **236** and **237** in the zero state. One of the cores **236** or **237**, for this discussion it is assumed core **237**, was already in the zero state, and **236** was in the one state. The passage of the pulse through the cores **236** and **237** causes core **236** to change its state but not core **237**. Thus, there is a small output from core **237** and a large output from core **236**. The output from core **236** causes the silicon controlled rectifier **238** to conduct. The capacitor **241** has been charged by current flowing though the resistor **240** to ground from a source not shown but connected to the other end of the resistor **240**. When SCR **238** conducts, the capacitor **241** discharges through core **237**, the SCR **238** and the line **245**, applying a pulse through the even cores **235** and upwardly through the core **237**. This places core **237** into the one state and drives the even cores **235**, which were the cores through which the pulse from the capacitor **241** passed, into the zero state. When the first even core **235** goes into the zero state, its output drives the first odd core **235** into the one state through the loop **246** which connects two adjacent cores **235**. When the capacitor **241** has discharged, the SCR **238** stops conducting. The next pulse from the clock **61** is again applied downwardly through the cores **236** and **237**. Since core **237** is now in the one state, it is changed to the zero state, generating a large output signal which causes SCR **239** to conduct. The capacitor **241**, which has had time to recharge

between pulses, discharges through the SCR **239**, causing current to flow through the core **236** driving it into the one state. Thus, with each incoming pulse from the clock **61**, the one condition of the cores progresses down the counter. There are ten counter cores in each of the counters **62–67** and **52–57**, and two counter cores each in **58** and **68**, and each counter core represents a count of one. When the counter has reached the end of its capacity, it produces an output pulse for the next stage, and the process is repeated. The final output is taken through an SCR **242** which is turned on when the count is completed to close the output circuit.

The index register is a counter similar to that described above with the addition of an output SCR **226** for each core **225** of the register. The input pulses from the shift line **224** are applied to the base of the SCR **210** to render that SCR conductive and ground the capacitor **230** so that it discharges through the cores **225**. That core which is in the one state generates a large output pulse which is applied to the base electrode of its SCR **226** to render that SCR conductive. The capacitors **234** and **250** discharge through the conductive SCR's to set the cores **235** in timers **1** and **2**, and to reset the core **225** to the one state.

As mentioned above, the first and second pulses from the clock **21** in the ground equipment **11** are transmitted to the missile equipment **12**. They set the index register **73** into its first condition. Thereafter, as the pulses from the clock **21** are applied to the counters **13–19**, they are also applied to the transmission path **41** and thereby through the index register **73** to timers **1** and **2**. As one of the counters **13–19** in the ground equipment **11** is shifted, so are the counter stages in timers **1** and **2**, until the setting of the individual counter switch, **33–39**, is reached. It is really immaterial to this invention how the positions on the counter switches **33–39** are labeled. For example, the positions may be labeled with the actual value it is desired to insert into the individual missile counter stages, or they may be labeled to represent the time interval which the missile stages are to later reach. In either case, the individual idiosyncrasies of the particular equipment being used must be taken into consideration. For example, if the switch positions are labeled with the time interval to be counted by the missile stages, then consideration must be given to whether the inserted value is in the nines or the tens complement of that number. In the same manner, if the leading edges or the lagging edges of the pulses are to be used to cause desirable effects, this must also be taken into consideration when labeling the switch positions. In this explanation, it is assumed that the switches **33–39** are labeled to indicate the proper amount for the desired condition and equipment used. When the count in each of the counters **13–19** reaches the values set on the corresponding switch **33–39**, that counter stage in the ground equipment **11** which is receiving input pulses generates an output signal which causes the index register **23** to index to its next position and feed pulses to the next counter stage **13–19**. It will be recalled that counters **13–18** were described as having a capacity of 20 counts each whereas the counters of timers **1** and **2** have capacities of only 10 counts. The settings of the switches **33–38** in each of the counters **13–18** really represent counts of ten plus the desired count. However, for reasons of practical operation, this number of pulses may be more or less than ten depending upon the equipment and how it is used. Thus, when each counter in the timers **1** and **2** has cycled completely, through ten counts, the corresponding ground counters **13–18** have not yet reached the final count determined by the setting of the switches **33–38**. As the ground counters **13–19** continue to count, the counters of the timers **1** and **2** continue to step until they are set into the desired count. The index pulse output from each of the counters **13–19** is applied to the transmission path **41** and indexes the index register **73** also. In this manner, the counters in the ground equipment **11** and those in the missile equipment **12** are maintained in synchronism. When the counter stages in the timers **1** and **2** reach their capacities, several events take place. The shift pulse that cycled the counter stages is applied, as are all shift pulses, from gate **233** to the input of a one-shot multi-vibrator **220** to drive it into the unstable condition. The one-shot multi-vibrator **220** remains in its unstable condition for 50 microseconds when it recovers. This applies a 50 microseconds pulse to the monitor generator (not shown in FIG. 3) and thereby a pulse to the transmission path **41**. As a result, the B+ line **290** dips in potential. At the same time that the shift pulse from gate **233** was applied to the one-shot **220**, each of the counter stages in timers **1** and **2** which reached their capacity generated a cycle mark. The cycle mark from timer **1** is applied to the P input to flip-flop **222** and the cycle mark from timer **2** is applied to the P input to flip-flop **223**. Both flip-flops **222** and **223** are driven into their one states. When the B+ line dips due to the output from the one-shot **220**, a negative pulse is applied to the T input of flip-flop **222**, driving that flip-flop into the zero state, but leaving the flip-flop **223** in the one state. Flip-flop **222**, in changing from the one to the zero state generates a pulse which is applied to the input of the one-shot **220** to again set it into its unstable condition. In the meantime, with flip-flop **222** in the zero state and flip-flop **223** in the one state, both inputs to the gate **208** are low, its output is high, and the output from gate **209** is low, making the S, control input to the flip-flop **222** low and the C input to that gate high. When the one-shot **220** recovers from its second input pulse, a second pulse is applied to the transmission path **41**, the B+ line dips again, and the flip-flop **222** receives another pulse on its T input. This time the flip-flop **222** is driven into the one state due to the conditions of the S and C control inputs. When the flip-flop **222** changes to the one state, the flip-flop **223** is driven into the zero state, due to the output from flip-flop **222** being applied to the T input of flip-flop **223**, and, the potentials on the C and S inputs of flip-flop **222** are reversed. In changing to the zero state, flip-flop **223** applies a pulse to the input of the one-shot **220** to drive it into its unstable condition for the third time. When the one-shot **220** recovers, a third pulse is applied to the transmission path **41** and the B+ line again dips in potential. The dip of the B+ line drives the flip-flop **222** from the one state to the zero state to apply another pulse to the input of the one-shot **220** and cause a fourth pulse to be applied to the transmission path **41**. If timer **1** did not generate a cycle pulse, then the above procedure would be followed with the exception of the generation of the second pulse by the driving of the flip-flop **22** from the one to the zero states since that flip-flop would not have been driven into the one state to begin with. In the same manner, if timer **2** did not generate a cycle mark, then flip-flop **223** would not have been driven into the one state, and the third and fourth pulses would not be generated by the one-shot **220**.

The pulses generated by the one-shot **220** and applied through the monitor generator to the transmission path **41** are received in resquence in the ground equipment **11** on line **191**, see FIG. 2. The first pulse in any sequence is applied to the flip-flop **193** to change the condition of that flip-flop. This pulse is also applied to the T input to flip-flop **192**, but the potentials on the control inputs C and S of that flip-flop are such that it does not change its state. The shift mark that was applied to the missile equipment **12** to cycle it originated in gate **101**. The output from gate **101** in the gate logic is applied to a differentiating capacitor **206** and to a one-shot **205** to drive it into its unstable condition. The one-shot multi-vibrator **205** remains in its unstable condition for 500 microseconds, and at the end of that time, it applies a sampling pulse to gates **197**, **199** and **202**. Therefore, to obtain outputs from these gates, the other inputs to them must become low before the end of that 500 microseconds interval. As mentioned above, the first pulse (assuming that the total cycle mark complement of four is being received) changes the condition of flip-flop **193**. Since the flip-flops **192**, **193** and **194** were

cleared to the one state by the clear pulse applied to their P inputs, flip-flop **193** is changed to the zero state. This applies a low potential to one input to the gate **195**, and the other input has a low potential from the flip-flop **192**. The output from gate **195** is high and the output from gate **196** is low. This renders the potential of the C control input to flip-flop **192** low. The next pulse that comes in on line **191** is applied to both flip-flops **193** and **192**. However, flip-flop **193** is not affected by additional pulses and remains in the zero state until the next clear pulse is applied to its P input. Flip-flop **192** on the other hand, with flip-flop **193** in the zero state, changes its state with each pulse applied to its T input. Therefore, on the second pulse, flip-flop **192** changes to the zero state. On the third pulse which is applied to line **191**, flip-flop **192** changes to the one state, generating an output pulse which is applied to the T input of the flip-flop **194** to change that flip-flop to its zero state. The fourth pulse puts flip-flop **192** into zero state, making all of the flip-flop **192**, **193** and **194** zero. Thus, all of the gates **197**, **199** and **202** are open when the sampling pulse arrives. Each of the pulses from the missile equipment occupied 50 microseconds, which means that the above sequence of events occupied about 200 microseconds. At the end of the 500 microsecond interval, the one-shot **205** recovers and applies the sampling pulse to the gates **197**, **199** and **202**. Since they are all open, the signal passes through all of them and is applied to the T inputs to flip-flops **165**, **16** and **182**. Immediately subsequent to this, the lagging edge of the differentiated pulse from the capacitor **206** is applied to the P inputs of the flip-flops **192**, **193** and **194** to reset these flip-flops to their one states.

The flip-flops **164**, **165** and **166** are connected to the inputs to gates **167**, **168**, **171** and **172** to operate together. Gate **167** has three inputs; one from the one output of the flip-flop **164**, one from the zero output of flip-flop **165**, and a sampling input from the gate **185**. Gate **168** has an input connected to the zero output of the flip-flop **164**, an input connected to the one output of the flip-flop **165**, and a sampling input from gate **185**. Gate **171** has an input connected to the one output of the flip-flop **164**, an input connected to the zero output of the flip-flop **166** and a sampling input from gate **185**. And gate **172** has an input connected to the zero output from flip-flop **164**, an input connected to the one output from flip-flop **166** and a sampling input from gate **185**. Thus, gate **167** is open when flip-flop **164** is in the one state and flip-flop **165** is in the zero state; gate **168** is open when flip-flop **164** is in the zero state and flip-flop **165** is in the one state; gate **171** is open when flip-flop **164** is in the one state and flip-flop **166** is in the zero state; and gate **172** is open when the flip-flop **164** is in the zero state and flip-flop **166** is in the one state. From this, it can be seen that as one of the flip-flops of a pair changes its state, the condition of the associated gate changes, but if both of the flip-flops of a pair change state, the associated gate remains in the same condition. The condition of the flip-flop **164** is controlled by the passage of an output pulse from gate **163**, which occurs when the counter stages **13–19** cycle. So long as the flip-flops are in such condition that each of the gates has a high and a low input, the gates **167**, **168**, **171** and **172** remain closed. As connected, each gate has an input connected to the zero output of a flip-flop and an input connected to a one output of a flip-flop. With the flip-flops all in the same condition, all of the gates remain closed; when one flip-flop gets out of step, then one of the gates may have two low inputs and open. So long as the gates **167**, **168**, **171** and **172** remain closed, their outputs are low. Thus, the inputs to the gates **173** and **174** are low and these gates are open. The output from these gates are high, placing high inputs on the gate **178**, and keeping that gate closed. Thus, one input to gate **179** is low.

In the meantime, the shift mark from gate **198** was applied to flip-flop **182**. The pulse output from gate **101** is applied at the same time to flip-flop **181**. So long as the two pulses are applied to these flip-flops at the same time, they will change together and the inputs which are applied to gates **183** and **184** will change together. One input to gate **183** is connected to the zero output of flip-flop **181** and another input is connected to the one output from flip-flop **182**. One input to gate **184** is connected to the one output of flip-flop **181** and the other input is connected to the zero output of the gate **182**. So long as both flip-flops **181** and **182** are in the same state, the gates **183** and **184** are closed and the outputs from these gates are low. Thus, the inputs to gate **179** are low, and the output of that gate is high. The error stop flip-flop **105** does not change state under these conditions. However, should the output of the gate **179** go low because one of the inputs goes high, then the flip-flop **105** will change its condition and stop further pulses from passing through the gate **101**.

So far, the detailed operations of the individual components of the system have been explained. The following relates those operations to each other to describe the over-all operation of the system. The system of this invention is designed to set the timers **1** and **2** in the missile equipment **12** to a predetermined starting value using a transmission path of the minimum size, which is a single pair of wires or a single radio channel, in the smallest time. At the same time, the equipment must indicate to the ground station the proper or improper operation of the missile equipment.

Initially, switches **77** and **76** in the missile equipment are opened so that pulse outputs from the oscillators **51** and **61** will not be applied to timers **1** and **2**. Then, the predetermined values to be inserted into timers **1** and **2**, or the complements of those values depending upon the equipment and its labeling as explained above, are manually placed on the individual switches **33–39** of the ground equipment. For example, if the count desired from the timers **1** and **2** is 1234567, then the switches of the counters **19–13**, respectively, are set at the values "1," "2," "3," "4," "5," "6," and "7," with the amount "7" set on switch **33**, the amount "6" set on switch **34**, and so forth. The ground equipment **11** is energized and cleared to the desired initial state. Once this has been accomplished, the start switch **102** is closed. The first pulse from the clock **21** clears the missile equipment to a desired condition and sets the index register **73** to the count of one, and the following pulse sets a count of one in timers **1** and **2**. Since counter **13** had been cleared to a count of 1, subsequent pulses are then applied through the index register **23** to the counter **13** until nine pulses have been so applied. It was mentioned earlier that the capacity of the counters **13–19** is double that of the corresponding counters in the timers **1** and **2**. Assuming that the timers **1** and **2** and the counters **13–19** count forward, that the counters **13–19** count to nine to avoid a carry and the final answer is then corrected, and that the nines complement of the desired value is inserted into the timers **1** and **2**, then when switch arm **148** of counter **13** is set to "7," eleven pulses are applied to the counter before that "value" is reached. This applies nine pulses to counter stages **52** and **62** of timers **2** and **1** to cycle those counter stages completely, and then an additional two pulses to set each of them at the value "2," which is the nines complement of the desired count. This means that each counter stage of the timers **1** and **2**, is cycled to check its operation before it is finally set to the desired value. Whenever a pulse is applied to timers **1** and **2**, each of these timers generates a similar pulse output which is applied to the one-shot multi-vibrator **220** to transmit monitoring pulses back to the ground equipment **11**. The lack of synchronism between these shift pulses, or the absence of one or more of these pulses causes the monitor logic **24** in the ground equipment **11** to close gate **101** and stop the flow of further pulses. If the timers **1** and **2** are operating properly, then the setting operation continues. When the counter **13** has reached the position at which

the switch arm **148** is set, an index pulse is passed through the appropriate output gate **137–147** and the switch **148** to step the index register **23** one count. This closes the output gate **121** which directs pulses to counter **13** and opens gate **122** to feed the subsequent pulses to counter **14**. Similarly, the index pulse is received in the missile equipment and is applied to the index register **73** to step that register. Incoming pulses are now applied to counter stages **53** and **63** instead of to **52** and **62** of the timers **1** and **2**. Counter **14** is stepped through **12** counts, causing the counter stages **53** and **63** to cycle once completely and then to be set at the value "3" and to apply a carry to counter stages **54** and **64**. This operation continues until all of the counter stages in the timers **1** and **2** have been set at the desired value. When the last counter, **19**, has reached the setting of its switch **39**, it generates an index pulse which places the index counters **23** and **73** in the condition to shut off further flow of pulses to both the counters **13–19** and the timers **1** and **2**. The index pulse also adds "one" to stages **52** and **62** to complete the "tens" complement.

The missile equipment has been set to the predetermined count desired, and in the process, the timers **1** and **2** have been checked for proper operation. The missile equipment **12** is now ready for independent operation. When timers **1** and **2** are to be used, the switches **76** or **77** are closed, and the output from the oscillators **51** and **61** are applied to the individual timers **1** and **2**. Timers **1** and **2** count the pulses until the limits of their capacities are reached, and then the output SCR's are triggered into conduction and the output circuit is closed. The timers **1** and **2** have accomplished their purpose.

The above specification has described a new and improved system for setting large capacity counters to a prescribed value from a remote point in a comparatively short interval of time using a single transmission channel only and providing a check of the operation of the counters in the process. It is realized that the above description may indicate to others in the art additional ways in which the principles of this invention may be used without departing from its spirit. It is, therefore, intended that this invention be limited only by the scope of the appended claims.

What is claimed is:

**1.** An interval timer system which comprises counters for counting input pulses having a fixed rate, said system being capable of being preset from a distance, said system comprising a first counter having a plurality of first stages, a second counter having a plurality of second stages, said second counter being located at a distance remote from said first counter, a single communication channel connecting said first and said second counters, the count capacity of each of said first stages being double the count capacity of each corersponding second stage, a first stepping switch having a control input and a pulse input and having a separate output connected to the input of each of said first stages, a second stepping switch having a control and a pulse input and an output and having a separate output connected to the input of each of said second stages, means for presetting each of said first stages to a desired amount so that each of said first stages produces an output signal when it has counted the desired amount, means for supplying to the pulse input to said first and second stepping switches simultaneously pulses having a set rate so that said stepping switches transmit said pulses to the input of the individual stage to which it is set, means for connecting to the control input the preset output of each of said first stages to said first and second stepping switches to step said switches, and a transmission path for transmitting the pulses applied to said first and second counters from said first counter location to said second counter location, the second stepping switch and the second counter being operable to preset said second counter to a desired value under the control of said first counter.

**2.** A counter system in which a remote counter is preset to a prescribed value under the control of a distant counter, said system comprising a home station and a remote station, a single channel transmission path connecting said home and said remote stations, a first counter having a plurality of first stages at said home station, a second counter having a plurality of second stages at said remote station, means for presetting each stage of said first counter at a desired value so that said first stages generate an output signal when the count contained therein reaches said preset value, a source of pulses with a fixed known pulse rate, means for supplying pulses to single corresponding counter stages of said first and second counters simultaneously, means responsive to the signal generated when a first stage reaches the preset value to switch the pulses from said source to the inputs of the next stages of said first and second counters, and means for comparing the step-by-step operation of said first and second counter stages.

**3.** A system for setting a predetermined value into a counter from a distance with a limited transmission path and limited time, said system comprising at a first location a first counter having a plurality of first stages, a first stepping switch having a single information input and a plurality of information outputs, a separate one of said outputs being connected to an input to each of said first stages so that information pulses applied to the input of said first switch are applied to the input of said first stage to which said switch has stepped, a source of timed pulses connected to the information input of said first stepping switch, means for presetting each of said first stages to a desired value so that each of said first stages generates an output signal when its preset value is reached, means for connecting the preset outputs from said first stages to the control input of said first stepping switch so that said stepping switch steps to a new position whenever it receives a signal generated by said first stages, a second counter located at a second location which is remote from said first location, said second counter having second counter stages corresponding to said first counter stages a second stepping switch having a plurality of information outputs each of which is connected to a second counter stage and also having a single information input, a single channel transmission path connecting said first location with said second location, means for transmitting over said transmission path to the information input of said second switch pulses which correspond to the pulses applied to the information input of said first stepping switch, and means for connecting to the control input of said second stepping switch the preset signal outputs from said first counter stages so that said first and second stepping switches step in synchronism.

**4.** A counter system having a home installation and a remote installation in which the remote installation is to have information preset into it under the control of the home installation which includes a first master counter having a plurality of first stages, a pulse source, a stepping switch having a single information input and a single control input and a plurality of information outputs, a separate one of said outputs of said first switch being connected to each of the inputs to said first stages, the information input of said first switch being connected to the output from said source so that pulses from said source are applied to individual first stages through the appropriate setting of said first switch, and means for presetting each of said first stages to generate an output signal when it reaches a desired count, said output signals being applied to said control input to said first switch to step said first switch, a remote location having a second slave counter having a plurality of second stages, a second stepping switch having a single information input and a single control input and a plurality of information outputs, means for connecting said information outputs to inputs to individual second stages, a single channel transmission path connecting said home and said remote locations, means for connecting

said pulse source to said transmission path at one end, means for connecting the information input to said second stepping switch to the other end of said transmission path so that the pulses from said source are simultaneously applied to the first stages and to the corresponding second stages, means for connecting the control input to said second stepping switch to one end of said transmission path and the signal output from said first stages to the other end of said transmission path so that the signal outputs from said first stages step said first and second stepping switches simultaneously, means in said remote location for generating a pulse for each pulse received in said remote location, means for transmitting through said transmission path from said remote location to said home location pulses which are generated in said remote location, and means in said home location for comparing the pulses applied to said first counter with the pulses received from said remote location to determine the lack of correspondence therebetween.

5. The system defined in claim 4 further including in said home installation means for indicating lack of correspondence between pulses applied to said first counter from said source and pulses received from said remote location in response to pulses applied thereto, said indicating means being responsive to an output from said comparing means, and means responsive to the indication of lack of correspondence of said two set of pulses to terminate the transmission of pulses from said source to said first and said second stepping switches.

6. An interval timer comprising a multi-stage counter adapted to count input electrical pulses, means for presetting said counter to a desired value so that a subsequent operation of the counter to its capacity produces an output signal at the desired time interval, said presetting means comprising a stepping switch having as many step positions as there are stages in said counter, said stepping switch having an information output for each counter stage, means for connecting each of said switch outputs to the input of the corresponding counter stage, said switch having a single information input and a single control input, said control input serving to step said switch to its next position when energized, a transmission channel connected at one end to a remote location, means for receiving electrical pulses from a remote location, by means of said transmission channel, and applying said pulses to the information input of said switch, means for generating a signal to indicate the completion of each action by said counter, means for applying said generated signals to said transmission channel for transmission to said remote location, means for receiving control pulses by means of said transmission channel, means for applying said control pulses to the control input of said stepping switch so that information pulses are applied to individual stages to achieve the desired count in said individual stages and then the information input is switched to a subsequent stage, and means for driving said counter stages directly when said counter is to measure a desired time interval.

7. A system for setting a counter to a desired value so that it generates an output signal when it has counted less than its capacity, said system comprising a home station containing a master counter, a source of electrical pulses in said home station, a remote station containing a slave counter, means for connecting said home and said remote station, means in said home station for setting said master counter to generate a stepping pulse as each stage of said master counter reaches a desired count, means for applying pulses simultaneously to said master and said slave counters, and means for terminating the transmission of pulses to a slave counter stage when the corresponding master counter stage has reached the prescribed count.

8. The system defined in claim 7 further including a master stepping switch connected at its input to said pulse generating means and at each of its outputs to a stage of said master counter, a slave stepping switch having each of its outputs connected to a stage of said slave counter, a limited width transmission path connected at one end to said master stepping switch and counter and at the other end to the input to said slave stepping switch, and means connecting the output of each stage of said master counter to the stepping input of said master stepping switch to cause said master stepping switch to step to the next position when the count in said stage has reached the prescribed count, and to said transmission path to step said slave stepping switch to its next position.

9. The system defined in claim 11 further including means in said slave counter for generating a pulse each time it counts, means for applying said remote generated pulses to said transmission path for transmission to said home station, and means in said home station for comparing said home and said remote generated pulses.

10. The system defined in claim 11 further including means in said remote station for generating a cycle pulse each time a stage of said slave counter cycles, and means for applying said cycle pulses to said transmission path for transmission to said home station, and means in said home station for comparing said cycle pulses with pulses generated in said home station.

11. The system defined in claim 10 further including in said home station means for terminating the further transmission of pulses to said master and slave counters when the home and the remote generated pulses do not compare.

12. A counter system comprising a home station comprising a multi-stage master counter, a stepping switch having a plurality of separate outputs, each of said separate outputs being connected to a separate stage of said master counter in sequence, a source of electrical pulses, a remote station, a single channel transmission path connecting said home and remote stations, a multi-stage slave counter in said remote station, a remote stepping switch in said remote station and having a plurality of outputs with one of said outputs being connected to a separate slave counter stage in sequence, means for transmitting through said master stepping switch to the inputs of the individual master counter stages in sequence pulses from said source, means for transmitting simultaneously through said transmission path and said remote stepping switch said pulses from said source to the individual slave counter stages in sequence, means for setting said master counter stages individually to generate stepping signal when each of said master stages has reached a selected count, and means for applying said stepping signals to said master and said slave stepping switches to cause them to step to the next position.

13. The system defined in claim 12 further comprising means in said remote station for generating a check pulse for each input pulse received, means for transmitting said check pulses through said transmission path to said home station, and means in said home station for comparing each of said check pulses with home generated pulses and for terminating further operation of said system whenever there is no correspondence between the two sets of pulses.

14. A system for setting a counter from a distance so that it will produce an output when it has counted to a value less than its capacity, said system comprising a counter having at least one stage, a control station located at a distance from said counter, means for setting a desired value into said control station, means for generating at said control station pulses to be counted, means for transmitting said pulses to said counter, and means for terminating the transmission of further pulses when said value has been reached; said system further compriing means for generating a pulse in said counter for each pulse received by said counter, means for transmitting said counter-generated pulses to said control station, and means in said control station for comparing the pulses generated by said counter and said pulses generated by

said control station; said system further including additional stages for said counter, a stepping switch having a plurality of output contacts, one of said output contacts being connected to each stage of said stepping switch, means for connecting the pulses generated by said control station through said stepping switch to the individual stages of said counter, and means for stepping said switch to change the transfer of pulses from one of said counter stages to the next subsequent of said counter stages when the value in said one counter stage reaches the desired amount.



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