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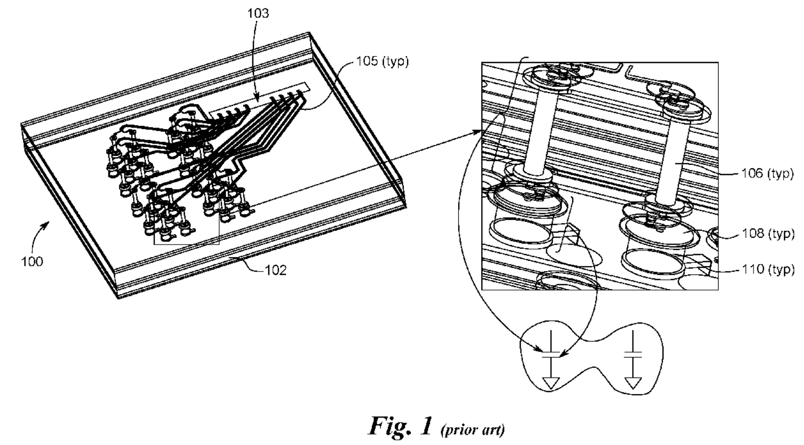


*Fig. 1* *(prior art)*

(57) **Abstract**: Methods and apparatus for inductive compensation in packages and PCB for assemblies with blind and buried vias. The apparatus employ micro-coil structures that electrically connect plated through hole (PTH) structures to Ball Grid Array (BGA) pads. The micro-coil structures create inductive effects that counteract capacitive reflections caused by the PTH and PGA pad structures, which form a natural plate-type capacitor. In addition, the inductive effects can be tuned by varying the amount of coil winding and/or the dimensions of the coil structures.

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# MICRO COIL APPARATUS FOR INDUCTIVE COMPENSATION IN PACKAGES AND PCB FOR ASSEMBLIES WITH BLIND AND BURIED VIAS

## BACKGROUND INFORMATION

In recent years, high speed communication links have been introduced have transfer rates of up to 100 Gigabits per second (Gb/s), with 400 Gb/s links and beyond in development. For example, the IEEE 802.3bj – 2014 standard defines specification for a 100 Gb/s Ethernet link using four 25 Gb/s lanes operating in parallel over copper backplanes in printed circuit boards (PCBs) and routing pathways in communication packages. In order to meet these high bandwidth capabilities, complex analog signal processing is performed at the Physical (PHY) layer to reduce errors that otherwise would result for various types of signal anomalies introduced in the analog signaling sent over the links and through the packaging routing pathways.

One problem with processing high-speed analog signals are errors causes by undesired capacitances in the signal routing circuitry. In particular, undesired capacitance is introduced by routing pathways formed in the PCBs and communication packages. Using inductance to compensate for capacitance is a well-known engineering principle. However, constructing an inductor in a multilayer package in a routing transparent manner is not. A construction which enables fine tuning is not known, as well.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified:

Figure 1 is a schematic diagram illustrating a conventional packaging scheme for high-speed communication employing a plated through hole (PTH) electrically coupled to a BGA pad and BGA solder ball, which forms a capacitive structure;

Figure 2a shows a side view of a PCB and package structure illustrating a plated through hole passing through a core layer of the PCB;

Figure2b shows a 3D view of a solid model of a pair of PTHs electrically coupled to respective BGA pads via a crankshaft structure;

Figure 3a shows a 3D view of a solid model of a pair of PTH structures electrically coupled to respective BGA pads via crankshaft structures

Figure 3b shows a 3D view of solid model of a pair of PTH structures electrically coupled to respective BGA pads via micro-coil structures;

Figure 4a shows another 3D view of solid model of a pair of PTH structures electrically coupled to respective BGA pads via micro-coil structures;

Figure 4b shows a detailed 3D view of a portion of a solid model illustrating a 2-coil micro-coil structure, according to one embodiment;

Figure 5 shows detailed views of six exemplary micro-coil structure configuration and a graph illustrating effective inductance levels using Ansys HFSS full wave 3D electromagnetic modeling software;

Figure 6 is a schematic diagram illustrating a COM reference package model specified by the IEEE 802.3bj – 2014 standard;

Figure 7a is a graph showing the results of differential injection loss test results for a COM reference package model, a COM package terminated with a PTH, crankshaft vias, and a BGA ball, and a COM package terminated with a PTH, micro-coil, and BGA ball;

Figure 7b is a graph showing the results of differential reflection loss test results for the COM reference package model, the COM package terminated with a PTH, crankshaft vias, and a BGA ball, and the COM package terminated with a PTH, micro-coil, and BGA ball;

Figure 8 is a schematic diagram of a circuit model used for an IEEE 100G BASE KR4 COM test;

Figure 9 is a graph illustrating modeled test results for an ISI COM package with FCI short channel, an ISI plus cross-talk crankshaft terminated package with FCI short channel, and an ISI plus cross-talk micro-coil terminated package with FCI short channel; and

Figure 10 is a cross-section view of a circuit board assembly including first and second COM packages having first and second semiconductor components coupled to one another along signal paths passing through micro-coil structures formed in a PCB.

## DETAILED DESCRIPTION

Embodiments of methods and apparatus for inductive compensation in packages and PCB for assemblies with blind and buried vias are described herein. In the following description, numerous specific details are set forth to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, *etc.* In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

For clarity, individual components in the Figures herein may also be referred to by their labels in the Figures, rather than by a particular reference number. Additionally, reference numbers referring to a particular type of component (as opposed to a particular component) may be shown with a reference number followed by "(typ)" meaning "typical." It will be understood that the configuration of these components will be typical of similar components that may exist but are not shown in the drawing Figures for simplicity and clarity or otherwise similar components that are not labeled with separate reference numbers. Conversely, "(typ)" is not to be construed as meaning the component, element, *etc.* is typically used for its disclosed function, implement, purpose, *etc.*

As discussed above, undesired capacitance is introduced by routing pathways formed in the PCBs and communication packages. This is illustrated in Figure 1, which shows a package 100 including a PCB board 102. The electrical connection between routing paths (depicted, in part, by electrical traces 105) in the PCB in the package are implemented using solder ball grid array (BGA) connections or the like, as detailed on the right-hand side of Figure 1. A component, such as a semiconductor die or package (not shown), is mounted to the BGA. The plated through holes (PTH) 106 used for the vias in combination with the BGA pads 108 and solder balls 110 form capacitor structures, as illustrated. In particular, PTH 106 functions as the top plate of the capacitor, with BGA pad 108 and solder ball 110 functioning as the bottom plate. This is not by design, but rather is a result of the particular physical structure of the PTHs and BGAs in the package, with the result being the capacitive structures have a negative impact on system margins because of reflections.

Further details of the PTH structure are shown in Figures 2a and 2b. As shown, PTH 106 extends through the core layer 200 of PCB 100. The bottom and top package via transition regions is referred to herein as the "crankshaft via area" 202 as shown in the 3D detail view of Figure 2b. As further shown, bottom crankshaft via area 202 is in the "shadow" of BGA pad 108.

In accordance with aspects of the invention, the structure in the crankshaft via area of the prior art is replaced with a micro-coil structure. For example, Figures 3a and 3b respectively shown the prior art structure including crankshaft via area 202 and the new configuration, which has replaced crankshaft via area 202 with a micro-coil structure 300.

Further details of one embodiment of micro-coil structure 300 are shown in Figure 4b. Generally, one or more micro-coils 400 are coupled between the base of PTH 106 and BGA pad 108. The inductance of the micro-coil structure is a function of the loop area and trace width, both of which can be controlled during manufacture. The inductance is also proportional to the square of the number of loops. By using a combination of loop area, trace width and number of loops, the amount of inductance can be precisely controlled.

Figure 4b illustrates a micro-coil with two windings, which yields above 1 picoHenry (pH) of inductance. As shown in Figure 4b, since a continuous coil loop cannot be formed using a step-wise manufacturing process (such as used for integrated circuit manufacture and in PCB and package manufacturing), each “loop” is shaped as illustrated. This results in a similar effect as if a continuous coil loop was formed (noting the corresponding inductance is a bit less than a continuous coil loop having similar dimensions).

Additional exemplary configurations of micro-coil structures are shown in Figure 5. As shown, there are three pair-wise sets of configurations that are modeled – 500a and 500b, 502a and 502b, and 504a and 504b. For each pair-wise set, the difference in the models is the arcuate length micro-coil structures 506, 508, and 510. As illustrated, the arcuate length of micro-coil structure 506 is approximately 360 degrees, while the arcuate length of micro-coil structure 508 is approximately 180 degrees and the arcuate length of micro-coil structure 510 is approximately 90 degrees.

A graph 512 is shown on the left-hand side of Figure 5 depicting an effective inductance (in nanoHenries (nH) vs. frequency (Hz x $10^{10}$) for the different micro-coil structure models, using Ansys HFSS full wave 3D electromagnetic modeling. As shown in graph 512, the models that have a longer coil have greater effective inductance up to approximately 28 GHz. However, at frequencies above 28 GHz, there is quite a variation in effective inductance.

The full wave 3D electromagnetic modeling suggest inductance between 50fH (femtoHenries) and 1000fH is feasible. It is projected that tuning resolution of a few fH may be achieved by just adding or subtracting more coil, like wrapping or unwrapping a spool and/or changing the dimensions of the coil. Some applications would require a single loop with between 50fH to 300fH.

IEEE 802.3bj COM Reference Package Model and Test Results

The IEEE 802.3bj – 2014 standard limits the reflections with a return loss specification. A channel operating margin (COM) reference package is also specified in IEEE 802.3bj – 2014, along with the procedure to compute COM, which is a signal-to-noise ratio in dB.

Figure 6 shows a COM reference package model 600, while Figures 7a an 7b are graphs illustrating differential insertion loss (IL) and differential reflection loss (RL) for the following three package selections.

1. COM reference package
2. Package with prior art crankshaft via

3. Package with micro-coil

The s-parameter data for a short backplane channel published in the public area of IEEE802.3bj was cascaded with each of the three following package selections. The package 1 and 2 models have about the same return loss. Package 2 has ~50fF more capacitance at the BGA than assumed in the COM reference package (180fF). The darkest traces in Figures 7a and 7b represent the micro-coil package and shows a smoother insertion loss and lower return loss for the 25Gb/s NRZ (non return to zero) pass band.

The COM results with a short IEEE channel model are as follows:

1. 2.6dB COM with the COM package model
2. 2.0dB COM with Package with Intel prior art crankshaft via
3. 3.6dB COM with Package with Intel m-coil

A COM of greater than 3dB is required to pass the IEEE 802.3bj – 2014 standard.

Figures 8 and 9 respectively show a circuit model 800 and a graph 900 depicting test results for an IEEE 100G BASE KR4 COM test. The COM reference package connection, crankshaft via BGA connection, and M-coil BGA connections were added to the IEEE posted channel FCI_CC_Short_Link_Pair_2_to_Pair_10_Through using BGA connections. The channel has two connectors with 5 cm backplane and line card trace routing. The backplane thickness is 6.4mm. The channel operating margin was modeled at a 25GB/s data rate. COM is 2dB for the COM reference package and non-compensated package crankshaft via termination, while COM is 3.6dB for micro-coil package BGA connection. In addition, the uncompensated ISI is 16mV better with the micro-coil scheme.

Figure 10 shows one embodiment of a PCB assembly 1000. PCB assembly 1000 includes a PCB 1002 in which various micro-coil structures 400 are formed in the manner described above. A first COM package 1104 including a semiconductor component 1106 coupled to a BGA package 1108 is mounted to PCB 1002 via a plurality of solder balls 1010. Similarly, a second COM package 1112 including a semiconductor component 1114 coupled to a BGA package 1116 is mounted to PCB 1002 via a plurality of solder balls 1018.

The micro-coil structures 400 are coupled to PTHs formed areas 1020 and 1022 in PCB 102. Various interconnect wiring and vias, collectively shown by an interconnect layer 1024 for simplicity, couples signals from the PTHs in areas 1020 and 1022. As will be understood by those having skill in the art, the interconnect wiring and vias may be formed in multiple layers in PCB 1002.

Signals generated by semiconductor components 1106 and 1114 are routed through PCB 1002 along routing paths that pass through micro-coil structures 400. As a result, the signals are subject to far less signal degradation due to capacitive coupling between the BGA pads and the bases of the PTHs.

Further aspects of the subject matter described herein are set out in the following numbered clauses:

1. An apparatus including a printed circuit board (PCB) comprising:

a first conductive layer including a ball grid array (BGA) pad;

second and third conductive layers, wherein the second conductive layer is disposed between the first and third conductive layers;

a core layer, disposed between the second and third conductive layers;

a plated through hole (PTH) passing through the core layer, the PTH having a base formed in the second conductive layer and conductively connecting the base to a trace in the third conductive layer; and

a micro-coil structure conductively connecting the base of the PTH and the BGA pad.

2. The apparatus of clause 1, wherein the micro-coil structure includes a first arcuate trace formed in a fourth conductive layer disposed between the first conductive layer and the second conductive layer.

3. The apparatus of clause 2, wherein the micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the second conductive layer.

4. The apparatus of clause 3, further comprising a buried via coupling the first arcuate trace to the second arcuate trace.

5. The apparatus of clause 3, wherein the first and second arcuate traces form a loop segment of at least 270 degrees.

6. The apparatus of clause 3, wherein the first and second arcuate traces form a multi-loop segment of at least 630 degrees.

7. The apparatus of any of clauses 2-6, wherein the micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the second conductive layer and a third arcuate trace formed in a sixth layer between the fifth layer and the second conductive layer.

8. The apparatus of any of the preceding clauses, wherein an inductance of the micro-coil structure offsets a capacitance generated by a gap between the PTH and the BGA pad.

9. The apparatus of any of the preceding clauses, wherein the micro-coil structure includes at least one trace that follows a radius offset from an axis coincident with a centerline axis of the PTH, and wherein the centerline axis of the PTH is substantially aligned with a centerline of the BGA pad.

10. The apparatus of any of the preceding clauses, wherein the micro-coil structure has an inductance of at least 1 pH.

11. The apparatus of any of clauses 1-9, wherein the micro-coil structure has an inductance between 50 fH and 300 fH.

12. An apparatus including a circuit board assembly, the apparatus comprising:

an integrated circuit;

a ball grid array electrically coupled to the integrated circuit; and

a printed circuit board (PCB) including:

a first conductive layer including a plurality of BGA pads coupled to the ball grid array;

second and third conductive layers, wherein the second conductive layer is disposed between the first and third conductive layers;

a core layer, disposed between the second conductive layer and the third conductive layer;

a plurality of plated through holes (PTHs) passing through the core layer, each of at least a portion of the plurality of PTHs having a based formed in the second conductive layer and conductively connecting the base to a trace in the third conductive layer; and

for each of at least a portion of the plurality of BGA pads, a respective micro-coil structure electrically coupled between a respective BGA pad and a respective PTH base in the second conductive layer.

13. The apparatus of clause 12, wherein at least one micro-coil structure includes a first arcuate trace formed in a fourth conductive layer disposed between the first conductive layer and the second conductive layer.

14. The apparatus of clause 13, wherein the micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the first conductive layer.

15. The apparatus of clause 13, wherein at least one micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the first conductive layer and a third arcuate trace formed in a sixth layer between the fifth conductive layer and the first conductive layer.

16. The apparatus of any of clauses 12-15, wherein an inductance of at least one micro-coil structure offsets a capacitance generated by a gap between the PTH base and the BGA pad to which that micro-coil structure is electrically coupled.

17. The apparatus of any of clauses 12-15, wherein at least one micro-coil structure includes at least one trace that follows a radius offset from an axis coincident with a centerline axis of one

of the PTHs, and wherein the centerline axis of the PTH is substantially aligned with a centerline of one of the BGA pads.

18. The apparatus of any of clauses 12-17, wherein the integrated circuit is a communications chip having a Physical (PHY) layer interface, and wherein at least one micro-coil structure is included in a receive or transmit pathway of a high-speed communications channel coupled to the PHY layer interface having a transmission bandwidth of at least 25 Gigabits per second.

19. The apparatus of any of clauses 12-18, wherein at least one micro-coil structure has an inductance of at least 1 pH.

20. The apparatus of any of clauses 12-18, wherein at least one micro-coil structure has an inductance between 50 fH and 300 fH.

21. An apparatus including a circuit board assembly, the apparatus comprising:

a printed circuit board (PCB);

a first ball grid array (BGA);

a first circuit component mounted to the PCB via the first BGA;

a second BGA; and

a second circuit component mounted to the PCB via the second BGA, wherein the PCB includes,

a first conductive layer including a first plurality BGA pads coupled to the first BGA and a second plurality of BGA pads coupled to the second BGA;

second and third conductive layers, wherein the second conductive layer is disposed between the first and third conductive layers;

first and second pluralities of plated through holes (PTHs), each of at least a portion of which having a base formed in the second conductive layer and conductively connecting the base to a trace in the third conductive layer;

first and second pluralities of micro-coil structures, wherein each of the first plurality of the micro-coil structures is electrically coupled between the base of a respective PTH among the first plurality of PTHs and a respective BGA pad among the first plurality of BGA pads, and wherein each of the second plurality of the micro-coil structures is electrically coupled between the base of a respective PTH among the second plurality of PTHs and a respective BGA pad among the second plurality of BGA pads; and

signal path routing coupling respective pairs of PTHs in the first and second plurality of PTHs that are coupled to respective micro-coil structures.

22. The apparatus of clause 21, wherein the PCB includes a core layer, and wherein the PTHs pass through the core layer.

23. The apparatus of clause 21 or 22, wherein at least one of the micro-coil structures includes a first arcuate trace formed in a fourth conductive layer disposed between the first conductive layer and the second conductive layer.

24. The apparatus of any of clauses 21-23, wherein at least one of the micro-coil structures includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the first conductive layer.

25. The apparatus of clause 24, wherein the at least one of the micro-coil structures further comprises a buried via coupling the first arcuate trace to the second arcuate trace.

26. The apparatus of clause 24, wherein the first and second arcuate traces form a loop segment of at least 270 degrees.

27. The apparatus of clause 24, wherein the first and second arcuate traces form a multi-loop segment of at least 630 degrees.

28. The apparatus of any of clauses 21-27, wherein at least one of the micro-coil structures has an inductance of at least 1 pH.

29. The apparatus of clause 21-27, wherein at least one of the micro-coil structures has an inductance between 50 fH and 300 fH.

30. The apparatus of any of clauses 21-29, wherein the signal path routing comprises one of traces or wiring in an internal layer in the PCB.

31. The apparatus of any of clauses 21-30, wherein the first circuit component and second circuit component are communication chips.

32. The apparatus of clause 31, wherein the communication chips support an Ethernet communication link having at least one lane with a bandwidth of at least 25 Gigabits per second, and wherein the transmission path for each of the at least one lane passes through a respective micro-coil structure.

33. The apparatus of clause 31, wherein the communication chips support an Ethernet communication link having four lanes, each having a bandwidth of at least 25 Gigabits per second, and wherein the transmission path for each lane passes through a respective micro-coil structure.

34. The apparatus of any of clauses 21-33, wherein an inductance of at least one of the micro-coil structures offsets a capacitance generated by a gap between the base of the PTH and the BGA pad the micro-coil structure is electrically coupled between.

35. The apparatus of any of clauses 21-34, wherein at least one micro-coil structure includes at least one trace that follows a radius offset from an axis coincident with a centerline axis of the PTH to which the micro-coil structure is coupled, and wherein the centerline axis of the PTH is

substantially aligned with a centerline of the BGA pad to which the micro-coil structure is electrically coupled.

Although some embodiments have been described in reference to particular implementations, other implementations are possible according to some embodiments. Additionally, the arrangement and/or order of elements or other features illustrated in the drawings and/or described herein need not be arranged in the particular way illustrated and described. Many other arrangements are possible according to some embodiments.

In each system shown in a figure, the elements in some cases may each have a same reference number or a different reference number to suggest that the elements represented could be different and/or similar. However, an element may be flexible enough to have different implementations and work with some or all of the systems shown or described herein. The various elements shown in the figures may be the same or different. Which one is referred to as a first element and which is called a second element is arbitrary.

In the description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

An embodiment is an implementation or example of the inventions. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the inventions. The various appearances "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.

Not all components, features, structures, characteristics, *etc.* described and illustrated herein need be included in a particular embodiment or embodiments. If the specification states a component, feature, structure, or characteristic "may", "might", "can" or "could" be included, for example, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

An algorithm is here, and generally, considered to be a self-consistent sequence of acts or operations leading to a desired result. These include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like. It should be understood, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

As discussed above, various aspects of the embodiments herein may be facilitated by corresponding software and/or firmware components and applications, such as software and/or firmware executed by an embedded processor or the like. Thus, embodiments of this invention may be used as or to support a software program, software modules, firmware, and/or distributed software executed upon some form of processor, processing core or embedded logic a virtual machine running on a processor or core or otherwise implemented or realized upon or within a computer-readable or machine-readable non-transitory storage medium. A computer-readable or machine-readable non-transitory storage medium includes any mechanism for storing or transmitting information in a form readable by a machine (*e.g.*, a computer). For example, a computer-readable or machine-readable non-transitory storage medium includes any mechanism that provides (*i.e.*, stores and/or transmits) information in a form accessible by a computer or computing machine (*e.g.*, computing device, electronic system, *etc.*), such as recordable/non-recordable media (*e.g.*, read only memory (ROM), random access memory (RAM), magnetic disk storage media, optical storage media, flash memory devices, *etc.*). The content may be directly executable ("object" or "executable" form), source code, or difference code ("delta" or "patch" code). A computer-readable or machine-readable non-transitory storage medium may also include a storage or database from which content can be downloaded. The computer-readable or machine-readable non-transitory storage medium may also include a device or product having content stored thereon at a time of sale or delivery. Thus, delivering a device with stored content, or offering content for download over a communication medium may be understood as providing an article of manufacture comprising a computer-readable or machine-readable non-transitory storage medium with such content described herein.

Various components referred to above as processes, servers, or tools described herein may be a means for performing the functions described. The operations and functions performed by various components described herein may be implemented by software running on a processing element, via embedded hardware or the like, or any combination of hardware and software. Such components may be implemented as software modules, hardware modules, special-purpose hardware (*e.g.*, application specific hardware, ASICs, DSPs, *etc.*), embedded controllers, hardwired circuitry, hardware logic, *etc.* Software content (*e.g.*, data, instructions, configuration information, *etc.*) may be provided via an article of manufacture including computer-readable or machine-readable non-transitory storage medium, which provides content that represents instructions that can be executed. The content may result in a computer performing various functions/operations described herein.

As used herein, a list of items joined by the term "at least one of" can mean any combination of the listed terms. For example, the phrase "at least one of A, B or C" can mean A; B; C; A and B; A and C; B and C; or A, B and C.

The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the drawings. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

What is Claimed is:

1. An apparatus including a printed circuit board (PCB) comprising:

a first conductive layer including a ball grid array (BGA) pad;

second and third conductive layers, wherein the second conductive layer is disposed between the first and third conductive layers;

a core layer, disposed between the second and third conductive layers;

a plated through hole (PTH) passing through the core layer, the PTH having a base formed in the second conductive layer and conductively connecting the base to a trace in the third conductive layer; and

a micro-coil structure conductively connecting the base of the PTH and the BGA pad.

2. The apparatus of claim 1, wherein the micro-coil structure includes a first arcuate trace formed in a fourth conductive layer disposed between the first conductive layer and the second conductive layer.

3. The apparatus of claim 2, wherein the micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the second conductive layer.

4. The apparatus of claim 3, further comprising a buried via coupling the first arcuate trace to the second arcuate trace.

5. The apparatus of claim 3, wherein the first and second arcuate traces form a loop segment of at least 270 degrees.

6. The apparatus of claim 3, wherein the first and second arcuate traces form a multi-loop segment of at least 630 degrees.

7. The apparatus of any of claims 2-6, wherein the micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the second conductive layer and a third arcuate trace formed in a sixth layer between the fifth layer and the second conductive layer.

8. The apparatus of any of the preceding claims, wherein an inductance of the micro-coil structure offsets a capacitance generated by a gap between the PTH and the BGA pad.

9. The apparatus of any of the preceding claims, wherein the micro-coil structure includes at least one trace that follows a radius offset from an axis coincident with a centerline axis of the PTH, and wherein the centerline axis of the PTH is substantially aligned with a centerline of the BGA pad.

10. An apparatus including a circuit board assembly, the apparatus comprising:

an integrated circuit;

a ball grid array electrically coupled to the integrated circuit; and

a printed circuit board (PCB) including:

a first conductive layer including a plurality of BGA pads coupled to the ball grid array;

second and third conductive layers, wherein the second conductive layer is disposed between the first and third conductive layers;

a core layer, disposed between the second conductive layer and the third conductive layer;

a plurality of plated through holes (PTHs) passing through the core layer, each of at least a portion of the plurality of PTHs having a based formed in the second conductive layer and conductively connecting the base to a trace in the third conductive layer; and

for each of at least a portion of the plurality of BGA pads, a respective micro-coil structure electrically coupled between a respective BGA pad and a respective PTH base in the second conductive layer.

11. The apparatus of claim 10, wherein at least one micro-coil structure includes a first arcuate trace formed in a fourth conductive layer disposed between the first conductive layer and the second conductive layer.

12. The apparatus of claim 11, wherein the micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the first conductive layer.

13. The apparatus of claim 11, wherein at least one micro-coil structure includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the first conductive layer and a third arcuate trace formed in a sixth layer between the fifth conductive layer and the first conductive layer.

14. The apparatus of any of claims 10-13, wherein an inductance of at least one micro-coil structure offsets a capacitance generated by a gap between the PTH base and the BGA pad to which that micro-coil structure is electrically coupled.

15. The apparatus of any of claims 10-13, wherein at least one micro-coil structure includes at least one trace that follows a radius offset from an axis coincident with a centerline axis of one of the PTHs, and wherein the centerline axis of the PTH is substantially aligned with a centerline of one of the BGA pads.

16. The apparatus of any of claims 10-15, wherein the integrated circuit is a communications chip having a Physical (PHY) layer interface, and wherein at least one micro-coil structure is included in a receive or transmit pathway of a high-speed communications channel coupled to the PHY layer interface having a transmission bandwidth of at least 25 Gigabits per second.

17. An apparatus including a circuit board assembly, the apparatus comprising:

a printed circuit board (PCB);

a first ball grid array (BGA);

a first circuit component mounted to the PCB via the first BGA;

a second BGA; and

a second circuit component mounted to the PCB via the second BGA, wherein the PCB includes,

a first conductive layer including a first plurality BGA pads coupled to the first BGA and a second plurality of BGA pads coupled to the second BGA;

second and third conductive layers, wherein the second conductive layer is disposed between the first and third conductive layers;

first and second pluralities of plated through holes (PTHs), each of at least a portion of which having a base formed in the second conductive layer and conductively connecting the base to a trace in the third conductive layer;

first and second pluralities of micro-coil structures, wherein each of the first plurality of the micro-coil structures is electrically coupled between the base of a respective PTH among the first plurality of PTHs and a respective BGA pad among the first plurality of BGA pads, and wherein each of the second plurality of the micro-coil structures is electrically coupled between the base of a respective PTH among the second plurality of PTHs and a respective BGA pad among the second plurality of BGA pads; and signal path routing coupling respective pairs of PTHs in the first and second plurality of PTHs that are coupled to respective micro-coil structures.

18. The apparatus of claim 17, wherein the PCB includes a core layer, and wherein the PTHs pass through the core layer.

19. The apparatus of claim 17 or 18, wherein at least one of the micro-coil structures includes a first arcuate trace formed in a fourth conductive layer disposed between the first conductive layer and the second conductive layer.

20. The apparatus of any of claims 17-19, wherein at least one of the micro-coil structures includes a second arcuate trace formed in a fifth conductive layer disposed between the fourth conductive layer and the first conductive layer.

21. The apparatus of claim 20, wherein the at least one of the micro-coil structures further comprises a buried via coupling the first arcuate trace to the second arcuate trace.

22. The apparatus of claim 20, wherein the first and second arcuate traces form a loop segment of at least 270 degrees.

23. The apparatus of claim 20, wherein the first and second arcuate traces form a multi-loop segment of at least 630 degrees.

24. The apparatus of any of claims 17-23, wherein the first circuit component and second circuit component are communication chips, wherein the communication chips support an Ethernet communication link having at least one lane with a bandwidth of at least 25 Gigabits per second, and wherein the transmission path for each of the at least one lane passes through a respective micro-coil structure.

25. The apparatus of any of claims 17-24, wherein at least one micro-coil structure includes at least one trace that follows a radius offset from an axis coincident with a centerline axis of the PTH to which the micro-coil structure is coupled, and wherein the centerline axis of the PTH is substantially aligned with a centerline of the BGA pad to which the micro-coil structure is electrically coupled.

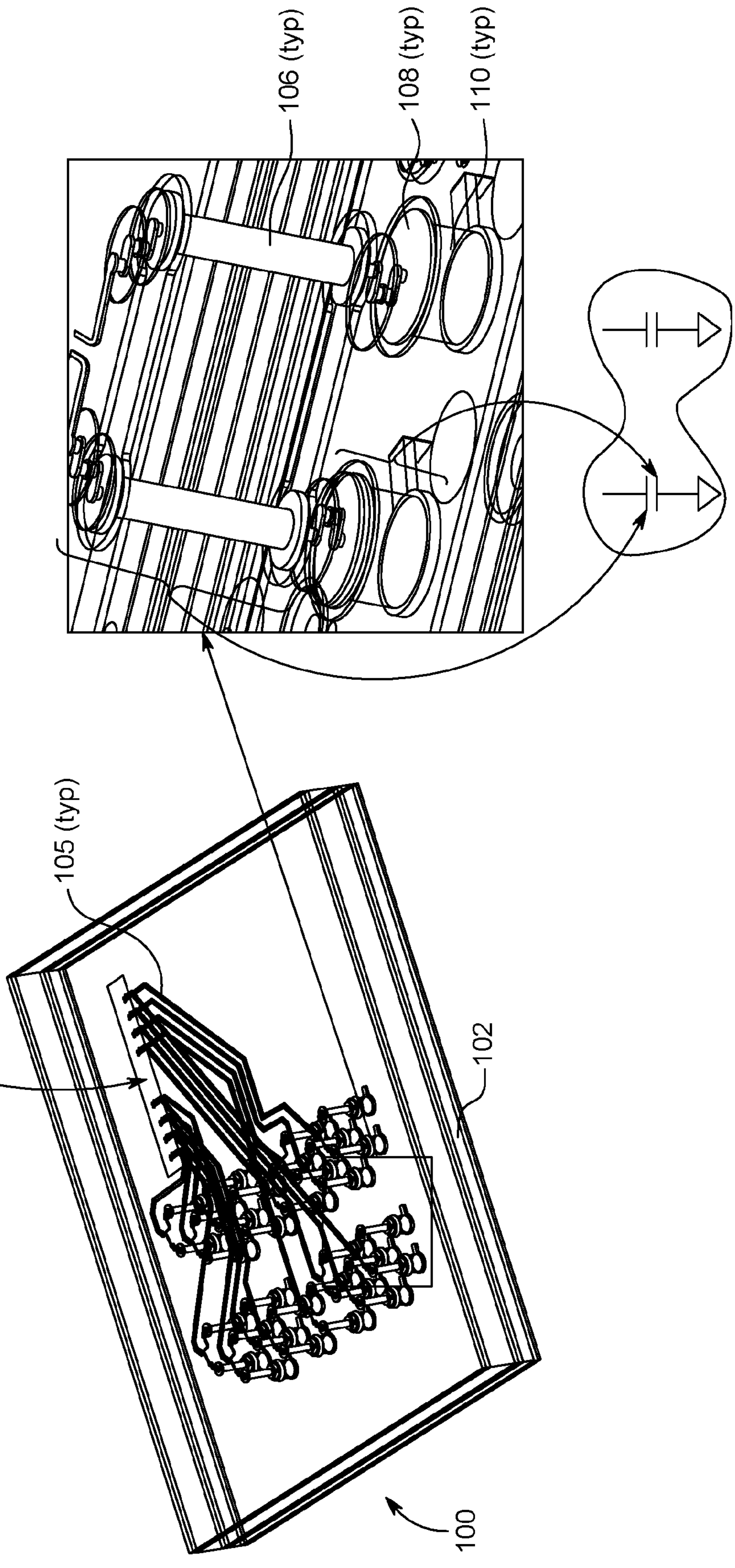



*Fig. 1* *(prior art)*

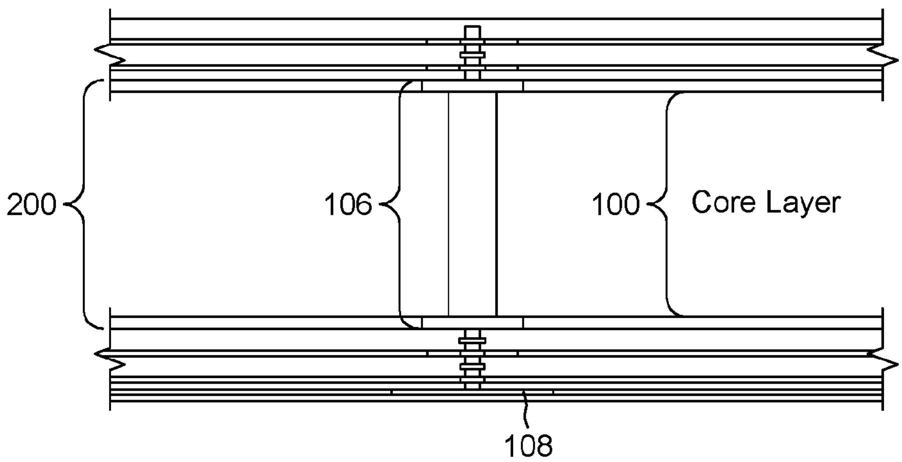



*Fig. 2a* *(prior art)*

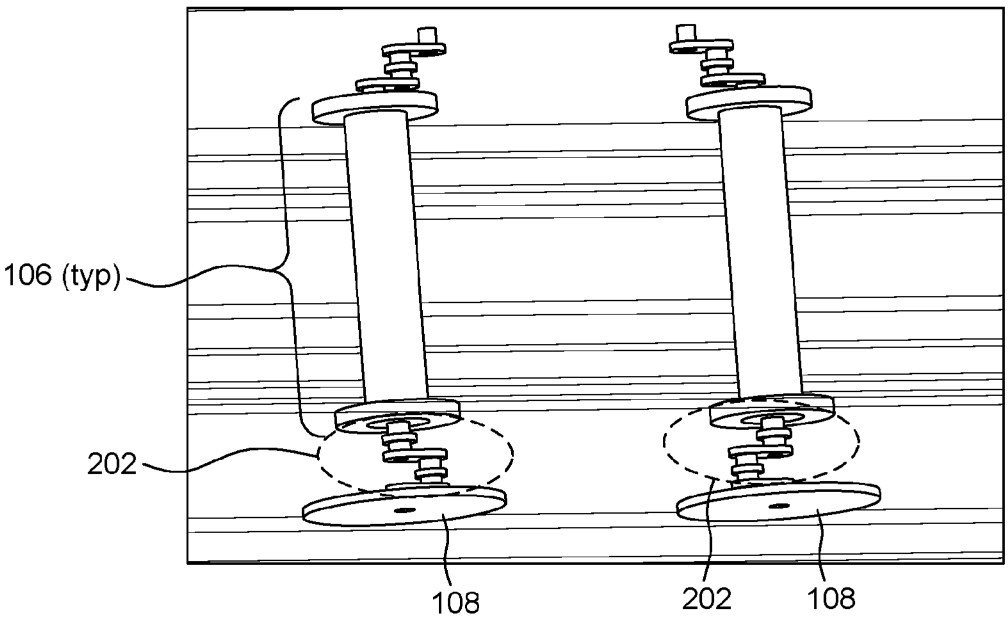



*Fig. 2b* *(prior art)*

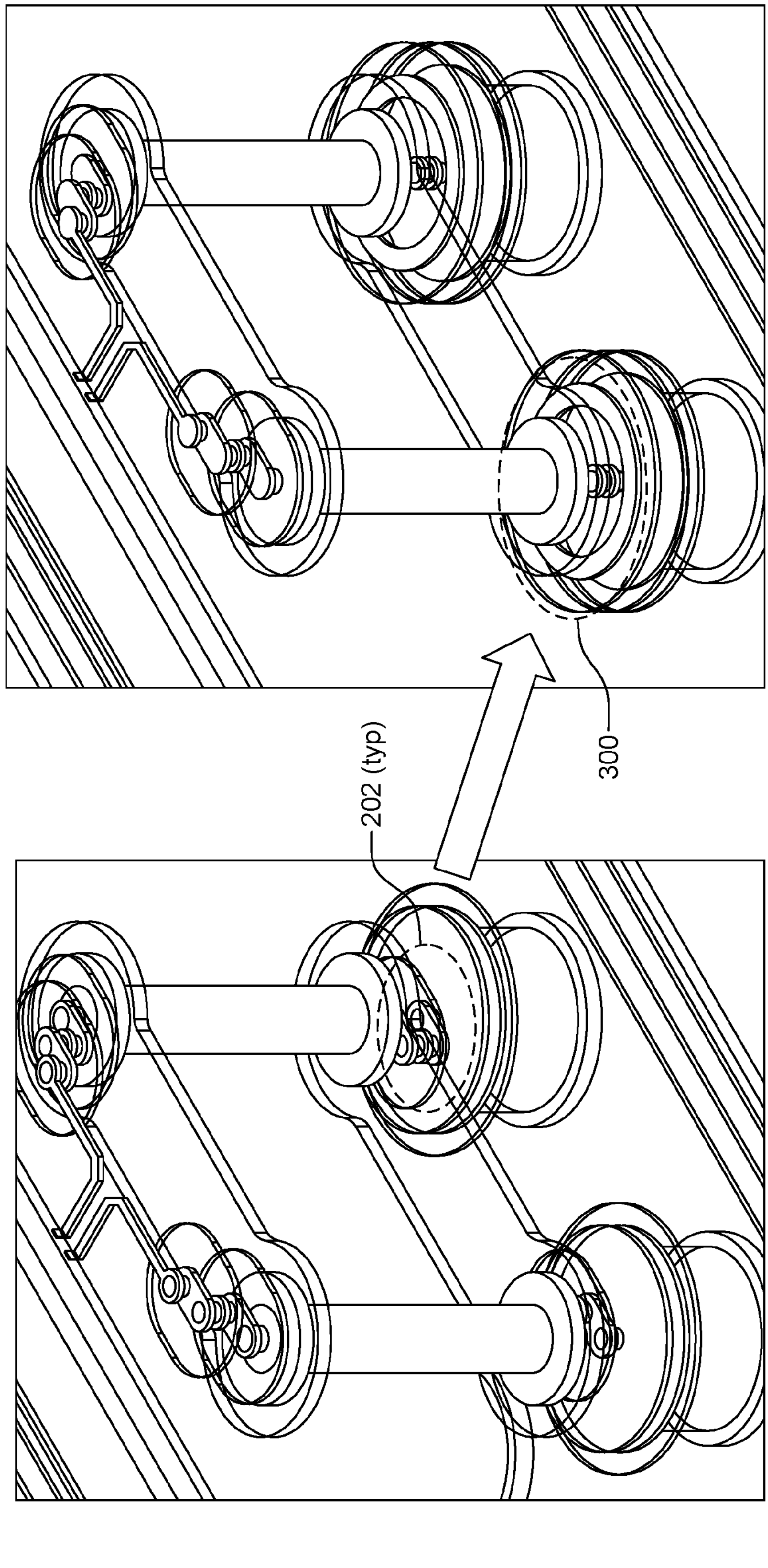



*Fig. 3b*

*Fig. 3a (prior art)*

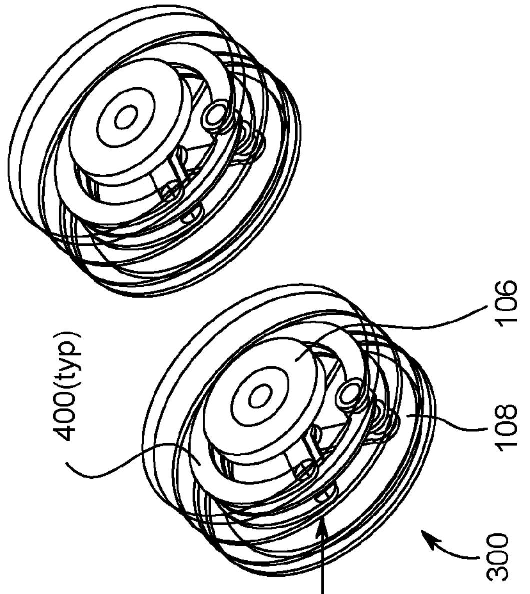



*Fig. 4b*

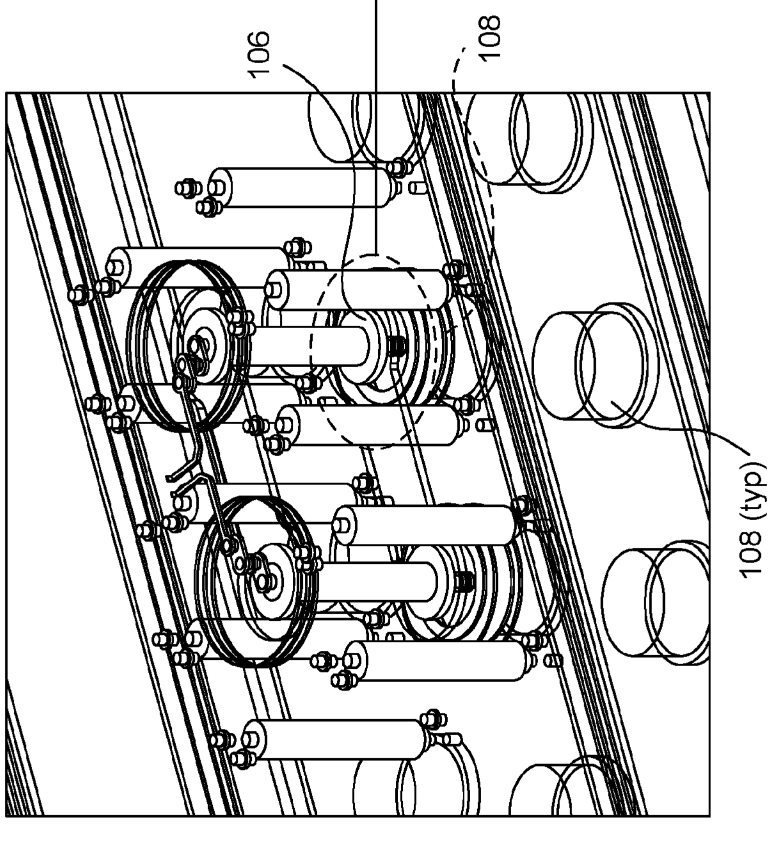



*Fig. 4a*

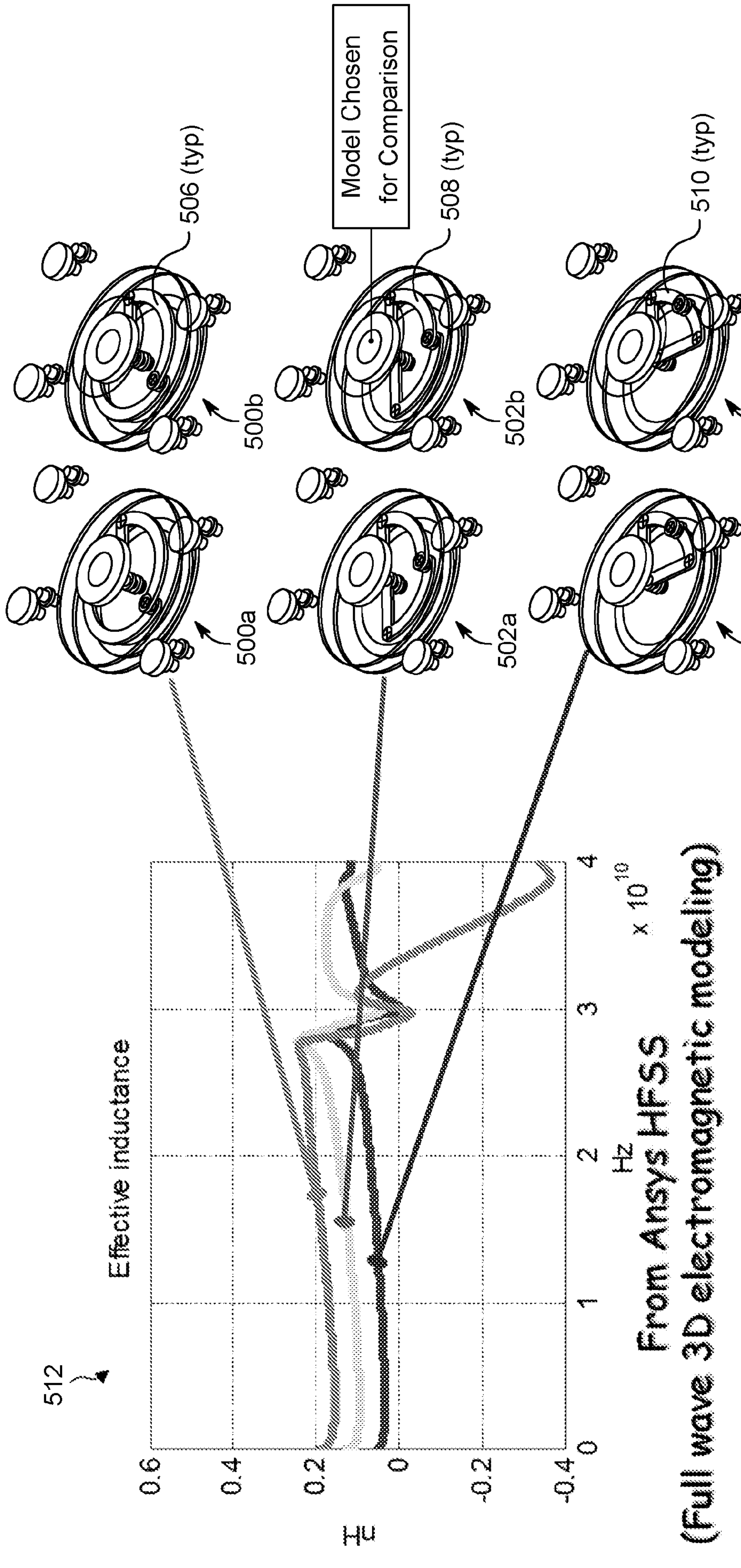

512
Effective inductance
nH
0.6
0.4
0.2
0
-0.2
-0.4
0
1
2
3
4
Hz
x 10^10
From Ansys HFSS
(Full wave 3D electromagnetic modeling)
500a
500b
502a
502b
504a
504b
506 (typ)
508 (typ)
510 (typ)
Model Chosen
for Comparison

*Fig. 5*

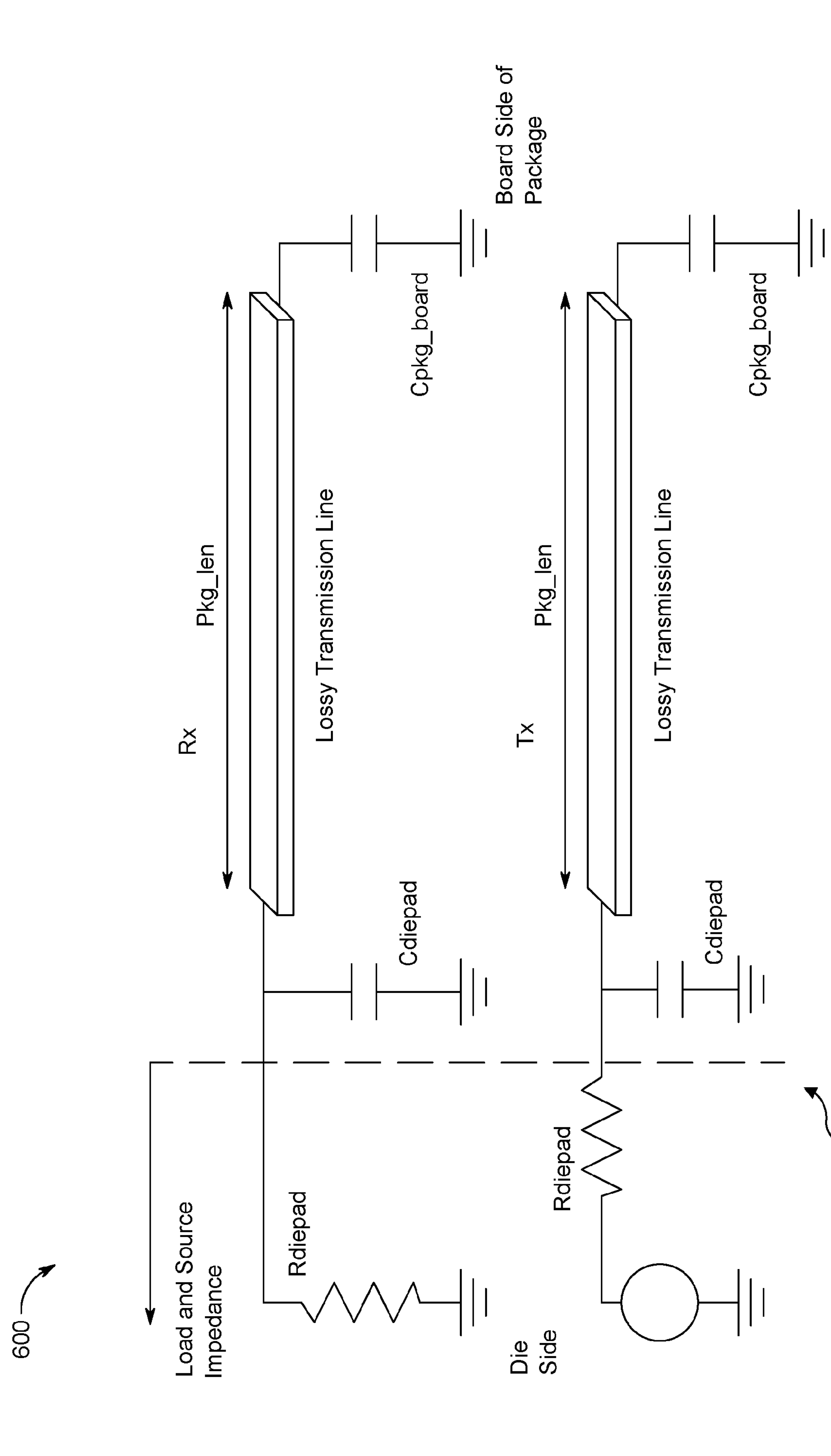

Board Side of
Package
Cpkg_board
Cpkg_board
Rx
Pkg_len
Lossy Transmission Line
Tx
Pkg_len
Lossy Transmission Line
Cdiepad
Cdiepad
Rdiepad
Rdiepad
600
600
Load and Source
Impedance
Die
Side

*Fig. 6*

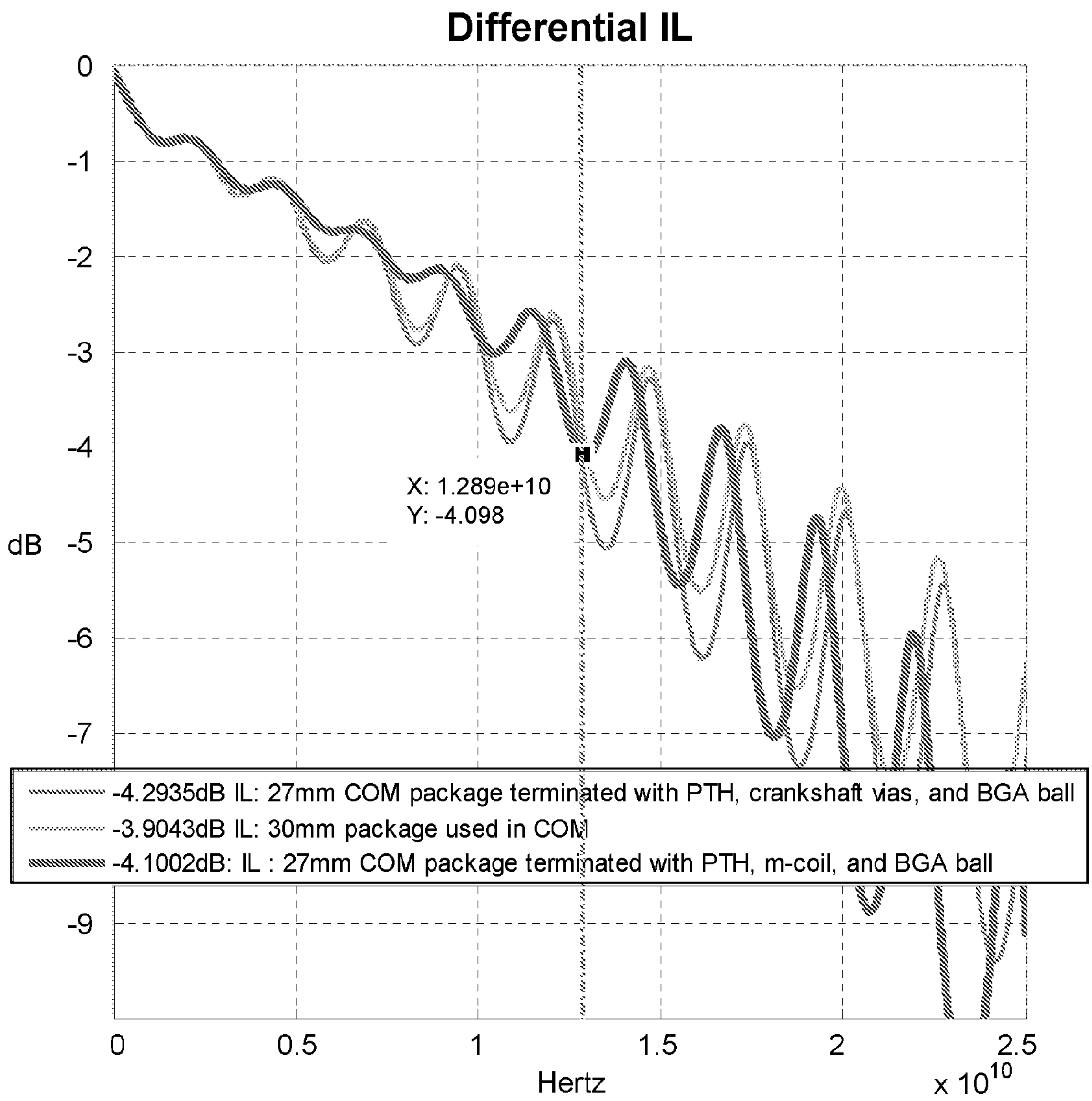
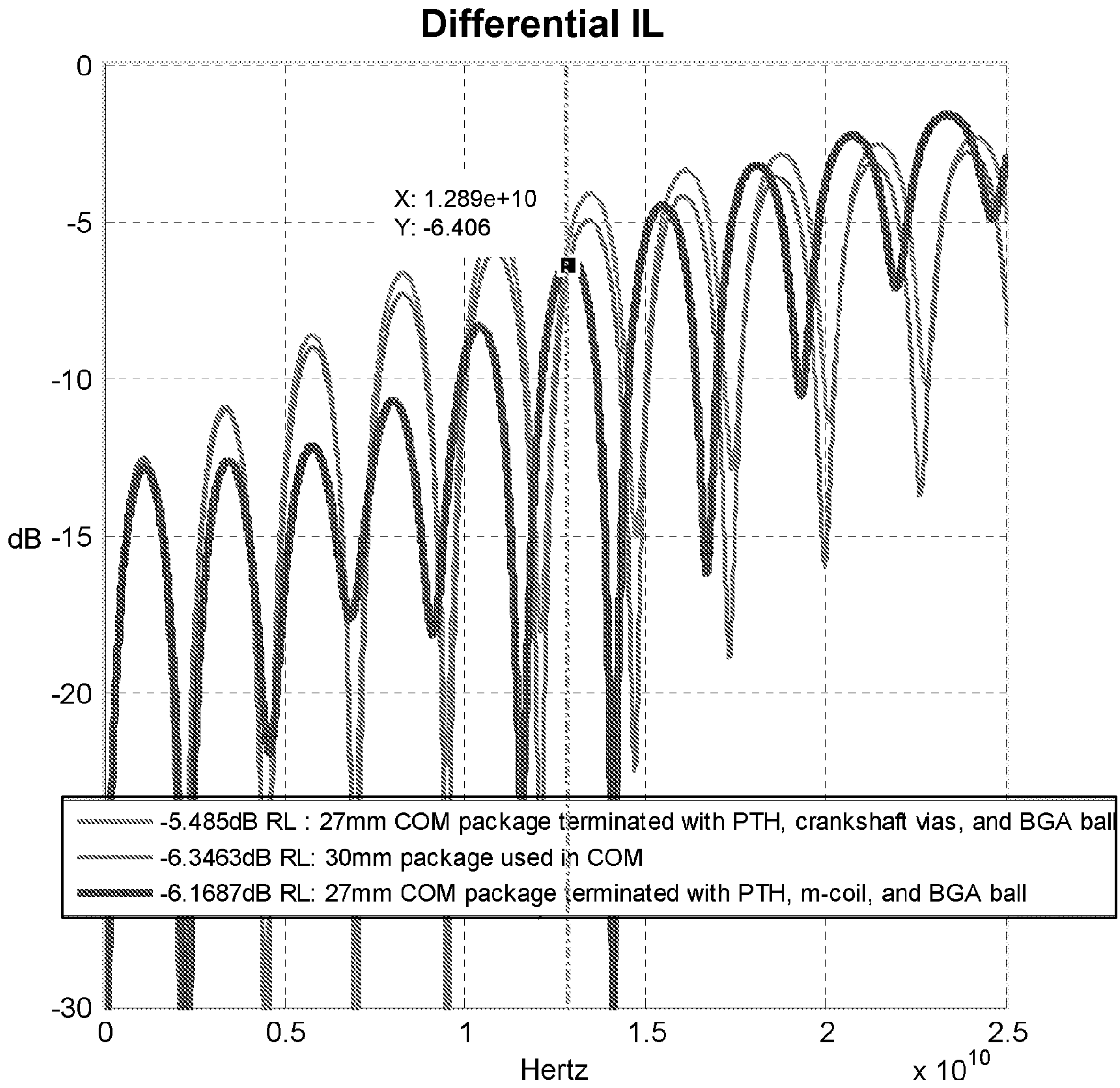

Differential IL
0
-1
-2
-3
-4
-5
-6
-7
-9
dB
X: 1.289e+10
Y: -4.098
-4.2935dB IL: 27mm COM package terminated with PTH, crankshaft vias, and BGA ball
-3.9043dB IL: 30mm package used in COM
-4.1002dB: IL : 27mm COM package terminated with PTH, m-coil, and BGA ball
0
0.5
1
1.5
2
2.5
Hertz
x 10^10

*Fig. 7a*



Differential IL
0
-5
-10
dB -15
-20
-30
X: 1.289e+10
Y: -6.406
-5.485dB RL : 27mm COM package terminated with PTH, crankshaft vias, and BGA ball
-6.3463dB RL: 30mm package used in COM
-6.1687dB RL: 27mm COM package terminated with PTH, m-coil, and BGA ball
0
0.5
1
1.5
2
2.5
Hertz
x 10^10


*Fig. 7b*

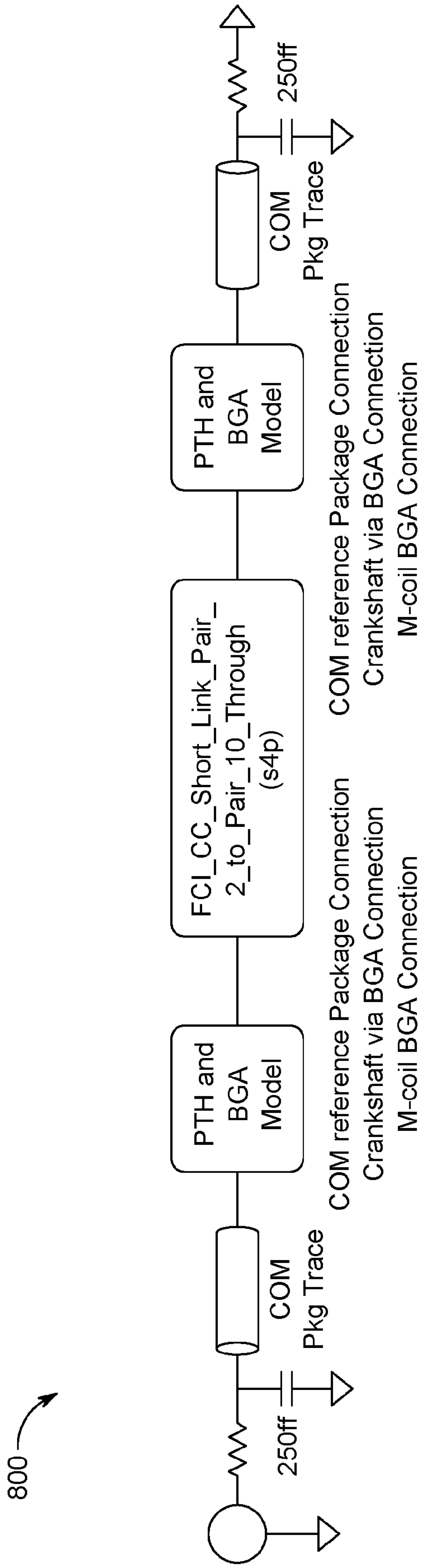

800
250ff
COM
Pkg Trace
PTH and
BGA
Model
COM reference Package Connection
Crankshaft via BGA Connection
M-coil BGA Connection
FCI_CC_Short_Link_Pair_
2_to_Pair_10_Through
(s4p)
COM reference Package Connection
Crankshaft via BGA Connection
M-coil BGA Connection
PTH and
BGA
Model
COM
Pkg Trace
250ff

*Fig. 8*

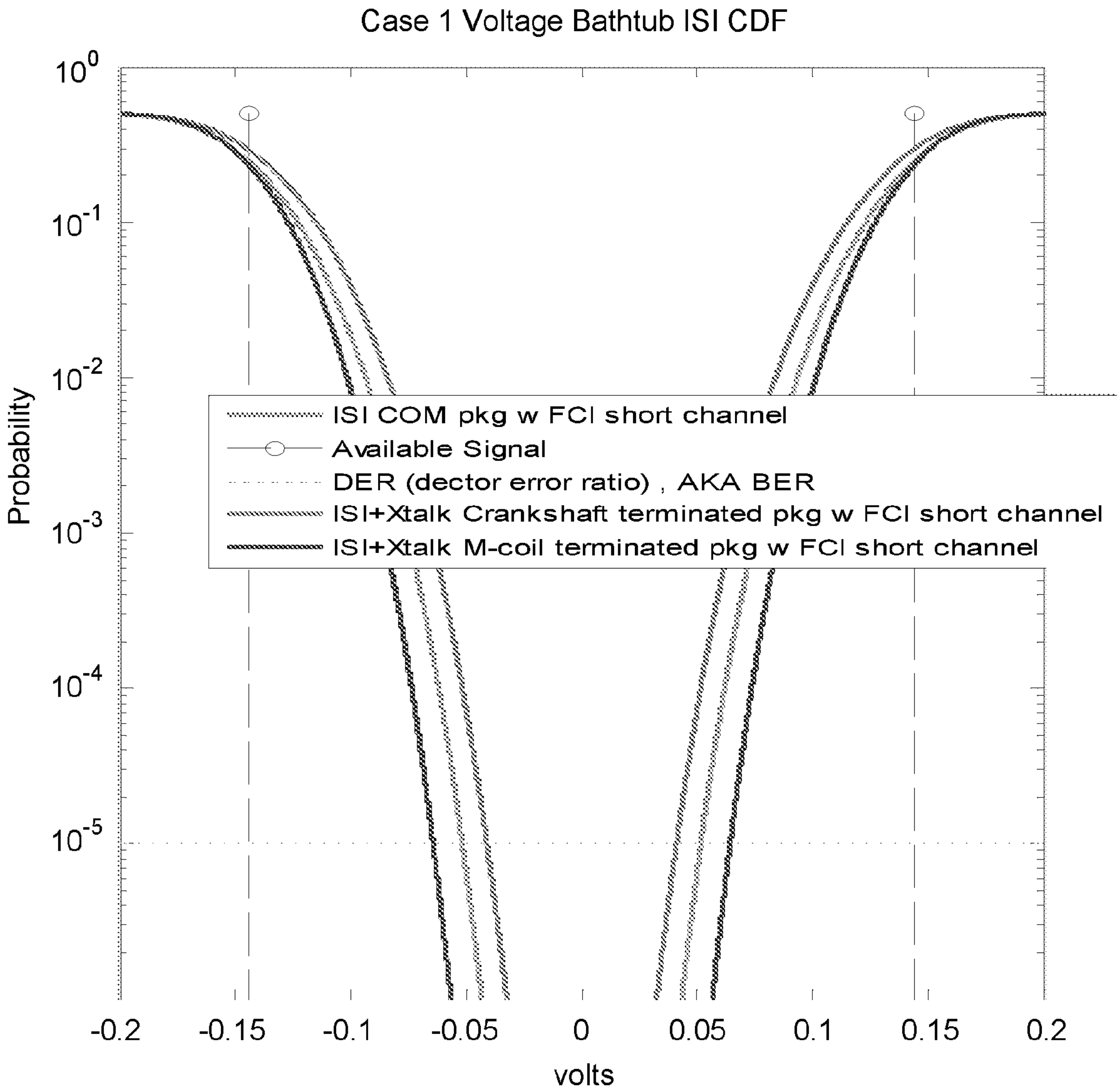

Case 1 Voltage Bathtub ISI CDF
Probability
volts
$10^{0}$
$10^{-1}$
$10^{-2}$
$10^{-3}$
$10^{-4}$
$10^{-5}$
-0.2
-0.15
-0.1
-0.05
0
0.05
0.1
0.15
0.2
ISI COM pkg w FCI short channel
Available Signal
DER (dector error ratio) , AKA BER
ISI+Xtalk Crankshaft terminated pkg w FCI short channel
ISI+Xtalk M-coil terminated pkg w FCI short channel

***Fig. 9***

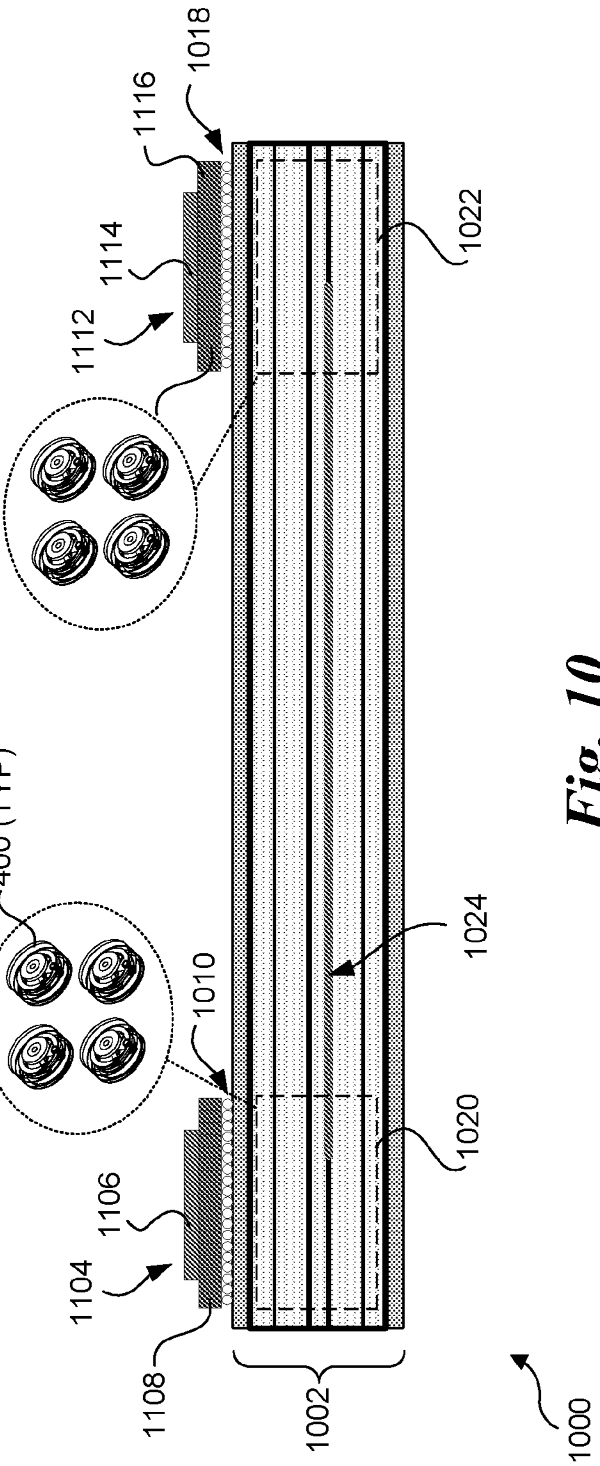

1018
1116
1114
1112
1022
400 (TYP)
1010
1024
1106
1104
1020
1108
1002
1000

*Fig. 10*

**INTERNATIONAL SEARCH REPORT**

International application No.
**PCT/US2016/067697**

**A. CLASSIFICATION OF SUBJECT MATTER**

**H05K 1/02(2006.01)i, H05K 1/11(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H05K 1/02; H01R 33/76; H01F 41/04; H01L 23/32; H01F 17/00; H01F 41/02; G01R 31/02; H01R 4/02; H05K 1/11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: printed circuit board (PCB), ball grid array (BGA) pad, core layer, plated through hole (PTH), micro-coil structure

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br><br>Y | JP 2011-210596 A (MURATA MFG CO., LTD.) 20 October 2011<br>See paragraphs [0025]-[0026], [0050]-[0054] and figures 9-10. | 1-2,10-11,14-15<br>,17-19<br>3-7,12-13 |
| Y | KR 10-1096108 B1 (KOREA INSTITUTE OF INDUSTRIAL TECHNOLOGY) 19 December 2011<br>See paragraphs [0030], [0037] and figures 1-3. | 3-7,12-13 |
| A | US 2014-0262498 A1 (U.S.A. AS REPRESENTED BY THE ADMINISTRATOR OF THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION) 18 September 2014<br>See paragraph [0024] and figure 5. | 1-7,10-15,17-19 |
| A | US 2004-0257099 A1 (TOSHIO KAZAMA) 23 December 2004<br>See paragraph [0055] and figure 8. | 1-7,10-15,17-19 |
| A | US 5852866 A (KLAUS KUETTNER et al.) 29 December 1998<br>See columnm 2, line 59 - column 6, line 29 and figures 1-4. | 1-7,10-15,17-19 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 30 March 2017 (30.03.2017) | **31 March 2017 (31.03.2017)** |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**INTERNATIONAL SEARCH REPORT**

International application No.
**PCT/US2016/067697**

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 21-23
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 21-23 were found unsearchable, because these claims refer to unsearchable multiple dependent claims, which are not drafted in accordance with the second (or third) sentence of PCT Rule 6.4(a).

3. ☒ Claims Nos.: 8-9,16,20,24-25
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

**INTERNATIONAL SEARCH REPORT**
Information on patent family members

International application No.
**PCT/US2016/067697**

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| JP 2011-210596 A | 20/10/2011 | None | |
| KR 10-1096108 B1 | 19/12/2011 | KR 10-2011-0059997 A | 08/06/2011 |
| US 2014-0262498 A1 | 18/09/2014 | None | |
| US 2004-0257099 A1 | 23/12/2004 | US 2003-0016037 A1<br>US 6781390 B2<br>US 6873168 B2 | 23/01/2003<br>24/08/2004<br>29/03/2005 |
| US 5852866 A | 29/12/1998 | None | |