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(54) **Title**: CONSTANT BRIGHTNESS LED DRIVE COMMUNICATIONS PORT

(57) **Abstract**: A light emitting diode (LED) is driven with a plurality of pulses having controllable pulse widths and positions within clock time periods that provide for both LED light intensity control and digital information communications from a single output node of an integrated circuit (IC) device. The LED light intensity is determined by the duty cycle of the pulses where the human eye integrates these light pulses from the LED into continuous light intensity levels. The digital information contained in the light output from the LED is detected by a photo-detector that converts the light pulses into electric signals that are demodulated and read by a circuit debugger and/or manufacturing test station. The aforementioned operations allow continuous visual display and data transmission using only one output node of the IC device. This is especially advantageous when using low pin count IC devices.

CONSTANT BRIGHTNESS LED DRIVE COMMUNICATIONS PORT

TECHNICAL FIELD

The present disclosure relates to low pin count integrated circuit devices, and more particularly, to a single pin having simultaneous dual uses on the integrated circuit package for providing both status communications and visual display.

BACKGROUND

A low pin count integrated circuit application often requires a light emitting diode (LED) for indication and/or status. In addition, all low pin count integrated circuit devices preferably have some type of communications channel during development and final production.

SUMMARY

Therefore, there is a need for a way to provide both visual indication and communications, *e.g.*, program operation, data and/or status, for a low pin count integrated circuit application.

According to an embodiment, a method for driving a light emitting diode (LED) and transmitting digital information using a single node of an integrated circuit device may comprise the steps of: generating a plurality of pulses from a single node of an integrated circuit device; and coupling the plurality of pulses from the single node of the integrated circuit device to a light emitting diode (LED); wherein the plurality of pulses from the single node of the integrated circuit device control light intensity from the LED and transmit digital information.

According to a further embodiment of the method, the light intensity from the LED may be substantially proportional to pulse widths of the plurality of pulses. According to a further embodiment of the method, each of the plurality of pulses may occur within two sequential clock times. According to a further embodiment of the method, a level change for each of the plurality of pulses may occur within two sequential clock times. According to a further embodiment of the method, a high to low level change may represent a logic 1 and a low to high level change may represent a logic 0. According to a further embodiment of the method, a low to high level change may represent a logic 1 and a high to low level change may represent a logic 0. According to a further embodiment of the method, the level change representing a logic 1 may occur at a different position within the two sequential clock times then the level change representing a logic 0.

According to a further embodiment of the method, may additionally comprise the steps of: converting light pulses from the LED to electrical pulses with a photo-detector; coupling the electrical pulses from the photo-detector to a data reception device; and converting the electrical pulses from the photo-detector back into the digital information.

According to another embodiment, an integrated circuit device may comprise: a digital processor and memory; a serial interface having an input coupled to the digital processor; a light emitting diode (LED) light intensity control circuit having an input coupled to the digital processor; a modulator having a first input coupled to an output of the serial interface and a second input coupled to an output of the LED light intensity control circuit; and a single node coupled to an output of the modulator.

According to a further embodiment, a LED may be coupled to the single node. According to a further embodiment, a current limiting resistor may be coupled between the LED and the single node.

According to yet another embodiment, a system for driving a light emitting diode (LED) and transmitting digital information using a single node of an integrated circuit device may comprise: an integrated circuit device generating a plurality of pulses from a single node thereof; and a light emitting diode (LED) coupled to the single node of the integrated circuit device; wherein the plurality of pulses from the single node of the integrated circuit device control light intensity from the LED and transmit digital information.

According to a further embodiment, the light intensity from the LED may be substantially proportional to pulse widths of the plurality of pulses. According to a further embodiment, each of the plurality of pulses occurs within two sequential clock times. According to a further embodiment, a level change for each of the plurality of pulses may occur within two sequential clock times. According to a further embodiment, a high to low level change may represent a logic 1 and a low to high level change may represent a logic 0. According to a further embodiment, a low to high level change may represent a logic 1 and a high to low level change may represent a logic 0. According to a further embodiment, the level change representing a logic 1 may occur at a different position within the two sequential clock times then the level change representing a logic 0.

According to a further embodiment, a photo-detector may be used for converting light pulses from the LED to electrical pulses; and a data reception device may be coupled to the photo-detector and adapted for receiving the electrical pulses; wherein the electrical pulses from the photo-detector may be converted back into the digital information by the data reception device.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure may be acquired by referring to the following description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a schematic block diagram of a low pin count integrated circuit device, according to a specific example embodiment of this disclosure;

Figure 2 illustrates schematic waveform timing diagrams to produce various LED light intensity outputs, according to the teachings of this disclosure; and

Figure 3 illustrates schematic waveform timing diagrams for high and low LED light intensity outputs when modulated with digital signals from a UART as shown in Figure 1, according to a specific example embodiment of this disclosure.

While the present disclosure is susceptible to various modifications and alternative forms, specific example embodiments thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific example embodiments is not intended to limit the disclosure to the particular forms disclosed herein, but on the contrary, this disclosure is to cover all modifications and equivalents as defined by the appended claims.

DETAILED DESCRIPTION

A light emitting diode (LED) is driven with a plurality of pulses having controllable pulse widths and positions within clock time periods that provide for both LED light intensity control and digital information communications from a single output node of an integrated circuit (IC) device, *e.g.*, low pin count IC device. Serial information (*e.g.*, data), *e.g.*, from a UART, and light intensity control of the LED are combined together in a light intensity and digital information modulator. The LED light intensity is controlled by the pulse output from the light intensity and digital information modulator. The human eye integrates light pulses from the LED into continuous light intensity levels depending upon the pulse widths thereof.

The digital information contained in the light output from the LED is detected by a photo-detector that converts the light pulses from the LED into electric signals that may be coupled to a demodulator that may be associated with a circuit debugger and/or manufacturing test station. The demodulated data output from the demodulator may be read by a digital processor associated with the circuit debugger and/or manufacturing test station. The aforementioned operations allow continuous visual display and data transmission using only one output node (*e.g.*, pin, ball bump, *etc.*) of the IC device. This is especially advantageous when using low pin count IC devices, *e.g.*, encapsulated in low pin count IC device packages.

Referring now to the drawings, the details of specific example embodiments are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Referring to Figure 1, depicted is a schematic block diagram of a low pin count integrated circuit device, according to a specific example embodiment of this disclosure. A low pin count integrated circuit (IC) device 102 may comprise a digital processor and memory 110, a serial interface 106, *e.g.*, UART, a LED light intensity control circuit 108 and a modulator 104 for combining the outputs from the serial interface 106 and the LED light intensity control circuit 108 in a serial stream of a plurality of pulses that may be applied to a LED 116 in series with a current limiting resistor 114. The output from the modulator 104 is coupled to the LED 116/resistor 114 through a single node 112 associated with the IC device 102.

Light pulses from the LED 116 may be received by a photo-detector 130 that converts these light pulses into electronic pulses that may be coupled to a demodulator 124 associated with a data reception device 122, *e.g.*, circuit debugger, manufacturing test station, *etc.* Light from the LED 116 may also be seen by a human eye 132 that integrates the light pulses therefrom into light intensity levels proportional to the pulse widths of these light pulses. The data reception device 122 may comprise the demodulator 124, a serial interface 126, *e.g.*, UART, and a debugging or test processor 128. The photo-detector 130 may be coupled to the demodulator 124 through node 134 of the data reception device 122.

It is contemplated and within the scope of this disclosure that the node 112 of the IC device 102 may be coupled directly to node 134 of the data reception device 122, wherein the photo-detector 130 is no longer required for data reception by the data reception device 122.

Referring to Figure 2, depicted are schematic waveform timing diagrams to produce various LED light intensity outputs, according to the teachings of this disclosure. The light intensity that appears to a human eye 132 will be substantially proportional to the integration of the pulse widths of the plurality of light pulses from the LED 116. The LED 116 will have a light output when current is flowing through the LED 116 and the integration of these plurality of light pulses is indicated by the cross-hatched areas shown in Figure 2. For example, pulse widths at a 50 percent duty cycle will produce light from the LED 116 at about half maximum brightness. Very high duty cycle pulse widths will produce light from the LED 116 at about a maximum brightness. And very low duty cycle pulse widths will produce light from the LED 116 at about a minimum brightness. The minimum pulse widths may be adjusted to point where the human eye 132 does not substantially perceive a light output from the LED 116, wherein the LED 116 will appear to be off to the human eye 132. Even at very low duty cycle (very small pulse widths) the data embedded in the plurality of light pulses, represented by arrows in the waveform timing diagrams of Figure 2, will be recoverable.

Referring to Figure 3, depicted are schematic waveform timing diagrams for high and low LED light intensity outputs when modulated with digital signals from a UART as shown in Figure 1, according to a specific example embodiment of this disclosure. High and low levels, *e.g.*, high and low voltages or high and low currents, representing data may be generated serially by the serial interface 106. A start pulse(s) may indicate the start of a serial data transmission. The start portion of the serial data transmission may be a plurality of low levels (logic zeros) (only one low level shown). The serial interface 126 may initiate receive data acquisition by locking onto the serial transmission clock rate that may be derived from the start portion of serial data transmission comprising the plurality of low levels (logic zeros).

Once the serial transmission clock rate has been determined and locked onto, each serial data symbol may be decoded to be either a logic "1" (*e.g.*, high level) or a logic "0" (*e.g.*, low level). As shown in Figure 3, a logic "1" symbol may be represented by a high level to a low level transition represented by a downward pointing arrow, and a logic "0" symbol may be represented by a low level to a high level transition represented by a upward pointing arrow. These level transitions may be determined between sequential clock times, represented by Ck1, Ck2, ... , *e.g.*, a level transition occurring between clock times may be decoded into either a logic "1" or a logic "0". For example, symbol decoding between clock times Ck2:Ck3 shows a level transition from a low level to a high level, indicating a data symbol representing a data "1", and between clock times Ck3:Ck4 and Ck:Ck5 shows level transitions from high levels to low levels, indicating data symbols representing two data bits, each having a logic "0" data value. Level transitions at the clock boundaries may be ignored as data symbols by the serial interface 126 but may be used to maintain clock timing synchronization. It is contemplated and within the scope of this disclosure that a data symbol representing "1" may also be a level transition from high to low, and a data symbol representing "0" may also be a level transition from low to high.

The light output from the LED 116 may be controlled by the pulse widths of the logic high pulses thereto. The longer the pulse widths (time durations) of high pulses, the brighter the light output from the LED 116. For a high light output from the LED 116, logic highs would be applied to the LED 116 for substantial portions of the waveform between the clock times. Conversely, for a very low light output (substantially no visual perception of light by a human eye 132) from the LED 116, logic highs would be applied to the LED 116 for substantially insignificant portions of the waveform between the clock times. Light output levels in-between substantially full light output and substantially no light output would be approximately proportional to the pulse widths at the high logic level, *e.g.*, Vdd (power source voltage). The widths of the pulses only affect the light intensity output from the LED 116 since data symbol detection occurs at logic level transitions between clock timing boundaries. The data coding may be, for example but is not limited to, Manchester coding.

While embodiments of this disclosure have been depicted, described, and are defined by reference to example embodiments of the disclosure, such references do not imply a limitation on the disclosure, and no such limitation is to be inferred. The subject matter disclosed is capable of considerable modification, alteration, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent art and having the benefit of this disclosure. The depicted and described embodiments of this disclosure are examples only, and are not exhaustive of the scope of the disclosure.

CLAIMS

What is claimed is:

1. A method for driving a light emitting diode (LED) and transmitting digital information using a single node of an integrated circuit device, said method comprising the steps of:

generating a plurality of pulses from a single node of an integrated circuit device; and

coupling the plurality of pulses from the single node of the integrated circuit device to a light emitting diode (LED);

wherein the plurality of pulses from the single node of the integrated circuit device control light intensity from the LED and transmit digital information.

2. The method according to claim 1, wherein the light intensity from the LED is substantially proportional to pulse widths of the plurality of pulses.

3. The method according to claim 1, wherein each of the plurality of pulses occurs within two sequential clock times.

4. The method according to claim 1, wherein a level change for each of the plurality of pulses occurs within two sequential clock times.

5. The method according to claim 4, wherein a high to low level change represents a logic 1 and a low to high level change represents a logic 0.

6. The method according to claim 4, wherein a low to high level change represents a logic 1 and a high to low level change represents a logic 0.

7. The method according to claim 4, wherein the level change representing a logic 1 occurs at a different position within the two sequential clock times then the level change representing a logic 0.

8. The method according to claim 1, further comprising the steps of:

converting light pulses from the LED to electrical pulses with a photo-detector;

coupling the electrical pulses from the photo-detector to a data reception device; and

converting the electrical pulses from the photo-detector back into the digital information.

9. An integrated circuit device, comprising:

a digital processor and memory;

a serial interface having an input coupled to the digital processor;

a light emitting diode (LED) light intensity control circuit having an input coupled to the digital processor;

a modulator having a first input coupled to an output of the serial interface and a second input coupled to an output of the LED light intensity control circuit; and

a single node coupled to an output of the modulator.

10. The integrated circuit device according to claim 9, further comprising a LED coupled to the single node.

11. The integrated circuit device according to claim 10, further comprising a current limiting resistor coupled between the LED and the single node.

12. A system for driving a light emitting diode (LED) and transmitting digital information using a single node of an integrated circuit device, said system comprising:

an integrated circuit device generating a plurality of pulses from a single node thereof; and

a light emitting diode (LED) coupled to the single node of the integrated circuit device;

wherein the plurality of pulses from the single node of the integrated circuit device control light intensity from the LED and transmit digital information.

13. The system according to claim 12, wherein the light intensity from the LED is substantially proportional to pulse widths of the plurality of pulses.

14. The system according to claim 12, wherein each of the plurality of pulses occurs within two sequential clock times.

15. The system according to claim 12, wherein a level change for each of the plurality of pulses occurs within two sequential clock times.

16. The system according to claim 12, wherein a high to low level change represents a logic 1 and a low to high level change represents a logic 0.

17. The system according to claim 15, wherein a low to high level change represents a logic 1 and a high to low level change represents a logic 0.

18. The system according to claim 15, wherein the level change representing a logic 1 occurs at a different position within the two sequential clock times then the level change representing a logic 0.

19. The system according to claim 12, further comprising:

a photo-detector for converting light pulses from the LED to electrical pulses; and

a data reception device coupled to the photo-detector and adapted for receiving the electrical pulses;

wherein the electrical pulses from the photo-detector are converted back into the digital information by the data reception device.

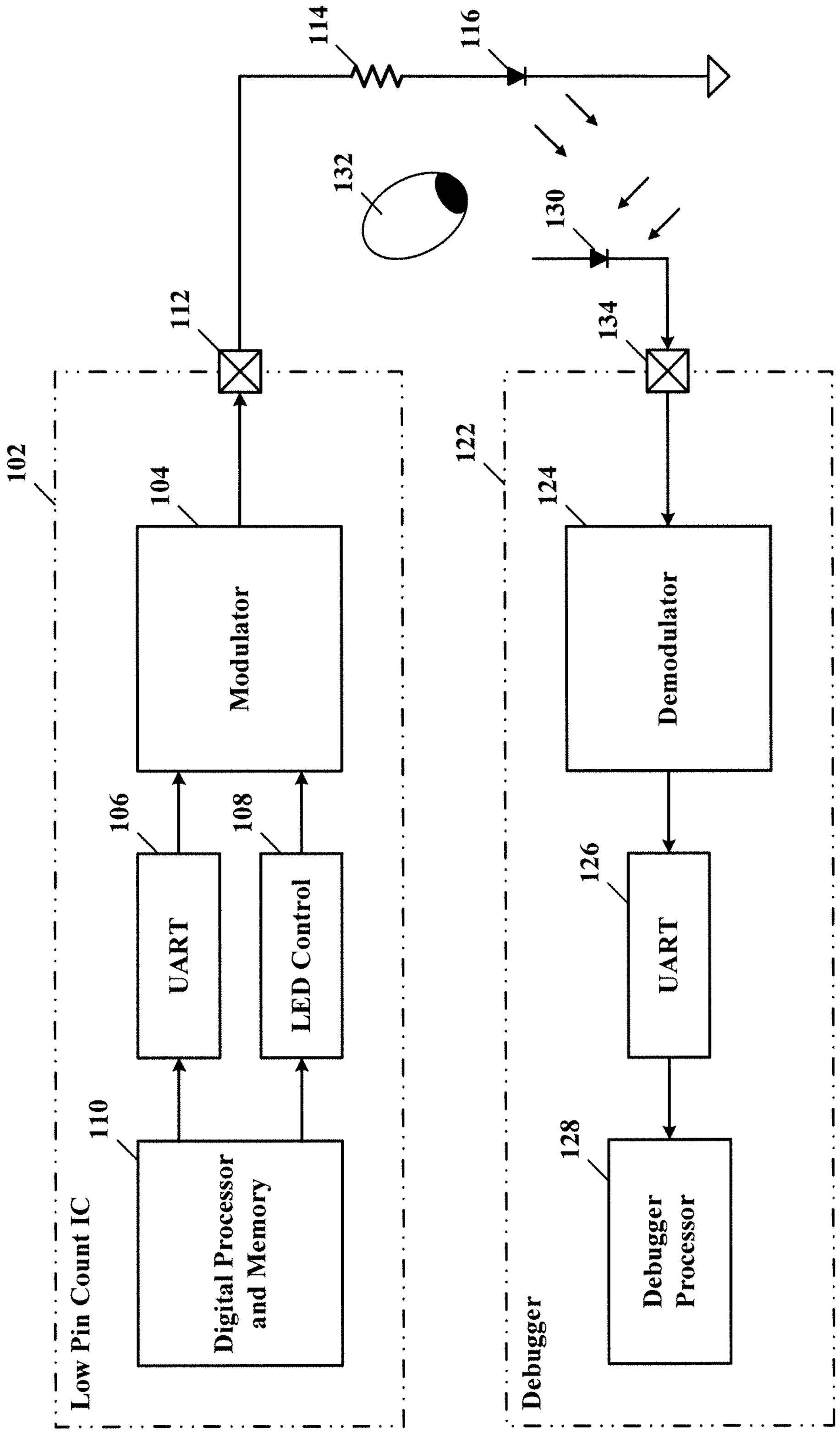
102
Low Pin Count IC
110
Digital Processor and Memory
106
UART
108
LED Control
104
Modulator
112
114
116
132
130
134
122
Debugger
124
Demodulator
126
UART
128
Debugger Processor

Figure 1

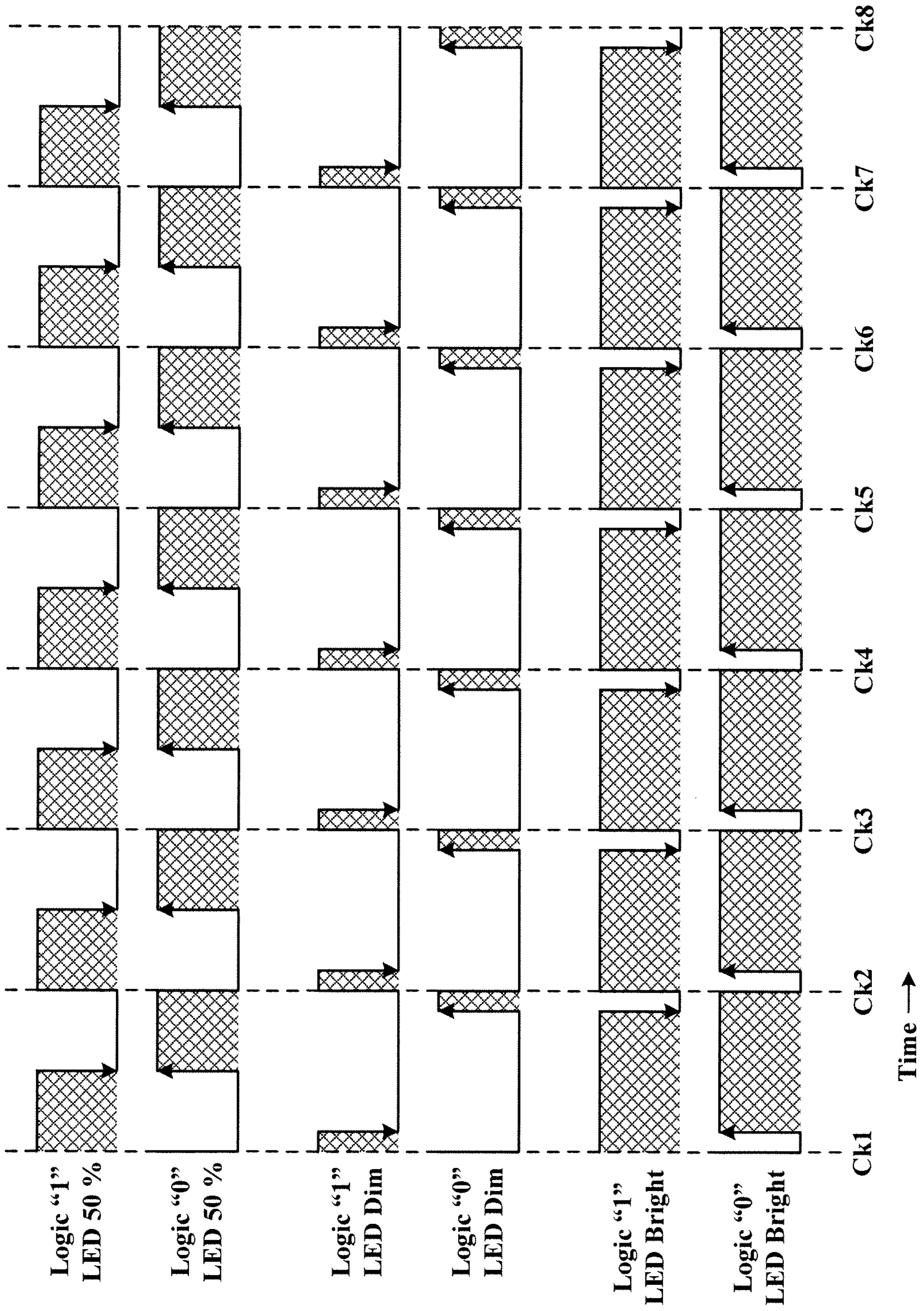
Logic "1" LED 50 %
Logic "0" LED 50 %
Logic "1" LED Dim
Logic "0" LED Dim
Logic "1" LED Bright
Logic "0" LED Bright
Ck1
Ck2
Ck3
Ck4
Ck5
Ck6
Ck7
Ck8
Time

Figure 2

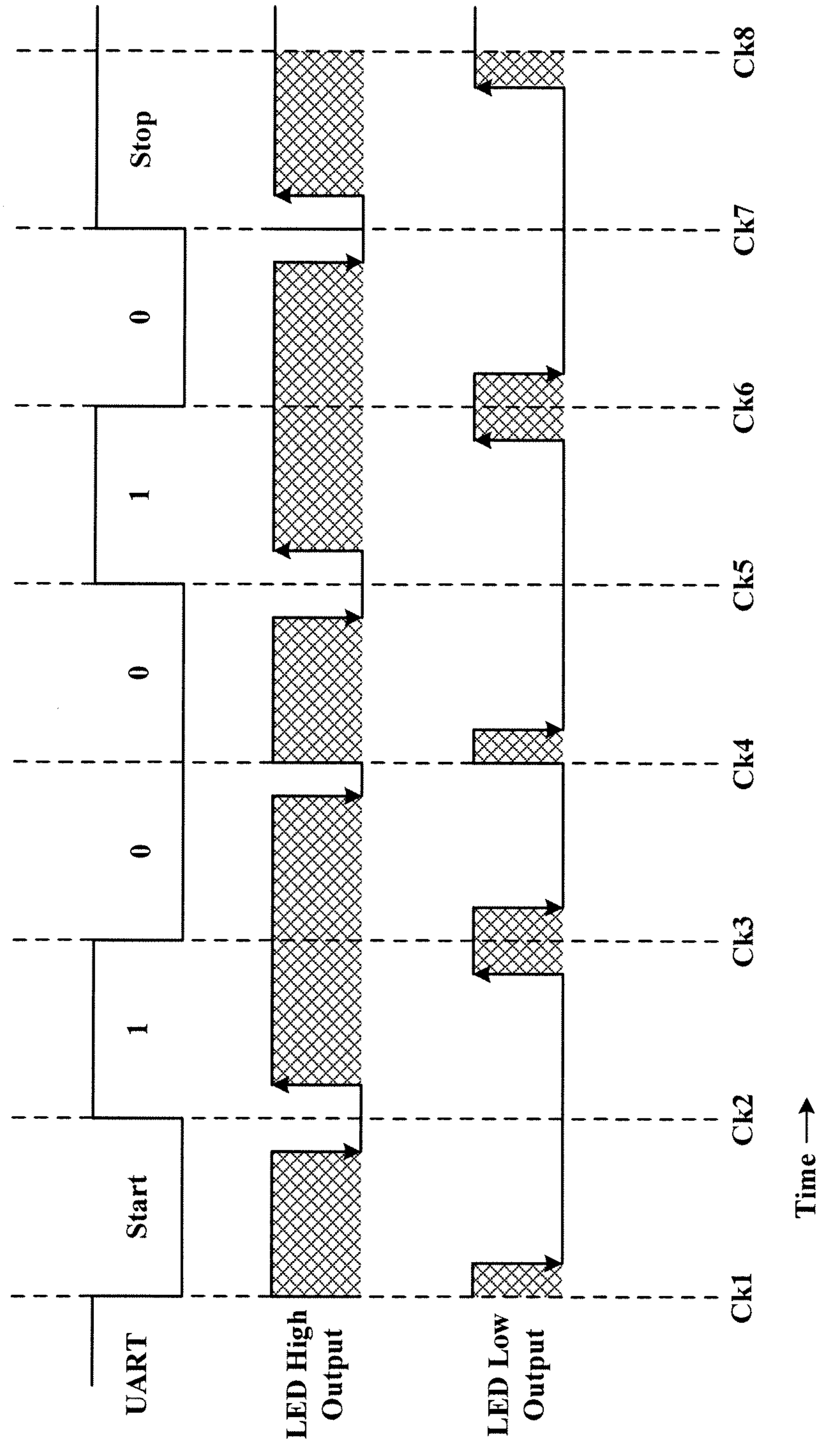
UART
LED High Output
LED Low Output
Start
1
0
0
1
0
Stop
Ck1
Ck2
Ck3
Ck4
Ck5
Ck6
Ck7
Ck8
Time →

Figure 3