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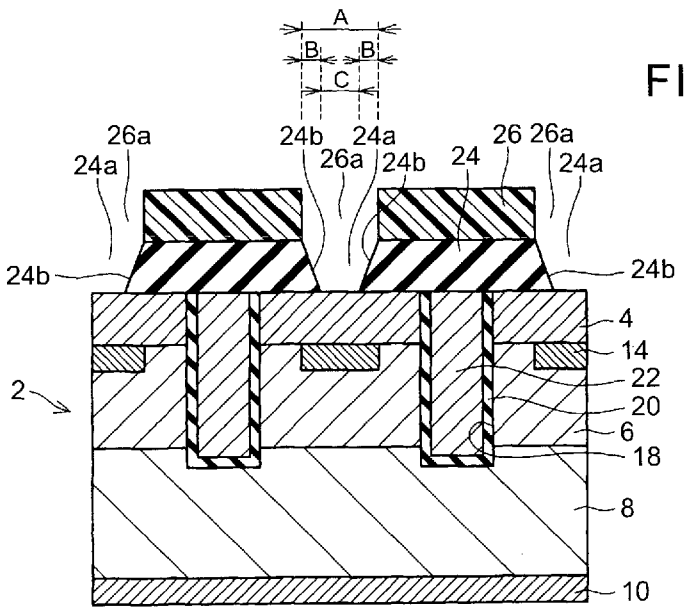
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[Continued on next page]

(54) Title: FORMING METHOD FOR FINE-WIDTH TRENCH AND SEMICONDUCTOR DEVICE

FIG. 8



(57) Abstract: An oxide film (24) is formed on a surface of a semiconductor substrate (2). A resist layer (26) is formed on a surface of the oxide film. The resist layer has an opening (26a). A tapered trench (24a) is formed by forming wall surfaces (24b) of the oxide film by etching a part of the oxide film exposed from the opening. The wall surfaces are inclined with respect to a direction perpendicular to the surface of the semiconductor substrate and reach the surface of the semiconductor substrate. A space between the wall surfaces is narrowed towards the surface of the semiconductor substrate. The semiconductor substrate is etched through the tapered trench. A width of the tapered trench formed on the surface of the semiconductor substrate is smaller than a width of the opening formed in the resist layer.

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FORMING METHOD FOR FINE-WIDTH TRENCH AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The invention relates to a forming method for a fine-width trench and a semiconductor device.

2. Description of Related Art

[0002] When a trench is formed in a surface of a semiconductor substrate, resist is applied on a surface of the semiconductor substrate, and exposure processing and development processing are performed. These processing form a resist layer in which an opening is formed. By etching the semiconductor substrate through the resist layer, a trench is formed in the surface of the semiconductor substrate. A minimum dimension of a width of the opening that is able to be formed in the resist layer is decided depending on a semiconductor manufacturing apparatus. In general, it is not possible to form a trench having a finer width than the minimum dimension that is manageable by the semiconductor manufacturing apparatus.

[0003] Japanese Patent Application Publication No. 2010-62477 (JP 2010-62477 A) discloses a technology for forming a fine-width trench. According to the technology, a fine-width trench is formed as follows. (1) An oxide film is formed on a surface of a semiconductor substrate, and a nitride film is formed on the oxide film. (2) A resist layer, in which a plurality of openings is formed, is formed on the nitride film by using a photolithography method. The plurality of openings corresponds to a plurality of gate electrode trenches, which will be formed in (4) described later. (3) The nitride film and the oxide film is etched through the resist layer in which the plurality of openings is formed. A plurality of openings is formed in the nitride film and the oxide film. The plurality of openings in the nitride film and the oxide film correspond to the gate electrode

trenches that will be formed in (4) described below. (4) Anisotropic etching of the semiconductor substrate is performed through the nitride film and the oxide film in which the plurality of openings is formed. Thus, a plurality of trenches is formed. These trenches are the gate electrode trenches and different from the fine-width trenches described herein. A width of the openings formed in (2) described above is equal to or larger than the minimum dimension manageable by the semiconductor manufacturing apparatus. (5) Thermal treatment is performed to form a thermal oxidation film. Then, a thermal oxidation film is formed on a wall surface of the gate electrode trench. On the wall surface of the gate electrode trench, an interface between the semiconductor substrate and the oxide film is exposed. Oxidation of the semiconductor substrate progresses from the exposed interface along the interface between the semiconductor substrate and the oxide film, and a bird's beak of the thermal oxidation film is formed. As a result, a thermal oxidation film is formed, which extends from the wall surface of the gate electrode trench towards the neighboring gate electrode trench along the surface of the semiconductor substrate. The bird's beak does not extend to an intermediate range between the neighboring gate electrode trenches, and the thermal oxidation film is not formed in the intermediate range between the neighboring gate electrode trenches. The thermal oxidation film becomes a part of an interlayer insulation film that insulates a trench gate electrode and a surface electrode from each other. (6) The semiconductor substrate is etched through the thermal oxidation film. Then, a range between the neighboring thermal oxidation films is etched, thereby forming a trench.

[0004] In the foregoing, where a width of the semiconductor substrate that is present between the neighboring gate electrode trenches is A, an extending distance of the bird's beak formed from the wall surface of the gate electrode trench along the interface between the semiconductor substrate and the thermal oxidation film is B, and a width of a range where the thermal oxidation film is not formed within the intermediate range between the neighboring gate electrode trenches is C, a relation of $C = A - 2 \times B$ holds. According to the above method, it is possible to form a trench with an opening width of C between the neighboring gate electrode trenches.

[0005] In the foregoing method, a dimension managed by a photolithography method is A, which has a minimum dimension because of the limit of the apparatus. According to the above method, it is possible to form a trench with an opening width smaller than the dimension A by a dimension of 2 × B. By setting the dimension A to the minimum dimension manageable on the apparatus side, it is possible to form a trench having an opening width finer than the minimum dimension.

[0006] In the foregoing, a trench with an opening width finer than the minimum dimension manageable on the apparatus side is formed by using the length B of the bird's beak that extends from the wall surface of the gate electrode trench along the interface between the semiconductor substrate and the oxide film. However, it is difficult to control the extending distance B of the bird's beak to a fixed value. When the semiconductor devices having the fine-width trenches by using the foregoing method are mass-produced, opening widths of the fine-width trenches are greatly varied.

SUMMARY OF THE INVENTION

[0007] The invention provides a forming method for a fine-width trench and a semiconductor device, in which variation of an opening width of the fine-width trench is suppressed when the semiconductor device having the fine-width trench is mass-produced.

[0008] A forming method for a fine-width trench according to a first aspect of the invention includes: forming an oxide film on a surface of a semiconductor substrate; forming a resist layer on a surface of the oxide film, the resist layer having an opening; forming a tapered trench by forming wall surfaces of the oxide film by etching a part of the oxide film exposed from the opening; and etching the semiconductor substrate through the tapered trench. The wall surfaces is inclined with respect to a direction perpendicular to the surface of the semiconductor substrate and reaches the surface of the semiconductor substrate. A space between the wall surfaces is narrowed towards the surface of the semiconductor substrate. A width of the tapered trench formed on the surface of the semiconductor substrate is smaller than a width of the opening formed in the resist layer.

[0009] The forming method according to the first aspect of the invention may further include forming wall surfaces of the tapered trench by etching the semiconductor substrate, the wall surfaces of the tapered trench being inclined with respect to the direction perpendicular to the surface of the semiconductor substrate. Furthermore, a space between the wall surfaces of the tapered trench may be narrowed towards a deep portion of the semiconductor substrate.

[0010] The forming method according to the first aspect of the invention may further include forming wall surfaces of the tapered trench by etching the semiconductor substrate, the wall surfaces of the tapered trench being perpendicular to the surface of the semiconductor.

[0011] The forming method according to the first aspect of the invention may further include narrowing a width of the tapered trench formed on the surface of the semiconductor substrate to be smaller than a minimum width of an opening that is formed in the resist layer by using a photolithography method.

[0012] A semiconductor device according to a second aspect of the invention includes a plurality of trench gate electrodes, a source region or an emitter region, a base layer, a contact region, an oxide film and a surface electrode. The source region or the emitter region is positioned between the trench gate electrodes and formed at a position facing a surface of a semiconductor substrate. The base layer is positioned between the trench gate electrodes and formed at a position separated from the surface of the semiconductor substrate by the source region or the emitter region. The contact region is formed in a part of the base layer. The oxide film covers surfaces of the trench gate electrodes and has an opening that is formed between the trench gate electrodes. The surface electrode is in contact with the source region or the emitter region through the opening, and is insulated from the trench gate electrodes by the oxide film. Wall surfaces of the opening of the oxide film formed between the trench gate electrodes are inclined with respect to a direction perpendicular to the surface of the semiconductor substrate. A space between the wall surfaces is narrowed towards the source region or the emitter region. A trench is formed to reach the contact region from the opening of the oxide film

and passes through the source region or the emitter region. The trench is filled with the surface electrode.

[0013] In the second aspect, when the semiconductor device is unipolar, it may be considered that the semiconductor device includes the source region. When the semiconductor device of the second aspect is bipolar, it may be considered that the semiconductor device includes the emitter region. In the semiconductor device of the second aspect, the opening is formed in the oxide film, and the opening is defined by the wall surfaces that are inclined so that the space between the wall surfaces is narrowed towards the source region or the emitter region. Since the trench is formed in the surface of the semiconductor substrate while masking the semiconductor substrate by the above oxide film, it is possible to make the fine trench filled with the surface electrode. In short, according to the semiconductor device of the second aspect, it is possible to achieve a fine opening width of the trench formed in the surface of the semiconductor substrate. For example, it is possible to achieve a finer opening width of the trench than the minimum opening width that is able to be formed in the resist layer by using the photolithography method.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Features, advantages, and technical and industrial significance of exemplary embodiments of the invention will be described below with reference to the accompanying drawings, in which like numerals denote like elements, and wherein:

FIG. 1 shows a first step of a manufacturing process of a semiconductor device according to a first example of the invention;

FIG. 2 shows a second step of the manufacturing process of the semiconductor device according to the first example;

FIG. 3 shows a third step of the manufacturing process of the semiconductor device according to the first example;

FIG. 4 shows a fourth step of the manufacturing process of the semiconductor device according to the first example;

FIG. 5 shows a fifth step of the manufacturing process of the semiconductor device according to the first example;

FIG. 6 shows a sixth step of the manufacturing process of the semiconductor device according to the first example;

FIG. 7 shows a seventh step of the manufacturing process of the semiconductor device according to the first example;

FIG. 8 shows an eighth step of the manufacturing process of the semiconductor device according to the first example;

FIG. 9 shows a ninth step of the manufacturing process of the semiconductor device according to the first example;

FIG. 10 shows a tenth step of the manufacturing process of the semiconductor device according to the first example, and also shows a sectional view of the semiconductor device according to the first example;

FIG. 11 shows a sectional view of a semiconductor device according to a second example of the invention;

FIG. 12 shows a sectional view of a semiconductor device according to a third example of the invention;

FIG. 13 shows a sectional view of a semiconductor device according to a fourth example of the invention;

FIG. 14 shows a sectional view of a semiconductor device in a case where a contact trench is formed without carrying out miniaturizing processing for an opening width according to the examples of the invention; and

FIG. 15 shows a sectional view of a semiconductor device for showing a problem when a manufacturing method in FIG. 14 is used.

DETAILED DESCRIPTION OF EMBODIMENTS

[0015] Listed below are main characteristics of examples explained later. Technical elements described below are independent from each other, and technical utility is obtained by each of or various combinations of the technical elements. (Characteristic

1) A contact trench having a fine width is formed between neighboring trench gate electrodes. (Characteristic 2) A source region and a source electrode are formed on a surface side, and a drain layer and a drain electrode are formed on a back side, thereby structuring a trench gate electrode-type vertical MOS. (Characteristic 3) An emitter region and an emitter electrode are formed on a surface side, and a collector layer and a collector electrode are formed on a back side, thereby structuring a trench gate electrode-type vertical IGBT. (Characteristic 4) A semiconductor substrate is formed of SiC.

[0016] A semiconductor device according to a first example has a structure shown in FIG. 10, and is a MOS in which resistance between a source region 4 and a drain layer 10 is changed by using a trench gate electrode 22. Contact trenches 28 are formed, which pass through the source region 4 and reach contact regions 14. An opening width C of the contact trenches 28 is smaller than a minimum opening width that can be made in a resist layer by using a photolithography method. Therefore, a distance between neighboring trench gate electrodes 22, 22 is reduced compared to a case of a related art.

[0017] A manufacturing method is explained with reference to FIG. 1 to FIG. 10.

[0018] FIG. 1 shows a first step of a manufacturing process for a semiconductor device according to the first example of the invention. In this step, a SiC substrate 2 is prepared, which contains n-type impurity at a concentration suitable for a drift layer 8. FIG. 2 shows a second step of the manufacturing process for the semiconductor device according to the first example. In this step, p-type impurity is implanted deeply from a surface of the substrate 2 to form a base layer 6, n-type impurity is implanted shallowly from the surface of the substrate 2 to form a source layer 4, and n-type impurity is implanted from a back surface of the substrate 2 to form a drain layer 10. The drift layer 8 is at a depth where no impurity is implanted. FIG. 3 shows a third step of the manufacturing process for the semiconductor device according to the first example. In this step, resist is applied on the surface of the substrate 2, and the resist is exposed and then developed by using a mask (not shown), thereby forming a resist layer 12 in which openings 12a are formed. Next, p-type impurity is implanted in a state where the

substrate 2 is masked by the resist layer 12 in which the openings 12a are formed, thereby forming contact regions 14. The base layer 6 has a low impurity concentration in which an inversion layer will be formed at a position that faces the trench gate electrode 22 described later. The base layer 6 does not come into ohmic contact with a source electrode 30 described later. The contact regions 14 have an impurity concentration that comes into ohmic contact with the source electrode 30. After p-type impurity is implanted into the contact regions 14, the resist layer 12 is removed, thermal treatment of the semiconductor substrate is carried out to activate the implanted impurity. At this stage, activation of the impurity is completed, and it is thus no longer necessary to conduct high-temperature thermal treatment thereafter. According to the manufacturing method of this example, it is possible to prevent deterioration of a thermal oxidation film and polysilicon described later due to exposure to thermal treatment.

[0019] FIG. 4 shows a fourth step of the manufacturing process for the semiconductor device according to the first example. In this step, resist is applied on the surface of the substrate 2, and the resist is exposed and then developed by using a mask (not shown), thereby forming a resist layer 16 in which openings 16a are formed. Next, anisotropic etching is carried out on the substrate 2 through the resist layer 16 in which the openings 16a are formed, and gate electrode trenches 18 are formed at the positions of the openings 16a. The gate electrode trenches 18 pass through the source layer 4 and the base layer 6, and reach the drift layer 8. The mask for forming the openings 12a shown in FIG. 3 and a mask for forming the openings 16a shown in FIG. 4 are different from each other. However, as alignment is achieved by using marking for positioning, a positional relation, in which the opening 16a is positioned between the neighboring openings 12a, 12a, is obtained. The gate electrode trench 18 is formed between the neighboring contact regions 14, 14. FIG. 5 shows a fifth step of the manufacturing process for the semiconductor device according to the first example. In this step, the resist layer 16 shown in FIG. 4 is removed, and thermal treatment of the substrate 2 is carried out. Thus, the thermal oxidation film (SiO_2) 20 is formed on the surface of the substrate 2, and wall surfaces and bottom surfaces of the gate electrode trenches 18.

[0020] FIG. 6 shows a sixth step of the manufacturing process for the semiconductor device according to the first example. In this step, polysilicon is deposited on an upper surface of the substrate 2. The polysilicon is also deposited inside the gate electrode trenches 18. The polysilicon is deposited until the polysilicon deposited inside the trenches 18 become higher than the surface of the substrate 2. Next, a surface of the polysilicon is etched, and the thermal oxidation film 20 formed on the surface of the substrate 2 is exposed. Thus, the section shown in FIG. 6 is obtained. An inside of the trenches 18 is filled with the polysilicon 22, the wall surfaces and bottom surfaces of which are covered by the thermal oxidation film 20. The surface of the polysilicon 22 is leveled with the surface of the thermal oxidation film 20. Polysilicon 22 functions as the trench gate electrodes 22.

[0021] FIG. 7 shows a seventh step of the manufacturing process for the semiconductor device according to the first example. In this step, an oxide film (SiO_2) 24 is deposited across surfaces of the thermal oxidation film 20 and the polysilicon 22. The thermal oxidation film 20 becomes a part of the oxide film 24. The oxide film 24 formed at this stage becomes an interlayer insulation film of the completed semiconductor device. The interlayer insulation film is required to have a function of protecting the polysilicon 22 from a shock of bonding a wire to the surface of the semiconductor device, and is thus needed to be formed thick. Next, resist is applied on a surface of the oxide film 24, and the resist is exposed and then developed by using a mask (not shown), thereby forming a resist layer 26 in which openings 26a are formed. The openings 26a are used for forming the contact trenches 28 described later. In order to reduce a size of the semiconductor device by narrowing a space between the neighboring gate electrode trenches 18, 18, narrowing an opening width of the contact trench is advantageous. However, a minimum width of the opening 26a that is able to be formed by a photolithography method is restricted depending on a manufacturing apparatus and so on, and is not able to be 0.8 μm or smaller in the case of this example. A width A of the opening 26a shown in FIG. 7 is 0.8 μm. Nevertheless, in this example, the contact trenches 28 with an opening width of 0.8 μm or smaller are formed in way described below.

[0022] FIG. 8 shows an eighth step of the manufacturing process for the semiconductor device according to the first example. In this step, the oxide film 24 is etched through the resist layer 26 in which the openings 26a are formed. The oxide film 24 exposed in the openings 26a is etched. The etching conducted at this stage is dry etching that is carried out under etching conditions to incline wall surfaces 24b that define trenches 24a formed by the etching. An inclination angle of the wall surfaces 24b is controllable by adjusting pressure of atmospheric gas during the dry etching, ion acceleration voltage used for the etching, or conditions for deposition on wall surfaces, which happens accompanied by etching (for example, deposition easily happens on the wall surfaces when a ratio of a carbon in gas is increased). The wall surfaces 24b are inclined so that a space between the wall surfaces 24b (in other words, a width of the trench 24a) is narrowed towards the substrate 2. As a result, the width of the trench 24a becomes the smallest at the deepest point that is in contact with the substrate 2. The maximum opening width A of the trench 24a is equal to the width of the opening 26a of the resist layer 26, and is adjusted to the minimum width (0.8 μm in the first example) achievable by the photolithography method as stated earlier. On the contrary, a minimum width (a width at a point in contact with the substrate 2) C of the trench 24a is smaller than A because the wall surfaces 24b are inclined. When a width of the inclined wall surface 24b is B, a relation of $C = A - 2 \times B$ holds. As stated below, the oxide film 24 serves as a mask when etching the substrate 2. A width of openings formed in the mask is C stated above. The opening width C is smaller than the minimum width A achievable by the photolithography method, and is not achievable by the photolithography method. In this example, the fine opening width C, which cannot be achieved by the photolithography method, is achieved by making the wall surfaces 24b inclined. The oxide film 24 serves as an interlayer insulation film when then semiconductor device is completed. As stated above, the interlayer insulation film needs to be thick. Since the oxide film 24 is thick, a distance of B explained above becomes long even if the inclination angle of the wall surface 24b is small. It is possible to miniaturize an opening width by the inclined wall surfaces 24b. When the oxide film 24 is thick, it is necessary to make the resist layer 26

thick as the resist layer 26 covers the oxide film 24 in areas except the openings, and protects the oxide film 24 from the etching. The minimum opening width A that can be formed in the thick resist layer 26 tends to be large. Therefore, it is highly necessary to miniaturize the opening width by the inclined wall surfaces 24b.

[0023] FIG. 9 shows a ninth step of the manufacturing process for the semiconductor device according to the first example. In this step, anisotropic etching is carried out on the surface of the semiconductor substrate 2 through the oxide film 24 in which the openings 24a are formed. As a result, the trenches 28 are formed in the surface of the semiconductor substrate 2. Etching is carried out until the trenches 28 pass through the source layer 4 and reach the contact regions 14. Trenches formed in the substrate 2 at this stage are referred to as the contact trenches 28. The opening width of the contact trenches 28 on the surface of the substrate 2 is C, and is finer than the minimum opening width achievable by the photolithography method. In this example, the contact trenches 28 are formed by performing etching under etching conditions by which wall surfaces perpendicular to the surface of the substrate 2 are obtained. As stated later, etching conditions to incline wall surfaces that define the contact trenches may be used. In any case, the opening width C of the contact trenches 28 on the surface of the substrate 2 is miniaturized. Therefore, a distance between the trench gate electrodes 22, 22 is reduced, thereby reducing a size of the semiconductor device. As evident from FIG. 7 and FIG. 8, a residual range of the oxide film 24 is restricted by the resist layer 26, and forming ranges of the contact trenches 28 are restricted by the openings 24a of the oxide film 24. In short, the residual range of the oxide film 24 and the forming positions of the contact trenches 28 are restricted by the same resist layer 26. The residual range of oxide film 24 and existence positions of the contact trenches 28 are self-aligned, and the positional relation between the residual range of oxide film 24 and the existence positions of the contact trenches 28 is maintained fixed accurately.

[0024] FIG. 10 shows a tenth step of the manufacturing process for the semiconductor device according to the first example, and also shows a sectional view of the semiconductor device according to the first example. In this step, the electrode 30 is

deposited on the surface side of the substrate 2, and an electrode 32 is deposited on a back side of the substrate 2. Thus, a vertical MOS using the trench gate electrodes 22 is obtained. The surface electrode 30 becomes a source electrode and the back electrode 32 becomes a drain electrode. Since the contact trenches 28 are formed, the source region 4 is in direct contact with the source electrode 30, and the base layer 6 is in contact with the source electrode 30 through the contact regions 14.

[0025] FIG. 14 and FIG. 15 show sectional view of a semiconductor device in a case where contact trenches are formed without performing the miniaturizing processing for an opening width according to the first example of the invention. In short, FIG. 14 and FIG. 15 show a case where the a resist layer 70, in which openings 70a for forming contact trenches are formed, is formed directly on a surface of a substrate 2 (a case where the oxide film 24 shown in FIG. 7 is not used). In this case, an opening width of the contact trench 78 is not miniaturized. When widths of the openings 12a (openings that decide forming ranges of the contact regions 14) shown in FIG. 3 and the openings 70a (openings that decide forming ranges of contact trenches 78) shown in FIG. 14 are both a minimum dimension, regions are formed in which a surface electrode (30 in FIG. 10) comes into direct contact with the base layer 6 without the contact regions 14, because of misalignment between the openings 12a and the openings 70a. When no potential is applied to trench gate electrodes 22 and a MOS is off, a depletion layer expands upwardly and downwardly from a pn interface of the base layer 6 and the drift layer 8. Breakdown voltage of the MOS is ensured by the depletion layer. In the case where there are regions where the surface electrode 30 is in direct contact with the base layer 6 without the contact regions 14, when the depletion layer expanded in the base layer 6 reaches the surface electrode 30, the depletion layer no longer expands. Therefore, necessary breakdown voltage may not be ensured. Meanwhile, when the miniaturizing processing shown in FIG. 8 to FIG. 10 is employed, it is possible to form the contact trenches 28 within the forming ranges of the contact regions 14, and the regions where the surface electrode 30 is in direct contact with the base layer 6 without the contact regions 14 are not formed.

Therefore, it is possible to expand the depletion layer in a wide range of the base layer 6 and necessary breakdown voltage is ensured easily.

[0026] (Second example) In a second example, as shown in FIG. 11, a substrate 2 is etched under conditions by which wall surfaces 38a that define contact trenches 38 are inclined, thereby forming the contact trenches 38. According to the second example, forming ranges of contact regions 14 are miniaturized. Therefore, it is possible to reduce a size of a semiconductor device further. In the case of FIG. 11, when a manufacturing method is used, in which impurity is implanted into a base layer 6 by using the contact trenches 38 to form the contact regions 14, it is impossible to sufficiently reduce resistance between the surface electrode 30 and the contact region 14. In this example, a manufacturing method is used, in which the contact regions 14 are formed in advance and the contact trenches 38 that reach the contact regions 14 are formed. Therefore, it is possible to sufficiently reduce resistance between the surface electrode 30 and the contact region 14. Normally, in the case where the contact regions 14 are formed first and etching is carried out thereafter, impurity implanted into the contact regions 14 is dispersed by thermal treatment conducted after the contact regions 14 are formed, and formation ranges of the contact regions 14 are thus expanded. When the contact regions 14 come close to gate electrode trenches 18, threshold voltage of a MOS becomes unstable. Therefore, in this embodiment, SiC is used for the semiconductor substrate 2, and Al is implanted to obtain the contact regions 14. In this case, Al implanted into the contact regions 14 is not dispersed thereafter, and the formation ranges of the contact regions 14 are not expanded. Hence, it is possible to prevent fluctuation of threshold voltage of a MOS. A width F2 of the base layer 6 and the contact region 14, which separate the source electrode 30 and the trench gate electrode 22 from each other, affects breakdown voltage of a MOS. Compared to a width F1 shown in FIG. 10, it is obvious that $F1 < F2$. In short, breakdown voltage of the second example shown in FIG. 11 is higher than breakdown voltage of the first example shown in FIG. 10. In the first example, in order to ensure the same breakdown voltage as the second example, the distance F1 shown in FIG. 10 has to be increased to F2, and it is required to increase a space between the

neighboring trench gate electrodes. For the same breakdown voltage, the space between the neighboring trench gate electrodes is miniaturized more in the second example than the first example. With a semiconductor device according to the second example, a space between the trench gate electrodes is miniaturized. Therefore, it is possible to mass-produce a MOS in which contact resistance between a surface electrode and the contact region is low and fluctuation range of threshold voltage is small.

[0027] (Third example) As shown in FIG. 12, contact trenches 58 may be formed under conditions by which both horizontal bottom surface 58b and inclined wall surfaces 58a are formed. Even if there is the bottom surface 58b, advantages explained in the second example are obtained as long as a relation is maintained, in which a contact area between the pair of inclined wall surfaces 58a and a contact region 14 is larger than a contact area between the bottom surface 58b the contact region 14.

[0028] (Fourth example) As shown in FIG. 13, with a technology of forming inclined wall surfaces 24b in an oxide film 24, it is possible to obtain a relation in which a width E of an upper surface 24c of the oxide film 24 is smaller than a width D of a trench 18. In this case, it is possible to reduce a size of a semiconductor device even more.

[0029] Although the examples of the technology disclosed herein have been explained in detail, these examples are for illustrative purposes only. The invention includes various modifications and changes made in the specific examples illustrated above. For example, a p-type collector layer may be used instead of the n-type drain layer 10. In such a case, the source layer 4 becomes an emitter layer, and an IGBT is formed. In the case of an IGBT, an n-type buffer layer may be placed between the n-type drift layer 8 and the p-type collector layer 10. Also, the impurity implantation process for forming the contact regions 14 shown in FIG. 3 may not be carried out between FIG. 2 and FIG. 4, and the process may proceed to the step shown in FIG. 7 without forming the contact regions 14. In this case, impurity is implanted in the contact regions 14 by using the openings 26a. Thereafter, the processing of FIG. 8 and after is carried out to form the contact trenches 28. With this manufacturing method, positions of the contact regions 14 and the contact trenches 28 are restricted by the same openings 26a, and it is possible to

mass-produce a semiconductor device with a stable positional relationship between the contact regions 14 and the contact trenches 28.

CLAIMS:

1. A forming method for a fine-width trench, comprising:

forming an oxide film on a surface of a semiconductor substrate;

forming a resist layer on a surface of the oxide film, the resist layer having an opening;

forming a tapered trench by forming wall surfaces of the oxide film by etching a part of the oxide film exposed from the opening, the wall surfaces being inclined with respect to a direction perpendicular to the surface of the semiconductor substrate and reaching the surface of the semiconductor substrate, and a space between the wall surfaces being narrowed towards the surface of the semiconductor substrate; and

etching the semiconductor substrate through the tapered trench, wherein

a width of the tapered trench formed on the surface of the semiconductor substrate is smaller than a width of the opening formed in the resist layer.

2. The forming method for the fine-width trench according to claim 1, further comprising

forming wall surfaces of the tapered trench by etching the semiconductor substrate, the wall surfaces of the tapered trench being inclined with respect to the direction perpendicular to the surface of the semiconductor substrate, wherein

a space between the wall surfaces of the tapered trench is narrowed towards a deep portion of the semiconductor substrate.

3. The forming method for the fine-width trench according to claim 1, further comprising

forming wall surfaces of the tapered trench by etching the semiconductor substrate, the wall surfaces of the tapered trench being perpendicular to the surface of the semiconductor.

4. The forming method for the fine-width trench according to claims 1 to 3, further comprising

narrowing a width of the tapered trench formed on the surface of the semiconductor substrate to be smaller than a minimum width of an opening that is formed in the resist layer by using a photolithography method.

5. A semiconductor device comprising:

a plurality of trench gate electrodes;

a source region or an emitter region that is positioned between the trench gate electrodes and formed at a position facing a surface of a semiconductor substrate;

a base layer that is positioned between the trench gate electrodes and formed at a position separated from the surface of the semiconductor substrate by the source region or the emitter region;

a contact region formed in a part of the base layer;

an oxide film that covers surfaces of the trench gate electrodes and has an opening that is formed between the trench gate electrodes; and

a surface electrode that is in contact with the source region or the emitter region through the opening, and is insulated from the trench gate electrodes by the oxide film, wherein

wall surfaces of the opening of the oxide film formed between the trench gate electrodes are inclined with respect to a direction perpendicular to the surface of the semiconductor substrate,

a space between the wall surfaces is narrowed towards the source region or the emitter region,

a trench is formed to reach the contact region from the opening of the oxide film and passes through the source region or the emitter region, and

the trench is filled with the surface electrode.

FIG. 1

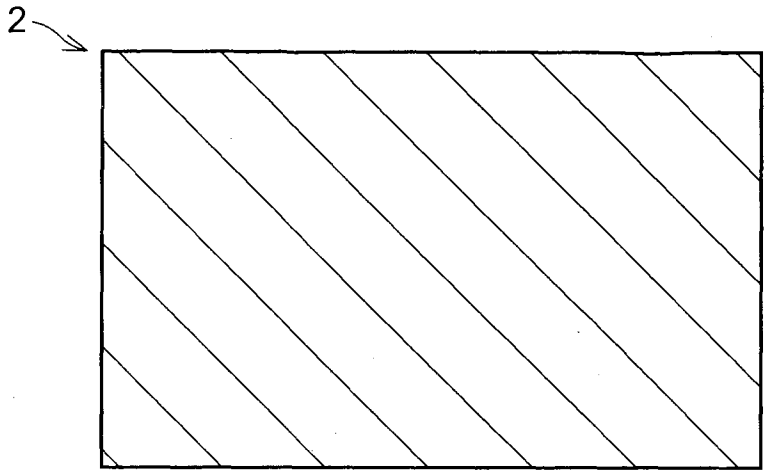


FIG. 2

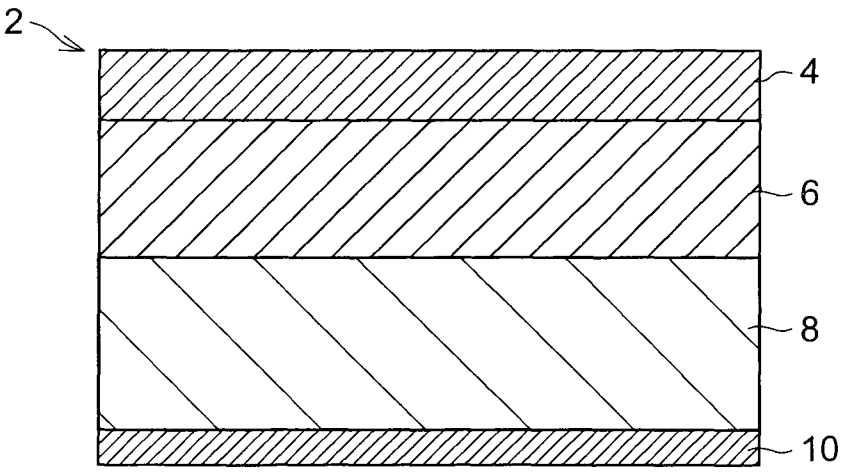


FIG. 3

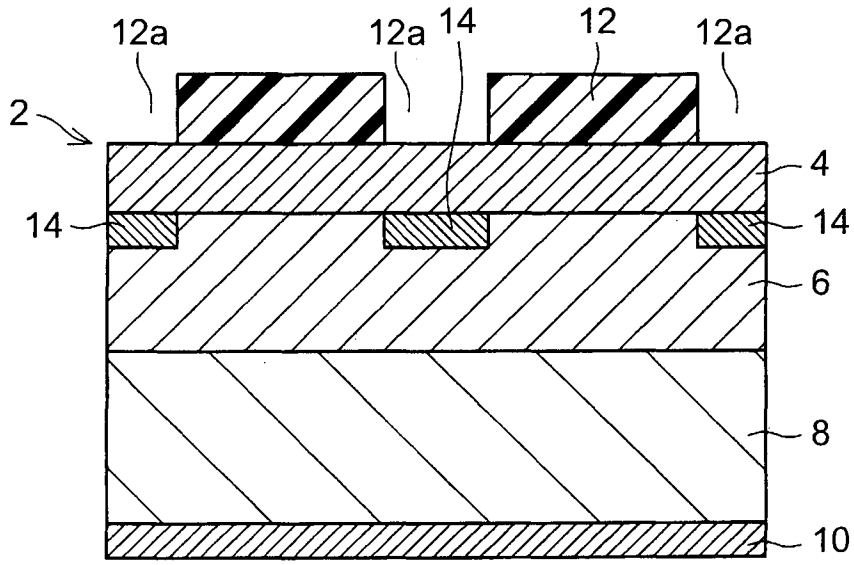


FIG. 4

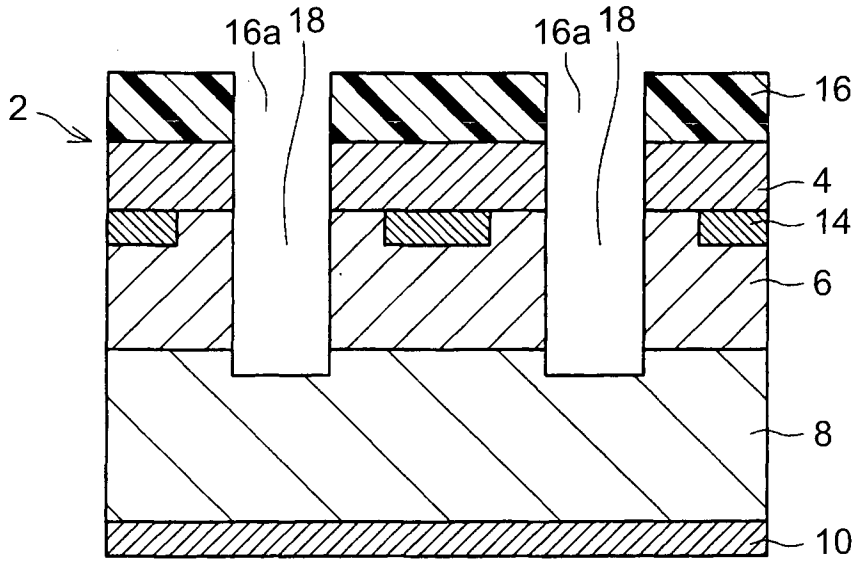


FIG. 5

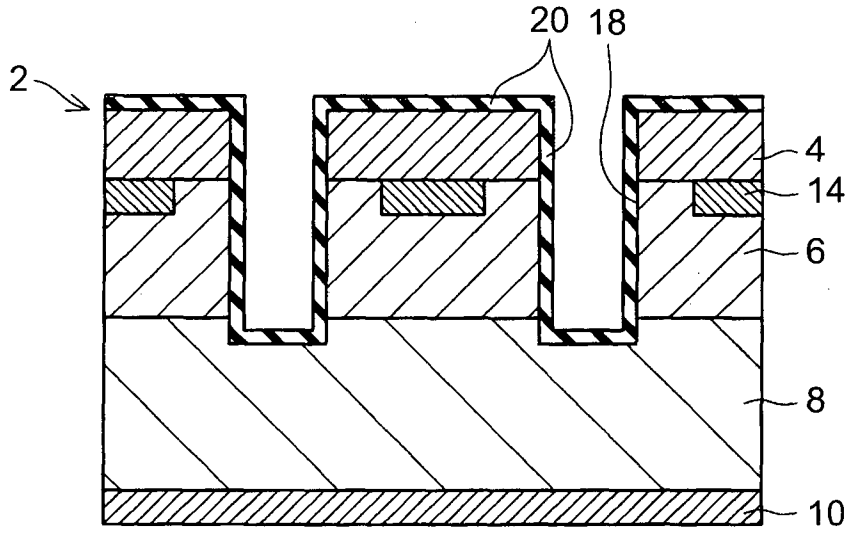


FIG. 6

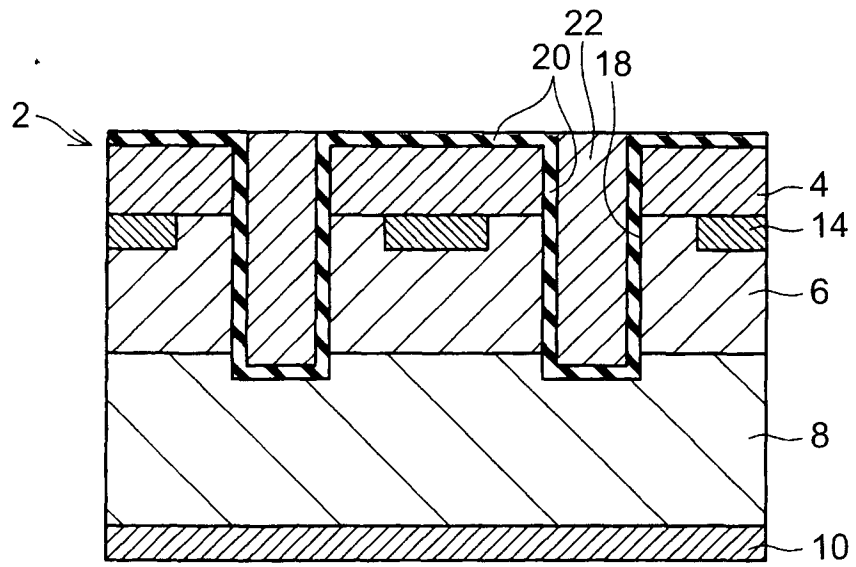


FIG. 7

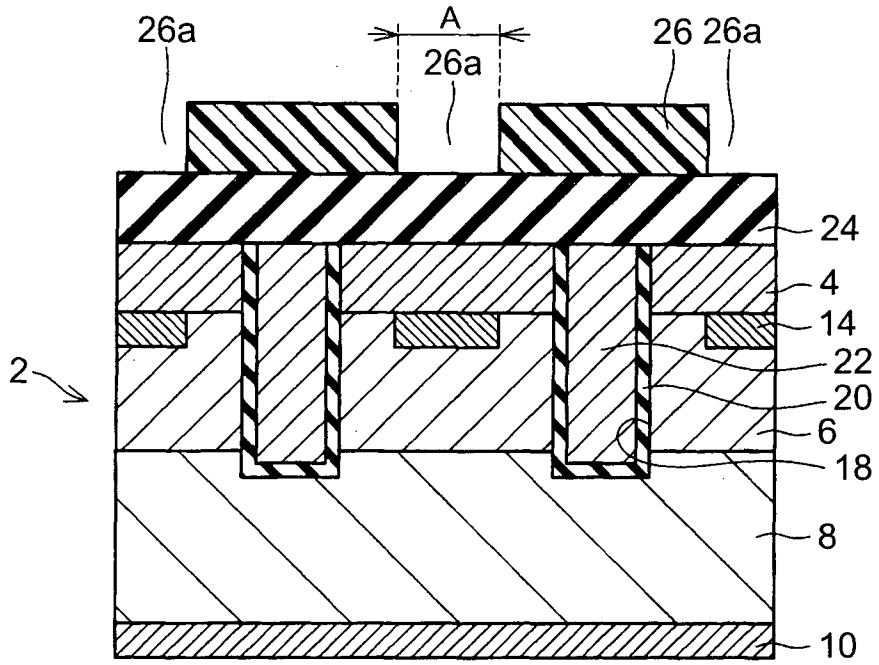

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FIG. 8

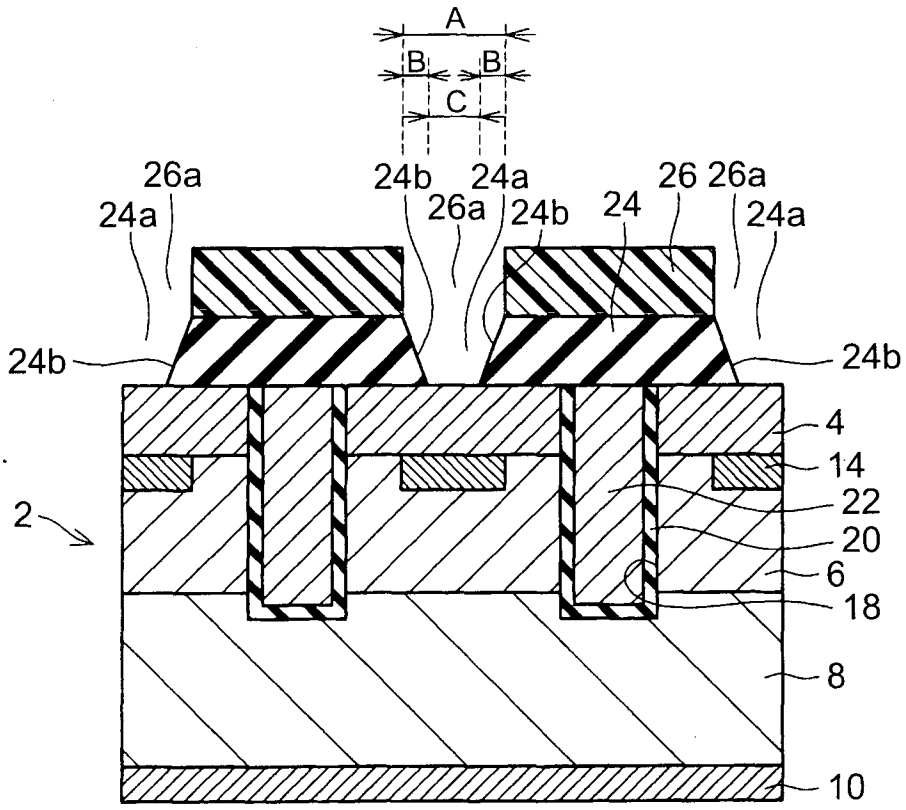

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FIG. 9

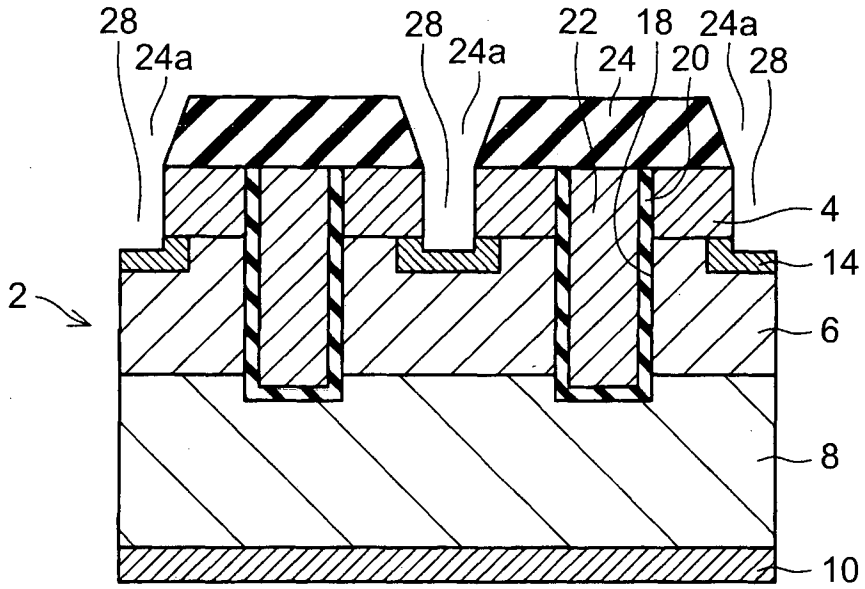

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FIG. 10

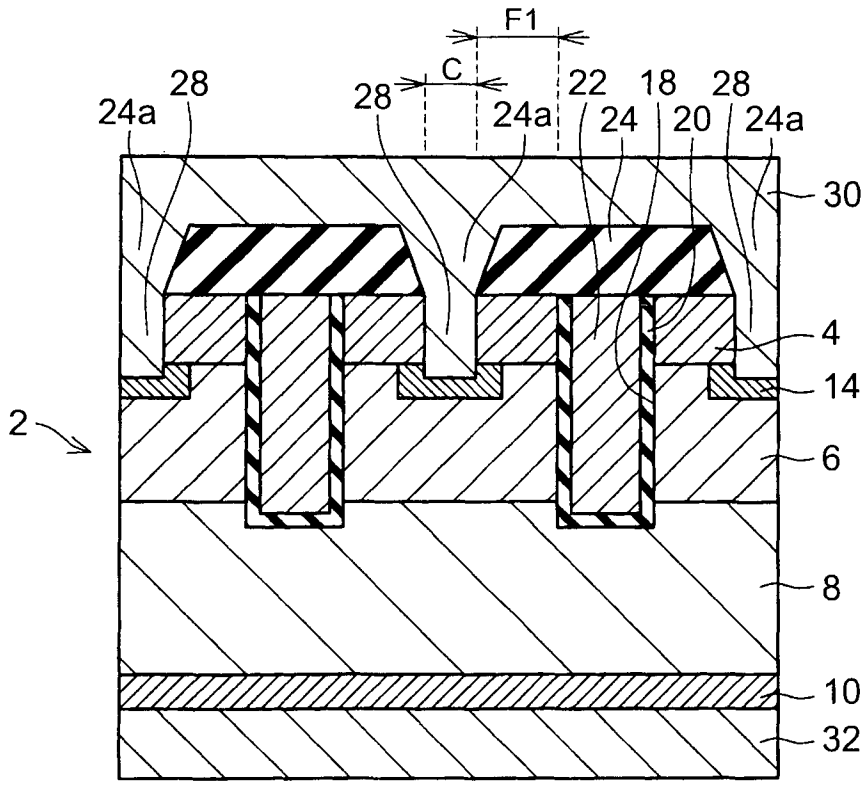

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FIG. 11

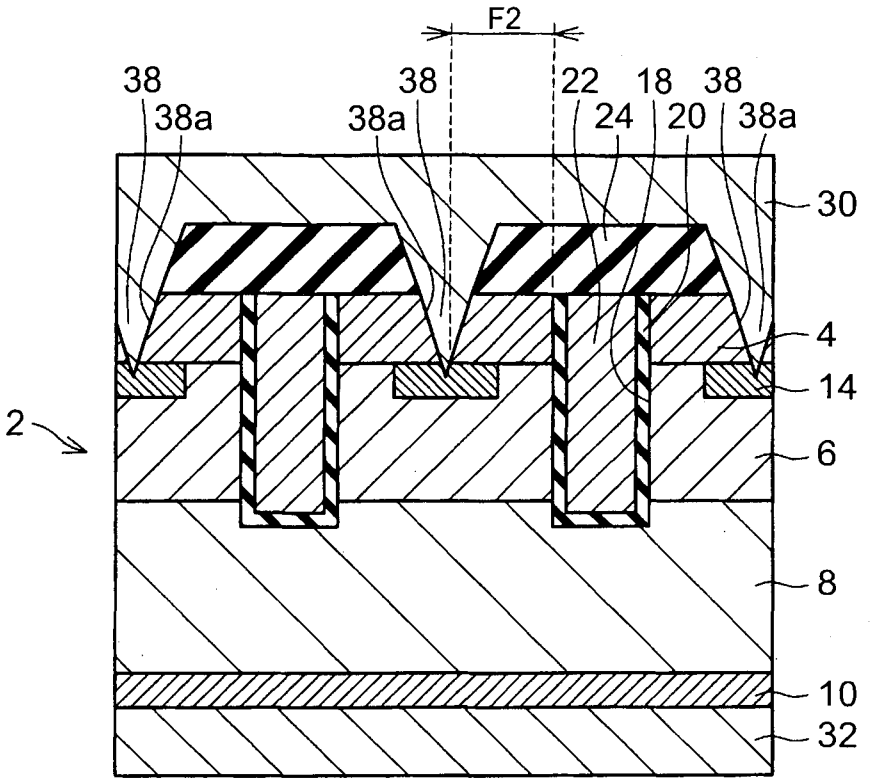

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FIG. 12

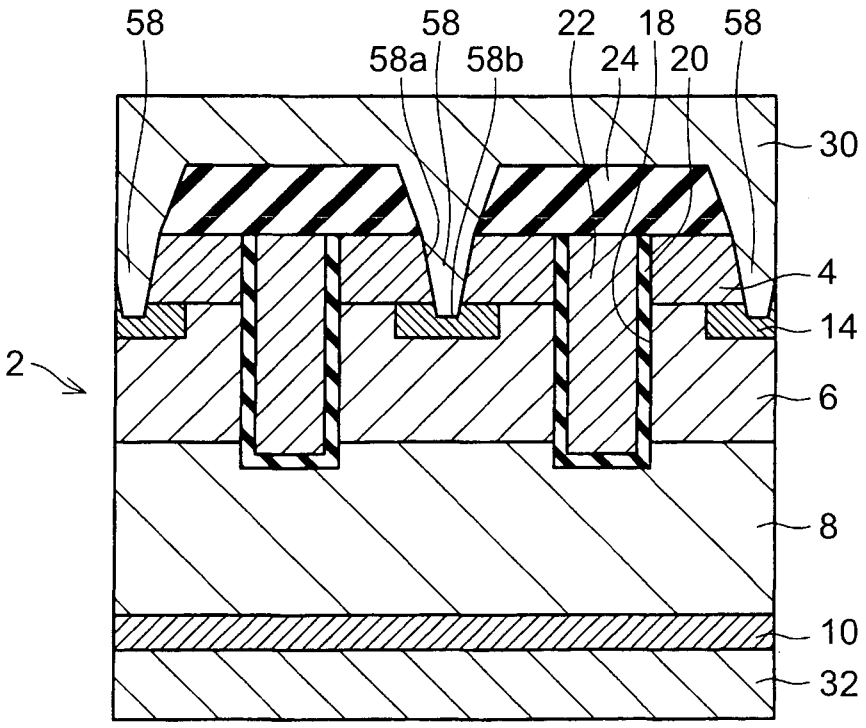

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FIG. 13

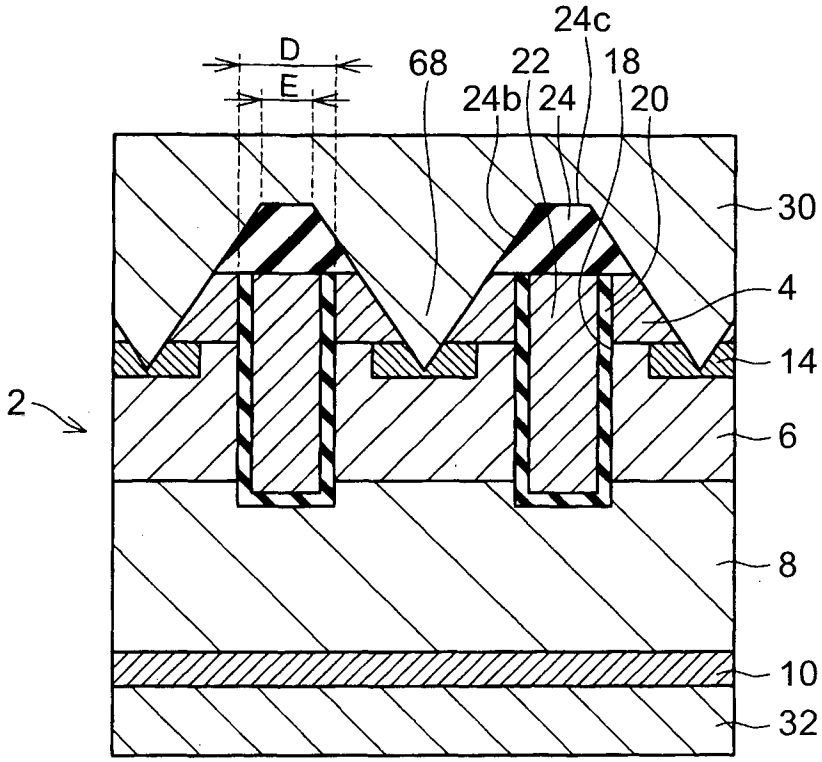

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FIG. 14

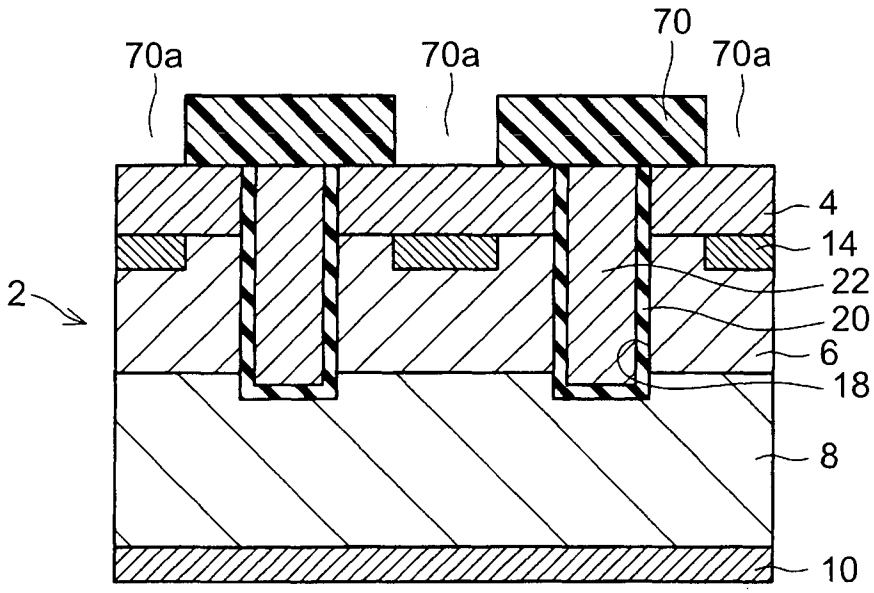
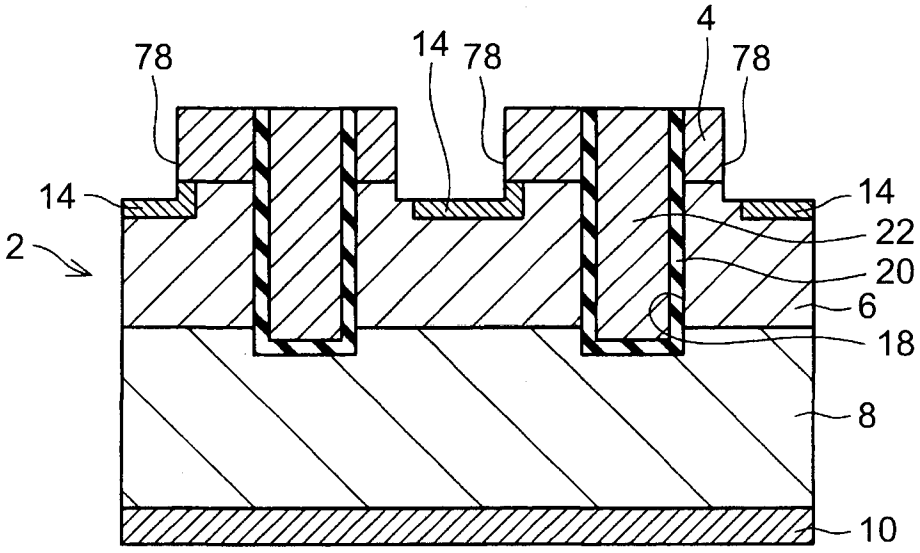

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FIG. 15



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2014/001911

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/308 H01L29/66
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 579 801 B1 (DAKSHINA-MURTHY SRIKANTESWARA [US] ET AL) 17 June 2003 (2003-06-17) column 5, line 25 - column 7, line 14; figures	1,2 4,5
X	US 5 858 824 A (SAITOH YOSHIHARU [JP]) 12 January 1999 (1999-01-12) column 5, line 55 - line 59; figures 1B-1D	1,3
X	US 2013/214391 A1 (CHOI SAMUEL S [US] ET AL) 22 August 2013 (2013-08-22) paragraphs [0035], [0046], [0053], [0054]; figures	1-4
X	US 2013/001684 A1 (HSIEH FU-YUAN [TW]) 3 January 2013 (2013-01-03) figure 4	5
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 January 2015	20/01/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gori, Patrice

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2014/001911

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 2008/150018 A1 (TANABE ATSUSHI [JP]) 26 June 2008 (2008-06-26) figures -----	5

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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