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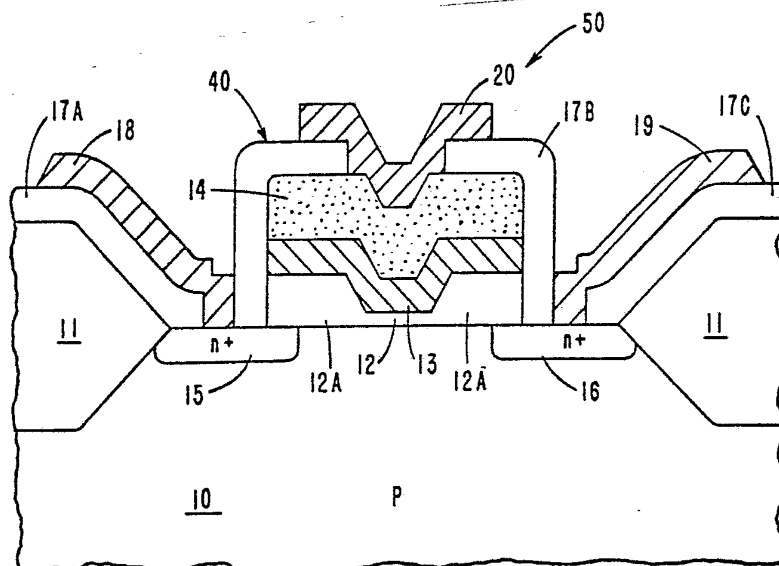

(57) Abstract

A non-volatile semiconductor memory device includes a semiconductor substrate (10) a layer of silicon dioxide (12) provided on the semiconductor substrate (10), a layer of silicon oxynitride (13) provided on the silicon dioxide layer (12) and a conductive gate electrode (14) provided on the silicon oxynitride layer (13). The non-volatile memory device may be a capacitor or, where source and drain regions (15, 16) are provided, a transistor. The silicon dioxide layer (12) may have portions (12A) of increased thickness adjacent the source and drain regions (15, 16). The device has a high charge retention capability.

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NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

Technical Field

This invention relates to non-volatile semiconductor memory devices of the kind including a
5 semiconductor substrate, a first insulator layer formed by a silicon dioxide layer provided on said substrate, a second insulator layer provided on said first insulator layer and a conductive gate electrode provided on said second insulator layer.

10 ## Background Art

Metal gate/silicon gate-insulator-semiconductor devices of the MNOS/SNOS type and their non-volatile charge retention are well-known. Briefly, when a large positive voltage is applied between the gate and the
15 silicon substrate of a MNOS (hereafter MNOS includes SNOS) device, as is done during a write operation, electrons will tunnel through the thin (10-50 Angstroms thickness) oxide layer and are stored in deep traps at the oxide-nitride interfact or in the nitride bulk under
20 the influence of a high electric field of the order of 10^7 volts per cm. Tunneling of electrons through oxide layers of thickness less than about 20 Angstroms is by direct tunneling and through oxide layers of thickness exceeding about 20 Angstroms is by Fowler-Nordheim
25 tunneling. As a result of this trapping of electrons in the gate dielectric the conductivity of the underlying semiconductor changes. If the semiconductor is of n-type material, the trapping of electrons may invert the semiconductor into p-type material. Once the electrons
30 are trapped in the gate dielectric, they remain there for a period of time even after removal of the voltage because the dielectric is non-conductive. This retention is known as non-volatile charge retention or "memory".

The electrons stored in the nitride gate dielectric eventually decay in a logarithmic fashion through two possible mechansisms: (1) back tunneling into the silicon substrate; (2) conduction through the nitride itself. Which of these is the dominant charge transfer mechanism depends on such parameters as (1) memory oxide thickness; (2) density of interface-states created by the lattice mismatch of the two dielectrics and; (3) energy and spatial distribution of traps in the nitride.

The memory device written in the above manner may be erased by applying a sufficiently large negative voltage to the transistor's gate with respect to the substrate to cause the electrons trapped in the nitride to return to the substrate and to replace them by trapped positive charges.

Improving charge retention and therefore, reliability, of non-volatile MNOS memory devices is always a goal in microelectronics technology, particularly in view of the ever-increasing use of these devices in microprocessors and minicomputers and other applications where storage of information for long periods of time is crucial.

As used herein, the term "retention" means the capability of the memory device to retain usable data for a period of time. "Endurance" means the capability of the device to endure erase/write cycling and still provide adequate retention.

One way of improving charge retention in these devices is to make the oxide layer relatively thick. However, a relatively thick memory oxide necessitates rather high voltages to write or erase the device, decreases the device erasure speed and reduces the size of the memory window.

A memory device of the kind specified is known from the article by P C Y Chen "Threshold-Alterable

Si-Gate MOS Devices" in IEEE Transactions on Electron Devices, Vol. ED-24, No. 5, May 1977, pages 584-586. Thus, the Chen article discloses a memory device having a polysilicon-nitride-oxide-silicon structure. This device has the disadvantage of a limited retention capability. The Chen article also discloses a structure wherein undesirable charge injection from the silicon gate electrode is prevented by providing a silicon oxynitride layer between the nitride and the polysilicon gate. This latter structure has the disadvantage that complex processing steps are required for its manufacture.

Disclosure of the Invention

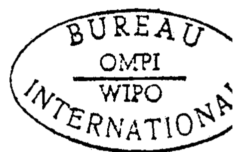
It is an object of the present invention to provide a non-volatile semiconductor memory device of the kind specified having a high degree of retention and which is simple to manufacture.

Therefore, according to the present invention, there is provided a non-volatile semiconductor memory device of the kind specified, characterized in that said second insulator layer is formed by a silicon oxynitride layer.

It is found that a memory device according to the invention has a high degree of charge retention as compared with a polysilicon-nitride-oxide-silicon structure device. Furthermore since only two insulator layers are provided, it will be appreciated that a device according to the invention is simple to manufacture because only a small number of process steps are required. The latter advantage leads to improved yields in manufacture and hence to a saving in manufacturing costs.

Brief Description of the Drawings

One embodiment of the present invention will now be described by way of example with reference to the



The single Figure, Fig. 1, is a cross-sectional representation of an embodiment of the non-volatile memory device according to the present invention.

Best Mode for Carrying Out the Invention

5 Referring now to Fig. 1, there is shown in this Figure a partial sectional view of a portion of an exemplary memory device 50 embodying the principles of the present invention. Fig. 1 in particular illustrates a trigate n-channel field effect transistor 50 having a 10 silicon gate-oxynitride-oxide-silicon or SO_nOS (where O_n designates oxynitride) gate structure 40. The device 50 of Fig. 1 comprises a single crystal silicon substrate 10 of one conductivity type, illustratively, p-type. The substrate 10 is partitioned into the device 15 active area by regions 11-11 of thick field oxide. The n-channel FET 50 includes a pair of n-type surface adjacent source and drain impurity regions 15 and 16, respectively, which are self-aligned with the overlying gate structure 40 and which define a channel region in 20 the substrate 10 lying between the source and drain regions 15, 16. The source and drain may be formed by any of the well-known techniques such as by selective diffusion of impurities through an oxide mask or by ion implantation.

25 The exemplary gate structure 40 consists of a central memory portion 12 having a thin (20-35 Angstroms thickness) memory oxide and flanked by two non-memory portions having thick (1,000-2,000 Angstroms thickness) non-memory oxide regions 12A-12A. Overlying these 30 memory and non-memory oxide regions is a uniform thickness (200-500 Angstroms thickness) silicon oxynitride gate insulator 13. The oxynitride 13 in turn is covered by a polycrystalline silicon electrode 14 of thickness (3,000-5,000) Angstroms. The memory oxide 12 and the 35 oxynitride 13 may be formed continuously in the same furnace deposition tube at the same temperature.

In this technique, the oxide 12 is formed by chemical vapor deposition at atmospheric pressure or by steam oxidation of the substrate 10 at a temperature of about 750°C. The oxynitride 13 is formed, immediately thereafter, by LPCVD (low pressure chemical vapor deposition) using reactant gases ammonia (NH_3), nitrous oxide (N_2O) and dichlorosilane (SiH_2Cl_2) in the proportion NH_3:N_2O:SiH_2Cl_2 of 3.5:2:1 at the same temperature as the oxide 12. The polysilicon gate electrode 14 is formed by LPCVD using silane.

The ranges of the oxide 12 and oxynitride 13 thicknesses provided above are nominal and are not limiting but are those considered convenient from the point of view of fabrication as well as with respect to convenient values of voltages with which the device may be operated. For example, for ± 15 volt write/erase operation, the oxide 12 and oxynitride 13 may be selected to have thicknesses of about 25 Angstroms and about 275 Angstroms, respectively. For ± 25 volt write/erase operation, a thicker oxynitride, of about 400 Angstroms thickness and an oxide 12 of about the same thickness as in the previous example may be used. It will be appreciated that a SO_nOS device having a very thick (i.e. greater than about 500 Angstroms thickness) oxynitride 13 not only requires significantly higher programming voltages, of the order of about ± (30-40) volts but also takes a longer time for fabricating the same, both of which features are disadvantageous from the present perspective of the microelectronics industry.

The gate electrode 14 may be of any known highly conductive material, for example, a metal such as aluminum, or alloys such as aluminum-1% silicon, or a refractory metal silicide such as tungsten disilicide or tantalum disilicide or molybdenum silicide. When the gate electrode 14 is made from a nonconductive material,

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it is doped with n-type impurities to provide a highly conductive gate electrode for the memory device.

The memory device 50 is provided with a thick insulating layer 17A-17B-17C made of, for example, phosphosilicate glass, which is appropriately patterned to cover the transistor structure. Insulating layer 17B electrically isolates the gate electrode 14 from the metal conductors 18 and 19. Metal conductors 18 and 19 made of, for example, aluminum make electrical contact with the source 15 and drain 16, respectively. Electrical conductor 20, made of the same material as conductors 18 and 19, is connected to the gate electrode 14.

Although a trigate structure 40 is shown and discussed herein, this invention is applicable to monogate and split gate structures also. The monogate structure consists of a pure memory portion like the central portion of the trigate structure 40 (Fig. 1) having a thin oxide layer and a relatively thick oxynitride layer. The split gate structure consists of a memory portion like the central portion of the trigate structure 40 and a single non-memory portion having thick oxide 12A and oxynitride 13 layers instead of two non-memory portions of structure 40 (Fig. 1).

Likewise, although the invention has been discussed in connection with a memory field effect transistor, it is applicable to other devices such as capacitors.

Characterization of the Device

To determine the retention characteristics of the present novel device, several n-channel trigate devices were fabricated, tested and the test results evaluated. These devices include the conventional silicon gate-nitride-oxide-silicon devices and the present silicon gate-oxynitride-oxide-silicon devices having the basic structure shown in Fig. 1. All the

devices had the same thickness memory oxide (20 Angstroms) and polysilicon gate (3,000 Angstroms). The test results which focus on the retention characteristics are summarized in Table I.

5 The procedure used for testing the above devices is well-known. The write and erase curves were generated, for example, by subjecting the devices to various pulse-stressing conditions (pulse amplitude and duration). The amplitude of the pulse was in the ranges

10 $\pm$ 13.5 volts to $\pm$ 16.5 volts, the positive and negative values being applicable to the write and erase charging characteristics, respectively. The duration of these pulses was in the range of 100 microseconds to about 1 second.

15 The data to determine the charge retention in the devices were obtained by: (1) initializing the devices and determining the initial write and erase threshold voltages; (2) obtaining retention graphs from these devices by storing the devices at an elevated

20 temperature of 100°C for a time of up to 10^5 seconds and determining the threshold voltages at intervals during this time. The initialization procedure (step 1) i.e. obtaining the initial written and erased state threshold voltages, involved applying a +15 volt pulse of 10

25 milliseconds duration and a -15 volt pulse of 100 millisecond duration, respectively, to the gates of the memory devices. Source 15, drain 16 and substrate 10 (Fig. 1) were all tied to ground during this investigation except during the threshold measurement. Using

30 the retention data obtained in the above fashion, Table I was constructed.

In Table I, "initial window" represents the initial memory margin of the device; "write state decay rate" is the slope of the write (threshold voltage)

35 curve; and "erased state decay rate" is the slope of the erase (threshold voltage) curve. The memory windows at one year and one decade shown in Table I were

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obtained by extrapolating the write and erase curves. Finally, "memory margin decay rate" is the sum of the written and erased state decay rates.

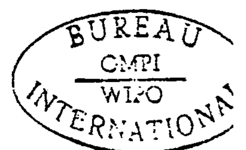
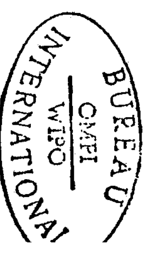


Table I

Structure	Wafer No.	Oxynitride/ Nitride Thickness(A)	Initial Window (volts)	Decay rate (V/Decade) Written State	Erased State	Extrapolated Window (V) at 1 yr.	at 10 yrs.
Silicon	A-1	297	5.5	0.32	0.16	1.91	1.43
Gate-	A-2	297	5.48	0.31	0.14	2.11	1.66
Oxynitride-	B-1	279	5.85	0.29	0.185	2.30	1.82
Oxide-	B-2	279	5.85	0.30	0.20	2.11	1.61
Silicon	C-1	262	5.70	0.30	0.13	2.48	2.05
	C-2	262	5.85	0.30	0.17	2.33	1.86
	D-1	244	5.55	0.31	0.17	1.96	1.48
	Average	274	5.68	0.30	0.165	2.17	1.70
	Average Memory margin decay rate = 0.465 V/Decade						
Silicon	X-1	293	7.35	0.43	0.515	0.28	-0.66
Gate-	Y-1	272	7.15	0.47	0.485	0.01	-0.95
Nitride-	Z-1	252	7.07	0.42	0.475	0.01	-0.89
Oxide-	Average	271	7.07	0.44	0.49	0.10	-0.83
Silicon	Average Memory margin decay rate = 0.93 V/Decade						



It is obvious from Table I that the present silicon-gate-oxynitride-oxide-silicon structure exhibits a significantly lower memory margin decay rate of 0.465 volts per decade than the memory margin decay rate of 0.93 volts per decade exhibited by the conventional SNOS structure. This indicates that the present SO_nOS device has superior charge retention capability than the SNOS device.

The device of the present invention was also tested for write/erase cycling (or endurance) effects. These tests showed that the read access performance was not noticeably affected even after 10,000 write/erase cycles, thus indicating that the cumulative write/erase stressing did not increase the rate of charge loss from the oxide-oxynitride gate insulator. In other words, the end result is that the present SO_nOS device is inherently better than the SNOS device because of the improved retention.

A full understanding of the physical phenomenon occurring in the present memory structure that results in the described improved characteristics is not now available. It is supposed that the unique properties of silicon oxynitride layer which are intermediate between those of the silicon oxide layer and the silicon nitride layer, contribute to these improvements by decreasing the charge trap density in the oxynitride layer. The utilization of structures in accordance with this invention does not require a full understanding of the physical mechanism in the devices' operation.

The results noted above have been limited to n-channel devices wherein the gates were doped with n-type impurities. However, the invention is not so limited. For example, a p-channel FET having the same structure as Fig. 1 or a combination of both p-channel FET and n-channel FET, i.e. CMOS FET may be constructed.

The improved charge retention obtained above with n-channel FETs should be equally valid for these devices also.

In summary, it has been demonstrated that the
5 retention of silicon gate devices has been greatly improved by means of a novel silicon oxide-oxynitride dual gate dielectric structure. An added benefit of this structure is that it can be formed with no more process steps than required for forming the conventional SNOS
10 devices.

CLAIMS:

1. A non-volatile semiconductor memory device, including a semiconductor substrate (10), a first insulator layer formed by a silicon dioxide layer (12) provided on said substrate (10), a second insulator
5 layer (13) provided on said first insulator layer (12) and a conductive gate electrode (14) provided on said second insulator layer (13), characterized in that said second insulator layer is formed by a silicon oxynitride layer (13).

2. A memory device according to claim 1, characterized in that said silicon oxynitride layer (13) has a thickness in the range of from 200 to 500 Angstroms.

3. A memory device according to claim 1, characterized in that said silicon dioxide layer (12) has a thickness in the range of from 20 to 35 Angstroms.

4. A memory device according to claim 1, characterized in that said conductive gate electrode (14) is formed of polycrystalline silicon.

5. A memory device according to claim 1, characterized in that said semiconductor substrate (10) is formed of single crystal silicon.

6. A memory device according to claim 1, characterized in that said silicon substrate (10) is of a first conductivity type, having provided therein source and drain regions (15, 16) of a second conduc-
5 tivity type thereby defining a channel region in said semiconductor substrate (10), and in that said silicon dioxide layer (12), said silicon oxynitride layer (13)

6. (concluded)
and said conductive gate electrode (14) are provided over said channel region.

7. A memory device according to claim 1, characterized in that said silicon oxynitride layer (13) is formed by low pressure chemical vapor deposition utilizing ammonia, dichlorosilane and nitrous
5 oxide.

8. A memory device according to claim 7, characterized in that said ammonia, dichlorosilane and nitrous oxide are provided in the proportion 3.5:1:2.

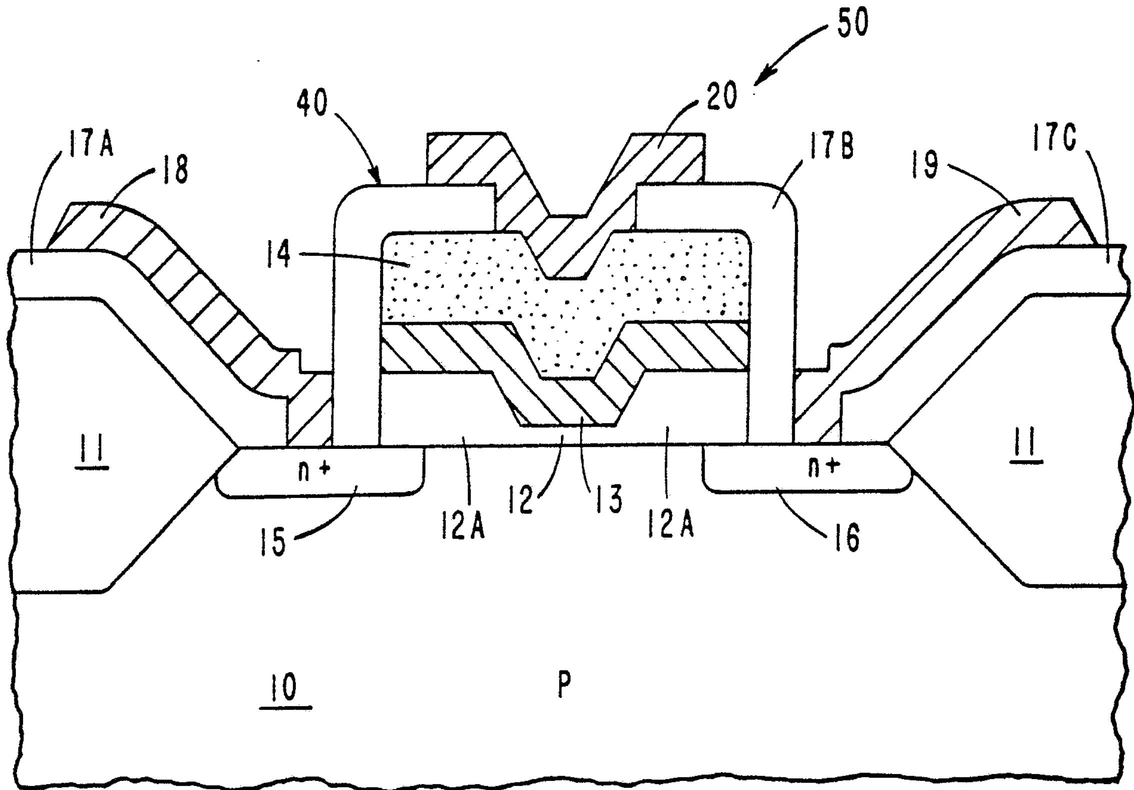


FIG. 1

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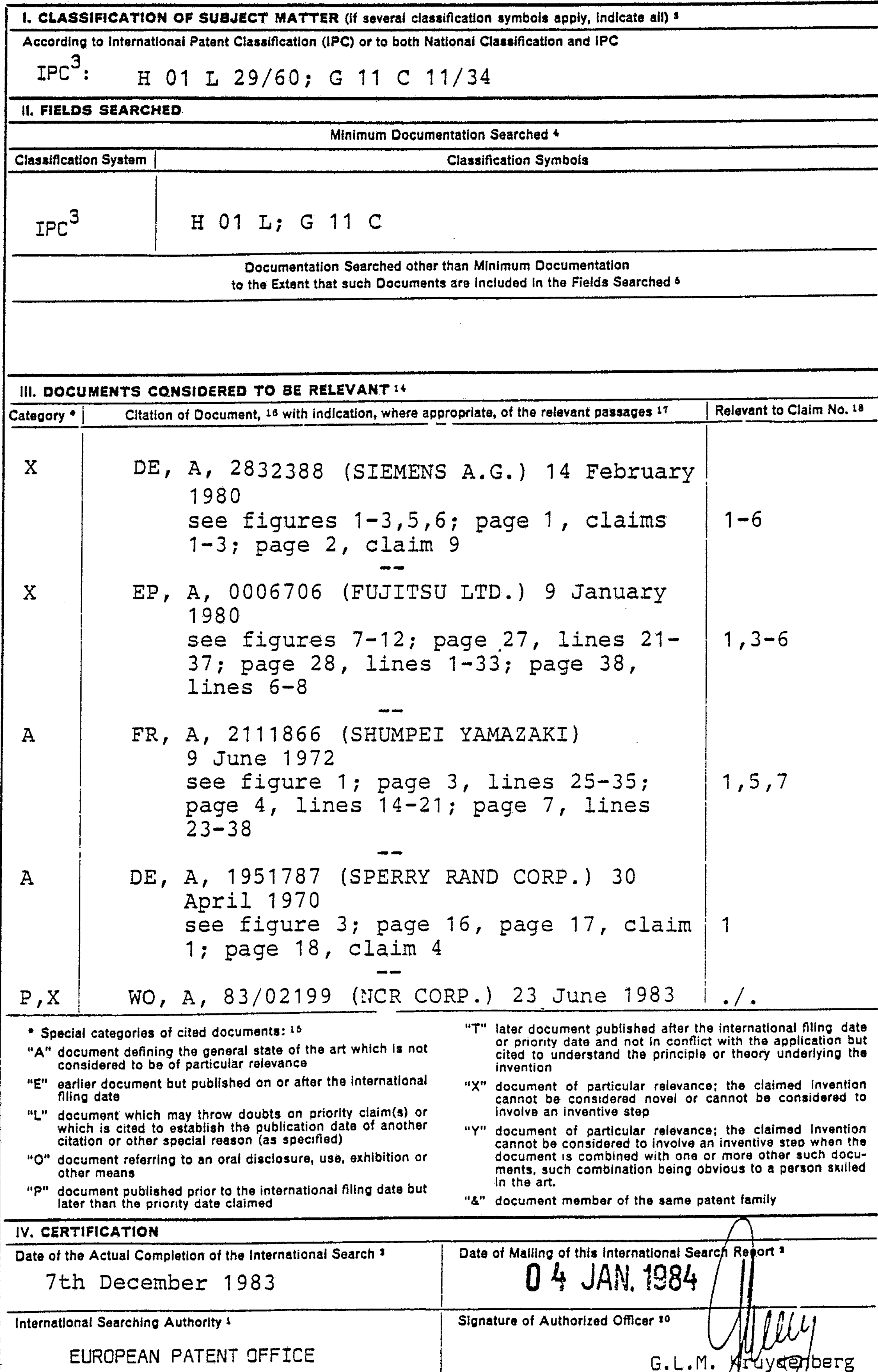

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 83/01219

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^3: H 01 L 29/60; G 11 C 11/34

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC^3	H 01 L; G 11 C

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	DE, A, 2832388 (SIEMENS A.G.) 14 February 1980 see figures 1-3,5,6; page 1, claims 1-3; page 2, claim 9 --	1-6
X	EP, A, 0006706 (FUJITSU LTD.) 9 January 1980 see figures 7-12; page 27, lines 21-37; page 28, lines 1-33; page 38, lines 6-8 --	1,3-6
A	FR, A, 2111866 (SHUMPEI YAMAZAKI) 9 June 1972 see figure 1; page 3, lines 25-35; page 4, lines 14-21; page 7, lines 23-38 --	1,5,7
A	DE, A, 1951787 (SPERRY RAND CORP.) 30 April 1970 see figure 3; page 16, page 17, claim 1; page 18, claim 4 --	1
P,X	WO, A, 83/02199 (NCR CORP.) 23 June 1983	./.

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
7th December 1983	04 JAN. 1984
International Searching Authority [1]	**Signature of Authorized Officer [10]**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No [18]
	see figures 1-3; page 7, lines 12-31; page 9, lines 26-28; page 13, lines 1-13; page 20, lines 6-17 ------	1-8

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 83/01219 (SA ' 5694)

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		JP-A-	55018099	07/02/80
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		EP-A-	0072603	23/02/83
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		US-A-	3878549	15/04/75
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