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(54) **Title:** DISTRIBUTED ELECTROSTATIC DISCHARGE PROTECTION FOR AN ON-PACKAGE INPUT/OUTPUT ARCHITECTURE

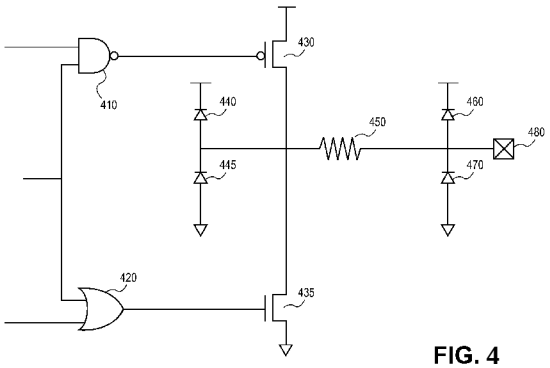

FIG. 4

(57) **Abstract:** An on-package interface. A first set of single-ended transmitter circuits on a first die. A first set of single-ended receiver circuits on a second die. The receiver circuits have a termination circuit comprising an inverter and a resistive feedback element. A plurality of conductive lines couple the first set of transmitter circuits and the first set of receiver circuits. The lengths of the plurality of conductive lines are matched.

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DISTRIBUTED ELECTROSTATIC DISCHARGE PROTECTION FOR AN ON-PACKAGE INPUT/OUTPUT ARCHITECTURE

TECHNICAL FIELD

[0001] Embodiments of the invention relate to input/output architectures and interfaces. More particularly, embodiments of the invention relate to high-bandwidth on-package input/output architectures and interfaces.

BACKGROUND

[0002] High bandwidth interconnections between chips using conventional input/output (I/O) interfaces require significant power and chip area. Thus, in applications requiring significantly reduced power consumption and/or smaller chip area, these conventional interfaces are not desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a block diagram of one embodiment of a multichip package (MCP) having on-package input/output (OPIO) interfaces between at least two chips.

Figure 2a is a circuit diagram of a first embodiment of a feedback inverter termination (FIT) scheme.

Figure 2b is a circuit diagram of a second embodiment of a feedback inverter termination (FIT) scheme.

Figure 2c is a circuit diagram of a third embodiment of a feedback inverter termination (FIT) scheme.

Figure 3 provides an example resistance characteristic of a FIT scheme.

Figure 4 is s circuit diagram of one embodiment of a distributed electrostatic discharge (ESD) protection scheme.

Figure 5 is a graph of impedance values using driver slices for both drivers with single resistance values and two resistance values.

Figure 6 is a block diagram of one embodiment of an electronic system.

DETAILED DESCRIPTION

[0003] In the following description, numerous specific details are set forth. However, embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0004] Described herein is an On-Package I/O (OPIO) interface that solves the problems of conventional I/O interfaces by providing very high bandwidth I/O between chips in a Multi Chip Package (MCP) with very low power, area and latency. OPIO may be useful, for example, to interconnect a processor to memory (eDRAM/DRAM), another processor, a chip set, a graphics processor, or any other chip in a MCP with an order of magnitude lower energy per bit and area per bandwidth compared to conventional I/O.

[0005] Various embodiments of the interfaces described herein include one or more of the following components: (1) a single-ended, high-speed I/O interface (e.g., CMOS interface) between IC chips in a MCP with a relatively small die-to-die gap; (2) an impedance matched transmitter (e.g., CMOS transmitter) with no receiver termination or very weak termination, and no equalization; (3) a forwarded clock signal for a cluster of signals with length-matched routing to minimize or eliminate per pin de-skew; and/or (4) reduced electrostatic discharge (ESD) protection (e.g., 70 V) to provide lower pad capacitances and higher data rates.

[0006] Close chip assembly in MCP enables very short length matched I/O traces, which in turn enables OPIO architectures described herein to run at high bandwidth using simplified single-ended I/O and clocking circuits to reduce power, area and latency. In one embodiment, high-speed, single-ended I/O

with minimum bump pitch reduces bump limited silicon area for required bandwidth.

[0007] In one embodiment, use of a CMOS transmitter and receiver with no or weak receiver termination and no equalization can reduce I/O power. In another embodiment, where distance between chips is longer, optional weak to fully matched receiver termination is enabled to achieve high data rate at the expense of I/O power. Simplified clocking with forwarded clock per cluster of signals and no per pin de-skew can be achieved due to careful length matched routing reduces clock power. Thus, the OPIO architectures described herein provide high bandwidth between chips at very low power, area and latency. MCP with OPIO provides product, process and die area flexibility without significant power and area overhead. The OPIO architectures described herein can also be extended to close discrete packages with full ESD protection for small form factor mobile applications at lower data rates. Multi-level (e.g., M-PAM) signaling can be used at higher data rates to keep the clock frequency down.

[0008] **Figure 1** is a block diagram of one embodiment of a multichip package (MCP) having on-package input/output (OPIO) interfaces between at least two chips. The example of Figure 1 illustrates two chips with interfaces; however, any number of chips within a package can be interconnected using the techniques described herein.

[0009] Package 100 may be any type of package that may contain multiple integrated circuit chips. In the example of Figure 1, package 100 contains chip 120 and chip 140. These chips may be, for example, processors, memory chips, graphics processors, etc.

[0010] In one embodiment, chip 120 includes OPIO transmitters 125 and OPIO receivers 130. Similarly, chip 140 includes OPIO transmitters 145 and OPIO receivers 150. Transmitters 125 are coupled with receivers 150 and transmitters 145 are coupled with receivers 130.

[0011] In one embodiment, gap 175 between chip 120 and chip 140 is relatively small. In one embodiment, gap 175 is less than 20 mm. In one embodiment, gap 175 is less than 10 mm. In one embodiment, gap 175 is approximately 1.5 mm. In

other embodiments, gap 175 may be less than 1.5 mm. In general, the smaller gap 175, the greater the bandwidth that may be provided between chips.

[0012] In one embodiment, the interfaces between transmitter 125 and receiver 150, and between transmitter 145 and receiver 130 are single-ended, relatively high-speed interfaces. In one embodiment, the interfaces are CMOS interfaces between chip 120 and chip 140. In one embodiment, transmitters 125 and 145 are impedance matched CMOS transmitters and no termination or equalization is provided. In one embodiment, transmitters 125 and 145 are impedance matched CMOS transmitters and very weak termination and no equalization is provided.

[0013] In one embodiment, a forwarded clock signal is transmitted for a cluster of signals. In one embodiment, length-matched routing is provided between the transmitters and the receivers. In one embodiment, minimal electrostatic discharge (ESD) protection (as little as 70 Volts) is provided for the interfaces between chips 120 and 140.

[0014] In one embodiment, use of a CMOS transmitter and receiver with no or weak receiver termination and no equalization can reduce I/O power. Simplified clocking with forwarded clock per cluster of signals and no per pin de-skew can be achieved due to careful length matched routing reduces clock power. Thus, the architectures described herein provide high bandwidth between chips at very low power, area and latency.

[0015] The architectures described herein can also be extended to close discrete packages with full ESD protection for small form factor mobile applications at lower data rates. Multi-level (e.g., M-PAM) signaling can be used at higher data rates to keep the clock frequency down.

[0016] Under certain conditions, the interface of Figure 1 may benefit from termination. However, conventional center-tap termination (CCTs) implemented using passive resistors consume static power and degrade I/O power efficiency. CCTs also typically consume significant die area and increase the I/O pad capacitance. Described herein is a non-linear termination approach that may significantly reduce the power/area/pad capacitance cost while preserving the benefits of a linear CCT.

[0017] **Figure 2a** is a circuit diagram of a first embodiment of a feedback inverter termination (FIT) scheme. The FIT of Figure 2a has a non-linear current-voltage (I-

V) characteristic to provide a voltage-dependent resistance that may be used for termination purposes.

[0018] Pad 210 provides an electrical interface with a remote portion of, for example, an interface (not illustrated in Figure 2). Pad 210 may be coupled with FIT, which includes inverter 220 (e.g., a CMOS inverter) and resistive element 230 coupled to provide feedback to inverter 220.

[0019] **Figure 2b** is a circuit diagram of a second embodiment of a feedback inverter termination (FIT) scheme. The FIT of Figure 2b has a non-linear current-voltage (I-V) characteristic to provide a voltage-dependent resistance that may be used for termination purposes.

[0020] Pad 240 provides an electrical interface with a remote portion of, for example, an interface (not illustrated in Figure 2b). Pad 240 may be coupled with FIT, which includes inverter 250 (e.g., a CMOS inverter) and resistor 245 with inverter 250 coupled to provide feedback to from the output of inverter 250 to the input of inverter 250.

[0021] **Figure 2c** is a circuit diagram of a first embodiment of a feedback inverter termination (FIT) scheme. The FIT of Figure 2c has a non-linear current-voltage (I-V) characteristic to provide a voltage-dependent resistance that may be used for termination purposes.

[0022] Pad 260 provides an electrical interface with a remote portion of, for example, an interface (not illustrated in Figure 2c). Pad 260 may be coupled with FIT, which includes resistor 270 coupled with and adjustable inverter 280 that may provide varying impedances.

[0023] **Figure 3** provides an example resistance characteristic of a FIT scheme. The large signal resistance is at a maximum at approximately Vcc/2 and decreases as the voltage approaches the supply rail values. This type of variation may be advantageous in source-series terminated (SST) links, which may be used, for example, in the interface of Figure 1.

[0024] Line 300 provides a linear I-V characteristic, for reference purposes. Line 310 represents a non-linear I-V characteristic, such as may be provided by the FIT scheme described herein. Boxes 350 and 360 indicate the smaller resistance values corresponding to 0/Vcc.

[0025] When an incident wave arrives at the receiver, the value is approximately Vcc/2 due to voltage division between the driver termination and the channel characteristic impedance. At this value, the receiver large signal termination resistance is at a maximum, maximizing the reflection and speeding the transition to the full supply rail value. Once the signal has settled close to 0/Vcc, the small signal resistance is smaller, which mitigates further reflections and reduces undershoot/overshoot.

[0026] Thus, the termination scheme described herein takes advantage of the inherently non-linear I-V characteristics of MOS devices to achieve the benefits of receiver CCT to reduce the termination power/area, while maintaining the signal integrity benefits provided by conventional CCT. Thus, the scheme described herein may be used to reduce the termination power in I/O links that may use CCT. It is particularly well suited to the interface of Figure 1 and other SST I/O interfaces that require only weak termination to improve signal integrity and reduce overshoot/undershoot. FIT may also significantly reduce the area and pad capacitance impact of CCT because it can be implemented using only active devices without relying on area-intensive passive devices.

[0027] Mobile, small form factor devices (e.g., thin laptops, tablets, smart phones) generally allocate limited power to chips due to thermal and battery life constraints. Conventional interfaces require significant power as compared to the interfaces described herein. The interfaces may be used to couple multiple chips and/or provide multiple links with in a MCP. The individual interfaces may be of varying widths, speeds and/or protocols (e.g., memory or non-memory), while using a common physical layer architecture.

[0028] **Figure 4** is s circuit diagram of one embodiment of a distributed electrostatic discharge (ESD) protection scheme. The scheme of Figure 4 may be used to provide a reduced level of ESD protection (e.g., 70 V vs. 240 V) as compared to traditional ESD schemes. The reduced level of ESD protection may be sufficient because the interface to be protected may only be subject to an ESD event during the manufacturing/assembly process. With appropriate protections during the manufacturing/assembly process, this level of ESD protection may be sufficient. The circuitry used to provide the reduced level of ESD protection may result in

smaller ESD circuitry, which may provide lower pad capacitance and higher operational frequencies.

[0029] Various embodiments of the ESD scheme described herein may be distributed. Conventional ESD protection lumps ESD diodes at the pad being protected. The pad capacitance from these devices is typically a very large portion of the total pad capacitance, which can reduce transmission bandwidth.

[0030] To overcome these bandwidth-limiting issues, a more complex architecture may be used, for example, transmitter and/or receiver equalization. A typical driver consists of transistors coupled with linear resistors coupled with the pad. The linear resistors provide some IR drop to the transistors in case of an ESD event, but the more typical use is to provide a more linear impedance looking back to the driver.

[0031] The concept illustrated in Figure 4 is to move some of the ESD protection from the pad to the transistor-resistor interface, which may function to increase the overall transmission bandwidth and may provide a more steady small signal impedance profile looking back to the pad.

[0032] In one embodiment, a variable size, segmented driver architecture is utilized. Impedance controller drivers may be built from multiple parallel segments. Impedance compensation for process/temperature variations may be provided by turning on/off parallel segments to achieve the desired driver impedance. Designing for process variation typically requires a fairly large driver in order to provide the impedance range desired.

[0033] Slow corner may require more (e.g., twice as many) segmented driver legs to provide the same impedance as fast corner. Large drivers add capacitance and reduce bandwidth. Impedance curves follow a 1/x distribution, so low range impedance values tend to require many more parallel driver legs, especially in slow corner. Using a variable size segmented driver can increase the driver impedance range with a smaller overall driver.

[0034] A simple case can be to use a second driver slice at R/2 (where R is the resistance used for the first driver slice) and only place these second driver slices at the end. This allows fast and slow corners to look the same as before, but in the slow process corner the reduce resistance legs can be used. This could allow for

reduced transmitter buffer size and can enable at reduction in transmitter size, reduced pad capacitance, bandwidth improvement and/or overall performance improvement.

[0035] In the example of Figure 4, logic gates 410 and 420 are coupled with the gates of transistors 430 and 435, respectively. Transistors 430 and 435 are coupled between the high and low supply voltages. Resistor 450 is coupled between transistors 430 and 435 and pad 480. The resistance value of resistor 450 is the R value used with respect to the resistance of the driver slice.

[0036] Diodes 440, 445, 460 and 470 operate to provide ESD protection to pad 480. By distributing multiple diodes, the diodes closest to pad 480 (i.e., diodes 460 and 470) may be smaller, and provide lower pad capacitance, which may improve the bandwidth that may be provided through pad 480.

[0037] **Figure 5** is a graph of impedance values using driver slices for both drivers with single resistance values and two resistance values. The example of Figure 5 is based on use of R and R/2; however, any number of resistance values and any relationship between the resistance values can be used.

[0038] In the example of Figure 5, if the target impedance is 35 ohms, 35 legs may be required using only a single R value. With the addition of R/2 legs, only 27 legs are necessary. The point at which legs are switched from the first resistance value to the second allows the designer to select the inflection point as well as the granularity around the target impedance value.

[0039] **Figure 6** is a block diagram of one embodiment of an electronic system. The electronic system illustrated in Figure 6 is intended to represent a range of electronic systems (either wired or wireless) including, for example, a tablet device, a smartphone, a desktop computer system, a laptop computer system, a server etc. Alternative electronic systems may include more, fewer and/or different components.

[0040] One or more of the components illustrated in Figure 6 may be interconnected utilizing the OPIO architectures described herein. For example, multiple processor chips may be interconnected, or a processor and a cache memory or dynamic random access memory, etc.

[0041] Electronic system 600 includes bus 605 or other communication device to communicate information, and processor(s) 610 coupled to bus 605 that may process

information. Electronic system 600 may include multiple processors and/or co-processors. Electronic system 600 further may include random access memory (RAM) or other dynamic storage device 620 (referred to as memory), coupled to bus 605 and may store information and instructions that may be executed by processor 610. Memory 620 may also be used to store temporary variables or other intermediate information during execution of instructions by processor(s) 610.

[0042] Electronic system 600 may also include read only memory (ROM) and/or other static storage device 630 coupled to bus 605 that may store static information and instructions for processor 610. Data storage device 640 may be coupled to bus 605 to store information and instructions. Data storage device 640 such as a magnetic disk or optical disc and corresponding drive may be coupled to electronic system 600.

[0043] Electronic system 600 may also be coupled via bus 605 to display device 650, which can be any type of display device, to display information to a user, for example, a touch screen. Input device 660 may be any type of interface and/or device to allow a user to provide input to electronic system 600. Input device may include hard buttons and/or soft buttons, voice or speaker input, to communicate information and command selections to processor(s) 610.

[0044] Electronic system 600 may further include sensors 670 that may be used to support functionality provided by Electronic system 600. Sensors 670 may include, for example, a gyroscope, a proximity sensor, a light sensor, etc. Any number of sensors and sensor types may be supported.

[0045] Electronic system 600 further may include network interface(s) 680 to provide access to a network, such as a local area network. Network interface(s) 680 may include, for example, a wireless network interface having antenna 685, which may represent one or more antenna(e). Network interface(s) 680 may also include, for example, a wired network interface to communicate with remote devices via network cable 687, which may be, for example, an Ethernet cable, a coaxial cable, a fiber optic cable, a serial cable, or a parallel cable.

[0046] In one embodiment, network interface(s) 680 may provide access to a local area network, for example, by conforming to IEEE 802.11b and/or IEEE 802.11g and/or IEEE 802.11n standards, and/or the wireless network interface may provide

access to a personal area network, for example, by conforming to Bluetooth standards. Other wireless network interfaces and/or protocols can also be supported.

[0047] IEEE 802.11b corresponds to IEEE Std. 802.11b-1999 entitled "Local and Metropolitan Area Networks, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Higher-Speed Physical Layer Extension in the 2.4 GHz Band," approved September 16, 1999 as well as related documents. IEEE 802.11g corresponds to IEEE Std. 802.11g-2003 entitled "Local and Metropolitan Area Networks, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, Amendment 6: Further Higher Rate Extension in the 2.4 GHz Band," approved June 27, 2003 as well as related documents. Bluetooth protocols are described in "Specification of the Bluetooth System: Core, Version 1.1," published February 22, 2001 by the Bluetooth Special Interest Group, Inc. Associated as well as previous or subsequent versions of the Bluetooth standard may also be supported.

[0048] In addition to, or instead of, communication via wireless LAN standards, network interface(s) 680 may provide wireless communications using, for example, Time Division, Multiple Access (TDMA) protocols, Global System for Mobile Communications (GSM) protocols, Code Division, Multiple Access (CDMA) protocols, and/or any other type of wireless communications protocol.

[0049] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0050] While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. An apparatus comprising:

an input/output (I/O) pad;

a first pair of diodes coupled with the pad and between a supply voltage and a ground potential;

a resistive element coupled to the pad and with a second pair of diodes coupled between the supply voltage and the ground potential.

2. The apparatus of claim 1 further comprising:

a first set of single-ended transmitter circuits on a first die;

a first set of single-ended receiver circuits on a second die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

a plurality of conductive lines between the first set of transmitter circuits and the first set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

3. The apparatus of claim 1 further comprising:

a second set of single-ended transmitter circuits on the second die;

a second set of single-ended receiver circuits on the first die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

a plurality of conductive lines between the second set of transmitter circuits and the second set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

4. The apparatus of claim 2, wherein the first die comprises at least a processor core, the apparatus further comprising a touch screen interface coupled with the processor core.

5. The apparatus of claim 2 wherein the first die, the second die and the plurality of conductive lines are all disposed within a single integrated circuit package.

6. A tablet computing device comprising:

a touch screen interface;

a first set of single-ended transmitter circuits on a first die;

a first set of single-ended receiver circuits on a second die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

a plurality of conductive lines between the first set of transmitter circuits and the first set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

7. The tablet of claim 6 further comprising:

a first set of single-ended transmitter circuits on a first die;

a first set of single-ended receiver circuits on a second die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

a plurality of conductive lines between the first set of transmitter circuits and the first set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

8. The tablet of claim 7 further comprising:

a second set of single-ended transmitter circuits on the second die;

a second set of single-ended receiver circuits on the first die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

a plurality of conductive lines between the second set of transmitter circuits and the second set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

9. The tablet of claim 7 wherein the first die, the second die and the plurality of conductive lines are all disposed within a single integrated circuit package.

10. A system comprising:

an omnidirectional antenna;

an input/output (I/O) pad;

a first pair of diodes coupled with the pad and between a supply voltage and a ground potential;

a resistive element coupled to the pad and with a second pair of diodes coupled between the supply voltage and the ground potential.

11. The system of claim 10 further comprising:

a first set of single-ended transmitter circuits on a first die;

a first set of single-ended receiver circuits on a second die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

a plurality of conductive lines between the first set of transmitter circuits and the first set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

12. The system of claim 11 further comprising:

a second set of single-ended transmitter circuits on the second die;

a second set of single-ended receiver circuits on the first die, wherein the receiver circuits have a termination circuit comprising an inverter and a resistive feedback element; and

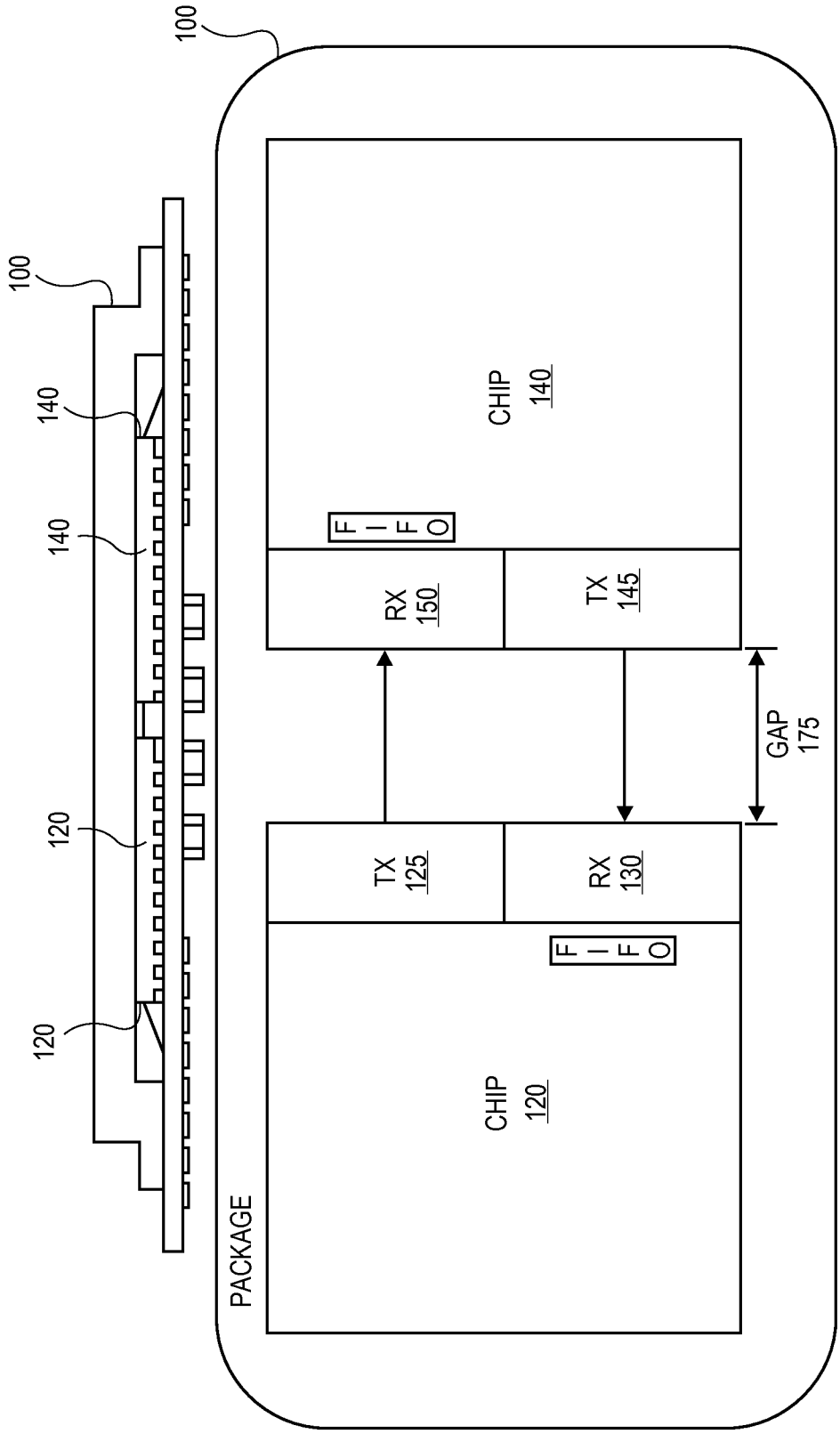
a plurality of conductive lines between the second set of transmitter circuits and the second set of receiver circuits, wherein the lengths of the plurality of conductive lines are matched.

13. The system of claim 11, wherein the first die comprises at least a processor core, the system further comprising a touch screen interface coupled with the processor core.

14. The system of claim 11, wherein the first die comprises at least a processor core, the apparatus further comprising a touch screen interface coupled with the processor core.

15. The system of claim 11 wherein the first die, the second die and the plurality of conductive lines are all disposed within a single integrated circuit package.

16. The system of claim 15 wherein the use of smaller and distributed ESD protection diodes significantly reduces I/O pad capacitance to improve bandwidth.


100
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PACKAGE
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GAP
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TX
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RX
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F I F O
CHIP
120

FIG. 1

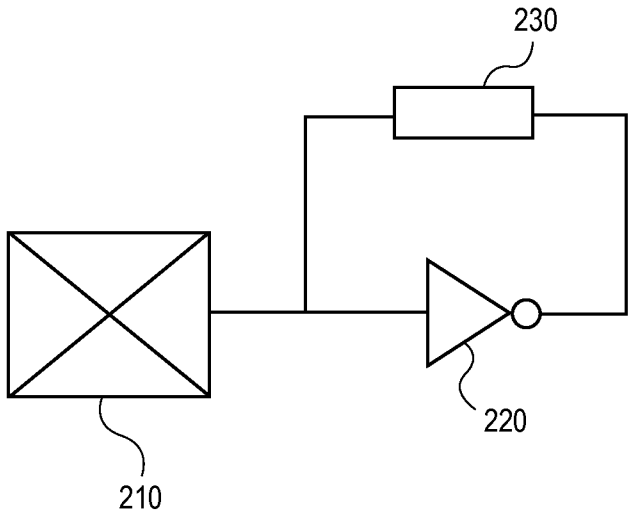

FIG. 2A

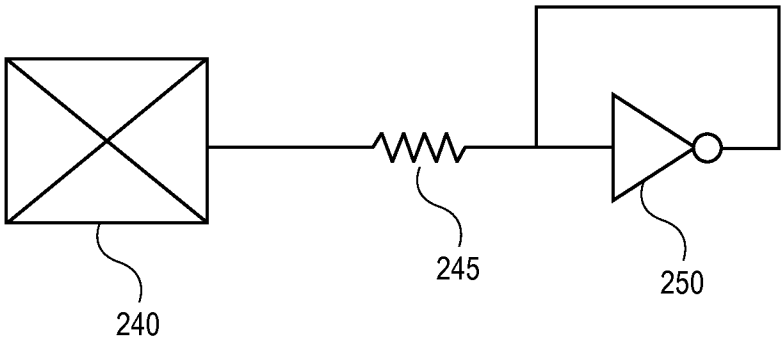

FIG. 2B

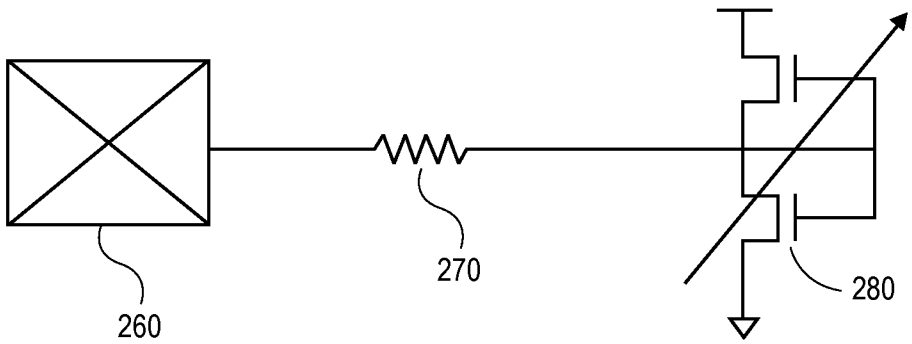

FIG. 2C

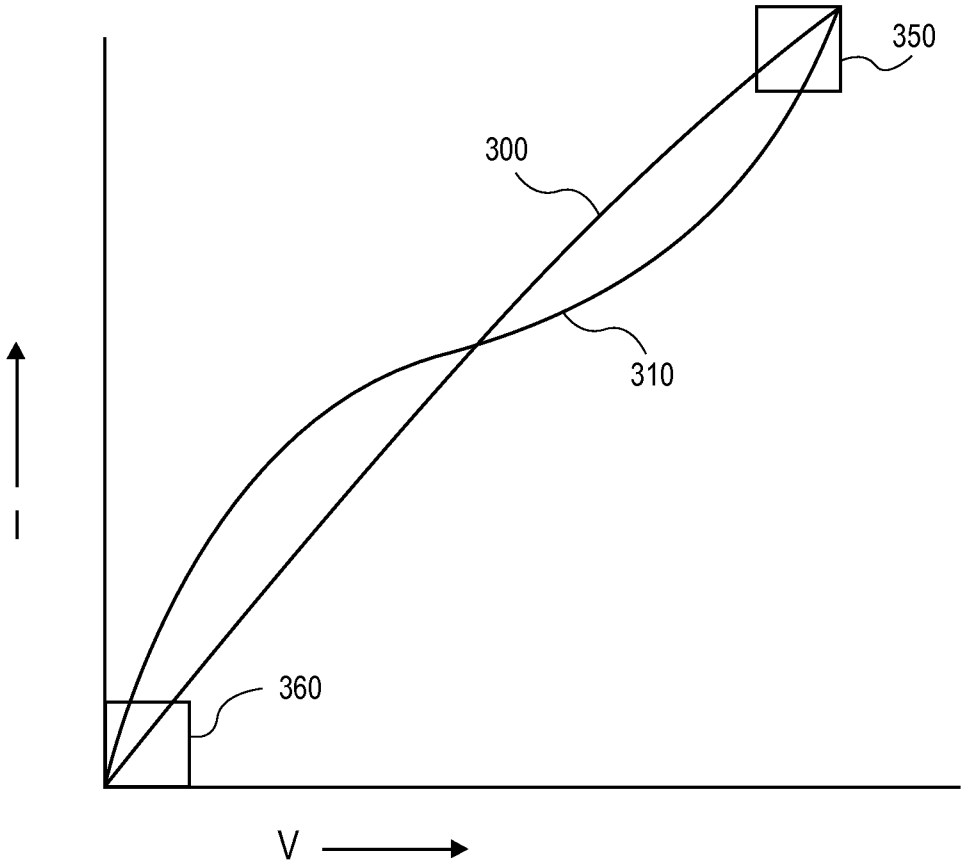

FIG. 3

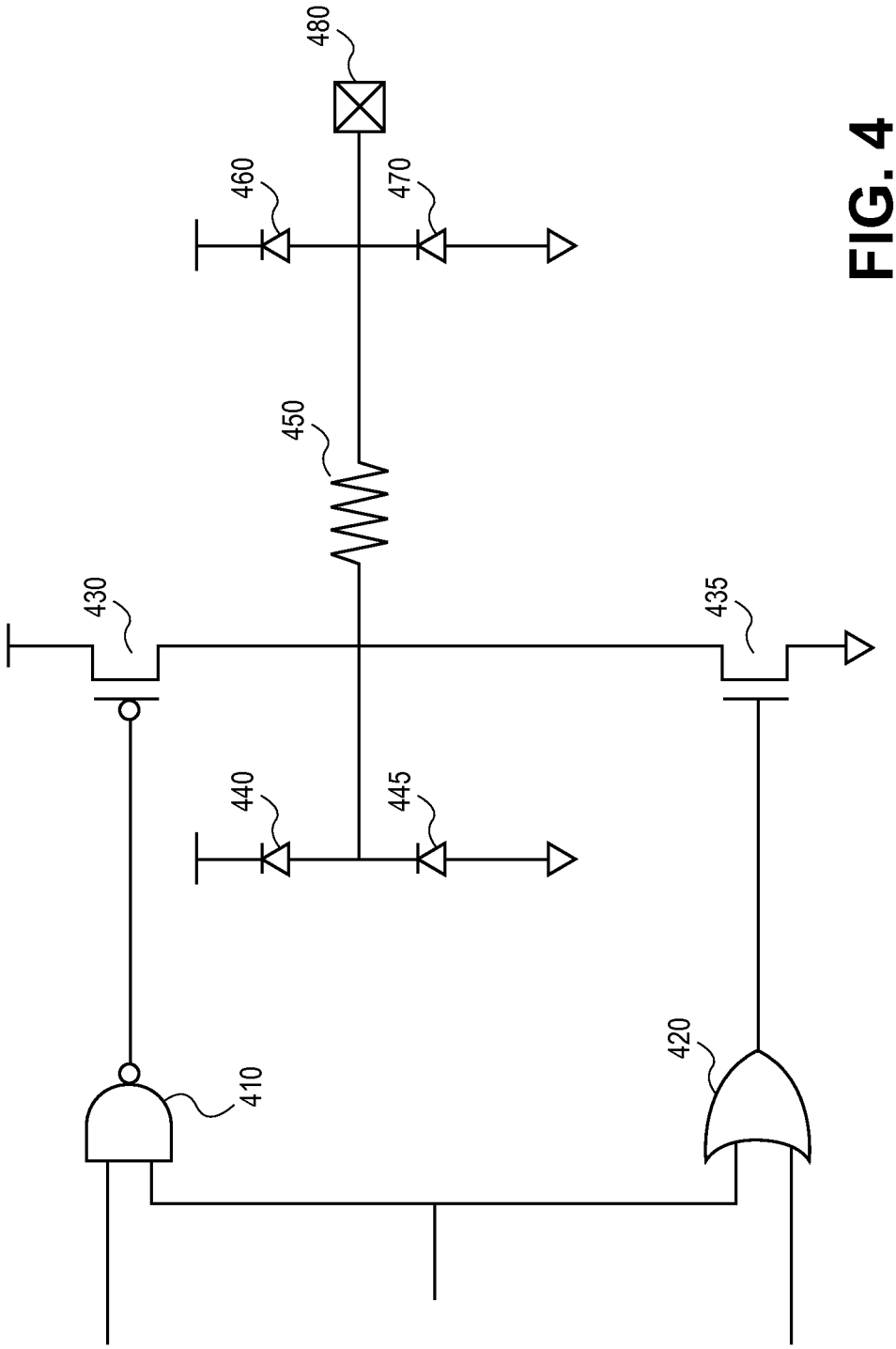

FIG. 4

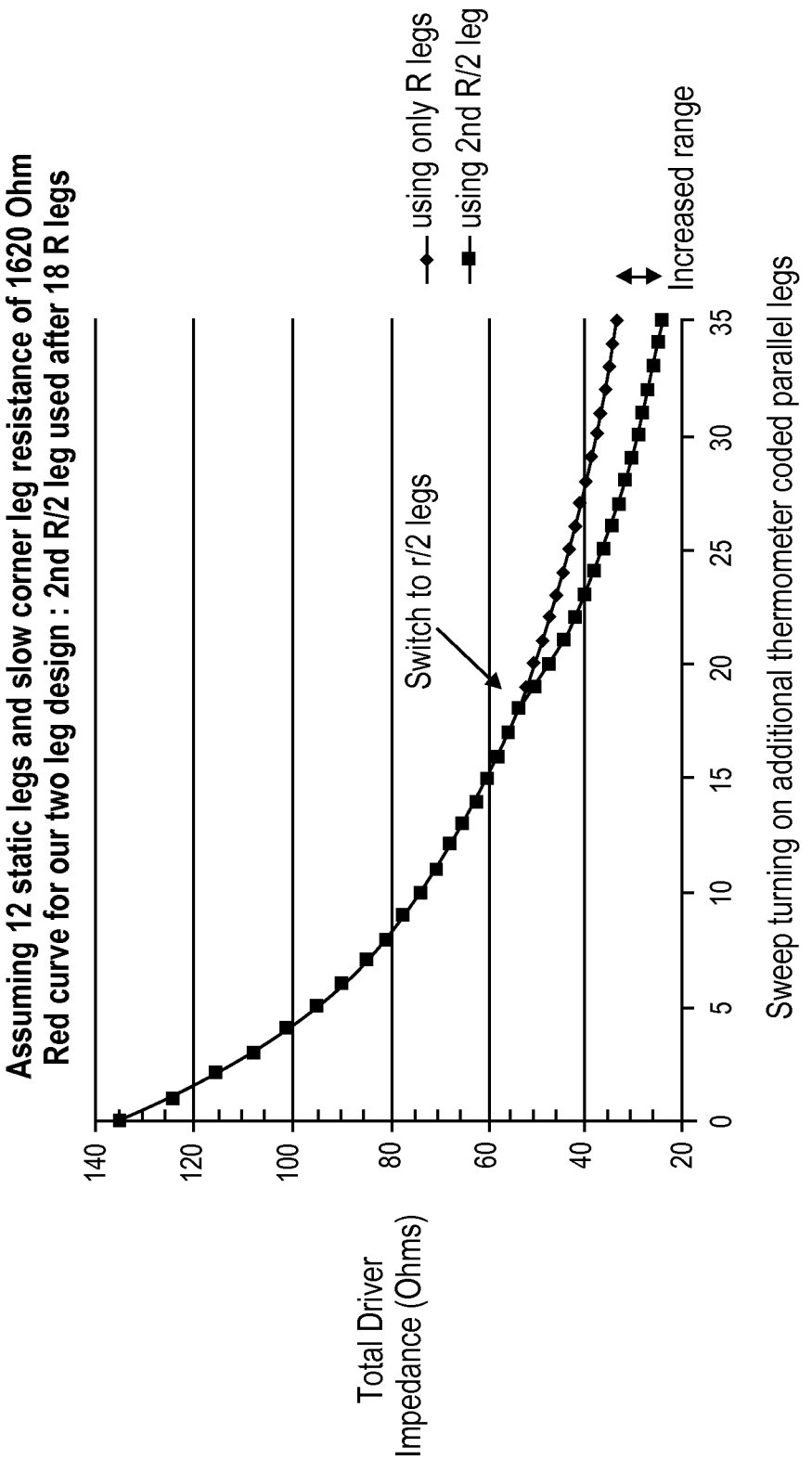
Assuming 12 static legs and slow corner leg resistance of 1620 Ohm
Red curve for our two leg design : 2nd R/2 leg used after 18 R legs
using only R legs
using 2nd R/2 leg
Switch to r/2 legs
Increased range
Total Driver Impedance (Ohms)
140
120
100
80
60
40
20
0
5
10
15
20
25
30
35
Sweep turning on additional thermometer coded parallel legs

FIG. 5

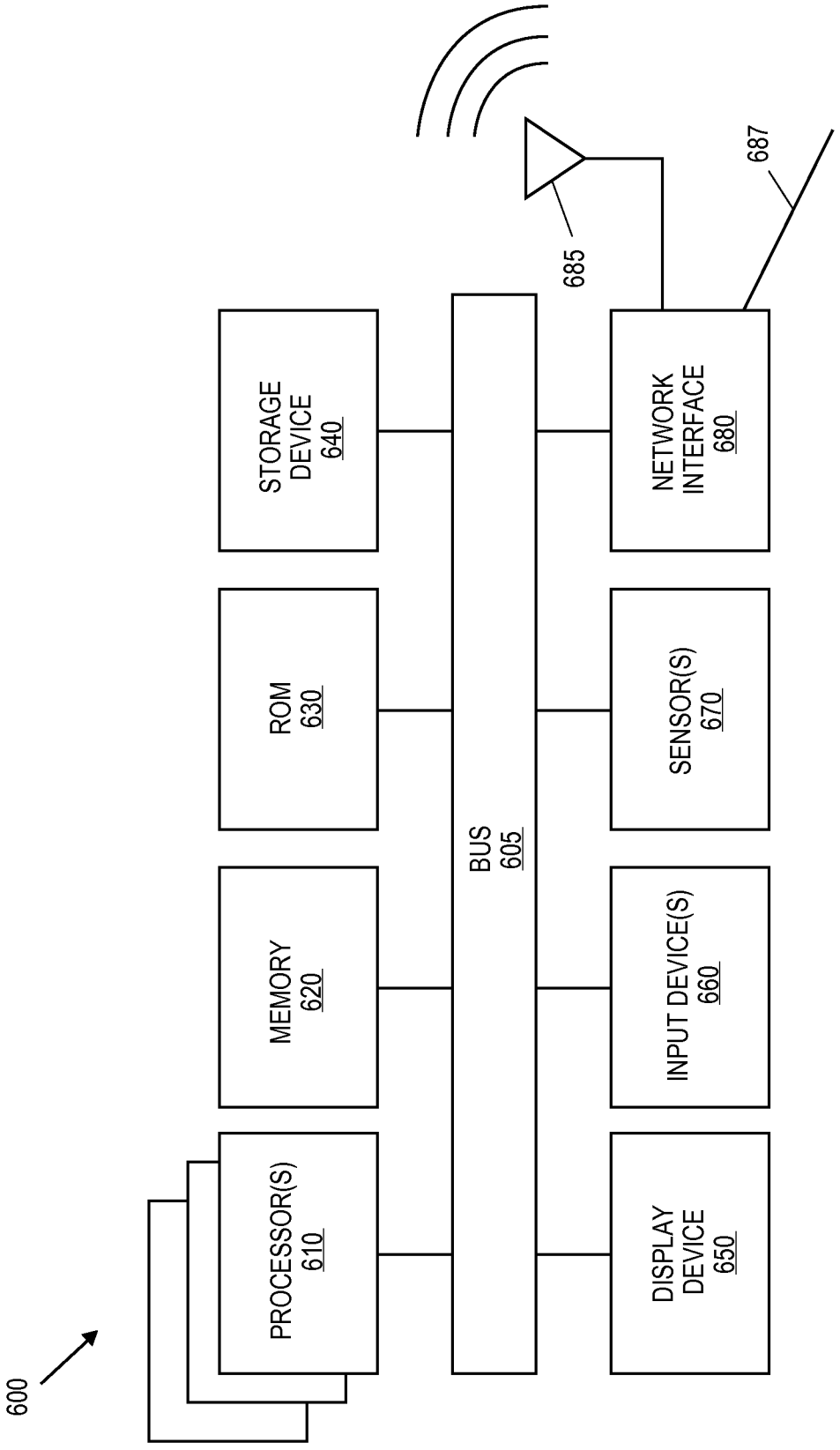
600
PROCESSOR(S)
610
MEMORY
620
ROM
630
STORAGE DEVICE
640
BUS
605
DISPLAY DEVICE
650
INPUT DEVICE(S)
660
SENSOR(S)
670
NETWORK INTERFACE
680
685
687

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US201 1/066985

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/00(2006.01)i, G06F 13/14(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/00; H05K 13/04; H03K 19/0175; H03K 17/16; H01L 29/06; H01L 29/10; H02H 9/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: "DIODE", "PAIR" , "ESD" , "PROTECTION" , "RESISTOR"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	W0 95-10855 Al (INTEL CORPORATION) 20 April 1995 See abstract, page 9 line 7 - page 16 line 14 and figures 2-3	1
A	US 2011-0249369 Al (RUEGER TIMOTHY T.) 13 October 2011 See abstract, paragraphs [0015]-[0063] and figure 2	1-16
A	US 6724223 B2 (ICHIGUCHI TETSUICHIRO et al.) 20 April 2004 See abstract, column 5 line 22 - column 22 line 23 and figure 15	1-16
A	US 7205787 Bl (ALI MASSOUMI and CHANDRASEKHARA SOMANATHAN) 17 April 2007 See abstract, column 3 line 40 - column 8 line 67 and figure 2B	1-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 SEPTEMBER 2012 (25.09.2012)	**26 SEPTEMBER 2012 (26.09.2012)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US20 11/066985

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