

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
22 January 2009 (22.01.2009)

PCT

(10) International Publication Number
WO 2009/010891 A1

- (51) **International Patent Classification:**
H04L 7/08 (2006.01) *H04J 3/06* (2006.01)
H03L 7/081 (2006.01)
- (21) **International Application Number:**
PCT/IB2008/051876
- (22) **International Filing Date:** 13 May 2008 (13.05.2008)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
07112613.0 17 July 2007 (17.07.2007) EP
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(81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) **Title:** A METHOD AND A DEVICE FOR DATA SAMPLE CLOCK RECONSTRUCTION

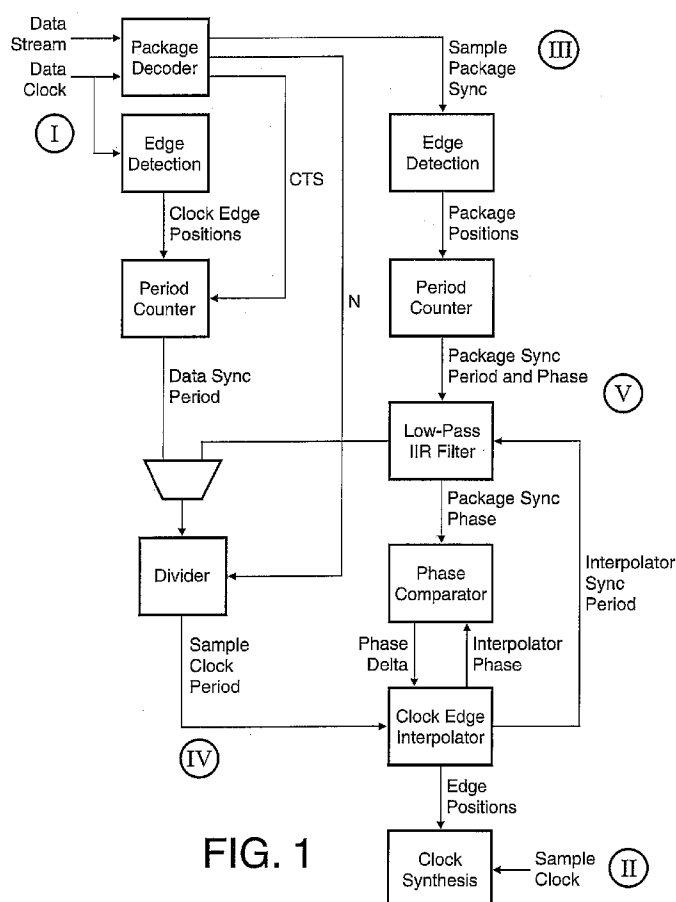


FIG. 1

(57) **Abstract:** A method and a device for data sample clock reconstruction of a data transmission is described, wherein data samples are extracted from a data stream, a first signal is generated whenever one of said data samples is extracted from the data stream, said first signal is converted to a second signal by essentially averaging out irregularities of the first signal, a data sample clock period is determined by using the period of the second signal, data sample clock edge positions are determined by interpolation on the basis of the sample clock period and a difference between the phase of the second signal and a reference phase, and a data sample clock is created from said determined data sample clock edge positions.

WO 2009/010891 A1



Published:

— *with international search report*

A METHOD AND A DEVICE FOR DATA SAMPLE CLOCK RECONSTRUCTION

FIELD OF THE INVENTION

The present invention relates to a method and a device for data sample clock reconstruction of a data transmission, in particular of a digital, packet based data transmission.

5 BACKGROUND OF THE INVENTION

The High-Definition Multimedia Interface (HDMI), DisplayPort (VESA) and Unified Display Interface (UDI) are provided for transmitting digital audiovisual signals from DVD players, set-top boxes, PCs and other audiovisual sources to television sets, projectors and other video displays. All these transmission systems can carry high quality
10 multi-channel audio data and can carry all standard and high-definition consumer electronics video formats.

Audio data being carried across a link, which is driven by a clock with constant frequency of the transport channel only, does not retain the original audio sample clock. The task of recreating this clock at the receiver is called audio clock regeneration.

15 An HDMI source determines the fractional relationship between the video/TMDS (transmission minimized differential signalling) clock frequency f_{TMDS} of the physical link and an audio reference sampling clock frequency f_{audio} and passes the numerator (N) and denominator (CTS) for that fraction to the receiver across the HDMI link. The resulting equation, which has to be considered for reference sampling clock reconstruction, is

20
$$f_{audio} = N/CTS \cdot f_{TMDS}.$$

The receiver can then recreate the audio reference sampling clock from the TMDS clock by using a clock divider and a clock multiplier, which is implemented as PLL (phase locked loop) structure typically using a pre-divider for the division and a feedback divider value for the multiplication.

For DisplayPort, both audio and video data are based on packet driven transmissions, and their average data rates are fully independent of a link symbol clock f_{ls_clk} as used for the transmission channel link. Therefore both audio and video clock have to be derived from f_{ls_clk} , which is crystal based and typically constant. For the video stream clock
5 frequency f_{strm_clk} this equation is

$$f_{strm_clk} = M/N \cdot f_{ls_clk},$$

where f_{ls_clk} is the link symbol clock. As for HDMI, the numerator and denominator for that fraction are passed from the transmitter to the receiver.

For UDI, an interface specification is not yet published, but it was claimed to
10 stay backward compatible to HDMI, which leads to equivalent constraints concerning the audio reference sampling clock recovery.

If the video and audio clock are asynchronous or there is some amount of jitter between both these clocks, the nominator or denominator value will typically alternate between different values. Since changes of this value do not have a specified relationship to
15 reference clock cycles, from which the reconstructed clock frequency is derived, a perfect reconstruction of that output clock from the reference clock is not possible in all cases. Therefore some additional synchronization mechanism for fine adjustment is required, which will most commonly drop or repeat audio samples or adjust the received CTS value temporarily.

20 US 2005/0220240 A1 discloses a method and a device for clock and data recovery wherein a clock synchronizer incorporates an elastic buffer. A received clock signal is used to clock data into the buffer, and a locally generated clock is used to clock data out of the buffer. The local clock is synthesised using a PLL, and a fill-level signal from the elastic buffer is used to control the local clock frequency so as to maintain a desired average quality
25 of data in the buffer, thereby achieving a synchronization of the received and local clocks. In preferred embodiments of this prior art, the fill-level signal is used to control a variable divider in the feedback pass of the PLL, which is supplied with a highly stable reference signal. Thus, a synchronized and low-jitter local clock is produced. So, according to this prior

art, a fill-level signal at the receiver's data buffer is used to control the nominator value accordingly.

A disadvantage of the PLL as technical solution with a pre-divider and feedback-divider is a quite low (<50kHz) intermediate frequency after the PLL pre-divider.

- 5 This leads to an increased amount of output jitter after multiplication by the PLL feedback function ($\times 3,000 \dots \times 80,000$ typically). Using this analog PLL approach, the jitter requirements of SPDIF (Sony/Philips digital interface) audio clocking are thus very difficult to achieve. Furthermore a FIFO (first-in/first-out) fill state control mechanism is mandatory in order to avoid data FIFO over- or underflows leading to data losses or idle states. Another
- 10 solution is the usage of a high-frequency crystal-stable oscillator with a fractional (sigma-delta principle) post-divider control, which can improve the jitter performance. Nevertheless the data FIFO fill state must be tracked and frequency corrections to the output clock must be applied, before the upper/lower FIFO fill-state will be exceeded.

SUMMARY OF THE INVENTION

- 15 An object of the present invention is to provide a data sample clock reconstruction of a data transmission, in particular from digitally encoded sample packages, without the need of a supplementary clock signal.

- In order to achieve the above and further objects, in accordance with a first aspect of the present invention, there is provided a method for data sample clock
- 20 reconstruction of a data transmission, comprising the steps of

- A) extracting data samples from a data stream,
- B) generating a first signal, whenever one of said data samples is extracted from the data stream,
- C) converting said first signal to a second signal by essentially averaging out
- 25 irregularities of the first signal,
- D) determining a data sample clock period by using the period of the second signal,
- E) determining data sample clock edge positions by interpolation on the basis of said sample clock period and a difference between the phase of the second signal and a
- 30 reference phase, and

F) creating a data sample clock from said determined data sample clock edge positions.

In order to achieve the aforementioned and further objects, in accordance with a second aspect of the present invention, there is provided a device for date sample clock reconstruction of a data transmission, comprising

an extracting unit extracting data samples from a data stream,

a signal generator generating a first signal, whenever the extracting unit extracts one of said data samples from the data stream,

an averaging unit converting said first signal to a second signal by essentially averaging out irregularities of the first signal,

a determining unit determining a data sample clock period by using the period of the second signal,

an interpolator determining data sample clock edge positions by interpolation on the basis of said sample clock period and a difference between the phase of the second signal and a reference phase, and

a clock synthesizer creating a data sample clock from said determined data sample clock edge positions.

The method and the device according to the present invention simplifies and improves the performance of data sample clock reconstruction and in particular of a synchronized clock reconstruction since the data sample clock can be reconstructed from data samples of a data stream without the need of a supplementary clock signal. In particular, a data sample clock reconstruction of a packet based data transmission can be achieved by the present invention so that a data sample clock can be reconstructed from digitally encoded data sample packages without the need of a supplementary clock signal. This is achieved by that the reconstructed data sample clock is locked to the rate of the extracted data samples, in particular the decoded data sample packages, even if their distribution in time is highly irregular. When using a digital system for clock synthesis, the method and device of the present invention can seamlessly be integrated into a digital clock synthesis based architecture as described e.g. in US 2005/0200393 A1, and can consequently benefit from its advantages over a traditional analog PLL approach.

Preferred embodiments of the present invention are defined in the dependent claims.

So, the data stream usually includes data samples of different kinds, and data samples of a predetermined kind are extracted from the data stream. In particular, said data samples of the predetermined kind are audio data samples. Namely, a typical application of the present invention is in receivers for audio/visual contents like HDMI-, DisplayPort- and UDI-receivers where a data sample clock reconstruction is minatory in order to ensure an isochroous transmission system for audio and/or video data.

Preferably, the first signal is a synchronization signal.

According to a further preferred embodiment, a third signal is created having a period corresponding to the sum of periods of a predetermined number of consecutive first signals wherein essentially averaging out irregularities of the first signal is achieved by essentially averaging out irregularities of the third signal so as to create the second signal as the averaged third signal. So, in this embodiment, the third signal is used for averaging-out of the irregularities of the first signal by that irregularities of the third signal are averaged out, and for creating the second signal by that the averaged third signal is provided as the second signal. The predetermined number of the first signals can be counted so as to create the third signal. According to a modification of this preferred embodiment, edge positions of the first signal are determined, and the predetermined number of the determined edge positions of the first signal are counted so as to create the third signal. Advantageously, the third signal can be created having a period with a length within which the difference between the phase of the second signal and the reference phase can be adjusted.

According to a further preferred embodiment, the averaging is carried out by filtering, in particular by a low-pass filtering. Moreover, due to the interpolation a fourth signal can be created on the basis of the sample clock period and of the difference between the phase of the second signal and the reference phase, said fourth signal being used to initialize the filtering. In particular, the fourth signal can be used to indicate a correlated interpolator synchronization period.

According to a still further preferred embodiment of the present invention, the data sample clock period is determined by dividing the period of the second signal by a predetermined numerator.

5 According to a still further preferred embodiment of the present invention, the phase of the second signal is compared with the reference phase before interpolation.

According to a still further preferred embodiment of the present invention, the difference between the phase of the second signal and the reference phase is corrected.

According to a still further preferred embodiment, it is possible to create the reference phase during interpolation.

10 In particular, the interpolation can be a phase interpolation.

Moreover, it is possible to schedule the data sample clock edge positions.

15 According to a further preferred embodiment of the present invention, data clocks are additionally extracted from the data stream, a data synchronization period is determined from the extracted data clocks, and the data synchronization period is used as an alternative to the period of the second signal for determining the data sample clock period. If, as in this embodiment, a supplementary data clock signal is available, the recovered data sample clock mean frequency can still be derived from the data clocks so that the phase of the regenerated data sample clock can be locked directly to the rate of the data samples (data pay load packages) which are extracted from the data stream. So, a cross-link between the
20 two synchronization paths can eliminate run-in delays which result from averaging out and particularly filtering out strong irregularities of the first signal and, thus, of the data samples.

In the aforementioned embodiment, the data sample clock period can be determined by dividing the data synchronization period by a predetermined numerator. In order to achieve the cross-link between the two synchronization paths in an advantages
25 manner, a multiplexing is carried out between the period of the second signal and the data synchronization period.

The data synchronization period can be created so as to correspond to the sum of periods of a predetermined number of consecutive data clocks. In order to achieve this, preferably the predetermined number of data clocks can be counted. Moreover, the data clock edge positions can be determined from the data clocks, and the predetermined number of data clock edge positions can be counted so as to create the data synchronization period.

Moreover, it is possible to obtain an information about the ratio between the data sample frequency and the data clock frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other objects and features of the present invention will become clear from the following description taken in conjunction with the accompanying drawings in which:

Figure 1 is a schematic block diagram of a device for data sample clock reconstruction according to an embodiment of the present invention;

Figure 2 shows the waveform of some signals occurred in the device of figure 1; and

Figure 3 is a schematic block diagram of an HDMI-receiver wherein the device of figure 1 is part of an audio clock recovery block.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The attached figures illustrate an embodiment of the present invention. A digital multi-media data stream provides data sample packages, which contain pixel color codes during active video and audio samples along with additional mode information during horizontal and vertical blanking intervals. The shown system aims at reconstructing a sample clock that is locked on the transmitted audio sample rate.

As shown in figures 1 and 2, a package decoder generates a sync (synchronization) signal, whenever a data sample package is extracted from the data stream.

This may result in a highly irregular sync pattern, to which the output data sample clock is to be locked. A unit for edge detection shown in the right-hand 'line' of the circuitry of figure 1 digitizes the sync signal positions to simplify further processing. The present invention does not stick to details of this mechanism, but allows different approaches here. The introduced example is based on the aforementioned method for digital clock synthesis (DCS).

In order to build a base period for phase correction intervals, a programmable number of package sync signals is counted by a period counter shown in the right-hand 'line' of the circuitry of figure 1. The resulting period (package sync period) along with the corresponding sync phase is passed to a low-pass filter also shown in the right-hand 'line' of the circuitry of figure 1 where the irregularities of the package sync signals are averaged out.

A clock edge interpolator also shown in the right-hand 'line' of the circuitry of figure 1 schedules the edge positions of the data sample clock to be synthesized. It can operate in a free-running mode on the mean sample clock frequency. Again different approaches from DCS for synthesis are possible here. Another counter included in the clock edge interpolator and therefore not individually shown in figure 1 for sample clock edges defines the reference phase of the interpolator respectively of the generated output clock. By this the interpolator sync period and phase is provided, quite similar to the package sync.

The locking is done by correcting differences (deltas) between the two sync phases by a temporary change in frequency of the synthesized sample clock. This temporary frequency offset is kept below an application dependent value in order not to introduce noticeable interferences to the target application. The length of the synchronization periods is adjusted accordingly, so that commonly expected phase deltas can be adjusted within one period (which is not strictly required though for the system to work, but simplifies setup and analysis) as shown in figure 2. Moreover, a correlated interpolator sync period can be used to initialize the history of the low-pass filter for package sync positions.

Since generation of sampling clocks usually demands for stable frequency and low jitter, the low-pass behaviour of the filter setup results in a relative long time constant. Consequently this may result in a significant run-in time for the system to get tuned to the mean frequency of the highly irregular input package syncs. In order to eliminate this

transient period, an optional circuitry shown in the left-hand 'line' of the circuitry of figure 1 can be used to utilize the data clock. This assumes that the source provides information about the ratio between data and sample clock frequency (e.g. values CTS and N for HDMI). The target frequency of the clock interpolator is not derived from the filtered package sync period then, but from the data sync period.

A typical application of the present invention is in receivers for audio/visual contents like HDMI-, DisplayPort- and UDI-receivers where a data sample clock reconstruction is minatory in order to ensure an isochroous transmission system for audio and/or video data. A schematic block diagram of a typical HDMI-receiver is shown in figure 2 wherein the device of figure 1 is part of the audio clock recovery block.

While the present invention has been described in terms of a preferred embodiment above, there are alterations, modifications, and equivalents, which all lie within the scope of the present invention. It should also be noted that there are many alternative ways of implementing the method and device of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, modifications and equivalents within the spirit and scope of the present invention.

Claims:

1. A method for data sample clock reconstruction of a data transmission, comprising the steps of

A) extracting data samples from a data stream,

B) generating a first signal, whenever one of said data samples is extracted from the data stream,

C) converting said first signal to a second signal by essentially averaging out irregularities of the first signal,

D) determining a data sample clock period by using the period of the second signal,

E) determining data sample clock edge positions by interpolation on the basis of said sample clock period and a difference between the phase of the second signal and a reference phase, and

F) creating a data sample clock from said determined data sample clock edge positions.

2. The method according to claim 1, wherein the data stream includes data samples of different kinds, and during step A data samples of a predetermined kind are extracted from the data stream.

3. The method according to claim 2, wherein said data samples of the predetermined kind are audio data samples.

4. The method according to at least any one of the preceding claims, wherein said first signal is a synchronization signal.

5. The method according to at least any one of the preceding claims, wherein step C further comprises creating a third signal having a period corresponding to the sum of periods of a predetermined number of consecutive first signals wherein essentially averaging out irregularities of the first signal is achieved by essentially averaging out irregularities of said third signal so as to create the second signal as the averaged third signal.

6. The method according to claim 5, wherein step C comprises counting the predetermined number of the first signals so as to create the third signal.

7. The method according to claim 5 or 6, wherein after step B and before step C
5 edge positions of the first signal are determined, and step C comprises counting the predetermined number of the determined edge positions of the first signal so as to create the third signal.

8. The method according to at least any one of claims 5 to 7, wherein in step C
10 the third signal is created having a period with a length within which the difference between the phase of the second signal and the reference phase can be adjusted.

9. The method according to at least any one of the preceding claims, wherein the averaging of step C is carried out by filtering.

10. The method according to claim 9, wherein said filtering is a low-pass filtering.

11. The method according to claim 9 or 10, wherein in step E due to the interpolation a fourth signal is created on the basis of the sample clock period and of the
20 difference between the phase of the second signal and the reference phase, said fourth signal being used to initialize the filtering.

12. The method according to claim 11, wherein the fourth signal indicates a correlated interpolator synchronization period.

13. The method according to at least any one of the preceding claims, wherein in step D the data sample clock period is determined by dividing the period of the second signal by a predetermined numerator.

14. The method according to at least any one of the preceding claims, comprising
30 a further step of comparing the phase of the second signal with the reference phase before step E.

15. The method according to at least any one of the preceding claims, wherein step E further comprises correcting the difference between the phase of the second signal and the reference phase.

5 16. The method according to at least any one of the preceding claims, wherein step E further comprises creating the reference phase.

17. The method according to at least any one of the preceding claims, wherein the interpolation of step E is a phase interpolation.

10

18. The method according to at least any one of the preceding claims, wherein step E further comprises scheduling the data sample clock edge positions.

19. The method according to at least any one of the preceding claims, comprising
15 the further steps of

- additionally extracting data clocks from the data stream in step A,
- determining a data synchronization period from the extracted data clocks,
- and
- using the data synchronization period as an alternative to the period of the

20 second signal for determining the data sample clock period in step D.

20. The method according to claim 19, wherein in step D the data sample clock period is determined by dividing the data synchronization period by a predetermined numerator.

21. The method according to claim 19 or 20, wherein step D comprises
25 multiplexing between the period of the second signal and the data synchronization period.

22. The method according to at least any one of the claims 19 to 21, wherein the data synchronization period is created having a period corresponding to the sum of periods of a predetermined number of consecutive data clocks.

23. The method according to claim 22, wherein the predetermined number of data
30 clocks is counted so as to create the data synchronization period.

24. The method according to claim 23, wherein data clock edge positions are determined from the data clocks, and the predetermined number of data clock edge positions are counted so as to create the data synchronization period.

25. The method according to at least any one of the claims 19 to 24, wherein step
5 A further comprises providing an information about the ratio between the data sample frequency and the data clock frequency.

26. A device for date sample clock reconstruction of a data transmission, comprising

an extracting unit extracting data samples from a data stream

10 a signal generator generating a first signal, whenever the extracting unit extracts one of said data samples from the data stream,

an averaging unit converting said first signal to a second signal by essentially averaging out irregularities of the first signal,

15 a determining unit determining a data sample clock period by using the period of the second signal,

an interpolator determining data sample clock edge positions by interpolation on the basis of said sample clock period and a difference between the phase of the second signal and a reference phase, and

20 a clock synthesizer creating a data sample clock from said determined data sample clock edge positions.

27. The device according to claim 26, wherein the extracting unit is adapted to extract data samples of a predetermined kind from the data stream including data samples of different kinds.

28. The device according to claim 27, wherein said data samples of the
25 predetermined kind are audio data samples.

29. The device according to at least any one of claims 26 to 28, wherein said first signal is a synchronization signal.

30. The device according to at least any one of claims 26 to 29, wherein the averaging unit further comprises a signal generator creating a third signal having a period corresponding to the sum of periods of a predetermined number of consecutive first signals, and is adapted to achieve the averaging-out of the irregularities of the first signal by essentially averaging out irregularities of said third signal so as to create the second signal as the averaged third signal.

31. The device according to claim 30, wherein the averaging unit further comprises a counter counting the predetermined number of the first signals so as to create the third signal.

32. The device according to claim 30 or 31, further comprising an edge position detector determining the edge positions of the first signal, wherein the averaging unit further comprises a counter counting the predetermined number of the determined edge positions of the first signal so as to create the third signal.

33. The device according to at least any one of claims 30 to 32, wherein the averaging unit is adapted to create the third signal having a period with a length within which the difference between the phase of the second signal and the reference phase can be adjusted.

34. The device according to at least any one of claims 26 to 33, wherein the averaging unit comprises a filter.

35. The device according to claim 34, wherein said filter is a low-pass filter.

36. The device according to claim 34 or 35, wherein the interpolator is adapted to create a fourth signal in the basis of the sample clock period and of the difference between the phase of the second signal and the reference phase, said fourth signal being used to initialize the filter.

37. The device according to claim 36, wherein the interpolator is adapted to create the fourth signal indicating a correlated interpolator synchronization period.

38. The device according to at least any one of claims 26 to 37, wherein the determining unit comprises a divider dividing the period of the second signal by a predetermined numerator so as to determine the data sample clock period.

39. The device according to at least any one of claims 26 to 38, further comprising
5 a comparator comparing the phase of the second signal with the reference phase.

40. The device according to at least any one of claims 26 to 39, wherein the interpolator further comprises a corrector correcting the difference between the phase of the second signal and the reference phase.

41. The device according to at least any one of claims 26 to 40, wherein the
10 interpolator further comprises a reference phase generator.

42. The device according to at least any one of claims 26 to 41, wherein the interpolator is adapted to carry out a phase interpolation.

43. The device according to at least any one of claims 26 to 42, wherein the interpolator comprises a data sample clock edge positions scheduler.

15 44. The device according to at least any one of claims 26 to 43, further comprising an additional extracting unit extracting data clocks from the data stream, and a further determining unit determining a data synchronization period from the extracted data clocks, said data synchronization period being used as an alternative to the period of the second signal for determining the data sample clock period.

20 45. The device according to claim 44, further comprising a divider dividing the data synchronization period by a predetermined numerator so as to determine the data sample clock period.

46. The device according to claim 44 or 45, further comprising a multiplexer multiplexing between the period of the second signal and the data synchronization period.

47. The device according to at least any one of claims 44 to 46, further comprising a data synchronization period generator creating the data synchronization having a period corresponding to the sum of periods of a predetermined number of consecutive data blocks.

48. The device according to claim 47, further comprising a counter counting the
5 predetermined number of data clocks so as to create the data synchronization period.

49. The device according to claim 48, further comprising a data clock edge position determining unit determining data clock edge positions from the data clocks, wherein the counter is adapted to count the predetermined number of data clock edge positions so as to create the data synchronization period.

10 50. The device according to at least any one of claims 44 to 49, wherein the extracting unit is further adapted to provide an information about the ratio between the data sample frequency and the data clock frequency.

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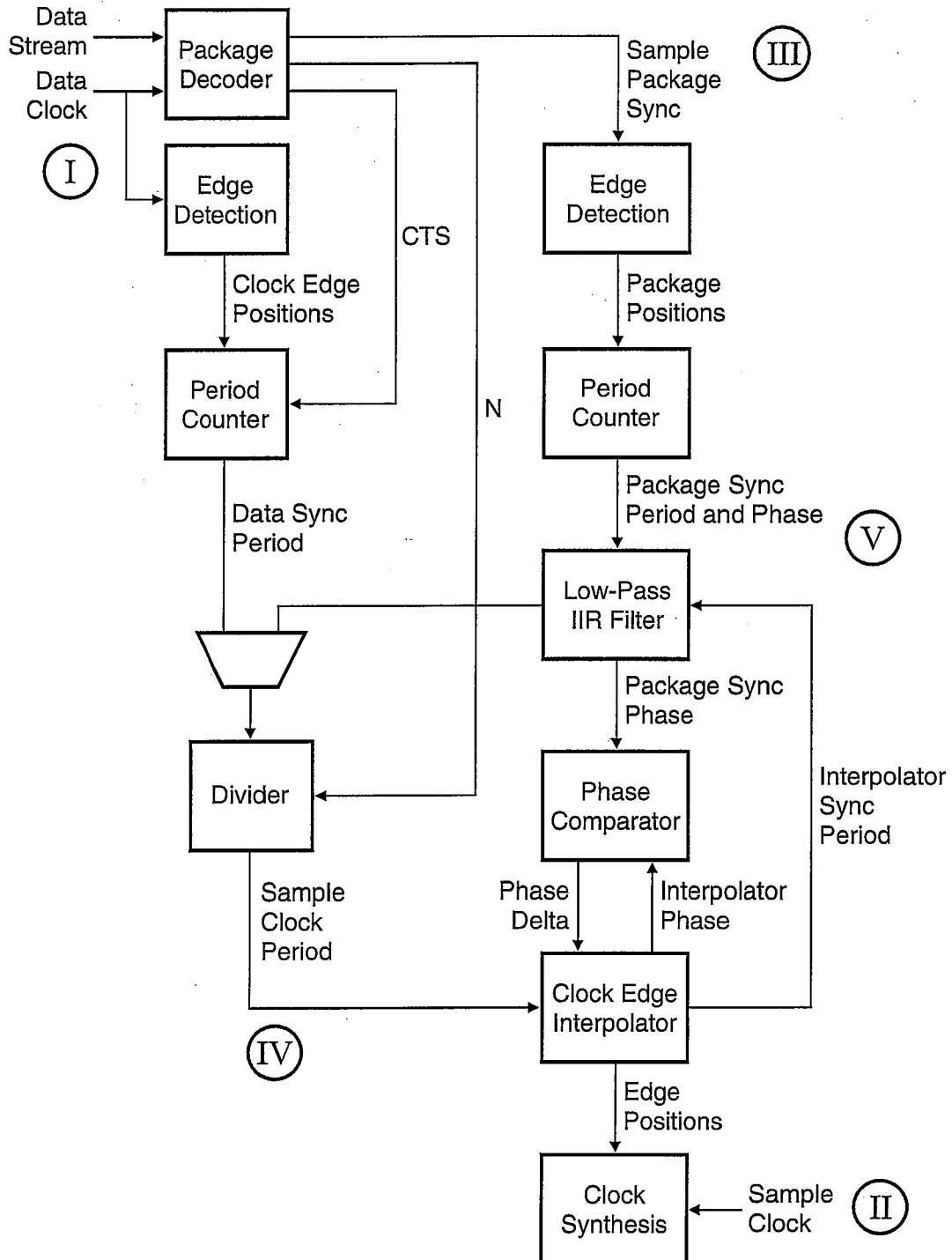


FIG. 1

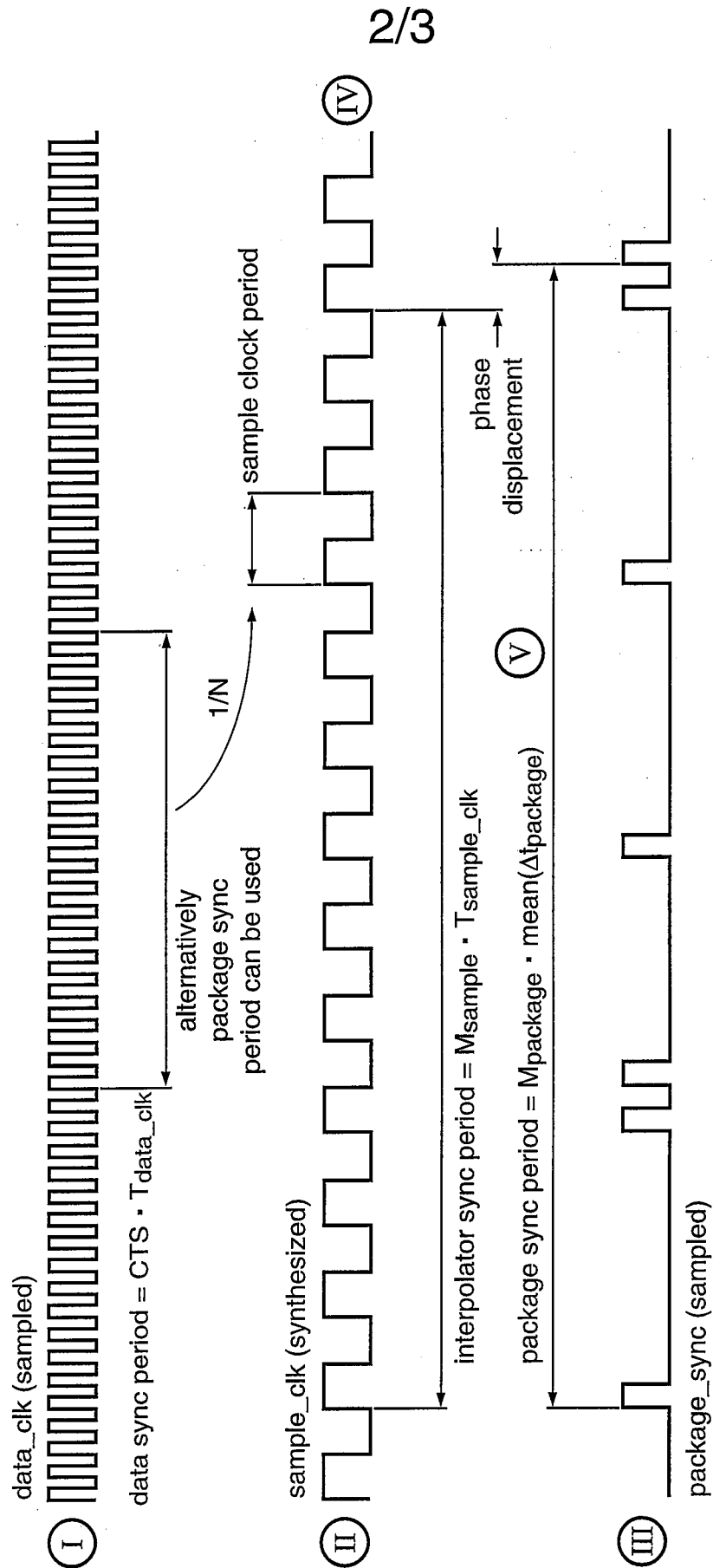


FIG. 2

3/3

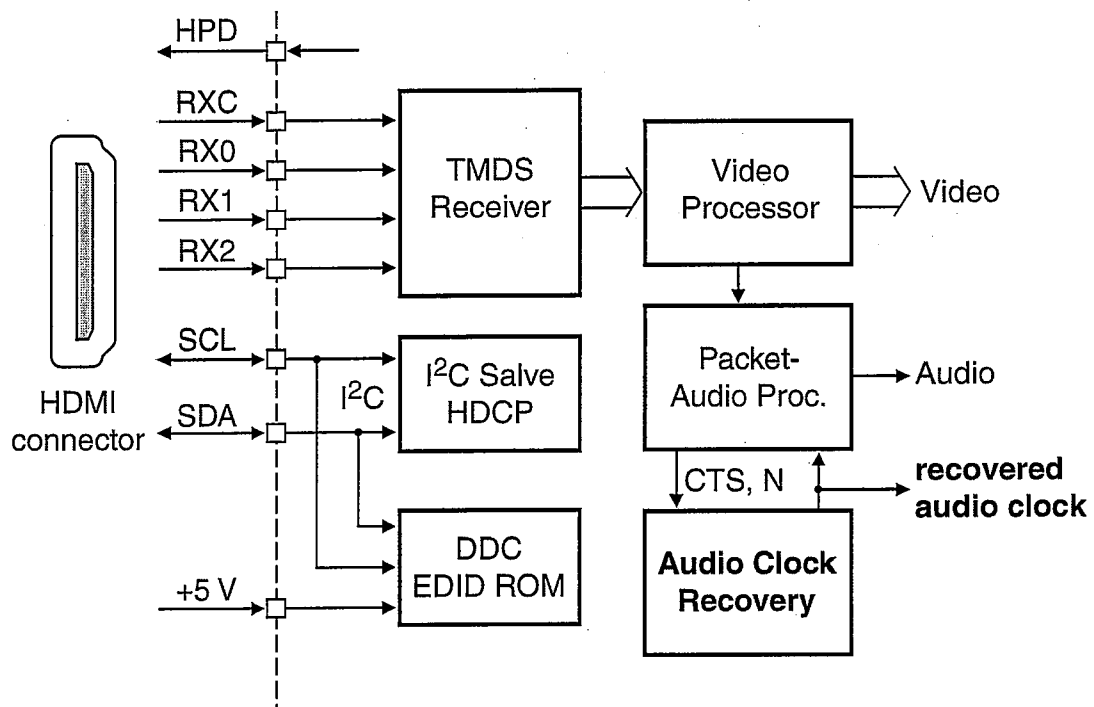


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051876

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L7/08 H03L7/081
ADD. H04J3/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H03L H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 1 294 116 A (NORTEL NETWORKS LTD [CA]) 19 March 2003 (2003-03-19) paragraph [0015] paragraph [0051] - paragraph [0052] figures 1,3,9a,9b,10	1-50
Y	US 2005/200393 A1 (FURTNER WOLFGANG [DE]) 15 September 2005 (2005-09-15) cited in the application paragraph [0124] - paragraph [0131] paragraph [0137] - paragraph [0138] figures 13-15,18	1-50
A	US 2007/005163 A1 (TAKAHASHI SATOSHI [JP] ET AL) 4 January 2007 (2007-01-04) paragraph [0036] - paragraph [0038] paragraph [0047] paragraph [0055]; figures 1,2,4	1-50
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

29 September 2008

Date of mailing of the international search report

07/10/2008

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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