Sept. 6, 1966 H. E. PETERSEN ET AL 3,271,744

HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

Filed Dec. 31, 1962 11 Sheets-Sheet 1

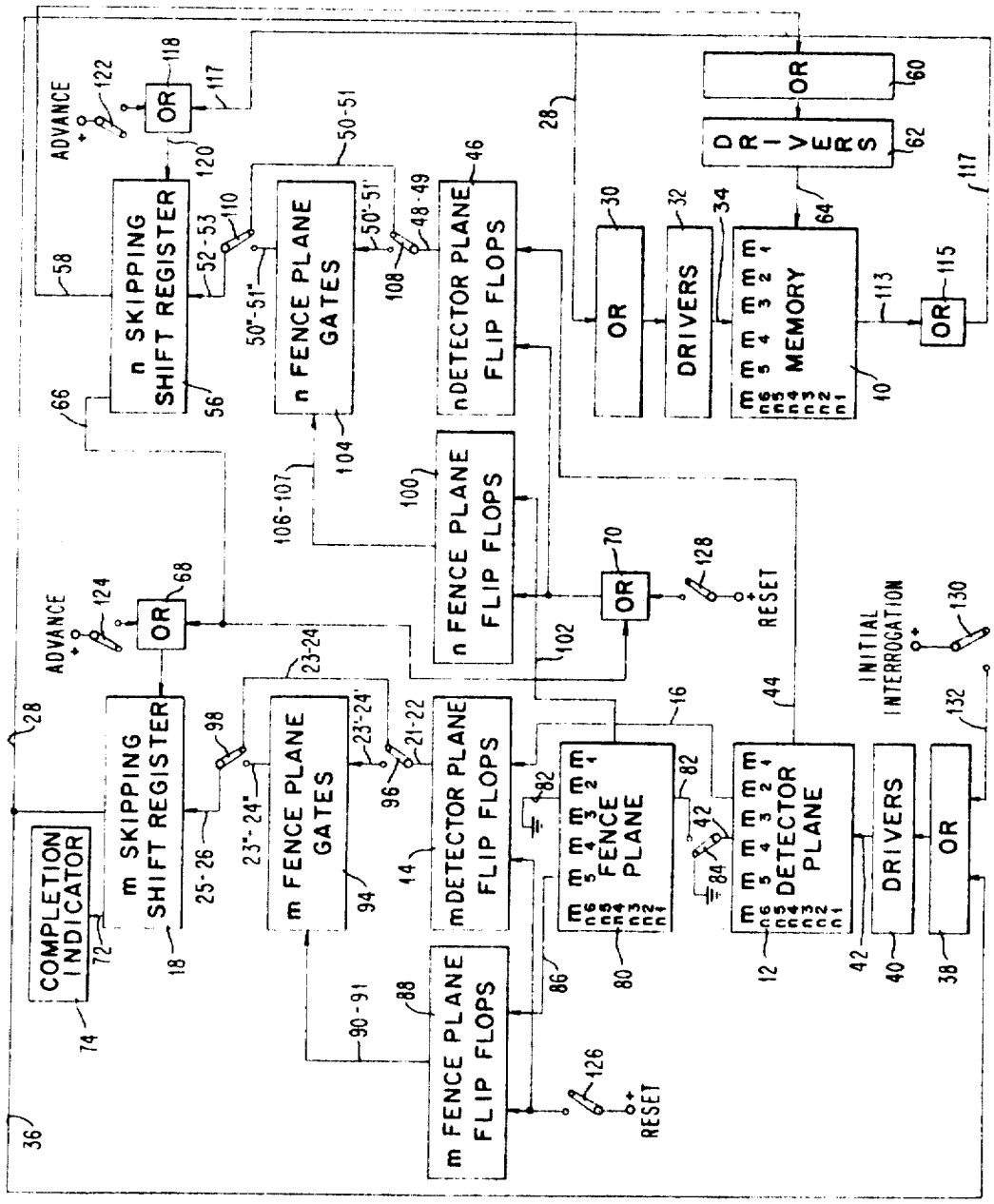
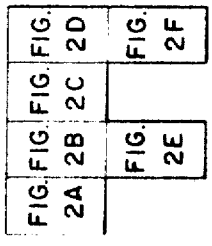


FIG. 1

FIG. 2



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HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

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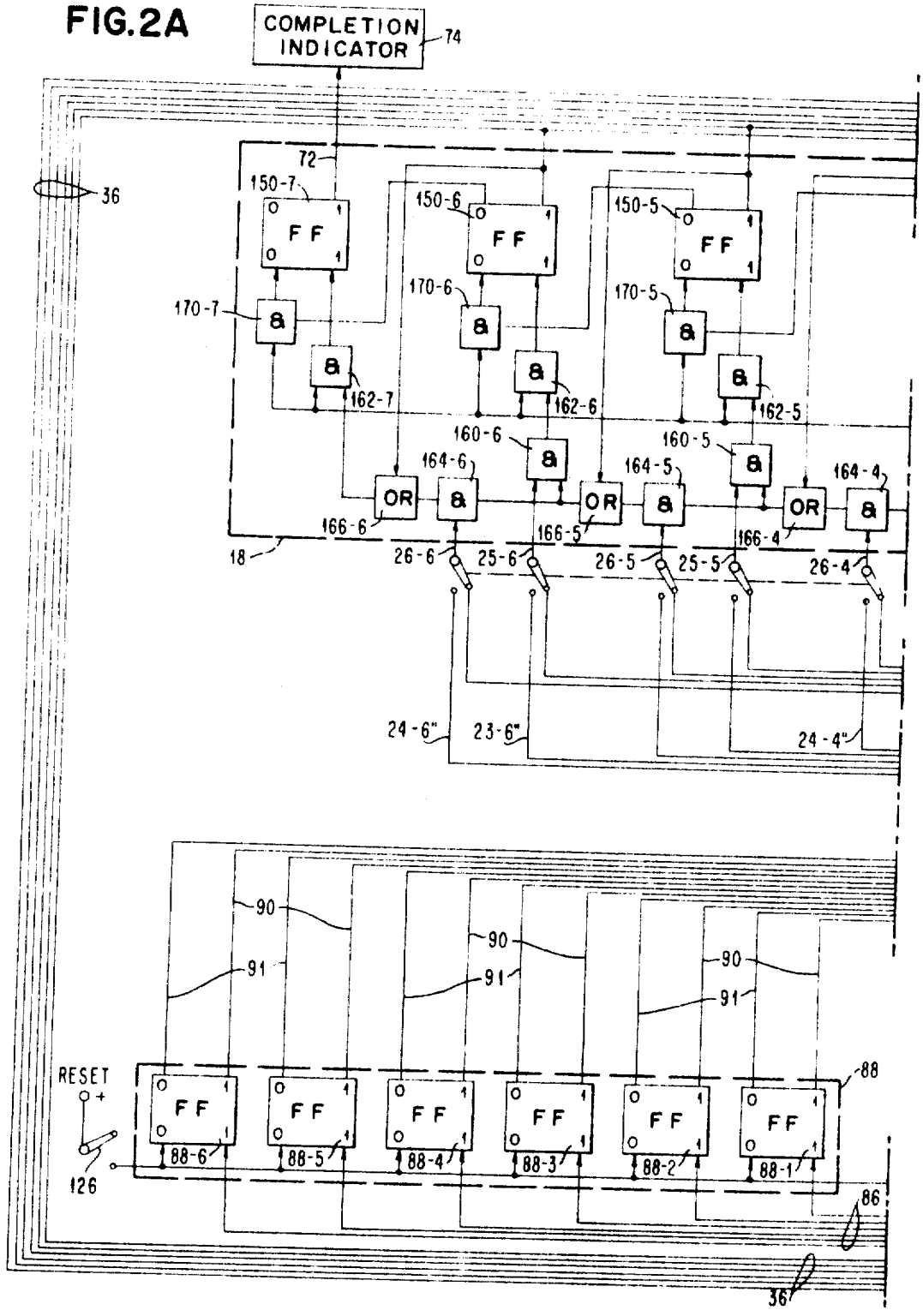
FIG.2A



HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

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FIG.2B

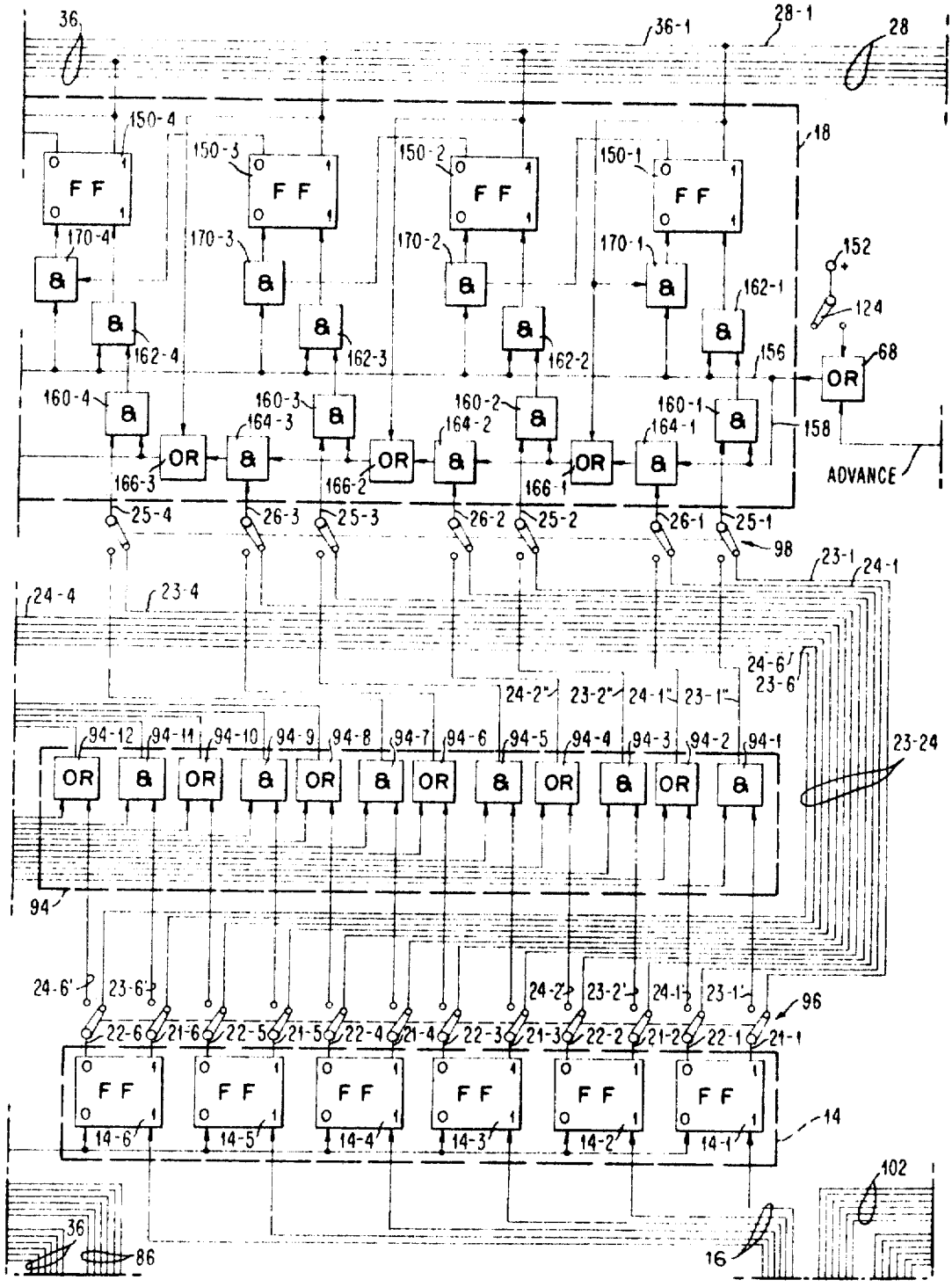
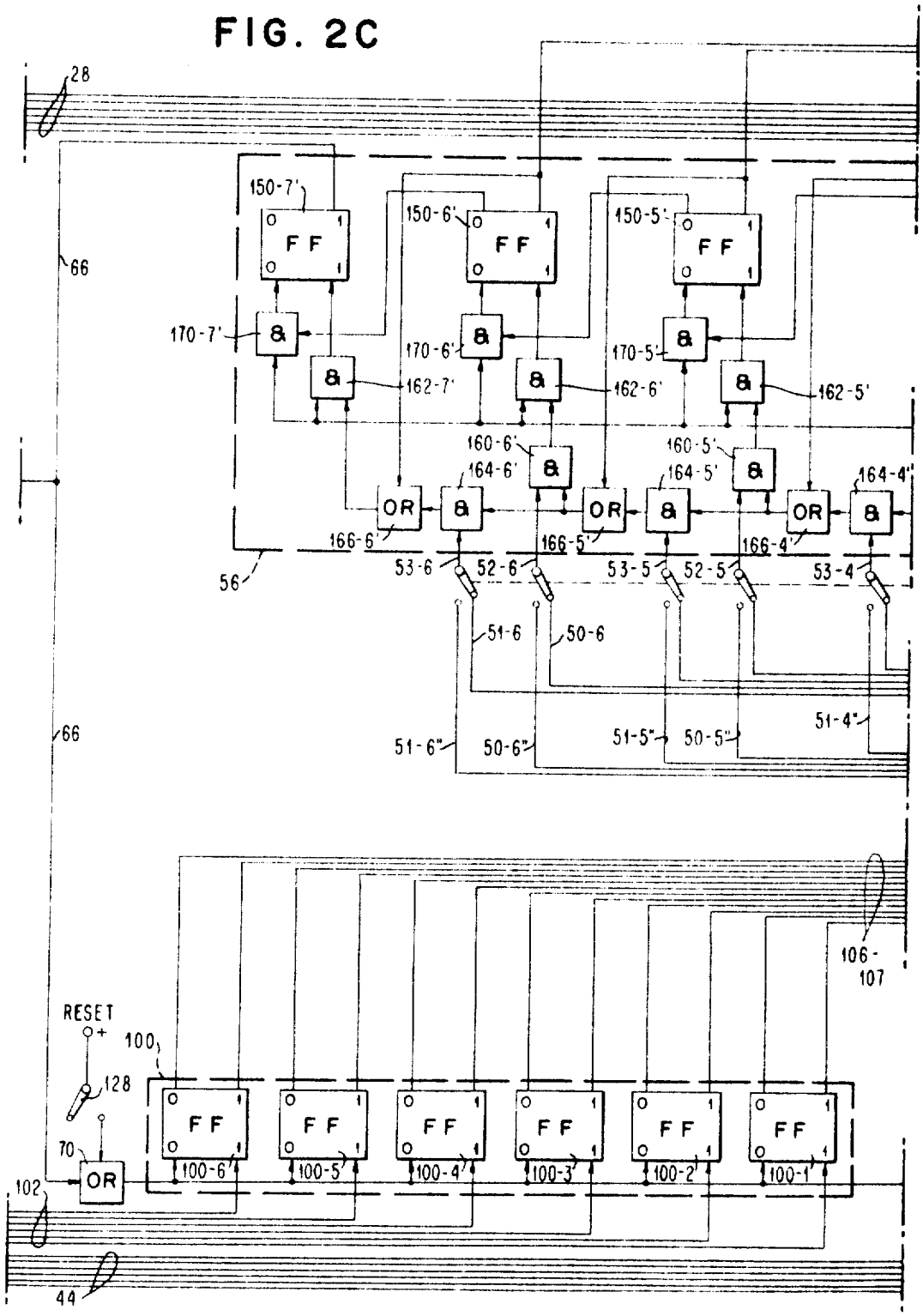


FIG. 2C


28
66
150-7'
150-6'
150-5'
F F
170-7'
170-6'
170-5'
&
162-7'
162-6'
162-5'
160-6'
160-5'
164-6'
164-5'
164-4'
OR
166-6'
166-5'
166-4'
56
53-6
52-6
53-5
52-5
53-4
51-6
50-6
51-6"
50-6"
51-5"
50-5"
51-4"
66
106-
107
RESET
+
100
128
70
OR
102
100-6'
100-5'
100-4'
100-3'
100-2'
100-1'
44

HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

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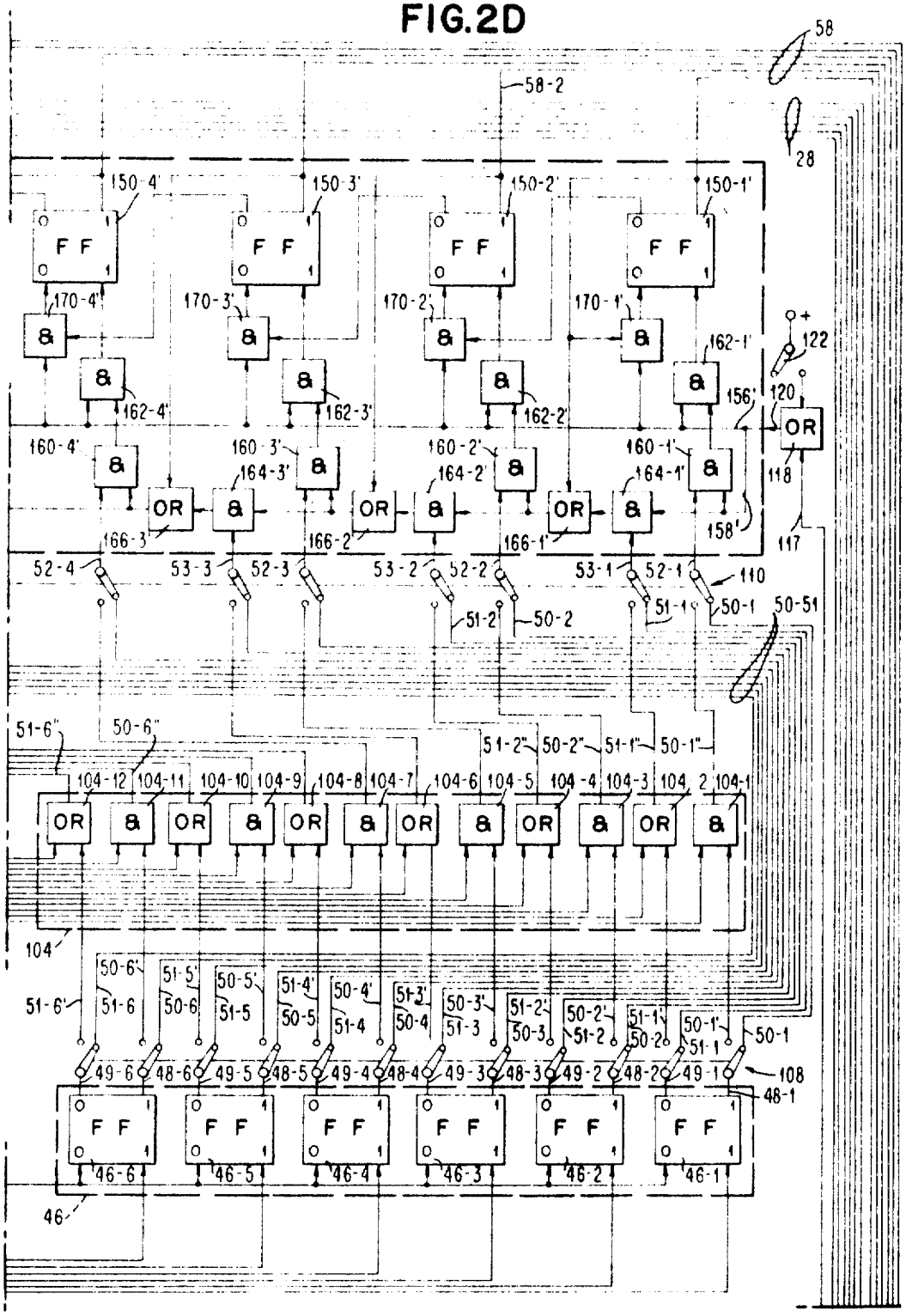
FIG.2D



HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

Filed Dec. 31, 1962 11 Sheets-Sheet 6

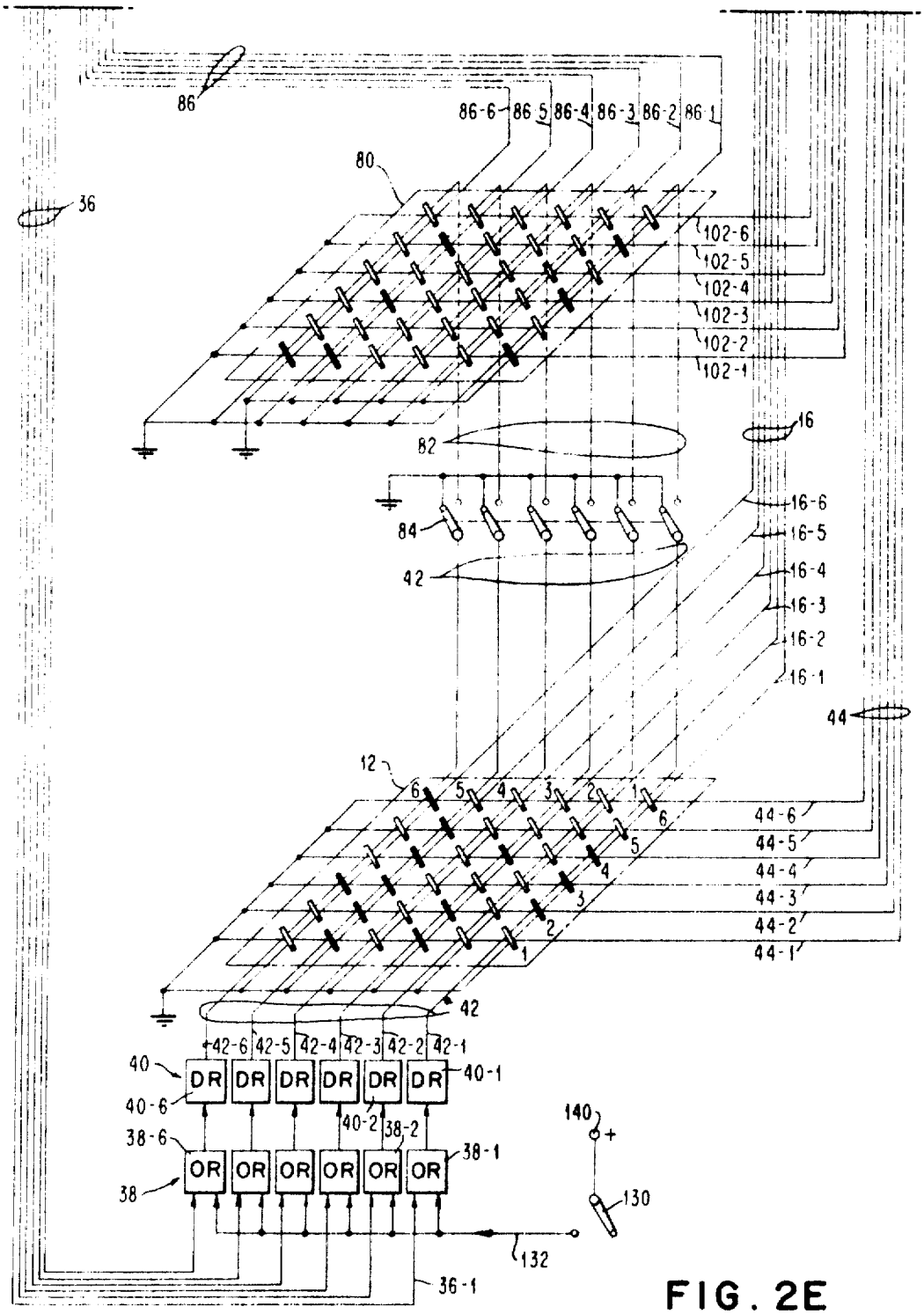


FIG. 2E

FIG. 2F

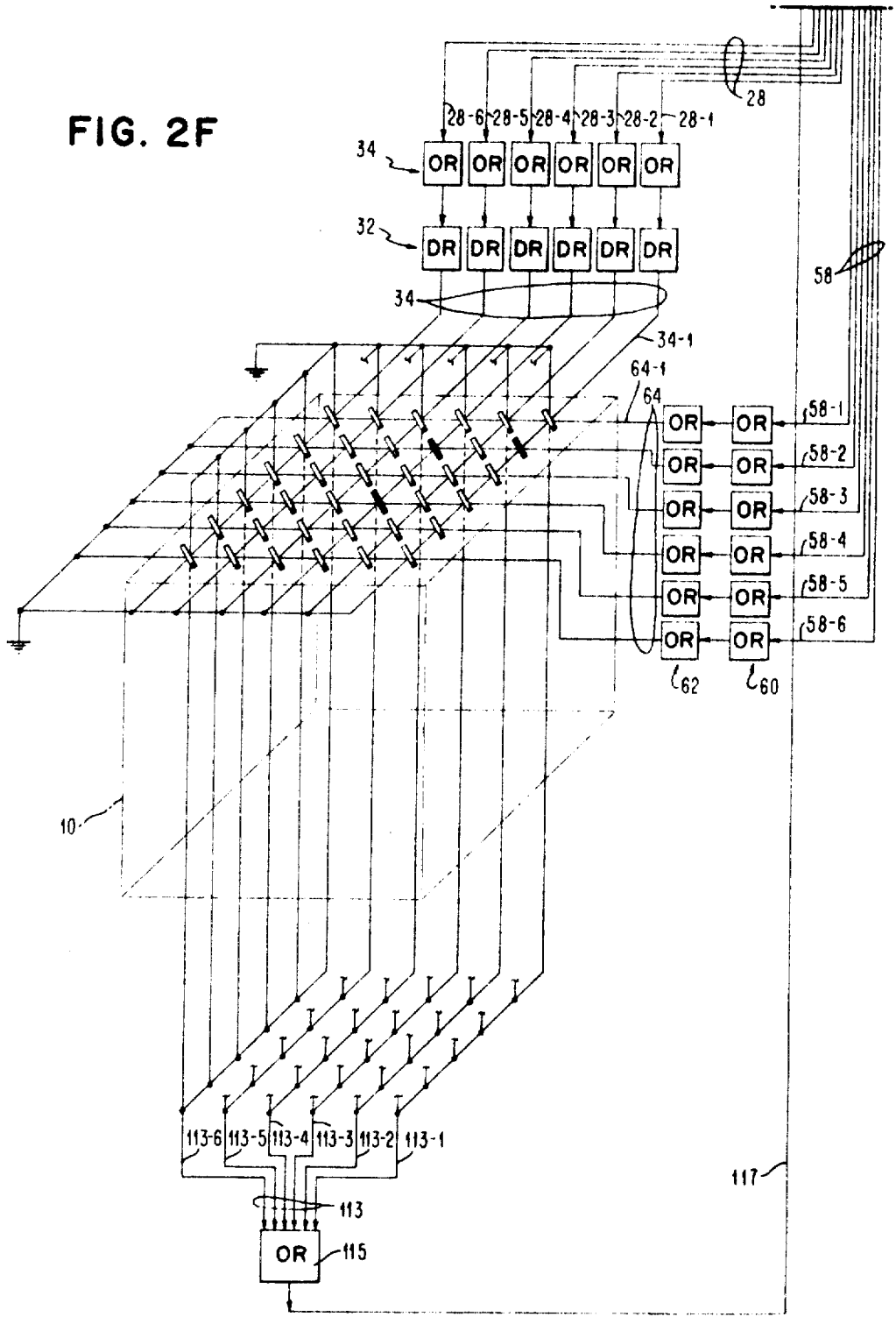
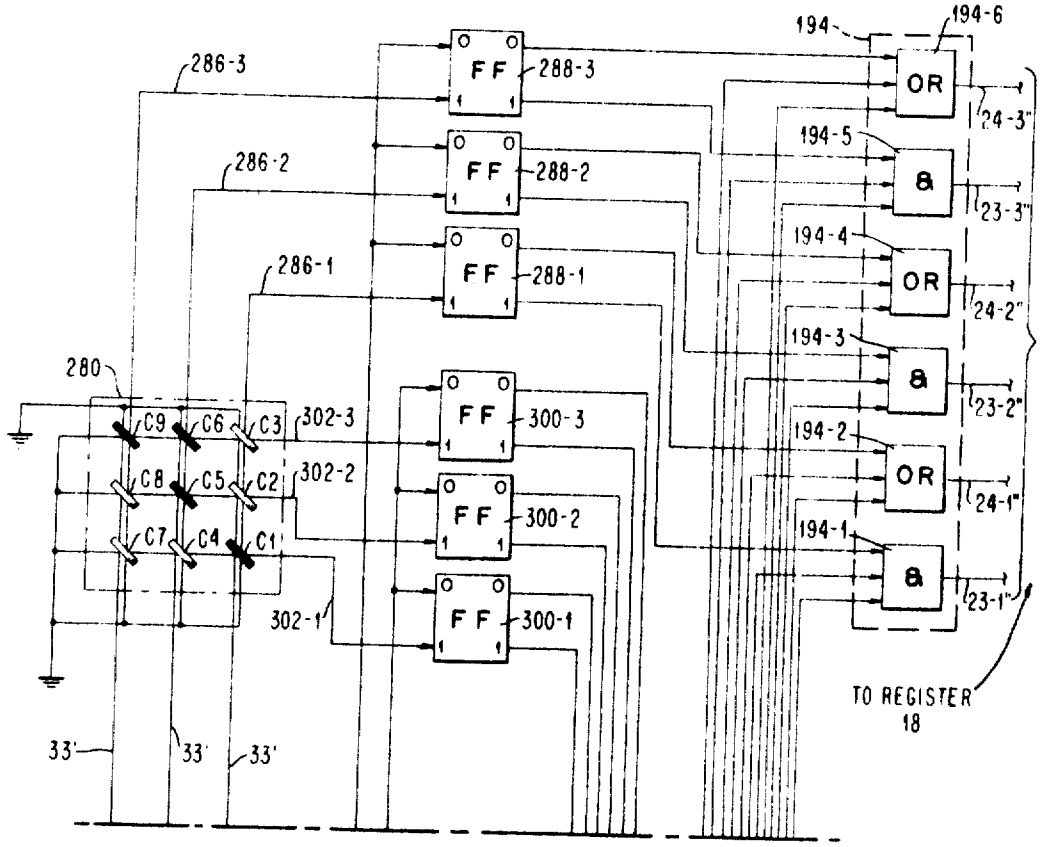

28
28-6
28-5
28-4
28-3
28-2
28-1
34
OR
32
DR
58
34
34-1
64-1
64
58-1
58-2
58-3
58-4
58-5
58-6
62
60
10
113-6
113-5
113-4
113-3
113-2
113-1
117
113
115

FIG.3


FIG. 3A
FIG. 3B

FIG.3A


194
194-6
286-3
FF
288-3
OR
24-3"
194-5
286-2
FF
288-2
&
23-3"
194-4
286-1
FF
288-1
OR
24-2"
194-3
280
FF
300-3
&
23-2"
194-2
C9
C6
C3
302-3
C8
C5
C2
302-2
FF
300-2
OR
24-1"
194-1
C7
C4
C1
302-1
FF
300-1
&
23-1"
TO REGISTER 18
33'
33'
33'

HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

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FIG. 3B

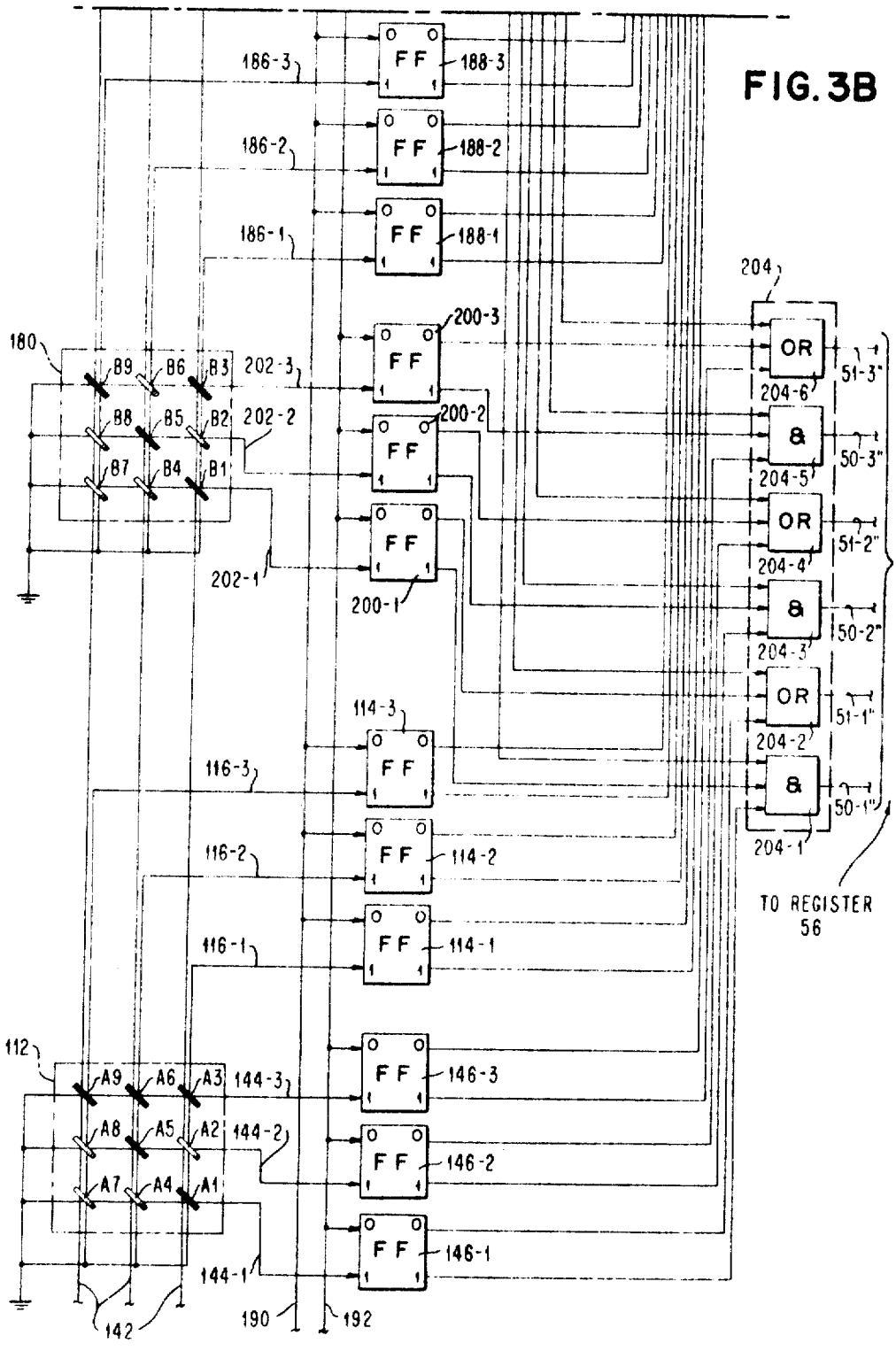


FIG.4

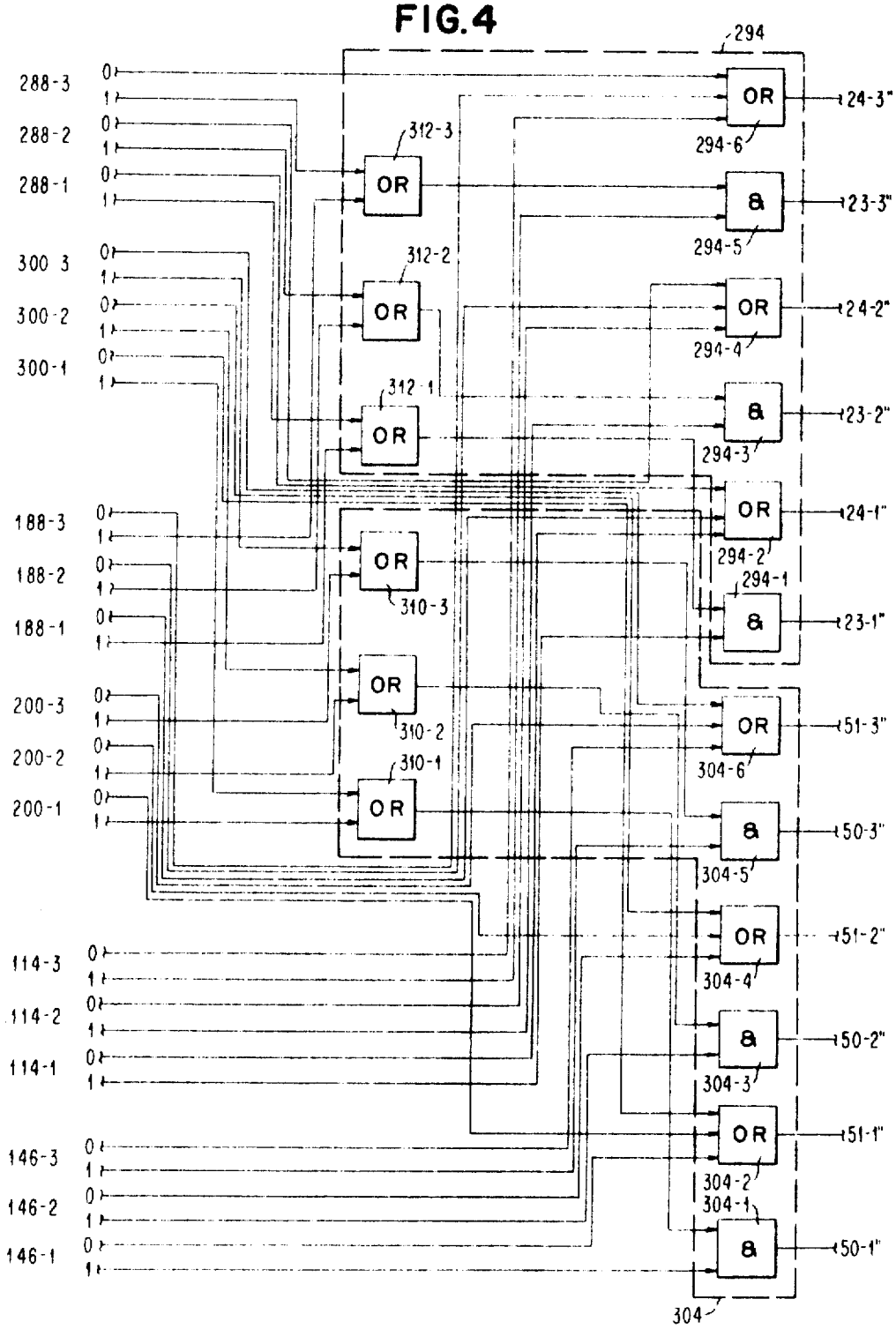
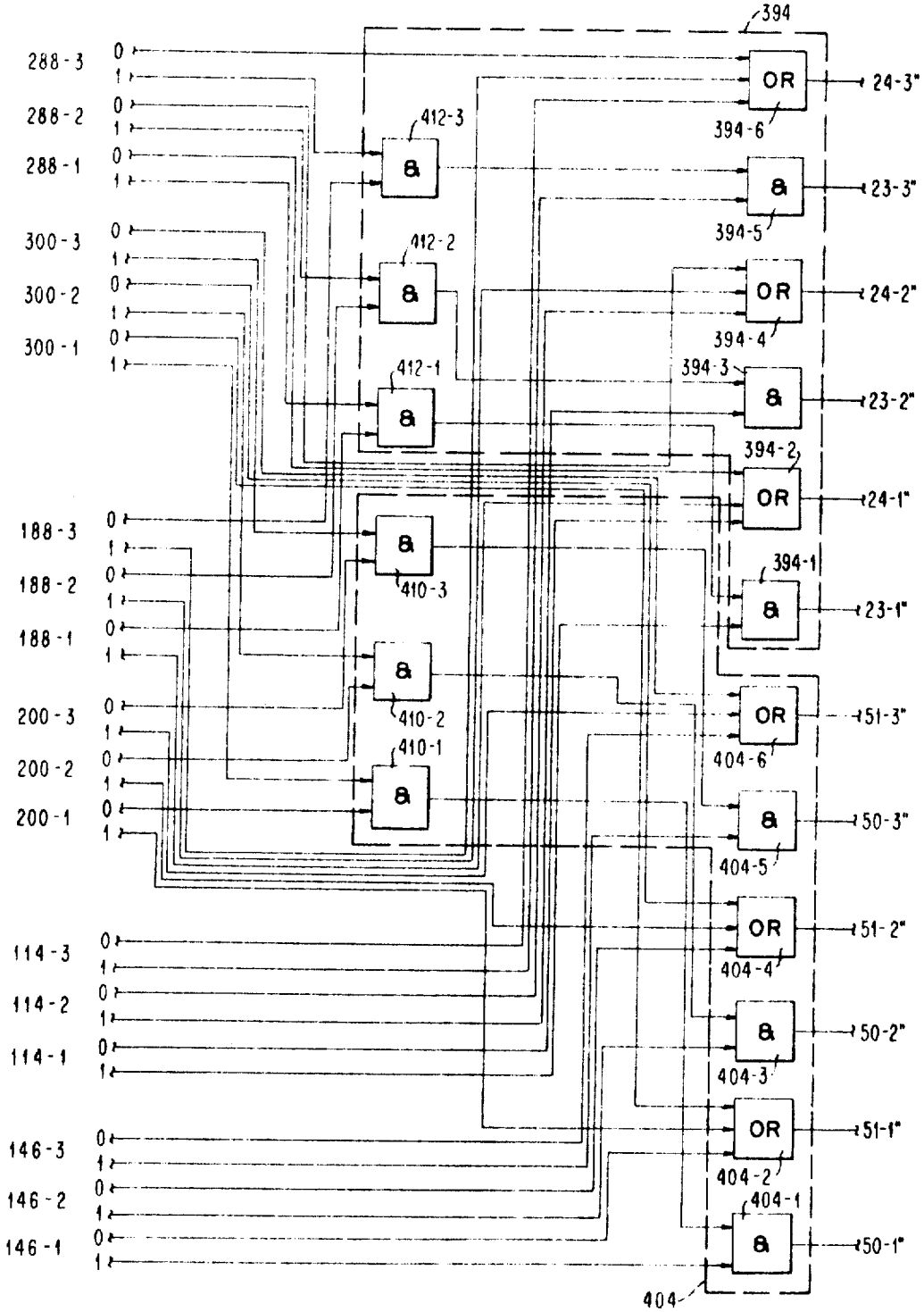

294
288-3
288-2
288-1
300 3
300-2
300-1
188-3
188-2
188-1
200-3
200-2
200-1
114-3
114-2
114-1
146-3
146-2
146-1
312-3
312-2
312-1
310-3
310-2
310-1
OR
&
294-6
294-5
294-4
294-3
294-2
294-1
304-6
304-5
304-4
304-3
304-2
304-1
304
24-3"
23-3"
24-2"
23-2"
24-1"
23-1"
51-3"
50-3"
51-2"
50-2"
51-1"
50-1"

FIG.5


394
288-3
288-2
288-1
300-3
300-2
300-1
188-3
188-2
188-1
200-3
200-2
200-1
114-3
114-2
114-1
146-3
146-2
146-1
412-3
412-2
412-1
410-3
410-2
410-1
OR
&
394-6
394-5
394-4
394-3
394-2
394-1
404-6
404-5
404-4
404-3
404-2
404-1
24-3"
23-3"
24-2"
23-2"
24-1"
23-1"
51-3"
50-3"
51-2"
50-2"
51-1"
50-1"
404

United States Patent Office 3,271,744
Patented Sept. 6, 1966

3,271,744

HANDLING OF MULTIPLE MATCHES AND FENCING IN MEMORIES

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Filed Dec. 31, 1962, Ser. No. 248,595
15 Claims. (Cl. 340—172.5)

The present invention relates to a data memory and more particularly to means for reading multiple matches of information out of such a memory and means for suppressing or fencing off certain predetermined portions of the memory during a read out operation.

While the principles of this invention may be applied to other types of memories, it would be particularly useful with an associative memory system. An associative memory system may be described generally as a system including word memory and means for simultaneously interrogating all words of the memory in accordance with selected data requirements. When this interrogation or association indicates that the interrogated portion of one or more words in the memory matches the selected data requirements, it is usually desired to extract the entire matching word or parts thereof from memory. A usual mode of operation is to interrogate a multiple word memory in accordance with association data and to register an indication of those words which match the association data. Thereafter, the matching words or portions thereof are read out to utilization circuits. Generally the words are read out serially by word and either serially or parallel by bit.

One aspect of the present invention is directed toward reading multiple matching words serially by word out of memory after the match indication has been recorded in a match indicating register.

A copending application Serial No. 120,213, filed June 28, 1961, and assigned to the assignee of the present invention discloses circuitry for use in connection with an associative memory wherein multiple matches of data in a single column of memory are recorded and are sequentially read out. The present invention provides for the interrogation and read out of an *mxn* word memory matrix with selective suppression or fencing out of predetermined portions of the memory.

It is a primary object of the present invention to provide improved memory read out apparatus.

It is another object of this invention to provide apparatus for sequentially reading out of memory selected words in accordance with the setting of storage elements in a detector plane corresponding to addresses in memory of the words which are to be read out.

Another object of this invention is to provide apparatus for reading from a memory selected words and for fencing out or suppressing selected areas of the memory from which words are not to be read.

A further object of this invention is to provide apparatus for reading from memory selected words and for fencing out or suppressing selected areas of the memory from which words are not to be read out by storing the fencing data in one or more fence planes.

It is a feature of this invention that certain portions of the memory may be isolated or fenced to exclude from read out any matching word that falls outside the fenced area. In addition to the foregoing mode of operation, the fencing feature may be used in other ways. For

example, the memory may store a large number of names and addresses, for example, the names and addresses of the subscribers to a large number of publications. A fencing plane may be used to store the memory addresses of those subscribers to a particular publication. It may then be desirable, using two subscription lists (that is fencing planes) and to manipulate these planes in various ways. The memory may be interrogated in accordance with one subscription list and thereafter the subscribers to the first list may be checked against the subscribers in a second list to determine which ones were duplicated on both lists. The first list may be checked for the presence of names on one or more additional lists; for the presence on one additional list but not on a third list; or for the presence on either one of two additional lists.

Another feature of this invention is logical combination of the data in the detector plane and the fence planes may be accomplished whereby the read out of a word of memory may be dependent selectively upon the presence of corresponding stored indications in the detector plane and in all fence planes, or in at least one fence plane, or in only one fence plane.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

In the drawings:

FIGURE 1 is a block schematic of the entire system.

FIGURE 2 shows the arrangement of FIGURES 2A through 2F which form a composite circuit schematic of the system.

FIGURE 3 shows the arrangement of FIGURES 3A and 3B which form a partial schematic diagram.

FIGURE 4 shows another partial schematic diagram.

FIGURE 5 shows a partial schematic diagram of another embodiment.

In general, the system comprises a memory having a detector plane, at least one fence plane and two shift registers. The memory is first interrogated in accordance with a given criteria and the addresses of words matching the interrogation criteria are stored in the detector plane. The multiple columns of the detector plane are then interrogated in parallel and a column shift register is set in accordance with the columns storing addresses. At the same time the row shift register is set in accordance with the rows containing data. The row shift register is reset and the columns are thereafter interrogated sequentially. The first column is interrogated and row registers corresponding to addresses in the first column only are set. The row registers are interrogated and corresponding words in memory are read out. After read out of the first column, the second column is interrogated and again row registers are set. The reading out column-by-column is continued until all columns have been read out at which time a completion-of-read-out indicator is actuated.

One or more fence planes may be provided for use in connection with the detector plane. The fence planes may be set to suppress the read out of given areas of the memory even though the detector plane indicates the presence of data therein which corresponds to the interrogation criteria.

Referring to FIGURE 1, a block schematic of the system is illustrated. The *nxm* word memory **10** may be, for example, a magnetic core memory consisting of 36

tiple bit words where the words are arranged in a 6 array. In this case $n=6$ and $m=6$. An nxm ctor plane **12**, which may be physically a part of the ıory **10**, records multiple match indications received esponse to an interrogation of the memory **10** or in other suitable manner. The plane **12** has six ver- columns m and six horizontal rows n. An m de- ɔr plane flip-flop (FF) unit **14**, connected by a group nes **16**, registers the m columns of detector plane **12** in :h data are recorded.

n m skipping shift register **18**, connected by lines **21–23–24**, **25–26**, is associated with the FF unit **14** to trol sequential interrogation of the m columns. The ɔuts of the m register **18** are applied through a plu- ty of lines **28**, OR gates **30** and drivers **32** to coin- nt selection lines **34** of memory **10** to effect, in coop- ion with signals on other coincidence lines, the read- out of words. The outputs of m register **18** also are lied over lines **36**, OR gates **38** and drivers **40** to lines lo effect sequential interrogation of the detector plane

The detector plane **12** also is connected by a group of s **44** to an n detector plane flip-flop (FF) unit **46**. s group of flip-flops is connected by lines **48–49**, **50–52–53** to an n skipping shift register **56**. The outputs ı register **56** are applied over lines **58**, OR gates **60** and ers **62** to coincident selection lines **64** to cooperate h outputs on coincidence lines **34** to read out words m the memory **10**. Coincidence of a signal on a line and a line **34** is effective to read out a word located he intersection of the two lines.

Another output from the n register **56**, over line **66**, is olied in parallel to OR gates **68** and **70**. The outputs OR gates **68** and **70** respectively are effective to start errogation of the next m column of plane **12** which ıtains a set core and to reset FF unit **46**. Upon com- tion of the read out of all words indicated in the detec- plane **12**, an output from n register **18** is applied over ine **72** to actuate a completion indicator device **74**.

An nxm fencing plane **80**, similar to detector plane **12**, ɔrovided into which fencing data are entered, by means l shown, to fence off portions, rows and/or columns, the detector plane **12** which are to be ignored during given read out operation. The fence plane **80** is linked the lines **82** which are extensions, through switches , of the lines **42**. The fence plane **80** is connected by a ɔup of lines **86** to an m fence plane flip-flop (FF) unit , which is identical to FF unit **14**. The FF unit **88** is nnected by lines **90–91** to an m fence plane gate unit **94**, ferred to hereinafter as m gates **94**. It is noted that oups of gang switches **96** and **98** may be set selectively the lines **23–24**, or lines **23'–24'** to respectively exclude include m gates **94** in the circuit between FF unit **14** d m register **18**.

An n fence plane flip-flop (FF) unit **100** is connected the fence plane **80** by a group of lines **102**. The FF it **100** is identical to FF unit **88**. The unit **100** is con- cted to an n fence plane gate unit **104** by lines **106–7**. The n gates **104** are identical to the m gates **94**. ıe n gates **104** may be included selectively in the lines 1–51 or **50'–51'** between FF unit **46** and n register **56** ' groups of switches **108** and **110**.

Each time a word is read out of memory **10**, a signal applied over a line **113** to an OR gate **115** and over a ıe **117** to an OR gate **118**. The output of OR gate **118** applied over a line **120** to advance the n register **56**. second input to the OR gate **118** is by means of a vitch **122** which may be operated manually or otherwise apply an advance pulse to n register **56**. Similarly, a vitch **124** is provided to apply an advance pulse through R gate **68** to the m register **18**. A pair of switches **126** ıd **128** are provided for resetting the FF units **88**, **14**, **00** and **46**, the reset pulse to FF **100** and FF **46** being ɔplied through OR gate **70**. A switch **130** is provided

for applying an initial interrogation pulse in parallel through a line **132** to all OR gates **38**.

Hereinafter and in the claims, the detector plane **12**, fence plane **80**, as well as the various fence plane and detector plane gate and flip-flop units may also be referred to as registers.

Referring to FIGS. 2A through 2F, a preferred embodiment of the system schematically illustrated in FIG. 1 is shown. FIG. 2 shows the arrangement of FIGS. 2A through 2F to form a composite schematic.

While the embodiment shown in FIGS. 2A through 2F has values of $n=6$ and $m=6$ and is illustrated as comprising a core memory, it will be understood that this is merely illustrative. Normally much larger memories will be utilized and various changes, including the substitution of other types of memories may be made without departing from the scope of the invention.

The system will be described first without use of the fence plane **80**. Therefore, switches **84** (FIG. 2E), **96**, **98** (FIG. 2B), **108** and **110** (FIG. 2D) are set to the positions shown.

Initially, the memory **10** is interrogated in accordance with usual associative memory techniques or, in some other way, the cores in plane **12** are set in accordance with the words which it is desired to read out. To start read out of the desired words from the memory **10**, the switches **126** and **128** (FIGS. 2A and 2C) are closed momentarily to reset FF units **88**, **14**, **100** and **46** to their 0 states.

The switch **130** (FIG. 2E) is closed momentarily to apply a signal from a power source represented by terminal **140** over the line **132**, where it is applied in parallel to a group of six OR gates **38**. The output of the OR gates are applied to a group of six drivers **40** which apply currents through six lines **42** linking the m columns of core plane **12**, through switches **84** to ground. For each core in the plane **12** which is in its set condition the current in the corresponding line **42** induces a current in the corresponding lines **16** and **44**. The cores of planes **12** and **80** are of the type which may be read out non-destructively. A suitable core is described in an article by V. L. Newhouse which is published in the "Proceedings of the IRE," November 1957, pages 1484–1492. A core is described wherein the application of magnetizing pulses much larger than the coercive force do not give rise to permanent changes of magnetization provided that that duration of the pulses is sufficiently short. Other suitable non-destructive read out memory elements are multi-aperture devices, or two-core per bit devices where the cores are destructively but independently read out, whereby a stored bit may be read out twice.

The currents in lines **16** are applied to flip-flops **14–1** through **14–6**, setting corresponding flip-flops to their 1 states. The currents applied to lines **44** are similarly applied to flip-flops **46–1** through **46–6**. For each flip-flop **14** which is set to its 1 state, an output is applied through corresponding lines **21**, **23** and **25** to the m register **18**. For each flip-flop **14** which is not set to its 1 state, an output is applied through corresponding lines **22–24** and **26** to the m register **18**. Thus, of each pair of line groups **21–23–25** or **22–24–26**, one will have a signal thereon whereas the other will not. Similarly, the 0 and 1 outputs of FF unit **46** are applied over lines **48**, **50**, **52** or **49**, **51**, **53** to the n register **56**.

Before proceeding with the description of the circuit, the n and m registers **18** and **56** will be described. Since registers **18** and **55** are identical, the description of one will suffice for both. The m register **18** includes seven flip-flops **150–1** through **150–7**. These flip-flops have their 0 and 1 inputs arranged at the bottom and their 0 and 1 outputs arranged at the top. Each flip-flop **150** is a conventional flip-flop which switches to its 1 state when a signal is applied to the 1 input and which, in the 1 state, provides an output from the 1 output terminal.

Similarly, a signal applied to the 0 input switches the flip-flop to its 0 state providing an output on the 0 output terminal. The flip-flops **150–1** through **150–6** correspond to the six *m* columns of cores in the plane **12** whereas FF **150–7** is responsive to an output from FF **150–6** to indicate that all six columns of the plane **12** have been interrogated.

It is not necessary to reset registers **18** and **56** to their 0 states since these registers will be set in accordance with the outputs of the planes **12** and **80**. The *m* register **18** is started by closing the switch **124** (FIG. 2B) to apply a pulse from the power source indicated by terminal **152** through the OR gate **68** to a line **154**. The line **154** branches into lines **156** and **158**. Depending upon the contents of the detector plane **12**, one or more of the lines **25** may have a signal thereon. The input on line **154** is effective to flip to its 1 state the first flip-flop **150** corresponding to the line **25** which has a signal thereon. If a signal is present on the first line **25–1**, the signal on line **158** gates that signal through an AND gate **160–1** and the same signal on line **156** gates the output of AND **160–1** through an AND gate **162–1** whereby it is applied to the 1 input of FF **150–1**.

If there is no signal on line **25–1**, then there must be a signal on a line **26–1** which is connected to the 0 terminal of the same flip-flop **14–1** that applies signals to line **25–1**. Therefore, the signal on line **158** is gated through AND gate **164–1**, through an OR gate **166–1** where it is applied to AND gate **160–2** to gate through a signal on the line **25–2** to AND gate **162–2** and to the 1 input terminal of FF **150–2**. If there is no signal on line **25–2**, there will be one on line **26–2** to gate the signal on line **158** through AND gate **164–2**. Thus, it is seen that a signal applied to the line **154** is applied through line **158**, AND gates **164** and OR gates **166** to the first AND gate **160** corresponding to a 1 input on a line **25**.

When flip-flop **150–1** is in its 1 state, its output is applied to an AND gate **170–1** and OR gate **166–1**. The 1 outputs of subsequent flip-flops **150** are applied to AND gates **170** corresponding to the next succeeding flip-flop.

The gates **170** effect the turning off of a flip-flop **150** when the next succeeding pulse is applied to the line **156**. After setting the first flip-flop **150** by the pulse from line **154** the next succeeding AND gate **160** is conditioned through the OR gate **166** corresponding to the flip-flop **150** which is in its 1 state. Thus, subsequent pulses on line **158** are superfluous whereas the same pulses on line **156** are effective to turn off the flip-flop **150** which is on and to turn on the next conditioned flip-flop **150**.

The output from an actuated flip-flop **150–1** through **150–6** is applied to corresponding lines **28** and **36**. During operation, successive advance signals applied to the line **66** by *n* register **56** and through OR gate **68** to the line **154** successively advance the *m* register **18** until the last *m* column containing a set core is read out. The next advance pulse on line **154** then switches the flip-flop **150–7** to its 1 state, applying an output signal on line **72** to actuate the completion indicator device **74** to indicate completion of the read out. This device **74** may be a bell, light, relay, switch, etc.

The *n* register **56** operates in an identical manner, the corresponding components being designated similarly to those in unit **18**; however, those in **56** contain a prime reference.

To continue with the system description, assume that only those cores which are shown as solid black in *m* columns **1**, **3**, **5** and **6** and in *n* rows **1**, **2**, **3**, **4**, **5** and **6** of core plane **12** (FIG. 2E) are set to indiate words which are to be read out of memory **10**. The switch **130** (FIG. 2E) is closed momentarily and currents on the lines **42** induce output pulses on lines **16–1**, **16–3**, **16–5**, **16–6**, **44–1**, **44–2**, **44–3**, **44–4**, **44–5** and **44–6**. Accordingly, flip-flops **14–1**, **14–3**, **14–5**, **14–6**, **46–1**, **46–2**, **46–3**, **46–4**, **46–5** and **46–6** are set to their 1 states and signals are applied to *m* register **18** through lines **25–1**, **25–3**, **25–5**, **25–6**, **26–2** and **26–4**, and to *n* register **56** through lines **52–1**, **52–2**, **52–4**, **52–5** and **52–6**.

The switch **214** (FIG. 2B) is closed momentarily and the resulting signal on line **158** gates the signal on line **25–1** through AND gate **160–1**; the signal on line **156** gates the output of AND **160–1** through AND **162–1** to the 1 input terminal of FF **150–1**, setting this flip-flop to its 1 state and applying a signal to the corresponding lines **28–1** and **36–1** and to AND gate **170–1** and OR gate **166–1**. The switch **122** (FIG. 2D) is not closed at this time and therefore no signals are applied to the lines **58**. With a signal on line **34–1** (FIG. 2F) but not on any line **64** (FIG. 2F), read out of information from memory **10** is not affected.

Next, the switch **128** (FIG. 2C) is closed momentarily to reset FF unit **46**. The signal on line **36–1** is applied to OR gate **38–1** and, through driver **40–1**, applies a pulse to line **42–1**. The signal on line **42–1** is effective through the set core at the intersections of lines **44–2**, **44–3** and **44–4** with line **16–1** to induce currents in the latter three lines **44**. The current in line **16–1** is superfluous since FF **14–1** was previously set to its 1 state and has not been reset. The currents in lines **44–2**, **44–3** and **44–4** are effective to set corresponding flip-flops **46–2**, **46–3** and **46–4** to their 1 states.

The output of FF **44–2** is applied over line **52–2** to AND gate **160–2'** in *n* register **56**. Switch **122** is closed momentarily to apply an advance signal through OR gate **118** and line **120**. The line **120** branches into lines **156'** and **158'**. Since there is no signal on line **52–1**, the signal on line **158'** advances, in the manner described hereinbefore, to gate the signal on line **52–2** through AND gate **160–2'** to AND gate **162–2'** where it is gated by the signal on line **156'** to the 1 input of FF **150–2'**, setting this flip-flop to its 1 state.

FF **150–1** in *m* register **18** and FF **150–2'** in *n* register **56** are now in their 1 states and are applying signals to corresponding lines **28–1** and **58–2**. Coincident currents on lines **34–1** and **64–2** (FIG. 2F) thus read out the word in memory **10** at the address defined by the intersection of these lines. The read out pulse is applied over line **113–1** to OR gate **115** and over line **117** to OR gate **118**.

The advance pulse from OR gate **118** to lines **156'** and **158'** sets FF **150–3'** to its 1 state and resets FF **150–2'** to its 0 state. The word at the intersection of lines **34–1** and **64–3** is read out. The resulting signal on line **112–1** advances *n* register **56** to set FF **150–4'** and resets FF **150–3'**. The corresponding word is read out of memory **10**.

Since no other flip-flops **46** are set to the 1 state, the advance pulse on lines **156'** and **158'** sets FF **150–7'** to its 1 state producing an output on line **66** which is applied to OR gates **68** and **70**. The output from OR gate **70** resets FF unit **46**. The output of OR gate **68** is applied to the lines **156** and **158** to switch to its 1 state the next flip-flop **150** associated with a flip-flop **14** which is in its 1 state.

In the present example the next flip-flop **14** which has been set to its 1 state is FF **14–3**. Therefore, an output is applied to the line **36–3**, through OR gate **38–3** and driver **40–3** to line **42–3** to induce outputs on lines **44–1** **44–2** and **44–4**, setting flip-flops **46–1**, **46–2** and **46–4** to their 1 states. Current also is induced in line **16–3** but is superfluous since FF **14–3** is aready in its 1 state.

The switch **122** (FIG. 2D) is closed momentarily to apply an advance pulse through OR gate **118** to *n* register **56**. This pulse sets FF **150–1'** to its 1 state. At this time coincidence of pulses on lines **34–3** and **64–1** effects read out of the word in memory at the corresponding address. The resultant output on line **113–3** to OR gate **115** is applied through OR gate **118** to switch FF **150–1'** to its 0 state and to switch FF **150–2'** to its 1 state. At this time a coincidence of pulses on lines **34–3** and

4–2 effects the read out of the word in memory **10** at ıe corresponding address. The *n* register **56** is advanced › turn on FF **150–4'** causing the corresponding word › be read out. Since no more flip-flops **46** are in the 1 ate, the resulting output pulse form OR gate **115** is fed ack to turn FF **150–7'** on, to again reset FF unit **46** and › advance *m* register **18**.

In the foregoing manner *m* columns **5** and **6** of plane **2** are interrogated sequentially, setting corresponding ip-flops **46**. Each time the flip-flops **46** are set, the vitch **122** is closed to start the sequential advancing of register **56** with the resultant read out of words in ıemory **10**.

When the last *m* column has been completely read out, ıe resulting output pulse from memory **10** is effective ırough register **56** and line **66** to advance *m* register **8** to turn FF **150–7** on which produces an output on ne **74** to completion indicator device **74** to indicate that ll words corresponding to cores set in the detector plane **2** have been read out.

Fencing operation

Under special conditions it may be desired to inhibit ıe read out of particular sections of the memory **10**, ven though the detector plane **12** contains match indica- ons in those inhibited areas. In such an event, the in- ibited area is fenced out whereby the interrogation auto- atically skips those areas.

Assume that it is desired to fence off columns **2**, **3** and and rows **2**, **4** and **6** of detector plane **12**. To accomplish iis fencing, at least one core is set in each of the unfenced olumns **1**, **5** and **6** and the unfenced rows **1**, **3**, and **5**, of nce plane **80**. Further, it is required that none of the ores in the fenced off rows and columns be set. Obvious- , the connections to the 0 to 1 inputs or from the 0 and 1 itputs of FF units **88** and **100** could be reversed where- / the set cores could be in the rows and columns which e to be fenced out.

Accordingly, the seven cores shown as solid in plane) are set. Assume also that cores are set in plane **12** in the foregoing example of multiple match read out. he switches **84**, **96**, **98**, **108** and **110** are set to their alter- ıte positions. Switches **126** and **128** are closed momen- rily to reset FF units **88**, **14**, **100** and **46**. The switch **30** is closed momentarily to provide interrogation of l columns of plane **12**, and as in the prior example, out- ıt signals are derived on lines **16–1**, **16–3**, **16–5**, **16–6**, **1**, **44–2**, **44–3**, **44–4**, **44–5** and **44–6**, setting cor- sponding flip-flops **14** and **46** to their 1 states. The sig- ıls on lines **42** flow through the switches **84**, lines **82** ıd the associated columns of fence plane **80**. The cur- ınts flowing through fence plane **80** induce currents in ıes **86–1**, **86–5**, **86–6**, **102–1**, **102–3** and **102–5**.

Accordingly, flip-flops **88–1**, **88–5**, **88–6**, **100–1**, **100–3** ıd **100–5** are set to their 1 states. Referring now to gate ıit **94** (FIG. 2B), the odd number gates **94–1**, **94–3**, **1–5**, etc. are AND gates. The even-numbered gates **1–2**, **94–4**, **94–6**, etc. or OR gates. The AND gates **94** e connected to the 1 outputs of flip-flops **88** and **14** hereas the OR gates **94** are connected to the 0 outputs flip-flops **88** and **14**. Similarly, in gate unit **104**, the ld-numbered AND gates **104** are connected to the 1 ıtputs of the flip-flops **100** and **46** whereas the even- ımbered OR gates **104** are connected to the 0 outputs flip-flops **100** and **46**.

FF **14–1** is set to its 1 state and therefore applies an put to AND gate **94–1**. FF **88–1** is set to its 1 state ıd therefore applies a second input to AND gate **94–1** gate through the signal from FF **14–1** and thus set e FF **150–1** to its 1 state when the advance signal is ıplied by closing switch **124**. At this point the effect the currents on lines **44** and **102** is unimportant since e FF units **100** and **46** will be reset to their 0 states by osing switch **128** (FIG. 2C). The output of FF **150–1** applied through line **36–1** to OR gate **38–1** and driver **40–1** to line **42–1**. Again outputs are derived on lines **16–1**, **86–1**, **44–2**, **44–3**, **44–4**, **102–1**, **102–3** and **102–5** to set corresponding flip-flops in units **100** and **46** to their 1 states. The units FF **88–1** and FF **14–1** were not reset.

The switch **122** is closed to apply an advance signal. Since FF **150–3'** which is the first flip-flop **150'** corresponding to flip-flops **100** and **46** both of which are in their 1 states, the signal on lines **156'** and **158'** advances to set FF **150–3'** in its 1 state. At this time, FF **150–1** is still set in its 1 state and coincidence of signals on lines **34–1** and **64–3** is effective to read the word out of memory **10** at the corresponding address. The resultant output on line **117** applies an advance pulse to *n* register **56**. The advance signal proceeds down the lines **156'** and **158'**, in *n* register **56**, seeking the next register position corresponding to flip-flops **100** and **46** both of which are set to their 1 states. In accordance with the stated example, there is no such coinicidence of flip-flops in their 1 states and the advance signal is propagated through AND gates **164'** and OR gates **166** to set flip-flop **150–7'** to its 1 state. An advance signal over line **66** resets FF units **100** and **46** and applies an advance signal to *m* register **18**.

The remaining flip-flops **14** which are set to their 1 states are FF **14–3**, **14–5** and **14–6**. The remaining flip-flops **88** which are set in their 1 states are FF **88–5** and **88–6**. As in the case of FF units **100** and **46**, there must be coincidence of 1 states in corresponding flip-flops **88** and **14** in order to have a corresponding flip-flop **150** set to its 1 state. Thus, FF **150–5** and **150–6** may be set to their 1 states. Therefore, the advance signal through OR gate **68** advances through *m* register **18** to set FF **150–5** in its 1 state, thus producing an output on lines **28–5** and **36–5**. The signal on line **36–5** is applied through OR gate **38–5** and driver **40–5** to lines **42–5** and **82–5**. The signals on lines **42–5** and **82–5** induce outputs on lines **16–5** and **86–5**, both of which are superfluous since the corresponding flip-flops **14–5** and **88–5** are already set in their 1 states. Currents also are induced on lines **44–1**, **44–2**, **44–3**, **44–4**, **44–5**, **102–1**, **102–3** and **102–5**. Flip-flops **46–1**, **46–2**, **46–3**, **46–4**, **46–5**, **100–1**, **100–3** and **100–5** are set to their 1 states. The switch **122** is closed to apply an advance signal to *n* register **56**. This signal advances down the lines **156'** and **158'** seeking a flip-flop position corresponding to coincidently set flip-flops **100** and **46**. The first such flip-flop is FF **150–1'** and the word corresponding to lines **34–5** and **64–1** is read out of memory **10**.

Since row **2** of plane **80** is fenced out and FF **100–2** is not set, the setting of FF **46–2** is ineffective. FF **100–3** and FF **46–3** are both set so the word corresponding to lines **34–5** and **64–3** is read out. Row **4** is fenced out and is thus skipped. FF **100–5** and FF **46–5** are both set so the word corresponding to lines **34–5** and **64–5** is read out. Neither FF **100–6** nor **46–6** is not set and the advance signal following read out of the word at the intersection of lines **34–5** and **64–5** proceeds to set flip-flop **150–7'** to produce a reset output from OR **70** and an advance signal to *m* register **18**. This advance pulse advances to set FF **150–6**. The resultant interrogation of column six of planes **12** and **80** sets flip-flops **46–3**, **46–6** and **100–1**. Flip-flops **14–6** and **88–6** remain set.

When switch **122** (FIG. 2D) is closed, the signal on lines **156'** and **158'** fail to detect any coincidence on flip-flops **46** and **100** so FF **150–7'** is set to its 1 state. The output of FF **150–7'** resets FF units **46** and **100** and advances *m* register **18** to set FF **150–7**. The output of FF **150–7** signals completion of the operation.

Multiple fence planes

Referring to FIGURES 3A and 3B, a variation of a portion of the system shown in FIGURES 2A–2F is illustrated wherein a detector plane **112**, similar to detector plane **12** of FIGURE 2E, and two fence planes **180** and **280**, each similar to fence plane **80** in FIGURE 2E are provided. The illustration in FIGURE 3 is on a smaller scale wherein $n=3$ and $m=3$, whereas in FIGS. 2A–2F,

$n=6$ and $m=6$. For convenience in comparison with the embodiment in FIGS. 2A–2F, consider that the three n lines and the three m lines from each plane **112, 180** and **280** correspond to the first three such lines in the embodiment of FIGURES 2A–2F.

This embodiment illustrates that a novel and useful system may be provided by ANDing the contents of a detector plane with the contents of two or more fence planes.

The detector plane **112** and the fence planes **180** and **280** are coincidently interrogated by signals on the lines **142** which correspond to the lines **42–82** in FIGURE 2E. Assume that the cores **A1, A3, A5, A6** and **A9** in plane **112** have been set. Assume that cores **B1, B3, B5** and **B9** in plane **180** and cores **C1, C5, C6** and **C9** in plane **280** have been set.

The n outputs of plane **112** are on lines **144–1, 144–2, 144–3**, connecting to the 1 inputs of corresponding flip-flops **146–1, 146–2, 146–3**. Similarly the m outputs are on lines **116–1, 116–2** and **116–3**, connecting respectively to the 1 inputs of flip-flops **114–1, 114–2** and **114–3**.

The n output lines **202** and **302** of planes **180** and **280** respectively, similarly connect to the 1 inputs of corresponding flip-flops **200** and **300**. The m output lines **186** and **286** of planes **180** and **280** respectively connect to the 1 inputs of flip-flops **188** and **288**. As in the case of flip-flop units **88** and **14**, in FIGURES 2A and 2B, a common reset line **190** is provided for m flip-flop units **114, 188** and **288**. Similarly, a common reset line **192** is provided for n flip-flop units **146, 200** and **300**.

A gating unit **194** generally corresponding in function to the gating units **94** in FIGURE 2 is interposed between the m flip-flop units **114, 188** and **288** and the m register **18**. Similarly, a gating unit **204** corresponding to unit **104** in FIG. 2 is interposed between n flip-flops **146, 114, 200, 188, 300** and **288** and the register flip-flop units **146, 200** and **300** and the n register **56**.

AND gates **204–1, 204–3** and **204–5** have as inputs the 1 outputs of n flip-flops **146, 200** and **300** as follows:

146–1, 200–1, 300–1 connected to AND **204–1**
146–2, 200–2, 300–2 connected to AND **204–3**
146–3, 200–3, 300–3 connected to AND **204–5**

OR gates **204–2, 204–4** and **204–6** have as inputs the 0 outputs of n flip-flops **146, 200** and **300** as follows:

146–1, 200–1, 300–1 connected to OR **204–2**
146–2, 200–2, 300–2 connected to OR **204–4**
146–3, 200–3, 300–3 connected to OR **204–6**

AND gates **194–1, 194–3** and **194–5** have as inputs the 1 outputs of m flip-flop **114, 188** and **288** as follows:

114–1, 188–1 and **288–1** connected to AND **194–1**
114–2, 188–2 and **288–2** connected to AND **194–3**
114–3, 188–3 and **288–3** connected to AND **194–5**

OR gates **194–2, 194–4** and **194–6** have as inputs the 0 outputs of m flip-flops **114, 188** and **288** as follows:

114–1, 188–1 and **288–1** connected to OR **194–2**
114–2, 188–2 and **288–2** connected to OR **194–4**
114–3, 188–3 and **288–3** connected to OR **194–6**

The outputs of the AND gates **194–1, 194–3** and **194–5** are applied to lines **23–1″, 23–2″** and **23–3″** as the inputs to the first three stages of the register **18**, just as were the outputs of the AND gates **94** in FIGURE 2. The outputs of the OR gates **194–2, 194–4** and **194–6** are applied to lines **24–1″, 24–2″** and **24–3″**. The outputs of AND and OR gates **204** similarly are applied to lines **50″** and **51″** as inputs to register **56**.

Thus, it is seen that, for example, the coincidence of signal on the n lines **144–1, 202–1** and **302–1** will produce an output from AND gate **204–1** to condition the first stage of the register **56**. Similarly, the coincidence of outputs on m lines **116–1, 186–1** and **286–1** will produce an output from AND gate **194–1** to condition the first stage of the register **18**. Thus, with the first stages of both registers **18** and **56** set, read out is effected from a corresponding address in the memory **10**. When there is not the foregoing coincidence of outputs, the corresponding OR gates **194** or **204** are actuated, causing the interrogation pulse to the registers **18** and **56** to be advanced to the next stages which are conditioned.

Obviously, switches may be provided for selectively including either or both fencing planes **180** and **280**.

With the cores set as indicated in FIG. 3, there is coincidence of set cores in all three planes in the following three instances: **A1, B1, C1**; **A5, B5, C5**; and **A9, B9, C9**. Accordingly, the three words corresponding to addresses **A1, A5** and **A9** will be read out of the memory in the manner described with respect to FIGURE 2.

Referring to FIGURE 4, two circuit blocks **294** and **304** are shown which may be substituted in FIGURE 3 for blocks **194** and **204** respectively. This embodiment illustrates another variation of the system wherein the contents of the detector plane **112** are ANDed with the contents of either fence plane **180** or **280**.

The inputs to the blocks **294** and **304** are the same as the inputs to the blocks **194** and **204** in FIGURE 3. These inputs are the 0 and 1 outputs of the flip-flops **114, 146, 188, 200, 288** and **300**, and are so indicated in the left-hand margin of FIGURE 4.

In the circuit block **304**, three OR gates designated **310–1, 310–2** and **310–3** are provided. OR gate **310–1** has as inputs the 1 output of flip-flops **200–1** and **300–1**. OR gate **310–2** has as inputs the 1 outputs of flip-flops **200–2** and **300–2**. OR gate **310–3** has as inputs the 1 outputs of flip-flops **200–3** and **300–3**.

In block **294** three OR gates **312–1, 312–2** and **312–3** are provided. OR gate **312–1** has as inputs the 1 outputs of flip-flops **188–1** and **288–1**. OR gate **312–2** has as inputs the 1 outputs of flip-flops **188–2** and **288–2**. OR gate **312–3** has as inputs the 1 outputs of flip-flops **188–3** and **288–3**.

Thus it is apparent that a given OR gate **310** or **312** will produce an output when either of the flip-flops connected as inputs is in its 1 state. Similarly, each gate **310** and **312** will produce an output when both of its inputs are in their 1 states.

The outputs of OR gates **310–1, 310–2** and **310–3** are applied respectively to AND gates **304–1, 304–3** and **304–5**. The second inputs to these AND gates are the 1 outputs of flip-flops **146–1, 146–2** and **146–3** respectively.

The outputs of OR gates **312–1, 312–2** and **312–3** respectively are connected as inputs to AND gates **294–1, 294–3** and **294–5**. The second inputs to these AND gates are the 1 outputs of flip-flops **114–1, 114–2** and **114–3**, respectively.

The OR gates **304–2, 304–4, 304–6, 294–2, 294–4** and **294–6** each have three inputs which are the 0 outputs of the flip-flops **114, 146, 188, 200, 288** and **300** as follows:

OR **304–2**	**146–1**	**200–1**	**300–1**
OR **304–4**	**146–2**	**200–2**	**300–2**
OR **304–6**	**146–3**	**200–3**	**300–3**
OR **294–2**	**114–1**	**188–1**	**288–1**
OR **294–4**	**114–2**	**188–2**	**288–2**
OR **294–6**	**114–3**	**188–3**	**288–3**

It is thus apparent that coincidence of a set core in plane **112** with a set core in either or both of planes **180** and **280** will produce an output from corresponding AND gates **304** and **294** to effect read out of a corresponding word from memory.

Referring to FIGURE 5, circuit blocks **394** and **404** are shown which may be substituted in FIGURE 3 for blocks **194** and **204** respectively. This embodiment illustrates a further variation of the system wherein the contents of the detector plane **112** may be ANDed with the contents of one or the other of the planes **180** and **280**, but not with both.

It will be noted that the circuits in FIGURE 4 and FIGRE 5 are substantially identical but have the following ferences. First, AND gates **410** and **412** have been bstituted for the OR gates **310** and **312** of FIGURE 4. condly, each of the AND gates has as its two inputs the utput of a flip-flop **288** or **300** and the 0 output of a -flop **188** or **200**. Thus the circuit of FIGURE 5 is ective to produce the read out of a word corresponding an address set in a core in the detector plane **112** proled that a corresponding core is set in the detector plane **0** but is not set in the corresponding core in fence ine **180**. Third, the 0 outputs of flip-flops **288** and **300** e applied as inputs to the OR gates **404** and **394** and the outputs of flip-flops **188** and **200** are applied as inputs these OR gates. Thus, in accordance with the setting cores in planes **112**, **180** and **280** as shown in FIGRE 3, only the word corresponding to the set core **A6** plane **112** will be read out.

While the invention has been particularly shown and scribed with reference to preferred embodiments there-, it will be understood by those skilled in the art that rious changes in form and details may be made therein thout departing from the spirit and scope of the inven-on.

What is claimed is:

1. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a first register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

a second register having *m* stages corresponding to the *m* columns of said first register,

a third register having *n* stages corresponding to the *n* rows of said first register,

a first skipping shift register having *m* stages corresponding to the *m* stages of said second register, operable in response to the setting of stages of said second register for setting corresponding stages of said first skipping shift register, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

a second skipping shift register having *n* stages corresponding to the *n* stages of said third register, operable in response to the setting of stages of said third register for setting corresponding stages of said second skipping shift register, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first register to set stages of said second and third registers corresponding to said *m* columns and *n* rows respectively which have elements set to said given state,

means for applying resetting inputs to said third register,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first register,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

2. The invention of claim **1** wherein said means for pplying interrogation inputs to said first skipping shift egister comprise means for applying an initial interrogaon input and means for applying the last said successive utput from said second skipping shift register.

3. The invention of claim **1** wherein said means for pplying interrogation inputs to said second skipping shift register comprise means for applying an initial interrogation input and means for applying inputs which are outputs from said memory in response to coincident application to said memory of an output from a set stage of said first skipping shift register and an output from a set stage of said second skipping shift registers.

4. The invention of claim **1** having indicator means responsive to the last said successive output from said first skipping shift register.

5. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a first register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

a second register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

third and fourth registers each having *m* stages corresponding to the *m* columns of said first and second registers respectively,

first logical means having *m* stages corresponding to the *m* stages of said third and fourth registers, each stage being set when the corresponding stages of said third and fourth registers are set,

a first skipping shift register having *m* stages corresponding to the *m* stages of said first logical means, settable in accordance with the setting of corresponding stages of said first logical means, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

fifth and sixth registers each having *n* stages corresponding to the *n* rows of said first and second registers respectively,

second logical means having *n* stages corresponding to the *n* stages of said fifth and sixth registers, each stage being set when the corresponding stages of said fifth and sixth registers are set,

a second skipping shift register having *n* stages corresponding to the *n* stages of said second logical means, settable in accordance with the setting of corresponding stages of said second logical means, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first and second registers for setting stages of said third and fifth registers corresponding to the *m* columns and *n* rows respectively of said first register which have elements set to said given state, and for setting stages of said fourth and sixth registers corresponding to the *m* columns and *n* rows respectively of said second register which have elements set to said given state,

means for applying resetting inputs to said fifth and sixth registers,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first and second registers,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

6. The invention of claim **5** wherein said means for applying interrogation inputs to said first skipping shift register comprise means for applying an initial interrogation input and means for applying the last said successive output from said second skipping shift register.

7. The invention of claim **5** wherein said means for

applying interrogation inputs to said second skipping shift register comprise means for applying an initial interrogation input and means for applying inputs which are outputs from said memory in response to coincident application to said memory of an output from a set stage of said first skipping shift register and an output from a set stage of said second skipping shift register.

8. The invention of claim 5 wherein said means for applying resetting inputs to said fifth and sixth registers comprise means for applying initial resetting inputs and means for applying the last said successive output from said second skipping shift register.

9. The invention of claim 5 having indicator means responsive to the last said successive output from said first skipping shift register.

10. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a first register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

a second register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

third and fourth registers each having *m* stages corresponding to the *m* columns of said first and second registers respectively,

first logical means having *m* stages corresponding to the *m* stages of said third and fourth registers, each stage being set when the corresponding stage of either of said third and fourth registers is set,

a first skipping shift register having *m* stages corresponding to the *m* stages of said first logical means, settable in accordance with the setting of corresponding stages of said first logical means, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

fifth and sixth registers each having *n* stages corresponding to the *n* rows of said first and second registers respectively,

second logical means having *n* stages corresponding to the *n* stages of said fifth and sixth registers, each stage being set when the corresponding stage of either of said fifth and sixth registers is set,

a second skipping shift register having *n* stages corresponding to the *n* stages of said second logical means, settable in accordance with the setting of corresponding stages of said second logical means, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first and second registers for setting stages of said third and fifth registers corresponding to the *m* columns and *n* rows respectively of said first register which have elements set to said given state, and for setting stages of said fourth and sixth registers corresponding to the *m* columns and *n* rows respectively of said second register which have elements set to said given state,

means for applying resetting inputs to said fifth and sixth registers,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first and second registers,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

11. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a first register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

a second register having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element corresponding to each word of said memory with selected ones of said elements set to a given state,

third and fourth registers each having *m* stages corresponding to the *m* columns of said first and second registers respectively,

first logical means having *m* stages corresponding to said third and fourth registers, each stage being set when only one of the corresponding stages of said third and fourth registers is set,

a first skipping shift register having *m* stages corresponding to the *m* stages of said first logical means, settable in accordance with the setting of corresponding stages of said first logical means, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

fifth and sixth registers each having *n* stages corresponding to the *n* rows of said first and second registers respectively,

second logical means having *n* stages corresponding to the *n* stages of said fifth and sixth registers, each stage being set when one only of the corresponding stages of said fifth and sixth registers is set,

a second skipping shift register having *n* stages corresponding to the *n* stages of said second logical means, settable in accordance with the setting of corresponding stages of said second logical means, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first and second register for setting stages of said third and fifth registers corresponding to the *m* columns and *n* rows respectively of said first register which have elements set to said given stage, and for setting stages of said fourth and sixth registers corresponding to the *m* columns and *n* rows respectively of said second register which have elements set to said given state,

means for applying resetting inputs to said fifth and sixth registers,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first and second registers,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

12. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a plurality of first registers each having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element in each said register corresponding to each word of said memory with said elements of said registers set selectively to given states,

a plurality of second registers each having *m* stages and each corresponding to one of said first registers,

a plurality of third registers each having *n* stages and each corresponding to one of said first registers,

a first logical circuit having *m* stages, each stage corresponding to a similar stage of all said second reg-

isters, each said stage of said first logical circuit being set when said similar stages of said second registers are set,

a first skipping shift register having *m* stages corresponding to the *m* stages of said first logical circuit, settable in accordance with the setting of corresponding stages of said first logical circuit, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

a second logical circuit having *n* stages each stage corresponding to a similar stage of said third registers, each said stage of said second logical circuit being set when said similar stages of said third registers are set,

a second skipping shift register having *n* stages corresponding to the *n* stages of said second logical circuit, settable in accordance with the setting of corresponding stages of said second logical circuit, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first registers for setting stages of said second and third registers corresponding to the *m* columns and *n* rows respectively of said first registers which have elements set to said given state,

means for applying resetting inputs to said third registers,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first registers,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

13. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a plurality of first registers each having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element in each said register corresponding to each word of said memory with said elements of said registers set selectively to given states,

a plurality of second registers each having *m* stages and each corresponding to one of said first registers,

a plurality of third registers each having *n* stages and each corresponding to one of said first registers,

a first logical circuit having *m* stages, each stage corresponding to a similar stage of all said second registers, each said stage of said first logical circuit being set when said similar stage of one of said second registers is set and said similar stage of at least one of the other said second registers is set,

a first skipping shift register having *m* stages corresponding to the *m* stages of said first logical circuit, settable in accordance with the setting of corresponding stages of said first logical circuit, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

a second logical circuit having *n* stages each stage corresponding to a similar stage of said third registers, each said stage of said second logical circuit being set when said similar stage of one of said third registers is set and said similar stage of at least one of the other said second registers is set,

a second skipping shift register having *n* stages corresponding to the *n* stages of said second logical circuit, settable in accordance with the setting of corresponding stages of said second logical circuit, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first registers for setting stages of said second and third registers corresponding to the *m* columns and *n* rows respectively of said first registers which have elements set to said given state,

means for applying resetting inputs to said third registers,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first registers,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

14. In a data processing system

a multiple word data memory having *n* rows and *m* columns,

a plurality of first registers each having *n* rows and *m* columns of register elements corresponding to the *n* rows and *m* columns of said memory, one element in each said register corresponding to each word of said memory with said elements of said registers set selectively to given states,

a plurality of second registers each having *m* stages and each corresponding to one of said first registers,

a plurality of third registers each having *n* stages and each corresponding to one of said first registers,

a first logical circuit having *m* stages each stage corresponding to a similar stage of all said second registers, each said stage of said first logical circuit being set when said similar stage of one of said second registers is set and said similar stage of only one of the other said registers is set,

a first skipping shift register having *m* stages corresponding to the *m* stages of said first logical circuit, settable in accordance with the setting of corresponding stages of said first logical circuit, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

a second logical circuit having *n* stages each stage corresponding to a similar stage of said third registers, each said stage of said second logical circuit being set when said similar stage of one of said third registers is set and said similar stage of only one of the other said registers is set,

a second skipping shift register having *n* stages corresponding to the *n* stages of said second logical circuit, settable in accordance with the setting of corresponding stages of said second logical circuit, and operable in response to successive interrogation inputs to provide outputs successively from set stages thereof,

means for simultaneously interrogating all *m* columns of said first registers for setting stages of said second and third registers corresponding to the *m* columns and *n* rows respectively of said first registers which have elements set to said given state,

means for applying resetting inputs to said third registers,

means for applying outputs from said *m* stages of said first skipping shift register to corresponding columns of said memory and said first registers,

means for applying outputs from said *n* stages of said second skipping shift register to corresponding rows of said memory,

means for applying interrogation inputs to said first skipping shift register,

means for applying interrogation inputs to said second skipping shift register.

15. The invention of claim 1 wherein said means for applying resetting inputs to said third register comprise means for applying an initial resetting input and means for applying the last said successive output from said second skipping shift register.

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