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(54) Title: TWO-PHASE, THREE-PHASE RECONFIGURABLE SWITCHED-CAPACITOR POWER CONVERTER

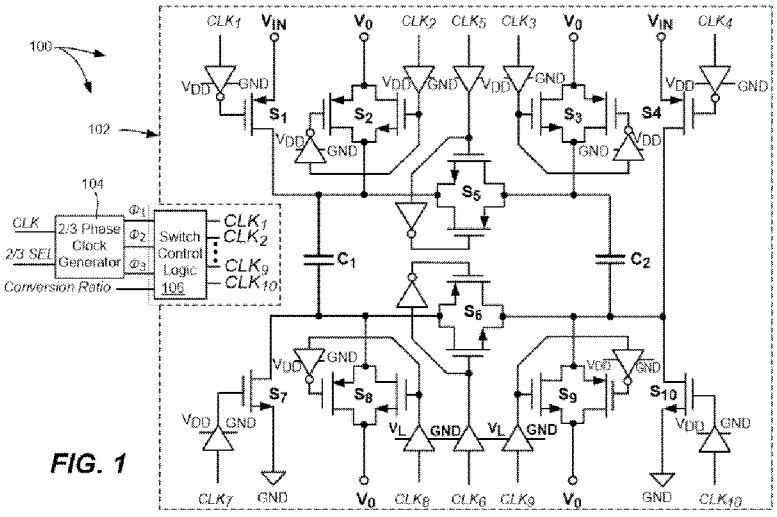

FIG. 1

(57) Abstract: The technology described herein is generally directed towards a reconfigurable switched-capacitor power converter that operates in multiple switching modes, including one or more implementations having a two-phase switching mode driven by a two-phase clock, and a three-phase switching mode driven by a three-phase clock. Various configurations of logic-controlled switches, corresponding to specified voltage conversion ratios, are achieved by driving certain switches according to the two-phase clock in the two-phase mode and the three-phase clock in the three-phase mode. For example, by using two flying capacitors and controlling ten switches to provide different configurations of alternating circuits, six different non-zero voltage conversion ratios are realizable.

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TWO-PHASE, THREE-PHASE RECONFIGURABLE SWITCHED-CAPACITOR POWER CONVERTER

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Provisional Application number 62/389,544, filed on March 2, 2016, entitled: "2-/3-Phase Reconfigurable Switched-Capacitor Power Converter," the entirety of which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure generally relates to switched-capacitor power converters that convert an input voltage to different output voltages.

BACKGROUND

[0003] Switched-capacitor power converters (SCPCs) are circuits that use logic-controlled switches to charge and discharge capacitors ("flying capacitors") in a cyclical signaling phase to convert an input voltage to different output voltages. SCPCs are widely used in energy-efficient applications, and may be particularly beneficial for wirelessly-powered devices such as wearable electronics, biomedical implants and smart sensor networks.

[0004] In general, SCPCs only use the flying capacitors as energy transmission components, (instead of bulky and costly power inductors, which thus may be eliminated in many circuits). Thus, unlike other switching converters and linear regulators, an SCPC can be easily fully integrated on-chip without sacrificing the compact size of the chip. As a result, switched-capacitor power converters are good candidates for low cost applications where the power management units need to

generate different power-supply voltages for different functional blocks, such as the internet-of-everything (IoE) and wearable devices.

[0005] One of the major performance indicators of an SCPC is its efficiency, which is expressed as the ratio of the actual output voltage V_O / $(m/n)V_{IN}$, where m/n represents the ideal (no-load) voltage conversion ratio. The efficiency can be high if V_O is close to (but lower than) $(m/n)V_{IN}$. The efficiency is low when V_O / $(m/n)V_{IN}$ is small compared to unity.

[0006] A two-phase SCPC with two flying capacitors usually realizes two or three voltage conversion ratios, such as 2/3X, 1/2X and 1/3X, where X represents the input voltage; (these example ratios are for step-down SCPCs; step-up SCPCs that increase the input voltage, and inverting SCPCs, are also known). This relatively small number of voltage conversion ratios means that high efficiency cannot be obtained over a wide range of input voltages and/or loading current. Additional voltage conversion ratios can be achieved by stacking power stages, but this means more flying capacitors and switches are needed, which limits the power delivering ability and increases the silicon size. If additional off-chip capacitors are used, the power density is negatively impacted.

SUMMARY

[0007] This Summary is provided to introduce a selection of representative concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used in any way that would limit the scope of the claimed subject matter.

[0008] Briefly, one or more aspects of the technology described herein are directed towards a switched-capacitor power converter that converts an input voltage to an output voltage according to a specified voltage conversion ratio of a plurality of realizable voltage conversion ratios. The switched-capacitor power converter comprises a power stage comprising flying capacitors and a plurality of logic-controlled switches coupled to the flying capacitors and a multiple clock phase generator configured to output switching signals in different, selectable clock phases, each of the different, selectable clock phases comprising alternating switching signals, wherein one of the different, selectable clock phases is selected based upon the specified voltage conversion ratio. The switched-capacitor power converter also comprises switch control logic coupled to the multiple clock phase generator and coupled to the set of logic-controlled switches to configure switch couplings to the flying capacitors of the power stage, comprising for each switch of the set of logic-controlled switches, to turn on the switch, turn off the switch or control an on or off state of the switch according to at least one of the alternating switching signals, wherein the switch control logic is arranged to configure alternating active circuits, corresponding to the alternating switching signals, that charge or discharge respective ones of the flying capacitors to provide the output voltage according to the specified voltage conversion ratio.

[0009] Other advantages may become apparent from the following detailed description when taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The technology described herein is illustrated by way of example and not limited in the accompanying figures in which like reference numerals indicate similar elements and in which:

[0011] FIG. 1 is a representation of one implementation of a two-phase and three-phase reconfigurable switched-capacitor power converter, according to one or more example implementations.

[0012] FIG. 2 is an example circuit diagram representing the power stage of a two-phase and three-phase reconfigurable switched-capacitor power converter, according to one or more example implementations.

[0013] FIGS. 3A and 3B are representations of one configuration of a two-phase and three-phase reconfigurable switched-capacitor power converter showing the connection of switches operating in a two-phase mode (FIG. 3A), in which the resultant circuits of each mode (FIG. 3B) are switched-in and switched out by the switches' states during each phase to provide a 1/3 voltage conversion ratio, according to one or more example implementations.

[0014] FIGS. 4A and 4B are representations of another configuration of a two-phase and three-phase reconfigurable switched-capacitor power converter showing the connection of switches operating in a two-phase mode (FIG. 4A), in which the resultant circuits of each mode (FIG. 4B) are switched-in and switched out by the switches' states during each phase to provide a 1/2 voltage conversion ratio, according to one or more example implementations.

[0015] FIGS. 5A and 5B are representations of another configuration of a two-phase and three-phase reconfigurable switched-capacitor power converter showing the connection of switches operating in a two-phase mode (FIG. 5A), in which the resultant circuits of each mode (FIG. 5B) are switched-in and switched out by the switches' states during each phase to provide a 2/3 voltage conversion ratio, according to one or more example implementations.

[0016] FIGS. 6A and 6B are representations of another configuration of a two-phase and three-phase reconfigurable switched-capacitor power converter showing the connection of switches operating in a two-phase mode (FIG. 6A), in which the resultant circuits of each mode (FIG. 6B) are switched-in and switched out by the switches' states during each phase to provide a 1/1 voltage conversion ratio, according to one or more example implementations.

[0017] FIGS. 7A and 7B are representations of another configuration of a two-phase and three-phase reconfigurable switched-capacitor power converter showing the connection of switches operating in a three-phase mode (FIG. 7A), in which the resultant circuits of each mode (FIG. 7B) are switched-in and switched out by the switches' states during each phase to provide a 1/4 voltage conversion ratio, according to one or more example implementations.

[0018] FIGS. 8A and 8B are representations of another configuration of a two-phase and three-phase reconfigurable switched-capacitor power converter showing the connection of switches operating in a three-phase mode (FIG. 8A), in which the resultant circuits of each mode (FIG. 8B) are switched-in and switched out by the switches' states during each phase to provide a 3/4 voltage conversion ratio, according to one or more example implementations.

[0019] FIG. 9A is representation of switch control logic of a two-phase, three-phase switched-capacitor power converter, according to one or more example implementations.

[0020] FIG. 9B is table representing clock selection of the switch control logic of FIG. 9A for controlling the switches to provide the various voltage conversion ratios, according to one or more example implementations.

[0021] FIG. 10A is a circuit diagram representing a circuit for generating the two-phase and three-phase clock signals, according to one or more example implementations.

[0022] FIG. 10B is a timing diagram representing the clock signals generated in the two-phase operating modes and three-phase operating modes, according to one or more example implementations.

[0023] FIG. 11 is a graph showing theoretical efficiencies versus $V_O/((m/n)V_{IN})$ of a conventional two-phase switched-capacitor power converter with two flying capacitors, a two-phase, three-phase switched-capacitor power converter with two flying capacitors according to one or more example implementations described herein, and the ideal low dropout regulator.

DETAILED DESCRIPTION

[0024] Various aspects of the technology described herein are generally directed towards a switched-capacitor power converter (SCPC), including a switching scheme for SCPCs. As will be understood, using the same number of flying capacitors as conventional schemes, the technology described herein is able to realize more voltage conversion ratios with fewer switches than existing designs.

[0025] The SCPC and switching scheme described herein is reconfigurable, using multiple phases to provide a wide range of voltage conversion ratios. In one or more non-limiting implementations, the SCPC operates in two switching modes, comprising a 2-phase mode, driven by a 2-phase clock, and a 3-phase mode, driven by a 3-phase clock. Thus, the two-phase, three-phase reconfigurable SCPC may be referred to herein as a "2-/3-phase reconfigurable SCPC," or "2-/3-phase SCPC" for short.

[0026] As will be understood, because of the multiple phases, more voltage conversion ratios are achievable for the same number of flying capacitors. Note that for any specified number of flying capacitors, the number of realizable conversion ratios for a 2-phase SCPC is limited; thus, as described herein three or even more phases are used to achieve more voltage conversion ratios for the same number of flying capacitors. As will be seen in the examples below, by considering an SCPC with two flying capacitors, with 2-phase operation only four voltage conversion ratios can be realized; however by including the 3-phase operation, the number of voltage conversion ratios is increased to six in a way that maintains high efficiency and overcomes the performance limits of having only 2-phase operation.

[0027] More particularly, by controlling the switches and driving them with the appropriate clock phases, the exemplified 2-/3-phase SCPC with two flying capacitors can be reconfigured to realize six voltage conversion ratios in one implementation, namely (1/4)X, (1/3)X, (1/2)X, (2/3)X, (3/4)X and 1X. Any of the capacitors including the flying capacitors can be on-chip or off-chip.

[0028] It should be understood that any of the examples herein are non-limiting. For example, various circuits reconfigured from a power converter having two flying

capacitors and ten switches driven with alternating switching signals corresponding to the two-phase and three-phase signals are represented herein, however it is understood that a different number of flying capacitors and/or switches, and/or using one or more additional phases may achieve benefits from and be encompassed by the technology described herein. As another example, step-up SCPCs may achieve benefits from and be encompassed by the technology described herein. As such, the technology described herein is not limited to any particular implementations, embodiments, aspects, concepts, structures, functionalities or examples described herein. Rather, any of the implementations, embodiments, aspects, concepts, structures, functionalities or examples described herein are non-limiting, and the technology may be used in various ways that provide benefits and advantages in power conversion concepts in general.

[0029] In general and as represented in FIG. 1, the 2-/3-SCPC exemplified herein (labeled 100) comprises three parts, namely a power stage 102, a 2-/3-phase clock generator 104 and switch control logic 106. The switches S_1 to S_{10} may comprise MOS (Metal Oxide Semiconductor) transistors (e.g., MOSFETs, or MOS field-effect transistors) or the like; for example, if MOS transistors are used, each MOS transistor has a gate-drive circuit to control the ON state and the OFF state. Each gate-drive circuit is powered by V_{DD}, (which may be the same as V_{IN}, although V_{DD} may be a different voltage and/or obtained from a different power supply as V_{IN}).

[0030] The flying capacitors C_1 and C_2 can be implemented by on-chip capacitors and/or off-chip capacitors such as ceramic capacitors. The switch driving signals, represented by CLK_1 to CLK_{10}, are generated from the switch control logic 106 according to the desired voltage conversion ratio (corresponding to the needed output voltage) at any given time.

[0031] The 2-/3-phase clock generator 104 provides the 2- or 3-phase clock signals Φ_1, Φ_2 and Φ_3 to the switch control logic 106. The switch control logic 106 may be implemented with straightforward multiplexers, may be synthesized using hardware description language by automatic design tools, or may be implemented in other ways to operate according to the logic table of Table I / FIG. 9B as described below. As is understood, in different configurations, various switches are driven by alternating switching signals corresponding to the alternating clock signals Φ_1 and Φ_2 in two-phase operation, or the alternating clock signals Φ_1, Φ_2 and Φ_3 in three-phase operation.

[0032] FIG. 2 shows a representation 202 of the power stage 102 of FIG. 1 of the 2-/3-phase reconfigurable switched-capacitor power converter in a modified form, in which the switches S_1 to S_{10} are shown as single pole, single throw switch symbols instead of transistors (and without associated drivers, inverters, V_{DD} and GND) for purposes of clarity. These switch symbols are likewise used in the various example configurations shown in FIGS. 3A, 4A, 5A, 6A, 7A and 8A.

[0033] FIGS. 3A represents a configuration 330 of the power stage's switches that operates in the 2-phase mode to provide a voltage conversion ratio of (1/3)X (where "X" represents V_{IN}). In general, for each figure of FIGS. 3A, 4A, 5A, 6A, 7A or 8A, the switches that are labeled with Φ_k (k=1, 2, 3) are turned on when Φ_k = "1" (the clock signal goes high) in that figure; the switches that are labeled with "1" are turned on (closed) in all phases in that figure, and the switches that are indicated with dashed lines and labeled with "0" are turned off (open) in all phases in that figure.

[0034] Thus, in the 2-phase configuration 330 of FIG. 3A, the switches S_2, S_4 and S_6 remain turned Off (0) regardless of whether the 2-phase clock signal is outputting

Φ_1 or Φ_2. The Φ_1-labeled switches (S_1, S_3, S_8 and S_{10}) are On when Φ_1 is 1 (high clock signal) and Off when Φ_1 is 0 (low clock signal). The Φ_2-labeled switches (S_5, S_7 and S_9) are On when Φ_2 is 1 (high clock signal) and Off when Φ_2 is 0 (low clock signal). The logic is such that in the 2-phase mode of operation, the signals Φ_1 and Φ_2 are the inverse signals of each other; (this holds true for each 2-phase configuration shown herein, as described below with reference to the timing diagram of FIG. 10B).

[0035] FIG. 3B shows the two alternating circuits 332 and 334 that result from each of the two clock phases Φ_1 and Φ_2, respectively, that is, the circuit 332 is active (switched in) while Φ_1 is high and Φ_2 is low, and the circuit 334 is active while Φ_1 is low and Φ_2 is high. The capacitors C1 and C2 are accordingly charged and discharged as the clock cycles alternate between the two phases to provide the desired 1/3X voltage output. In FIG. 3B, a loading capacitor C_L is shown as being connected to the output voltage V_O; the loading capacitor may be on-chip or off chip.

[0036] To summarize, in FIGS. 3A and 3B, during the time that clock signal Φ_1 is high and Φ_2 is low, the switches S_1, S_3, S_8 and S_{10} are turned on, whereby the flying capacitor C_1 is connected between V_{IN} and V_O and C_2 is connected between V_O and ground. During the time that clock signal Φ_2 is high and Φ_1 is low, the switches S_5, S_7 and S_9 are turned on, connecting C_1 and C_2 in series between V_O and ground, and the SCPC realizes the voltage conversion ratio of (1/3)X. In this configuration 330, the switches S_2, S_4 and S_6 are constantly turned off.

[0037] FIG. 4A shows a different configuration 440 of the SCPC wherein some of the switches S_1 - S_{10} are constant while others are switched in the 2-phase mode to provide a (1/2)X voltage output. The same drawing conventions are used in FIG. 4A

as in FIG. 3A (and similarly in FIGS. 5A, 6A, 7A and 8A), and thus it is seen that in this configuration 440 the switches S_5, S_6 and S_9 are constantly Off (0), the switches S_3 and S_{10} are constantly On (1), the switches S_1, S_4 and S_8 alternate between being On (when Φ_1 is high (1)) and Off (when Φ_1 is low (0)), and the switches S_2 and S_7 alternate between being On (when Φ_2 is high (1)) and Off (when Φ_2 is low (0)).

[0038] FIG. 4B shows the two alternating active circuits 442 and 444 that result from the two clock signals / switch-driving signals, that is circuit 442 is switched in when Φ_1 is high and Φ_2 is low, and circuit 444 is switched in when Φ_2 is high and Φ_1 is low. The capacitors C1 and C2 are accordingly charged and discharged to provide the desired 1/2X voltage output. In FIG. 4B, (similar to FIGS. 3B, 5B, 6B 7B and 8B), a loading capacitor C_L is shown as being connected to the output voltage V_O.

[0039] To summarize FIGS. 4A and 4B, during the time that clock signal Φ_1 is high and Φ_2 is low, the switches S_1, S_4 and S_8 are turned on. The flying capacitor C_1 is connected between V_{IN} and V_O and C_2 is connected between V_O and ground. During the time that clock signal Φ_2 is high and Φ_1 is low, the switches S_2 and S_7 are turned on, connecting C_1 on top of C_2 and between V_{IN} and V_O, and the SCPC realizes the voltage conversion ratio of (1/2)X. In this configuration 440, the switches S_5, S_6 and S_9 are constantly turned off and the switches S_3 and S_{10} are constantly turned on.

[0040] FIG. 5A is another two-phase configuration 550, which produces a 2/3X voltage output. FIG. 5A is generally similar to FIGS. 3A and 4A in terms of its components and drawing conventions, and thus for brevity the various states of the switches S_1 – S_{10} are only briefly described as S_5, S_8 and S_{10} being Off, S_2, S_3, S_4 and S_7 being driven On and Off in accordance with the signals of Φ_1 and S_1, S_6 and

S_9 being driven Off and On according to the signals of Φ_2. As can be seen, the two circuits 552 and 554 of FIG. 5B corresponding to FIG. 5A each result as one of the two clock phases Φ_1 and Φ_2 each respectively outputs its switch driving signals. The capacitors C1 and C2 are accordingly charged and discharged to provide the desired 2/3X voltage output.

[0041] More particularly, in FIGS. 5A and 5B, when signal Φ_1 is high, the switches S_2, S_3, S_4 and S_7 are turned On, whereby the flying capacitor C_1 is connected between V_{IN} and V_O and C_2 is connected between V_O and ground. when signal Φ_2 is high, the switches S_1, S_6 and S_9 are turned On, connecting C_1 and C_2 in series between V_{IN} and V_O, and the SCPC realizes the voltage conversion ratio of (2/3)X. In this configuration 550, the switches S_5, S_8 and S_{10} are constantly turned Off.

[0042] FIGS. 6A shows another configuration 660 and FIG. 6B shows the two circuits 662 and 664 that alternate in time based upon the driving signal states of Φ_1 and Φ_2. As is seen, the circuits 662 and 664 alternate according to Φ_1 and Φ_2 to provide a 1/1X voltage output. In FIGS. 6A and 6B, when Φ_1 is high, the switch S_1 is turned On, charging the flying capacitor C_1 to V_{IN}. When Φ_2 is high, the switch S_2 is turned On and the charge of C_1 is dumped to the output voltage. At any phase, the switches S_3, S_7 and S_{10} are constantly turned On, and the switches S_4, S_5, S_6, S_8 and S_9 are constantly turned Off. This SCPC configuration 660 realizes the voltage conversion ratio of 1/1X. Note that two phases provides 1/1X voltage with the switch control logic, rather than by adding another controller, for example.

[0043] FIG. 7A shows a configuration 770 of the power stage's switches that operates in the 3-phase mode to provide a voltage conversion ratio of (1/4)X. In the configuration 770, it is seen that switches S_2, S_4 and S_8 are constantly Off, switches

S_1 and S_6 are driven by On their switch driving signals (CLK_1 and CLK_6, respectively) when clock signal Φ_1 is high (and Off whenever Φ_1 is low), switch S_5 is On only when signal Φ_2 is high, switches S_3 and S_{10} are On only when signal Φ_3 is high, switch S_7 is On when either signal Φ_2 or Φ_3 is high (and Off at other times), and switch S_9 is On when either signal Φ_1 or Φ_2 is high (and Off at other times).

[0044] FIG. 7B shows the three alternating circuits 772, 774 and 776 that result from each of the three high clock phases Φ_1, Φ_2 and Φ_3, respectively, that is, the circuit 772 is switched in while Φ_1 is high, the circuit 774 is switched in while Φ_2 is high and the circuit 772 is switched in while Φ_3 is high.

[0045] To summarize the SCPC of FIGS. 7A and 7B, the 3-phase clock is used to drive the switches On and Off (other than the switches S_2, S_4 and S_8, which are constantly turned off). In Φ_1 (that is, Φ_1 is the only high clock signal), the switches S_1, S_6 and S_9 are turned On, connecting the flying capacitors C_1 and C_2 in series between V_{IN} and V_O, giving $V_{IN}=V_{C2}+V_{C1}+V_O$. In Φ_2 (that is, Φ_2 is the only high clock signal), the switches S_5, S_7 and S_9 are turned On, connecting C_1 and C_2 in series between V_O and ground, giving $V_O=V_{C1}-V_{C2}$. During the Φ_3 high clock signal, the switches S_3 and S_{10} are turned On, connecting C_2 in parallel with C_L and $V_O=V_{C2}$. Solving these equations gives $V_O=(1/4)V_{IN}$. Thus, this configuration realizes the voltage conversion ratio of (1/4)X.

[0046] FIG. 8A shows a configuration 880 of the power stage's switches that operates in the 3-phase mode to provide a voltage conversion ratio of (3/4)X. In the configuration 880, it is seen that switches S_2, S_8 and S_{10} are constantly Off, switches S_1 and S_6 are On when signal Φ_1 is high (and Off whenever Φ_1 is low), switch S_5 is On only when signal Φ_2 is high, switches S_3 and S_4 are On only when signal Φ_3 is

high, switch S_9 is On when either signal Φ_1 or Φ_2 is high (and Off at other times), and switch S_7 is On when either signal Φ_2 or Φ_3 is high (and Off at other times)

[0047] FIG. 8B shows the three alternating circuits 882, 884 and 886 that result from each of the three high clock phases Φ_1, Φ_2 and Φ_3, respectively, that is, the circuit 882 exists while Φ_1 is high, the circuit 884 exists while Φ_2 is high and the circuit 882 exists while Φ_3 is high. As is understood, the charging and discharging of the capacitors C1 and C2 as these phases alternate provides a (3/4)X voltage conversion ratio.

[0048] More particularly, in the 3-phase SCPC configuration 880 of FIGS. 8A and 8B, in Φ_1, the switches S_1, S_6 and S_9 are turned On, connecting the flying capacitors C_1 and C_2 in series between V_{IN} and V_O, giving $V_{IN}=V_{C2}+V_{C1}+V_O$. In Φ_2, the switches S_5, S_7 and S_9 are turned On, connecting C_1 and C_2 in series between V_O and ground, giving $V_O=V_{C1}+V_{C2}$. In Φ_3, the switches S_3 and S_4 are turned On, stacking C_2 on top of C_L and $V_O=V_{IN}-V_{C2}$. Solving these equations gives $V_O=(3/4)V_{IN}$. Thus, this configuration 880 realizes the voltage conversion ratio of (3/4)X. The switches S_2, S_8 and S_{10} are constantly turned off.

[0049] FIG. 9A shows an implementation of the switch control logic 106. This functional block provides the driving signals CLK_1 to CLK_{10} for the switches S_1 to S_{10} of the power stage 100, respectively. The exemplified switch control logic 106 has four input signals comprising the three clock signals Φ_1, Φ_2 and Φ_3 from the 2-/3-phase clock generator 104 (FIG. 1), and the voltage conversion ratio (VCR) signal.

[0050] The voltage conversion ratio signal determines the paths of the clock signals (Φ_1, Φ_2 and Φ_3) to the driving signals (CLK_1 to CLK_{10}). For example, when the voltage conversion ratio is 1X, CLK_1 corresponds to Φ_1 and CLK_2 corresponds to Φ_2,

meaning that the gate of the switch S_1 is in essence driven by Φ_1, and the gate of the switch S_2 is in essence driven by Φ_2. At the same time, $CLK_{4,5,6,8,9}=0$ and $CLK_{3,7,10}=1$, meaning that the switches S_4, S_5, S_6, S_8 and S_9 are constantly turned off, and the switches S_3, S_7 and S_{10} are constantly turned on. The voltage conversion ratio input may be obtained at the switch control logic as a value or the like (e.g., a bit pattern on three input lines or a pulsed pattern on one input line or the like can specify which one of the six ratios is desired, and possibly also used to specify a desired zero output state) from any suitable source, such as one or more power management units of a device that need to provide different power-supply voltages for different functional blocks.

[0051] The overall mapping of CLK_1 to CLK_{10} with voltage conversion ratios is summarized in Table I, replicated in FIG. 9B.

TABLE I. Clock selection of the switch control logic with voltage conversion ratios:

Switches	1/1X	2/3X	1/2X	1/3X	3/4X	1/4X
CLK_1 (S_1)	Φ_1	Φ_2	Φ_1	Φ_1	Φ_1	Φ_1
CLK_2 (S_2)	Φ_2	Φ_1	Φ_2	0	0	0
CLK_3 (S_3)	1	Φ_1	1	Φ_1	Φ_3	Φ_3
CLK_4 (S_4)	0	Φ_1	Φ_1	0	Φ_3	0
CLK_5 (S_5)	0	0	0	Φ_2	Φ_2	Φ_2
CLK_6 (S_6)	0	Φ_2	0	0	Φ_1	Φ_1
CLK_7 (S_7)	1	Φ_1	Φ_2	Φ_2	$\Phi_{2,3}$	$\Phi_{2,3}$
CLK_8 (S_8)	0	0	Φ_1	Φ_1	0	0
CLK_9 (S_9)	0	Φ_2	0	Φ_2	$\Phi_{1,2}$	$\Phi_{1,2}$
CLK_{10} (S_{10})	1	0	1	Φ_1	0	Φ_3

[0052] FIG. 10A shows one implementation of the 2-/3-phase clock generator 104 and FIG. 10B shows its timing diagram. The 2-/3-phase clock generator 104

comprises two D-flip-flops 1010 and 1012, three NAND gates 1014 - 1016, one INV gate 1018 and one XNOR gate 1022. The input signals include the system clock CLK and the 2/3SEL selection bit. The 2/3 SEL selection bit selects whether the clock generator provides the 2-phase clock or the 3-phase clock. The clock signals Φ_1, Φ_2 and Φ_3 are used to control the switches of the power stage as described herein.

[0053] More particularly, the exemplified 2-/3-phase clock generator 104 is designed as a finite state machine using two D flip-flops1010 and 1012. This finite state machine is driven by the system clock signal CLK. The clock signals Φ_1, Φ_2 and Φ_3 are connected to the switch control logic. The selection signal 2/3SEL decides the type of clock signals that the clock generator 104 provides. When 2/3SEL is low, the 2-phase clock signals Φ_1, Φ_2 are available; Φ_1 and Φ_2 are complementary and have 180 degrees phase shift. When 2/3SEL is high, the 3-phase clock signals Φ_1, Φ_2 and Φ_3 are available; Φ_1, Φ_2 and Φ_3 are shifted by 120 degrees with respect to each other.

[0054] FIG. 10B shows the timing diagram of the 2-/3-phase clock generator 104 of FIG. 10A. As is seen, in the two-phase mode, which in this example occurs when the 2/3 selection bit is low, clock signal Φ_3 is always low, while Φ_1 is high and Φ_2 low for one full clock cycle, followed by Φ_1 low and Φ_2 high for the next clock cycle, and so on in an alternating signal pattern. Note that the concepts of “high” and “low” can be reversed with appropriate inverter(s), such as with respect to the SEL bit value; (e.g., instead of what is shown in the example of FIG. 10B, the two-phase mode may exist when the SEL bit is low instead of high, and vice-versa), and thus it is understood that such values are only examples herein.

[0055] In the three-phase mode, which in this example occurs when the 2/3 selection bit is high, clock signal Φ_1 is high while Φ_2 and Φ_3 are low for one full clock cycle, then clock signal Φ_2 is high while Φ_1 and Φ_3 are low for the next full clock cycle, then clock signal Φ_3 is high while Φ_1 and Φ_2 are low for the next full clock cycle, followed by Φ_1 again high and so on in an alternating three-phase signal pattern. Note that in this example implementation, only one clock signal Φ_1, Φ_2 or Φ_3 is high at any time.

[0056] FIG.11 shows the theoretical efficiencies versus $V_O/((m/n)V_{IN})$ of the 2-phase SCPC, the 2-/3-phase SCPC and the ideal low dropout regulator (LDO). The 2-phase SCPC and the 2-/3-phase SCPC both have two flying capacitors. As the 2-/3-phase SCPC can realize the extra voltage conversion ratios of (1/4)X and (3/4)X, when $V_O/V_{IN}=0.3$ and $V_O/V_{IN}=0.7$, the efficiency can be improved by 25% and 22%, respectively. Note that for a 2-phase-only SCPC to realize (1/4)X and (3/4)X conversion ratios, such an SCPC needs three flying capacitors and fourteen switches; hence, the 2-/3-phase SCPC described herein is more component efficient with respect to capacitors and switches.

[0057] FIG. 12 describes the general operations in the form of a flow diagram. Note that the logic of FIG. 12 is ordinarily implemented in fixed hardware as generally described herein, although it is feasible to implement at least some parts of the SCPC in coded logic, e.g., by having a processor execute programmed instructions.

[0058] The logic begins at step 1202 where the specified voltage conversion ratio is obtained, e.g., via the conversion ratio's input line or lines of FIG. 9A. As set forth above, such a ration may be specified as a value from a power management unit or the like of a device that uses (is coupled to or incorporates) the SCPC.

[0059] Step 1204 represents setting the 2/3-phase selector (2/3 SEL) bit based upon the desired conversion ratio. Note that this may be done in the SCPC logic (for 1/4X or 3/4X, set the 2/3 SEL bit = 1, otherwise set the SEL bit = 0 (for 1/1X, 2/3X, 1/2X, 1/3X)). Alternatively, this bit value may be controlled by an external mechanism, such as the power management unit; for example, if using three bits to specify the conversion ratio, the most significant bit also may be used as the 2/3 SEL bit, with the two least two significant bits used to distinguish between the four two-phase conversion ratios when the 2/3 SEL bit is low, and (one of the least significant bits) used to distinguish between the two three-phase conversion ratios when the 2/3 SEL bit is high.

[0060] Step 1206 represents selecting the desired configuration, e.g., corresponding to the switch settings / clock signal couplings set forth in Table I (FIG. 9B). Step 1208 then drives the clocked switches to alternate between the two clock phases in the two-phase mode or the three clock phases in the three-phase mode. As described above, the active circuit portions of the configuration are switched in and switched out according to the alternating clock phases.

[0061] Step 1210 represents continuing the driving of the clocked switches until the specified voltage conversion ratio changes. At such a change, the logic of FIG. 12 repeats to produce the new specified voltage conversion ratio.

[0062] As can be seen, using as little as two flying capacitors, the 2-/3-phase reconfigurable SCPC can realize six selectable voltage conversion ratios. In one or more implementations comprising two flying capacitors, ten switches are controlled in two-phase operation or three-phase operation to provide the various configurations that result in the six selectable voltage conversion ratios.

[0063] One or more aspects are directed towards a switched-capacitor power converter for conversion of an input voltage to an output voltage according to a specified voltage conversion ratio of a plurality of realizable voltage conversion ratios. The switched-capacitor power converter comprises a power stage comprising flying capacitors and a plurality of logic-controlled switches coupled to the flying capacitors. A multiple clock phase generator of the switched-capacitor power converter is configured to output switching signals in different, selectable clock phases, each of the different, selectable clock phases comprising alternating switching signals, wherein one of the different, selectable clock phases is selected based upon the specified voltage conversion ratio. The switched-capacitor power converter also comprises switch control logic coupled to the multiple clock phase generator and coupled to the set of logic-controlled switches to configure switch couplings to the flying capacitors of the power stage, comprising for each switch of the set of logic-controlled switches, to turn on the switch, turn off the switch or control an on or off state of the switch according to at least one of the alternating switching signals, wherein the switch control logic is arranged to configure alternating active circuits, corresponding to the alternating switching signals, that charge or discharge respective ones of the flying capacitors to provide the output voltage according to the specified voltage conversion ratio.

[0064] The multiple clock phase generator may generate a two-phase clock comprising two alternating switching signals of the alternating switching signals to configure two alternating active circuits of the alternating active circuits when the two-phase clock is selected, or may generate a three-phase clock comprising three alternating switching signals of the alternating switching signals to configure three alternating active circuits of the alternating active circuits when the three-phase clock

is selected. At least one of the set of logic-controlled switches is controlled to turn on for two of the three alternating switching signals when the three-phase clock is selected.

[0065] In one or more implementations, the power stage comprises two flying capacitors, the set of logic-controlled switches comprises ten logic-controlled switches, and the plurality of realizable voltage conversion ratios comprises six different realizable voltage conversion ratios.

[0066] The multiple clock phase generator may generate a two-phase clock comprising two alternating switching signals of the alternating switching signals and a three-phase clock comprising three alternating switching signals of the alternating switching signals. When the power stage comprises two flying capacitors, and the set of logic-controlled switches comprises ten logic-controlled switches, the plurality of realizable voltage conversion ratios comprises six different realizable voltage conversion ratios. Two different realizable voltage conversion ratios, of the six different realizable voltage conversion ratios, that are realizable when the three-phase clock is selected, comprise a 1/4 voltage conversion ratio, and a 3/4 voltage conversion ratio. Four different realizable voltage conversion ratios, of the six different realizable voltage conversion ratios, are realizable when the two-phase clock is selected and two different realizable voltage conversion ratios, of the six different realizable voltage conversion ratios, are realizable when the three-phase clock is selected. The four different realizable voltage conversion ratios realizable when the two-phase clock is selected comprise a 1/1 voltage conversion ratio, a 2/3 voltage conversion ratio, a 1/2 voltage conversion ratio and a 1/3 voltage conversion ratio.

[0067] The set of logic-controlled switches may comprise a set of metal oxide semiconductor transistors.

[0068] One or more aspects are directed towards obtaining first input specifying a first voltage conversion ratio, configuring a switched capacitor power converter according to a first configuration, comprising selecting a two-phase clock comprising two alternating clock signals, and for each switch of a plurality of switches of the switched-capacitor power converter, at least one of turning on the switch, turning off the switch, or driving the switch to alternate between on and off states based on one of the two alternating clock signals, wherein the first configuration results in the first voltage conversion ratio, and outputting a first output voltage by coupling an input voltage to an output through the first configuration. Aspects include obtaining second input specifying a second voltage conversion ratio, configuring the switched capacitor power converter according to a second configuration, comprising selecting a three-phase clock comprising three alternating clock signals, and for each switch of the plurality of switches of the switched-capacitor power converter, turning on the switch, turning off the switch, or driving the switch between the on and off states based on at least one of the three alternating clock signals, wherein the second configuration results in the second voltage conversion ratio, and outputting a second output voltage by coupling the input voltage to the output through the second configuration.

[0069] Configuring the switched capacitor power converter according to the first configuration may comprise alternating between coupling the output to a first alternating circuit corresponding to a first alternating clock signal of the two alternating clock signals and a second alternating circuit corresponding to a second alternating clock signal of the two alternating clock signals.

[0070] Configuring the switched capacitor power converter according to the second configuration may comprise alternating between coupling the output to a first alternating circuit corresponding to a first alternating clock signal of the three alternating clock signals, a second alternating circuit corresponding to a second alternating clock signal of the three alternating clock signals, and a third alternating circuit corresponding to a third alternating clock signal of the three alternating clock signals.

[0071] For at least one switch of the plurality of switches in the second configuration, described herein in one or more implementations is driving a first switch between the on and off states based on at least one of the three alternating clock signals This may comprise driving the first switch to the on state for first and second alternating clock signals of the three alternating clock signals, and for a second switch of the plurality of switches in the second configuration, driving the second switch between the on and off states for a third alternating clock signal of the three alternating clock signals.

[0072] One or more aspects are directed towards a switched-capacitor power converter, comprising a capacitor set comprising flying capacitors, a set of logic-controlled switches coupled to the capacitor set, and a two-phase, three-phase clock generator configured to output two alternating switching signals in a two-phase mode of operation and output three alternating switching signals in a three-phase mode of operation. Switch control logic is coupled to the two-phase, three-phase clock generator and is coupled to control respective switches of the set of logic-controlled switches into respective on states, into respective off states, or into respective alternating on and off states corresponding to one of the two alternating switching signals in the two-phase mode of operation or corresponding to one or two of the

three alternating switching signals in the three-phase mode of operation. The switch control logic is configured to select a switch configuration and use the two-phase mode of operation or the three-phase mode of operation based on a specified voltage conversion ratio to be achieved by the switched-capacitor power converter.

[0073] The switch control logic may use the two-phase mode of operation and may configure the switch configuration to provide two alternating circuits corresponding to the two alternating switching signals, wherein the two alternating circuits charge or discharge the capacitor set to output an output voltage based on an input voltage and the specified voltage conversion ratio.

[0074] The switch control logic may use the three-phase mode of operation and may configure the switch configuration to provide three alternating circuits corresponding to the three alternating switching signals, wherein the three alternating circuits charge or discharge the capacitor set to output an output voltage based on an input voltage and the specified voltage conversion ratio.

[0075] The specified voltage conversion ratio may comprise an input value that is used by the two-phase, three-phase clock generator to select either the two-phase mode of operation or the three-phase mode of operation.

[0076] The capacitor set may comprise two flying capacitors and the set of logic-controlled switches may comprise ten switches, wherein six different, non-zero voltage conversion ratios, comprising the specified voltage conversion ratio, are realizable by the switched-capacitor power converter.

[0077] At least six different, non-zero voltage conversion ratios, comprising the specified voltage conversion ratio, are realizable by the switched-capacitor power converter, wherein at least four different non-zero voltage conversion ratios of the at

least six different, non-zero voltage conversion ratios are realizable in the two-phase mode of operation, and wherein at least two different non-zero voltage conversion ratios of the at least six different, non-zero voltage conversion ratios are realizable in the three-phase mode of operation.

[0078] The set of logic-controlled switches of the switched-capacitor power converter may comprise a set of metal oxide semiconductor transistors.

CONCLUSION

[0079] While the invention is susceptible to various modifications and alternative constructions, certain illustrated implementations thereof are shown in the drawings and have been described above in detail. It should be understood, however, that there is no intention to limit the invention to the specific forms disclosed, but on the contrary, the intention is to cover all modifications, alternative constructions, and equivalents falling within the spirit and scope of the invention.

[0080] In addition to the various implementations described herein, it is to be understood that other similar implementations can be used or modifications and additions can be made to the described implementation(s) for performing the same or equivalent function of the corresponding implementation(s) without deviating therefrom. Accordingly, the invention is not to be limited to any single implementation, but rather is to be construed in breadth, spirit and scope in accordance with the appended claims.

WHAT IS CLAIMED IS:

1. A system, comprising:

a switched-capacitor power converter for conversion of an input voltage to an output voltage according to a specified voltage conversion ratio of a plurality of realizable voltage conversion ratios, the switched-capacitor power converter comprising:

a power stage comprising flying capacitors and a plurality of logic-controlled switches coupled to the flying capacitors;

a multiple clock phase generator configured to output switching signals in different, selectable clock phases, each of the different, selectable clock phases comprising alternating switching signals, wherein one of the different, selectable clock phases is selected based upon the specified voltage conversion ratio; and

switch control logic coupled to the multiple clock phase generator and coupled to the set of logic-controlled switches to configure switch couplings to the flying capacitors of the power stage, comprising for each switch of the set of logic-controlled switches, to turn on the switch, turn off the switch or control an on or off state of the switch according to at least one of the alternating switching signals, wherein the switch control logic is arranged to configure alternating active circuits, corresponding to the alternating switching signals, that charge or discharge respective ones of the flying capacitors to provide the output voltage according to the specified voltage conversion ratio.

2. The system of claim 1, wherein the multiple clock phase generator generates a two-phase clock comprising two alternating switching signals of the alternating switching signals to configure two alternating active circuits of the

alternating active circuits when the two-phase clock is selected, or generates a three-phase clock comprising three alternating switching signals of the alternating switching signals to configure three alternating active circuits of the alternating active circuits when the three-phase clock is selected.

3. The system of claim 2, wherein at least one of the set of logic-controlled switches is controlled to turn on for two of the three alternating switching signals when the three-phase clock is selected.

4. The system of claim 1, wherein the power stage comprises two flying capacitors, wherein the set of logic-controlled switches comprises ten logic-controlled switches, and wherein the plurality of realizable voltage conversion ratios comprises six different realizable voltage conversion ratios.

5. The system of claim 1, wherein the multiple clock phase generator generates a two-phase clock comprising two alternating switching signals of the alternating switching signals and a three-phase clock comprising three alternating switching signals of the alternating switching signals, wherein the power stage comprises two flying capacitors, wherein the set of logic-controlled switches comprises ten logic-controlled switches, and wherein the plurality of realizable voltage conversion ratios comprises six different realizable voltage conversion ratios.

6. The system of claim 5, wherein two different realizable voltage conversion ratios, of the six different realizable voltage conversion ratios, that are realizable when the three-phase clock is selected, comprise a 1/4 voltage conversion ratio, and a 3/4 voltage conversion ratio.

7. The system of claim 5, wherein four different realizable voltage conversion ratios, of the six different realizable voltage conversion ratios, are realizable when the two-phase clock is selected and two different realizable voltage conversion ratios, of the six different realizable voltage conversion ratios, are realizable when the three-phase clock is selected.

8. The system of claim 7, wherein the four different realizable voltage conversion ratios realizable when the two-phase clock is selected comprise a 1/1 voltage conversion ratio, a 2/3 voltage conversion ratio, a 1/2 voltage conversion ratio and a 1/3 voltage conversion ratio.

9. The system of claim 1, wherein the set of logic-controlled switches comprises a set of metal oxide semiconductor transistors.

10. A method, comprising:

obtaining first input specifying a first voltage conversion ratio;

configuring a switched capacitor power converter according to a first configuration, comprising selecting a two-phase clock comprising two alternating clock signals, and for each switch of a plurality of switches of the switched-capacitor power converter, at least one of turning on the switch, turning off the switch, or driving the switch to alternate between on and off states based on one of the two alternating clock signals, wherein the first configuration results in the first voltage conversion ratio;

outputting a first output voltage by coupling an input voltage to an output through the first configuration;

obtaining second input specifying a second voltage conversion ratio;

configuring the switched capacitor power converter according to a second configuration, comprising selecting a three-phase clock comprising three alternating clock signals, and for each switch of the plurality of switches of the switched-capacitor power converter, turning on the switch, turning off the switch, or driving the switch between the on and off states based on at least one of the three alternating clock signals, wherein the second configuration results in the second voltage conversion ratio; and

outputting a second output voltage by coupling the input voltage to the output through the second configuration.

11. The method of claim 10, wherein configuring the switched capacitor power converter according to the first configuration comprises alternating between coupling the output to a first alternating circuit corresponding to a first alternating clock signal of the two alternating clock signals and a second alternating circuit corresponding to a second alternating clock signal of the two alternating clock signals.

12. The method of claim 10, wherein configuring the switched capacitor power converter according to the second configuration comprises alternating between coupling the output to a first alternating circuit corresponding to a first alternating clock signal of the three alternating clock signals, a second alternating circuit corresponding to a second alternating clock signal of the three alternating clock signals, and a third alternating circuit corresponding to a third alternating clock signal of the three alternating clock signals.

13. The method of claim 10, wherein, for at least one switch of the plurality of switches in the second configuration, driving a first switch between the on and off states based on at least one of the three alternating clock signals comprises driving the first switch to the on state for first and second alternating clock signals of the three alternating clock signals, and for a second switch of the plurality of switches in the second configuration, driving the second switch between the on and off states for a third alternating clock signal of the three alternating clock signals.

14. A switched-capacitor power converter, comprising:

a capacitor set comprising flying capacitors;

a set of logic-controlled switches coupled to the capacitor set;

a two-phase, three-phase clock generator configured to output two alternating switching signals in a two-phase mode of operation and output three alternating switching signals in a three-phase mode of operation; and

switch control logic coupled to the two-phase, three-phase clock generator and coupled to control respective switches of the set of logic-controlled switches into respective on states, into respective off states, or into respective alternating on and off states corresponding to one of the two alternating switching signals in the two-phase mode of operation or corresponding to one or two of the three alternating switching signals in the three-phase mode of operation, wherein the switch control logic is configured to select a switch configuration and use the two-phase mode of operation or the three-phase mode of operation based on a specified voltage conversion ratio to be achieved by the switched-capacitor power converter.

15. The switched-capacitor power converter of claim 14, wherein the switch control logic uses the two-phase mode of operation and configures the switch configuration to provide two alternating circuits corresponding to the two alternating switching signals, and wherein the two alternating circuits charge or discharge the capacitor set to output an output voltage based on an input voltage and the specified voltage conversion ratio.

16. The switched-capacitor power converter of claim 14, wherein the switch control logic uses the three-phase mode of operation and configures the switch configuration to provide three alternating circuits corresponding to the three alternating switching signals, wherein the three alternating circuits charge or discharge the capacitor set to output an output voltage based on an input voltage and the specified voltage conversion ratio.

17. The switched-capacitor power converter of claim 14, wherein the specified voltage conversion ratio comprises an input value that is used by the two-phase, three-phase clock generator to select either the two-phase mode of operation or the three-phase mode of operation.

18. The switched-capacitor power converter of claim 14, wherein the capacitor set comprises two flying capacitors, wherein the set of logic-controlled switches comprises ten switches, and wherein six different, non-zero voltage conversion ratios, comprising the specified voltage conversion ratio, are realizable by the switched-capacitor power converter.

19. The switched-capacitor power converter of claim 18, wherein at least six different, non-zero voltage conversion ratios, comprising the specified voltage conversion ratio, are realizable by the switched-capacitor power converter, wherein at least four different non-zero voltage conversion ratios of the at least six different, non-zero voltage conversion ratios are realizable in the two-phase mode of operation, and wherein at least two different non-zero voltage conversion ratios of the at least six different, non-zero voltage conversion ratios are realizable in the three-phase mode of operation.

20. The switched-capacitor power converter of claim 18, wherein the set of logic-controlled switches comprises a set of metal oxide semiconductor transistors.

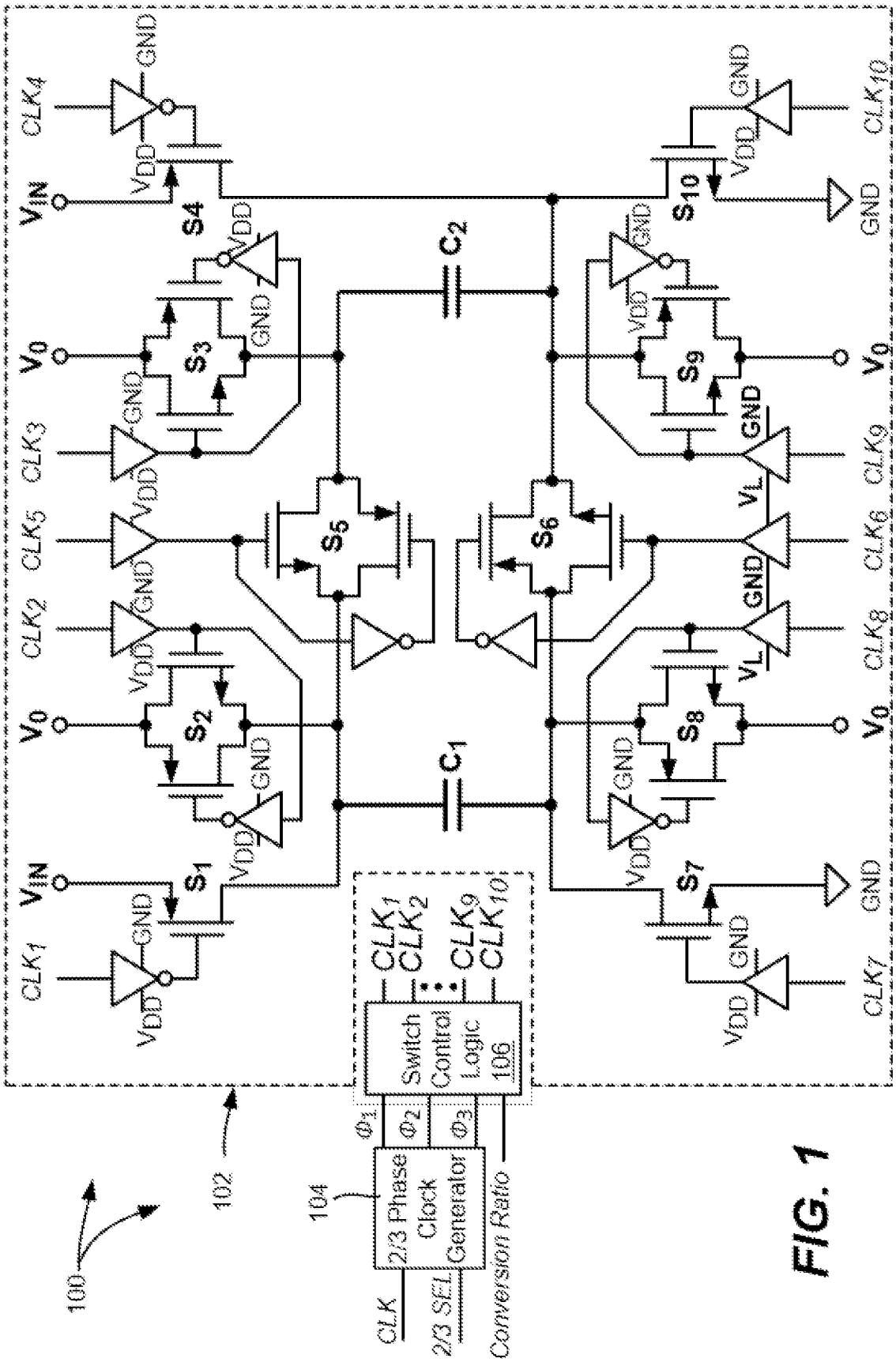
100
102
104
2/3 Phase Clock Generator
CLK
2/3 SEL
Conversion Ratio
Switch Control Logic 106
Φ1
Φ2
Φ3
CLK1
CLK2
CLK9
CLK10
VIN
V0
VL
VDD
GND
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
C1
C2
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
CLK8
CLK9
CLK10

FIG. 1

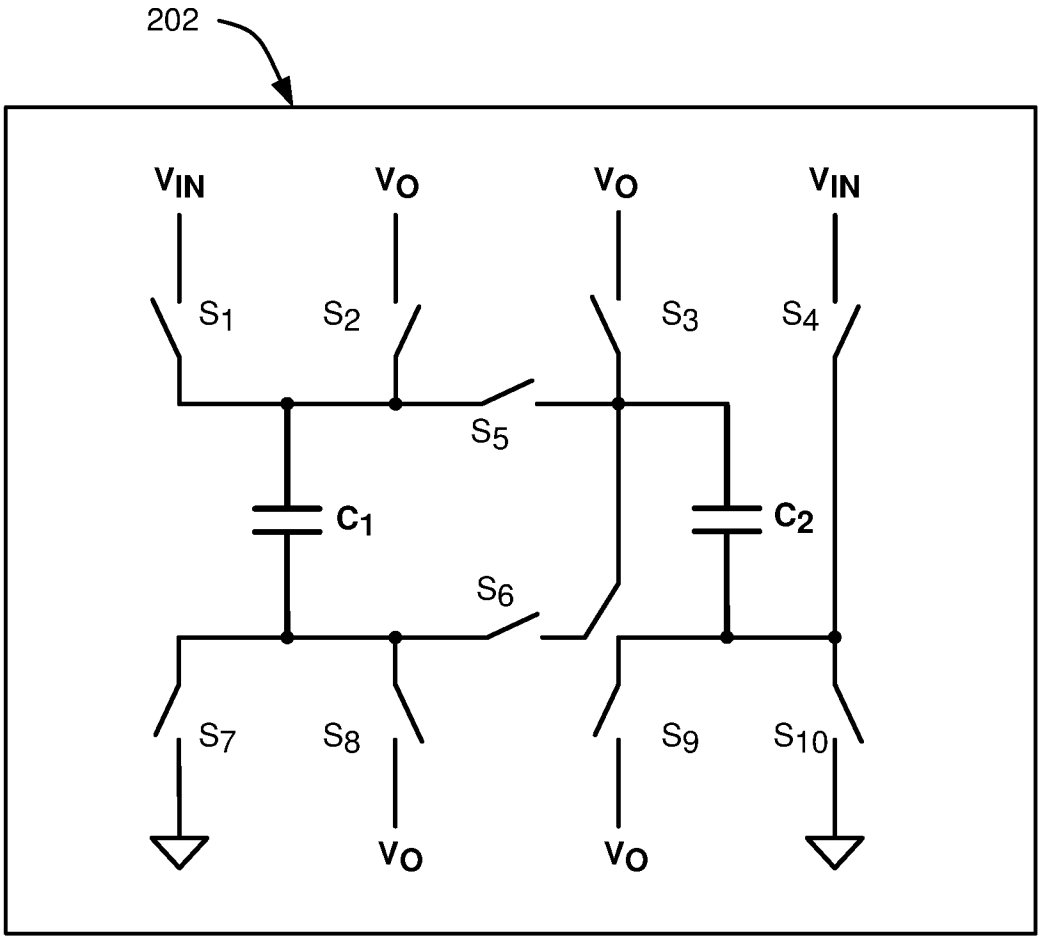

FIG. 2

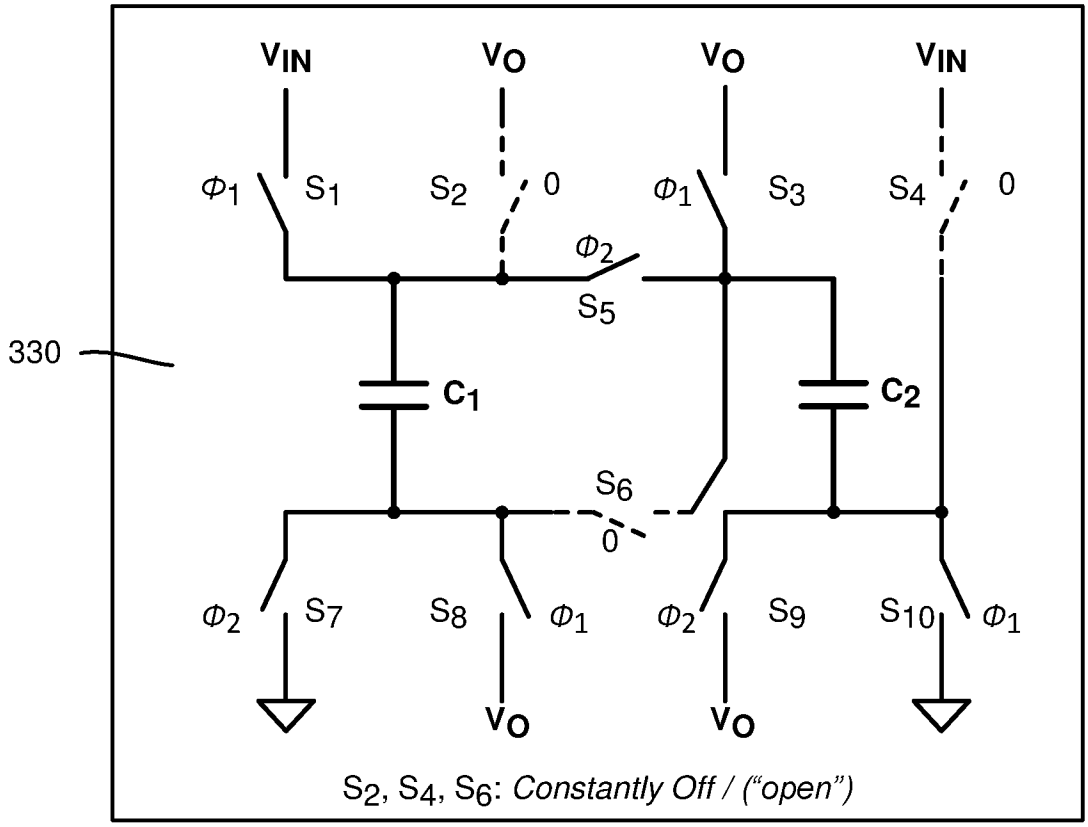
VIN
VO
VO
VIN
Φ1
S1
S2
0
Φ1
S3
S4
0
Φ2
S5
330
C1
C2
S6
0
Φ2
S7
S8
Φ1
Φ2
S9
S10
Φ1
VO
VO
S2, S4, S6: Constantly Off / ("open")

FIG. 3A

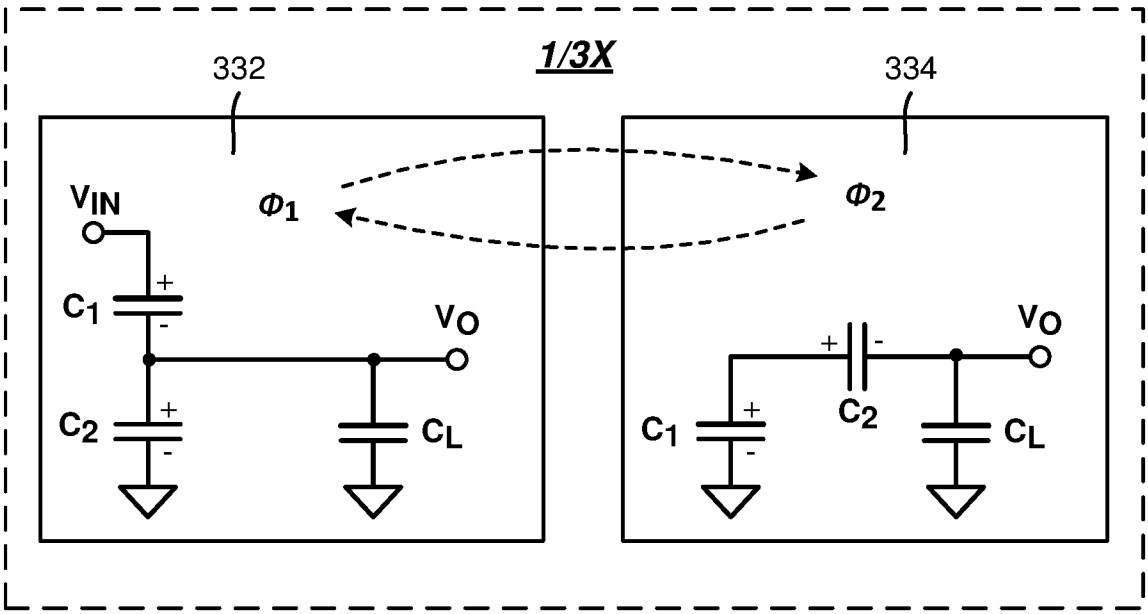
1/3X
332
334
VIN
Φ1
Φ2
C1
VO
C2
CL
C1
C2
VO
CL

FIG. 3B

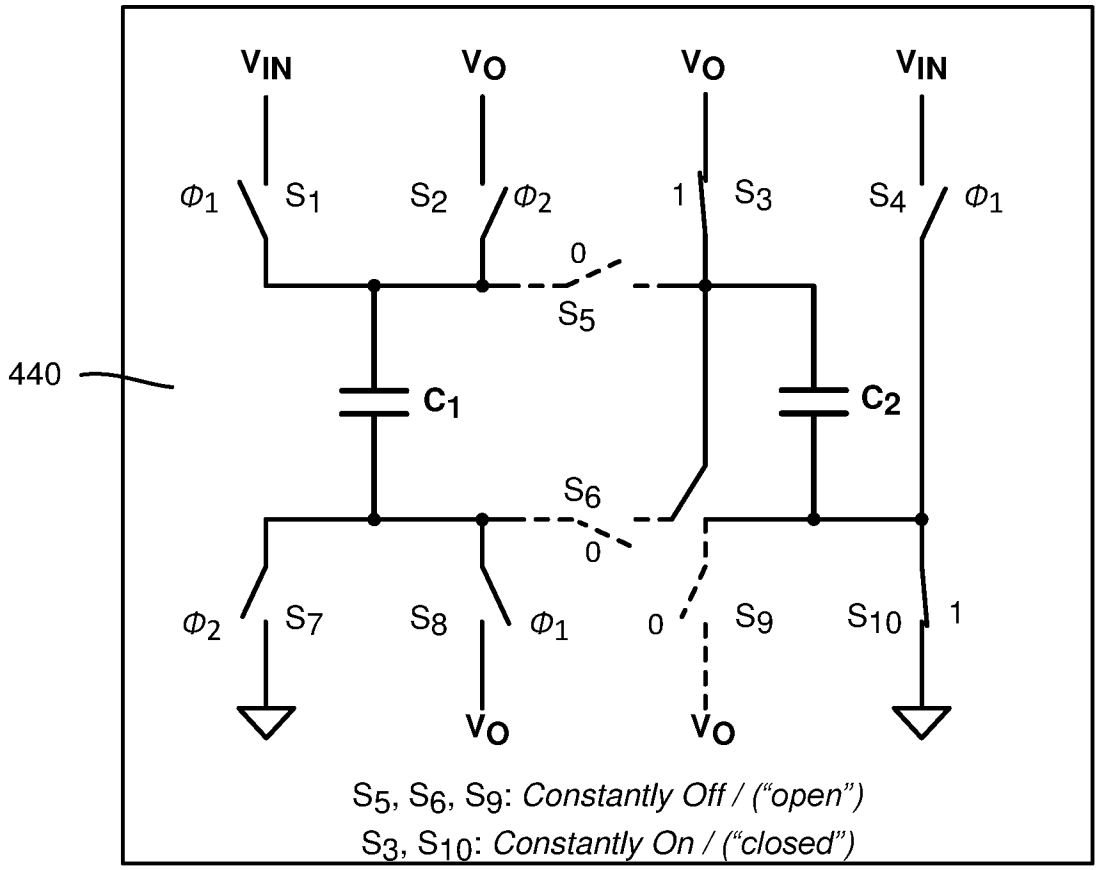
VIN
VO
VO
VIN
Φ1
S1
S2
Φ2
1
S3
S4
Φ1
0
S5
440
C1
C2
S6
0
Φ2
S7
S8
Φ1
0
S9
S10
1
VO
VO
S5, S6, S9: Constantly Off / ("open")
S3, S10: Constantly On / ("closed")

FIG. 4A

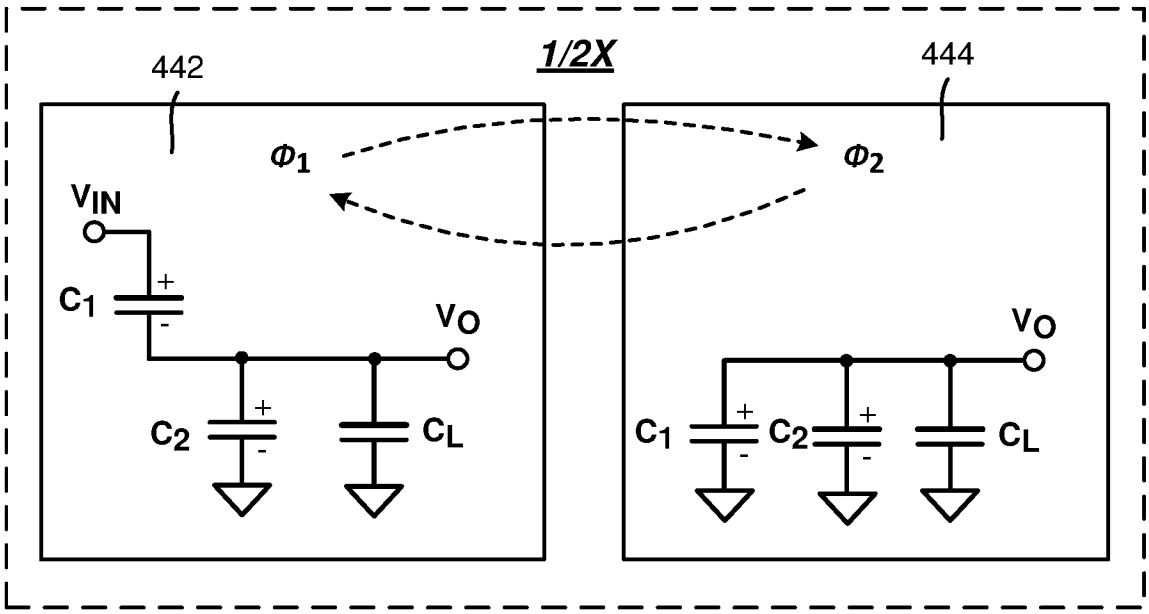
1/2X
442
444
Φ1
Φ2
VIN
C1
VO
C2
CL
C1
C2
CL
VO

FIG. 4B

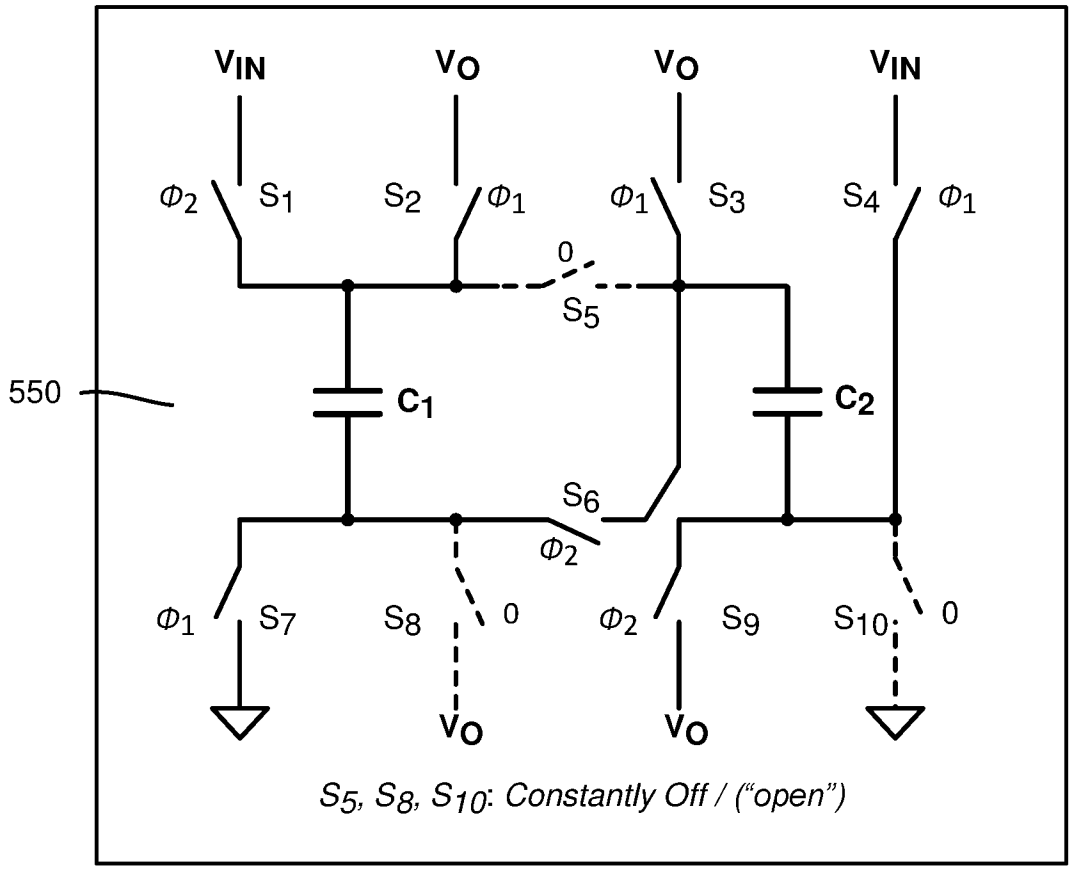
VIN
VO
VO
VIN
Φ2
S1
S2
Φ1
Φ1
S3
S4
Φ1
0
S5
550
C1
C2
S6
Φ2
Φ1
S7
S8
0
Φ2
S9
S10
0
VO
VO
S5, S8, S10: Constantly Off / ("open")

FIG. 5A

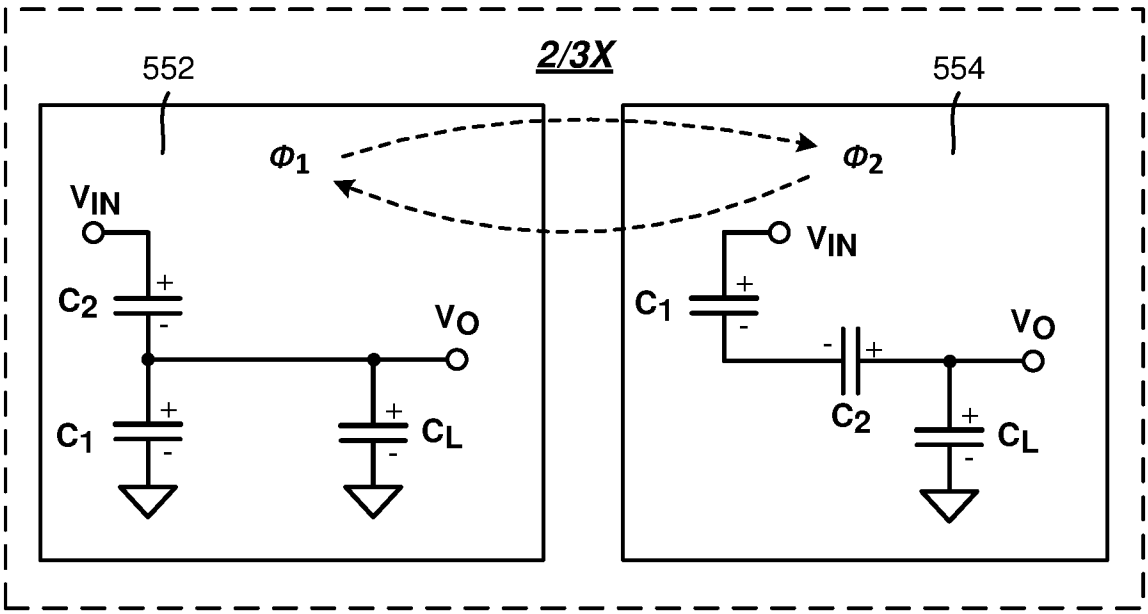
2/3X
552
554
Φ1
Φ2
VIN
C2
VO
C1
CL
VIN
C1
VO
C2
CL

FIG. 5B

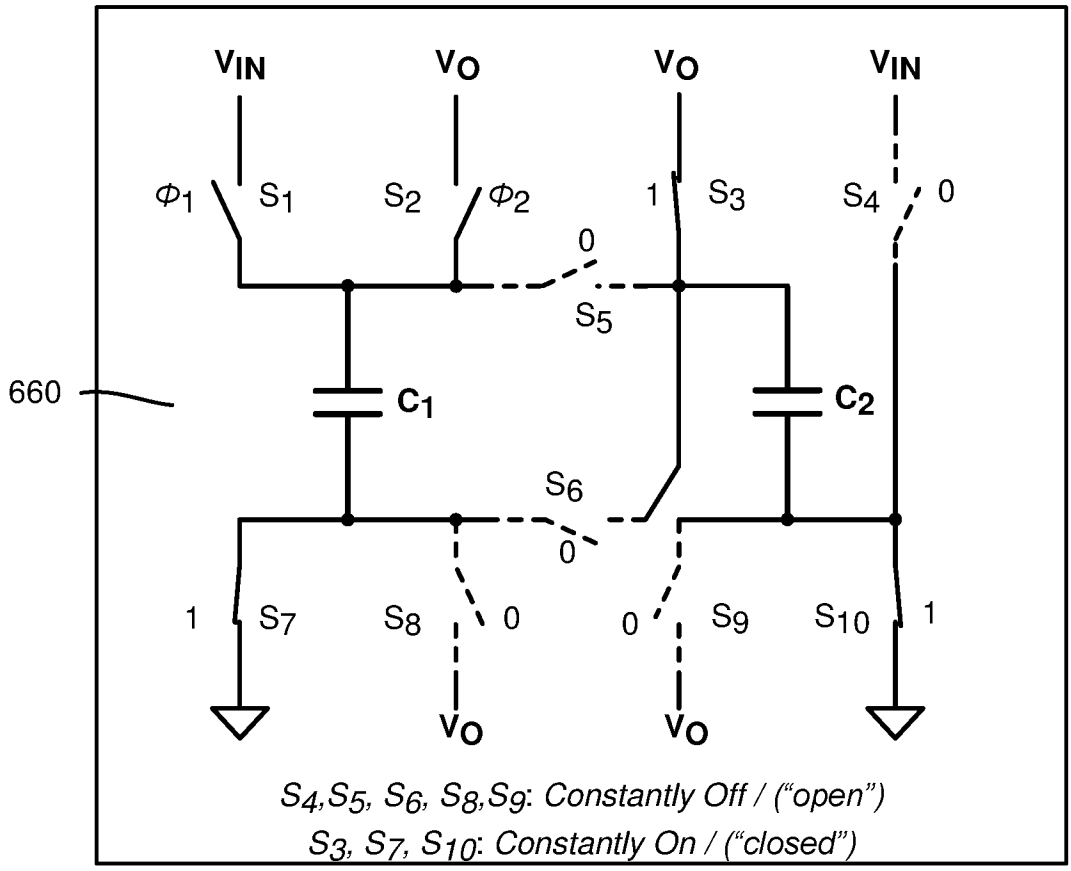
VIN
VO
VO
VIN
Φ1
S1
S2
Φ2
1
S3
S4
0
0
S5
660
C1
C2
S6
0
1
S7
S8
0
0
S9
S10
1
VO
VO
S4,S5, S6, S8,S9: Constantly Off / ("open")
S3, S7, S10: Constantly On / ("closed")

FIG. 6A

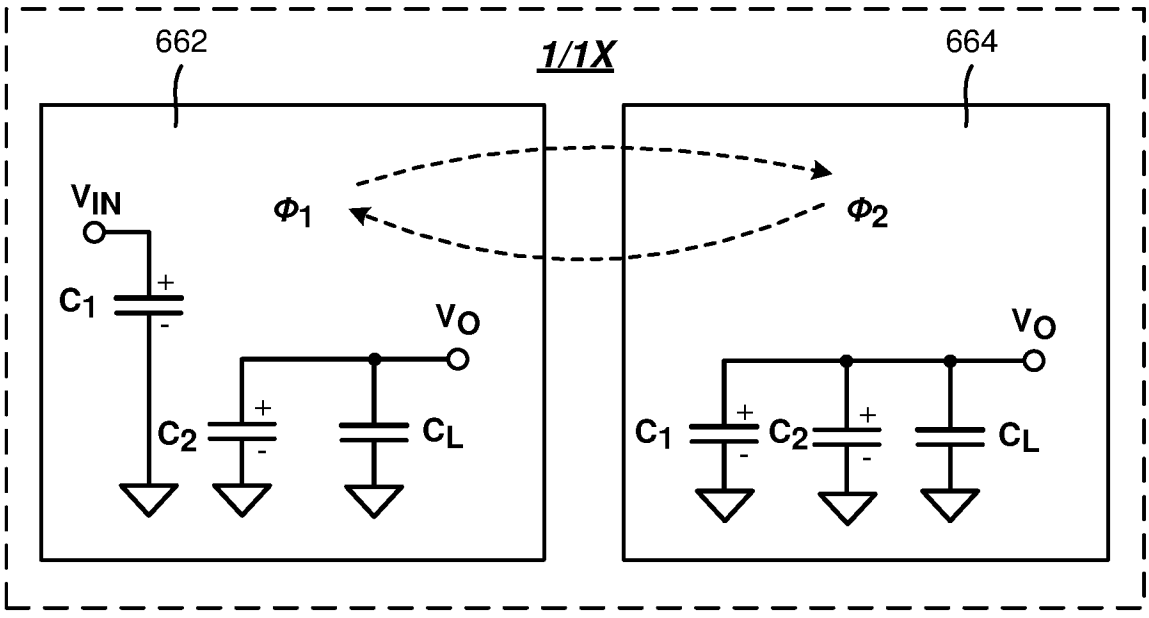
662
1/1X
664
VIN
Φ1
Φ2
C1
VO
C2
CL
C1
C2
CL
VO

FIG. 6B

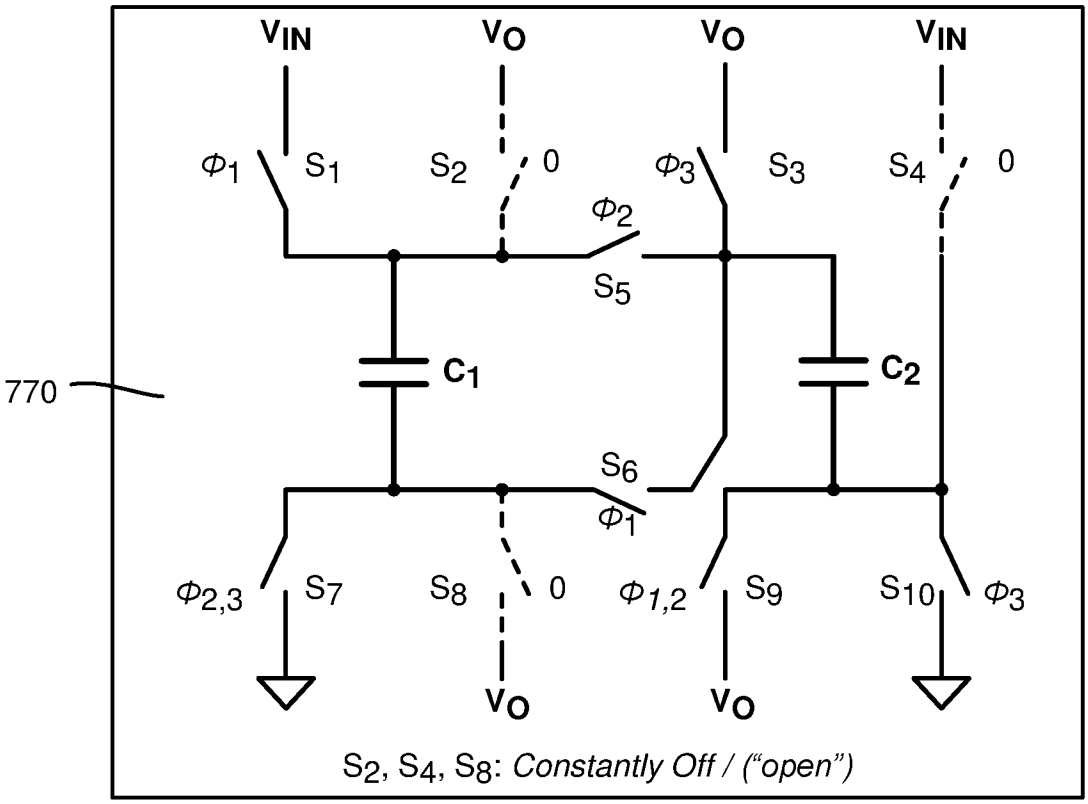
VIN
VO
VO
VIN
Φ1
S1
S2
0
Φ3
S3
S4
0
Φ2
S5
C1
C2
770
S6
Φ1
Φ2,3
S7
S8
0
Φ1,2
S9
S10
Φ3
VO
VO
S2, S4, S8: Constantly Off / ("open")

FIG. 7A

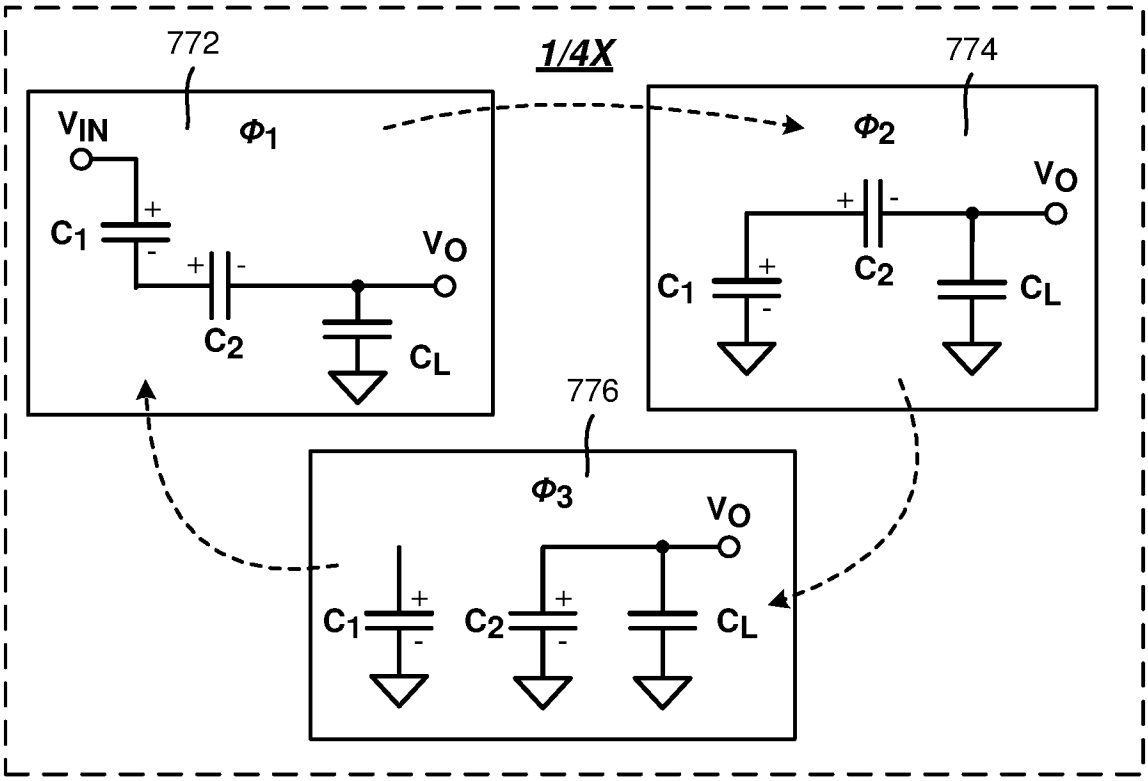
772
1/4X
774
VIN
Φ1
C1
VO
C2
CL
Φ2
VO
C1
C2
CL
776
Φ3
VO
C1
C2
CL

FIG. 7B

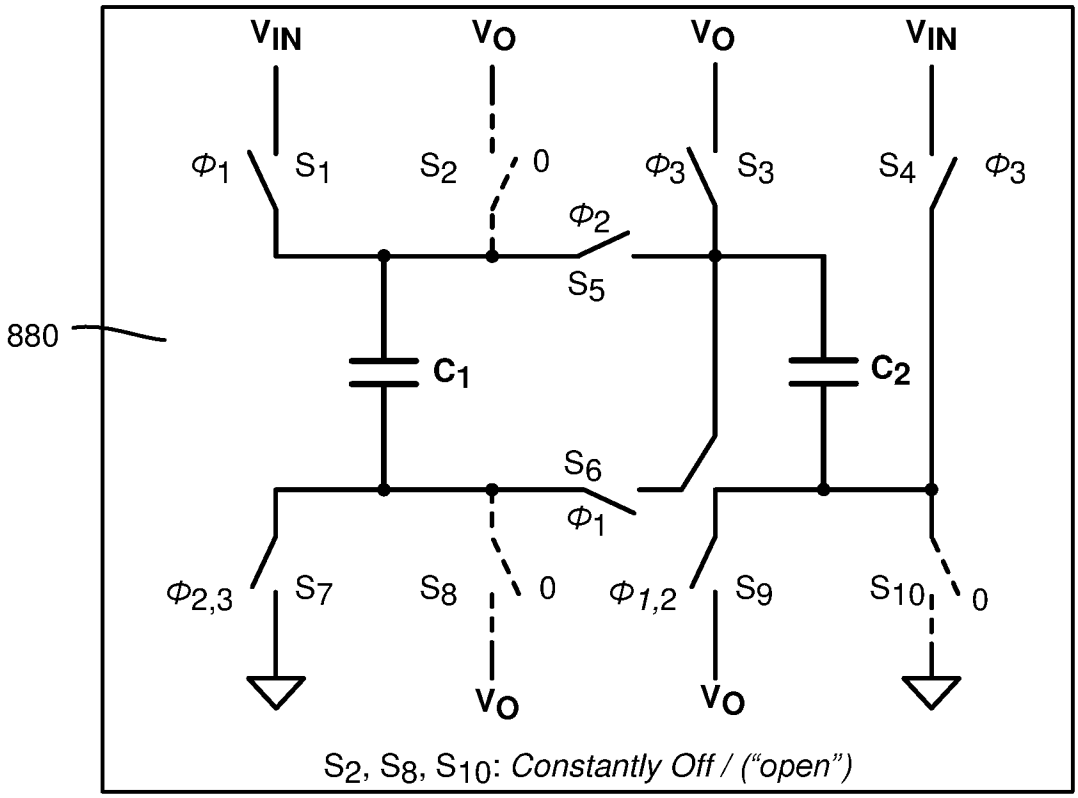
VIN
VO
VO
VIN
Φ1
S1
S2
0
Φ3
S3
S4
Φ3
Φ2
S5
880
C1
C2
S6
Φ1
Φ2,3
S7
S8
0
Φ1,2
S9
S10
0
VO
VO
S2, S8, S10: Constantly Off / ("open")

FIG. 8A

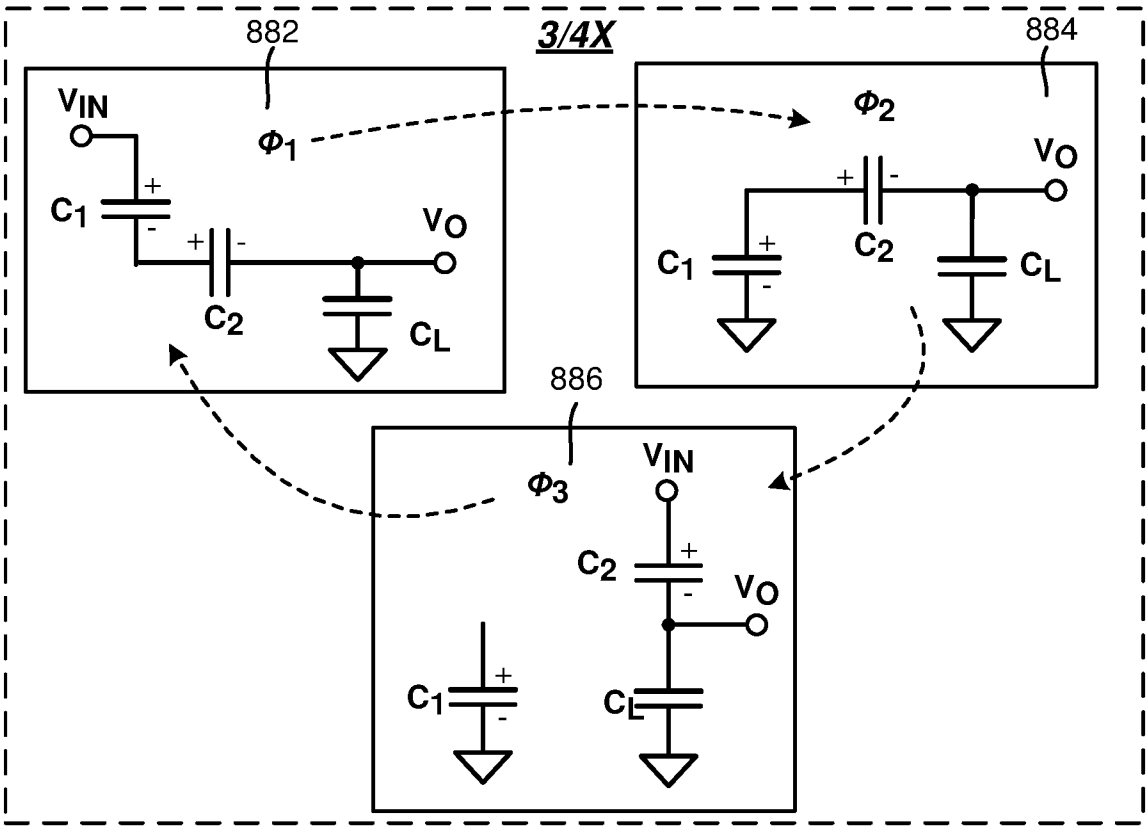
882
3/4X
884
VIN
Φ1
Φ2
VO
C1
C2
VO
C1
C2
CL
CL
886
Φ3
VIN
C2
VO
C1
CL

FIG. 8B

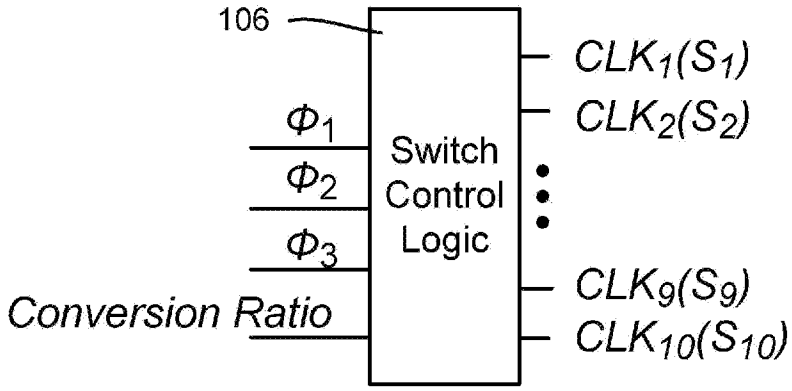

FIG. 9A

Switches	1/1X	2/3X	1/2X	1/3X	3/4X	1/4X
CLK_1 (S_1)	Φ_1	Φ_2	Φ_1	Φ_1	Φ_1	Φ_1
CLK_2 (S_2)	Φ_2	Φ_1	Φ_2	0	0	0
CLK_3 (S_3)	1	Φ_1	1	Φ_1	Φ_3	Φ_3
CLK_4 (S_4)	0	Φ_1	Φ_1	0	Φ_3	0
CLK_5 (S_5)	0	0	0	Φ_2	Φ_2	Φ_2
CLK_6 (S_6)	0	Φ_2	0	0	Φ_1	Φ_1
CLK_7 (S_7)	1	Φ_1	Φ_2	Φ_2	$\Phi_{2,3}$	$\Phi_{2,3}$
CLK_8 (S_8)	0	0	Φ_1	Φ_1	0	0
CLK_9 (S_9)	0	Φ_2	0	Φ_2	$\Phi_{1,2}$	$\Phi_{1,2}$
CLK_{10} (S_{10})	1	0	1	Φ_1	0	Φ_3

FIG. 9B

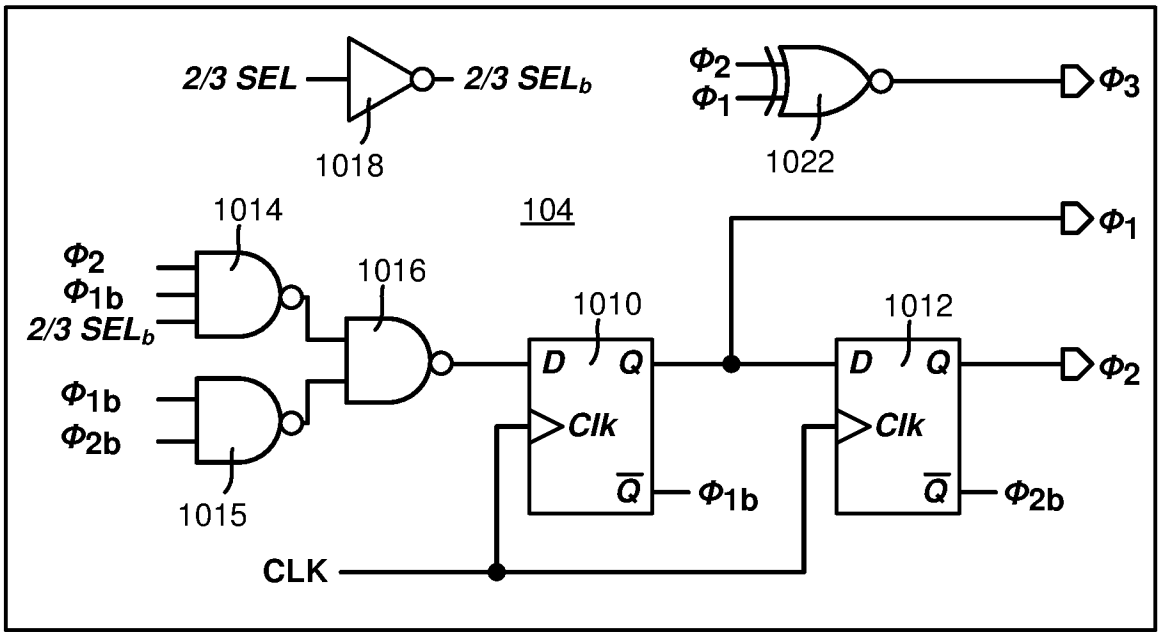

FIG. 10A

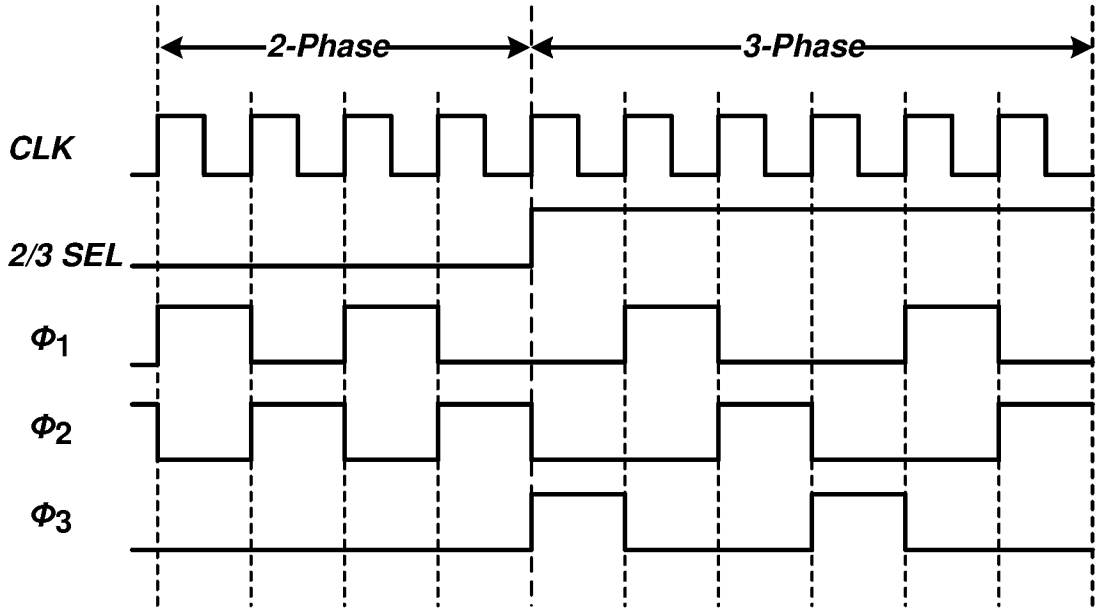

FIG. 10B

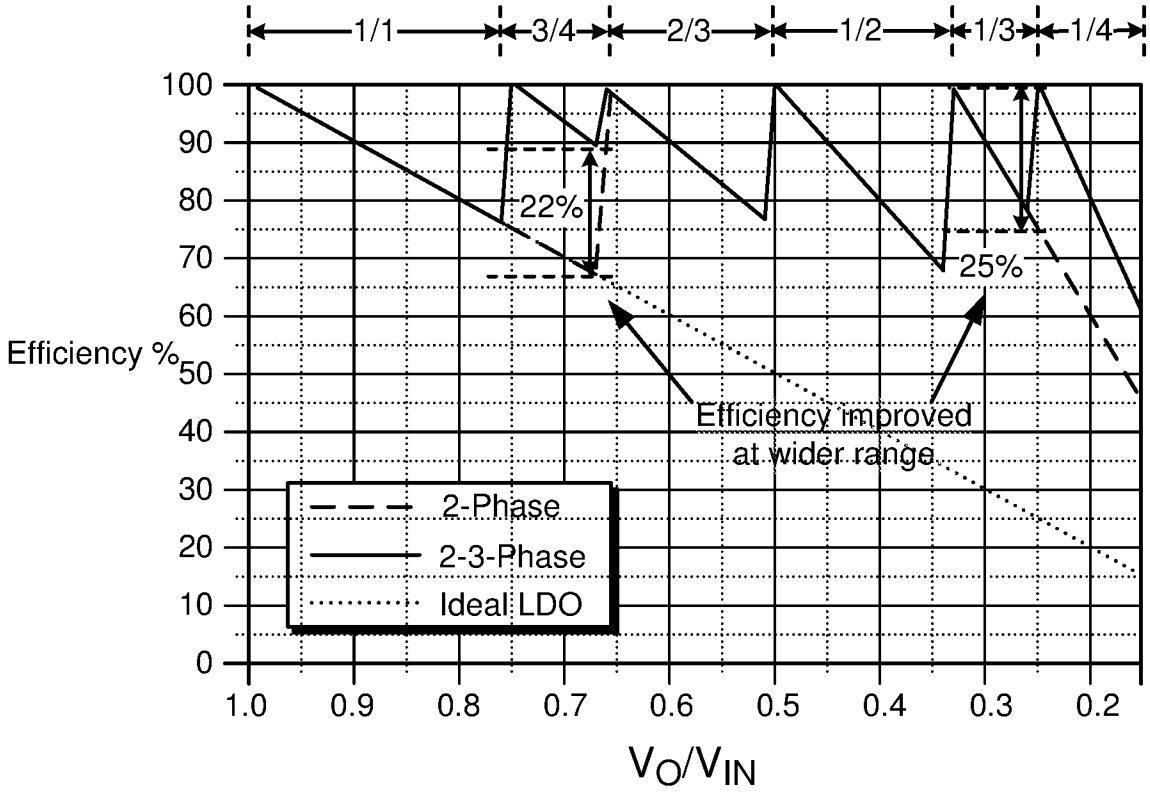
1/1
3/4
2/3
1/2
1/3
1/4
100
90
80
70
60
50
40
30
20
10
0
Efficiency %
22%
25%
Efficiency improved
at wider range
2-Phase
2-3-Phase
Ideal LDO
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
VO/VIN

FIG. 11

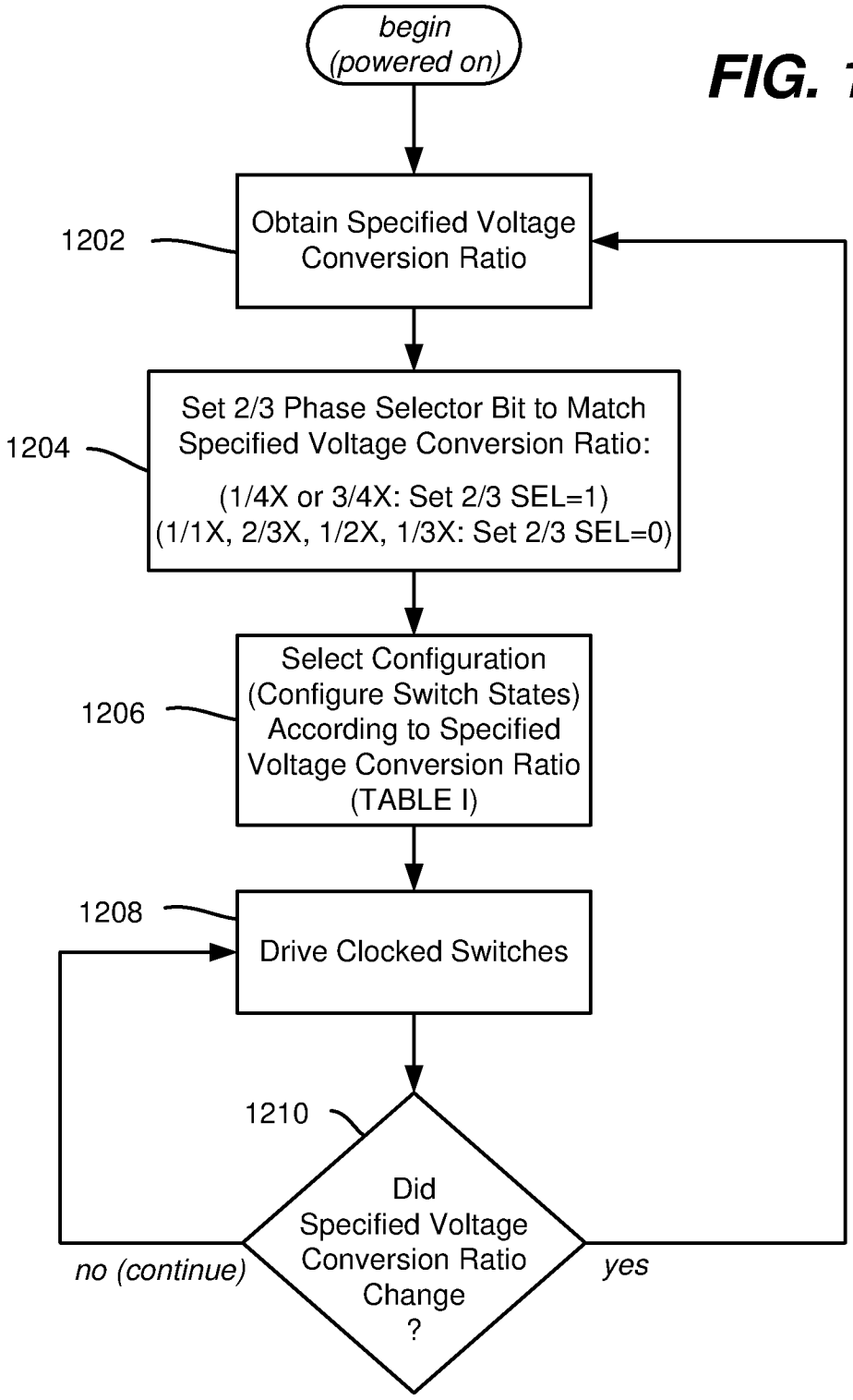
begin
(powered on)
1202
Obtain Specified Voltage Conversion Ratio
1204
Set 2/3 Phase Selector Bit to Match Specified Voltage Conversion Ratio:
(1/4X or 3/4X: Set 2/3 SEL=1)
(1/1X, 2/3X, 1/2X, 1/3X: Set 2/3 SEL=0)
1206
Select Configuration (Configure Switch States) According to Specified Voltage Conversion Ratio (TABLE I)
1208
Drive Clocked Switches
1210
Did Specified Voltage Conversion Ratio Change ?
no (continue)
yes

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/075412

A. CLASSIFICATION OF SUBJECT MATTER

H02M 3/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M,G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI: SCPC, reconfigure+, switch+, capacitor?, power, converter, mode, clock, two, phase, three, phase, voltage, conversion, ratios, alternat+, signal?, controller

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 104426356 A (NXP B.V.) 18 March 2015 (2015-03-18) see description, paragraphs [0041]-[0094], figures 1-9	1-20
A	CN 102262487 A (HIMAX TECHNOLOGIES LTD.) 30 November 2011 (2011-11-30) the whole document	1-20
A	CN 105229909 A (ARCTIC SAND TECHNOLOGIES INC.) 06 January 2016 (2016-01-06) the whole document	1-20
A	CN 105229908 A (ARCTIC SAND TECHNOLOGIES INC.) 06 January 2016 (2016-01-06) the whole document	1-20
A	US 2004264223 A1 (INTEL CORPORATION) 30 December 2004 (2004-12-30) the whole document	1-20
A	US 6834355 B2 (INTEL CORPORATION) 21 December 2004 (2004-12-21) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 May 2017	**09 June 2017**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**TANG,Hexiang**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)01061648114**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/075412

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	104426356	A	18 March 2015	EP	2846448	A1	11 March 2015
				US	2015069928	A1	12 March 2015
				US	9570976	B2	14 February 2017
CN	102262487	A	30 November 2011	CN	102262487	B	05 June 2013
					None		
				US	2010328252	A1	30 December 2010
				US	8384689	B2	26 February 2013
				TW	201100814	A	01 January 2011
				TW	I394958	B	01 May 2013
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				US	2014268945	A1	18 September 2014
				KR	20150131361	A	24 November 2015
				WO	2014150756	A1	25 September 2014
				US	9203299	B2	01 December 2015
				US	2014266132	A1	18 September 2014
				GB	201516834	D0	04 November 2015
				US	2016149478	A1	26 May 2016
				DE	112014001395	T5	17 December 2015
				US	8817501	B1	26 August 2014
				GB	2526493	A	25 November 2015
CN	105229908	A	06 January 2016	GB	201516830	D0	04 November 2015
				WO	2014143366	A1	18 September 2014
				GB	2526492	A	25 November 2015
				KR	20150132530	A	25 November 2015
				US	8619445	B1	31 December 2013
				TW	201448428	A	16 December 2014
				DE	112013006828	T5	10 March 2016
				US	2016028302	A1	28 January 2016
US	2004264223	A1	30 December 2004		None		
US	6834355	B2	21 December 2004	US	2002112194	A1	15 August 2002