



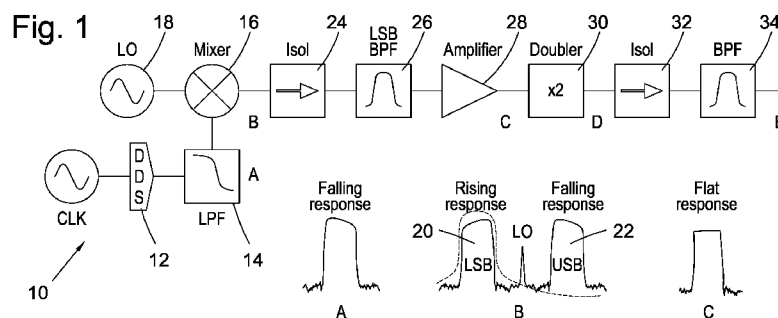
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(54) **Title:** CHIRP GENERATOR

(57) **Abstract:** A chirp generator comprises a direct digital synthesiser operable to generate a frequency chirp, wherein the frequency chirp is restricted to span less than one octave, a carrier signal that has a higher frequency than the frequency chirp, a mixer for mixing the frequency chirp and the carrier signal to produce a signal that has a lower sideband that has a rising frequency response and an upper sideband that has a falling frequency response, a filter for selecting one of the sidebands and rejecting the other sideband, and at least one component that has a frequency response that compensates for the frequency response of the selected sideband thereby to provide a substantially flat frequency chirp.

Chirp Generator

Field of the invention

The present invention relates to a chirp generator. In particular, the present invention relates to a chirp generator for use in radar applications.

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Background of the invention

Many radars and some spectrometers use swept frequency or chirp signals with output frequencies in the microwave or (sub-) millimetre wave range. Increasingly, such radars require wideband chirps with percentage bandwidths of 10% or more to achieve fine range resolution. It is also desirable that the chirp generator circuit yields chirps which are very linear, have good amplitude flatness, possess low phase noise and may be very short in duration. In some applications, it is also required that successive chirps are phase coherent (e.g. to allow Doppler processing). These various requirements can be in conflict with each other when the required bandwidth increases.

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Increasingly, direct digital synthesis is used to generate highly linear, low phase noise, repeatable, short duration chirps. Two particular approaches are commonly adopted when using direct digital synthesis to generate wideband chirps: (i) up-convert the direct digital synthesis chirp output onto a microwave carrier, or (ii) use the direct digital synthesis as a swept reference to control a microwave voltage controlled oscillator in a phase-locked loop. The former offers lower phase noise but the available bandwidth can be restricted due to the finite range of output frequencies available from direct digital synthesis chips and the presence of spurs in the direct digital synthesis output spectrum. The latter offers wider bandwidths but at the expense of higher phase noise and less dynamic agility due to the finite loop bandwidth of the phase-locked loop. The output of the chirp generator will often be at a microwave frequency and may be used directly or multiplied to higher frequencies. The process of frequency multiplication can degrade the chirp fidelity, but it is still preferable to have a good quality chirp source in the first place. For many applications, including submillimetre wave 3D imaging radar for personnel screening, the up-converted direct digital synthesis approach is preferred.

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Whilst direct digital synthesis chips offer many advantages they exhibit two particular drawbacks which hinder their use for wideband chirp generation. Firstly, the amplitude response of the direct digital synthesis follows a sinc ($\sin x/x$) response such that the chirp signal has a falling frequency response. Lack of amplitude flatness causes

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degradation of the range point response of a chirp radar. Secondly, the direct digital synthesis output spectrum contains discrete spurs at frequencies which are numerically linked to the output frequency. As the direct digital synthesis frequency is chirped, these spurs move up and down in the output spectrum, effectively contaminating the desired signal.

Some direct digital synthesis devices include a $1/\text{sinc}$ compensation filter which obviates the need to compensate for flatness, but most do not, especially the higher clock speed devices. A direct digital synthesis controlled voltage controlled oscillator and phase locked loop can circumvent the problems of flatness and spurs but suffers from other drawbacks as mentioned previously. As above, an equaliser filter can be used to flatten the DDS roll-off but this is undesirable, because such filters are inherently lossy. Some wideband radar systems using direct digital synthesis seem to accept the degradations as inevitable, but their performance is compromised.

Summary of the invention

According to the present invention there is provided a chirp generator comprising: a direct digital synthesiser operable to generate a frequency chirp, wherein the frequency chirp is restricted to span less than one octave; a carrier signal that has a higher frequency than the frequency chirp; a mixer for mixing the frequency chirp and the carrier signal to produce a signal that has a lower sideband that has a rising frequency response and an upper sideband that has a falling frequency response; a filter for selecting one of the sidebands and rejecting the other sideband, and at least one component that has a frequency response that compensates for the frequency response of the selected sideband thereby to provide a substantially flat frequency chirp.

The filter may be adapted to select the lower sideband and reject the upper sideband and the said at least one component has a frequency response that compensates for the rising frequency response of the lower sideband.

The filter may be adapted to select the upper sideband and reject the lower sideband and the said at least one component has a frequency response that compensates for the falling frequency response of the upper sideband.

The at least one component that has a falling frequency response may comprise an amplifier. It is fairly commonplace for such components to have a falling frequency response.

- 5 Between the mixer and the lower sideband filter, an isolator may be provided for suppressing reflection of the upper sideband energy.

A frequency doubler may be provided for doubling the bandwidth of the substantially flat frequency chirp. In this case, after the frequency doubler, an isolator and a
10 bandpass filter may be provided for removing unwanted frequency components from the frequency doubler.

Brief description of the drawings

Various aspects of the invention will now be described by way of example only, and
15 with reference to the following drawings, of which:

Figure 1 is a block diagram of a chirp generator;

Figure 2 shows various signals at different positions in the chirp generator Of
Figure 1, and

Figure 3 shows a response of an upper sideband bandpass filter for use in the
20 chirp generator of Figure 1.

Detailed description of the drawings

Figure 1 shows an up converted direct digital synthesizer chirp generator 10. This has a direct digital synthesizer 12 for creating a waveform from a fixed frequency reference
25 clock 10. It is typical to limit the maximum frequency from a direct digital synthesiser to 40% of the clock frequency. The frequency range of the chirp generated by the direct digital synthesizer 12 is restricted via control software to be just less than one octave. This prevents the second harmonic of the desired signal entering the chirped frequency band.

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The direct digital synthesizer is connected to a low pass filter 14. This is adapted to pass the highest frequency signal desired from the direct digital synthesiser whilst rejecting the dominant spur at $(f_{\text{CLK}} - f_{\text{OUT}})$, the clock frequency and its harmonics, and the aliased outputs of the direct digital synthesiser which appear above the clock
35 frequency and its harmonics. The low pass filter is connected directly to the

intermediate frequency input of a mixer 16. The signal input to the mixer 16 is shown in Figure 2A. This has a falling frequency response following a sinc envelope. This signal is mixed at the mixer 16 with the output of a higher frequency local oscillator 18.

5 Output from the mixer 16 is a signal that has both sum and difference terms. This is shown in Figure 2B. At this stage the signal has two bands, a lower sideband 20 and an upper sideband 22. The lower sideband 20 has a rising frequency response. The upper sideband 22 has a falling frequency response.

10 At its output, the mixer 16 is connected directly to an isolator 24 that is connected directly to a lower sideband bandpass filter 26. The lower sideband bandpass filter 26 is adapted to pass the lower sideband 20 and block the local oscillator leakage LO and the upper sideband 22 of Figure 2B. The isolator 24 is provided to minimise signal amplitude ripple by suppressing reflection of the rejected upper sideband.

15 Connected directly to the lower sideband bandpass filter 26 is an amplifier 28. The amplifier 28 intrinsically has a falling frequency response. This means that when the rising frequency lower sideband signal 20 passes through the amplifier 28 it is automatically frequency compensated to flatten the response. This is shown in Figure
20 2C.

The amplifier 28 is directly connected to a frequency doubler 30, which frequency doubles the flat response from the amplifier 28 to double the signal bandwidth. This is shown in Figure 2D. After the frequency doubler 20, a second isolator 32 and
25 bandpass filter 34 are used to clean the output signal and reject any unwanted leakage terms from the doubler 20 (for example leakage at frequencies f and $3f$). This provides a clean, flat output with the desired, extended bandwidth.

30 Whilst the amplifier of Figure 1 is shown as substantially flattening the response (see Figure 2C), in fact, the response can be flattened by the combined effects of all of the components after the lower band pass filter.

The system of Figure 1 is adapted to output a substantially flat, frequency doubled signal based on the lower sideband 20 output from the mixer 16. However, the
35 invention could equally be applied to provide a substantially flat, frequency doubled

signal based on the upper sideband 22 output from the mixer 16. In this case, the lower sideband bandpass filter 26 of Figure 1 would be replaced by an upper sideband bandpass filter. Figure 3 shows the response 36 of the upper sideband bandpass filter. From this, it can be seen that the upper sideband bandpass filter allows the upper sideband 22 to pass and blocks the lower sideband 20 and the local oscillator leakage. Because the upper sideband 22 has a falling response, the components after the upper sideband bandpass filter are selected to compensate for this. In particular, the amplifier, the frequency doubler, the isolator and the bandpass filter 34 are selected to compensate for the falling response of the upper sideband.

In practice, for both embodiments of the invention the components that are used to flatten the response have to be selected depending on their own frequency responses. This can be done by measuring or calculating the frequency responses. A common method for measuring the frequency response of such components is to use a scalar or vector network analyser or a tuneable signal source plus spectrum analyser.

A skilled person will appreciate that variations of the disclosed arrangements are possible without departing from the invention. Accordingly, the above description of the specific embodiment is made by way of example only and not for the purposes of limitation. It will be clear to the skilled person that minor modifications may be made without significant changes to the operation described.

CLAIMS

1. A chirp generator comprising:

a direct digital synthesiser operable to generate a frequency chirp,
wherein the frequency chirp is restricted to span less than one octave;

a carrier signal that has a higher frequency than the frequency chirp;

a mixer for mixing the frequency chirp and the carrier signal to produce
a signal that has a lower sideband that has a rising frequency response and an
upper sideband that has a falling frequency response;

a filter for selecting one of the sidebands and rejecting the other
sideband, and

at least one component that has a frequency response that
compensates for the frequency response of the selected sideband thereby to
provide a substantially flat frequency chirp.

2. A chirp generator as claimed in claim 1 wherein the filter is adapted to select
the lower sideband and reject the upper sideband and the said at least one
component has a frequency response that compensates for the rising frequency
response of the lower sideband.

3. A chirp generator as claimed in claim 1 wherein the filter is adapted to select
the upper sideband and reject the lower sideband and the said at least one
component has a frequency response that compensates for the falling
frequency response of the upper sideband.

4. A chirp generator as claimed in any of the preceding claims wherein a low pass
filter is provided between the direct digital synthesiser and the mixer for the
removal of unwanted higher frequency spurious output signals.

5. A chirp generator as claimed in any of the preceding claims wherein the at least
one component that has a falling frequency response comprises an amplifier.

6. A chirp generator as claimed in in any of the preceding claims comprising an
isolator between the mixer and the sideband filter.

7. A chirp generator as claimed in any of the preceding claims comprising frequency doubler for doubling the bandwidth of the substantially flat frequency chirp.
- 5 8. A chirp generator as claimed in claim 4 comprising an isolator and a bandpass filter for removing leakage from the frequency doubler.

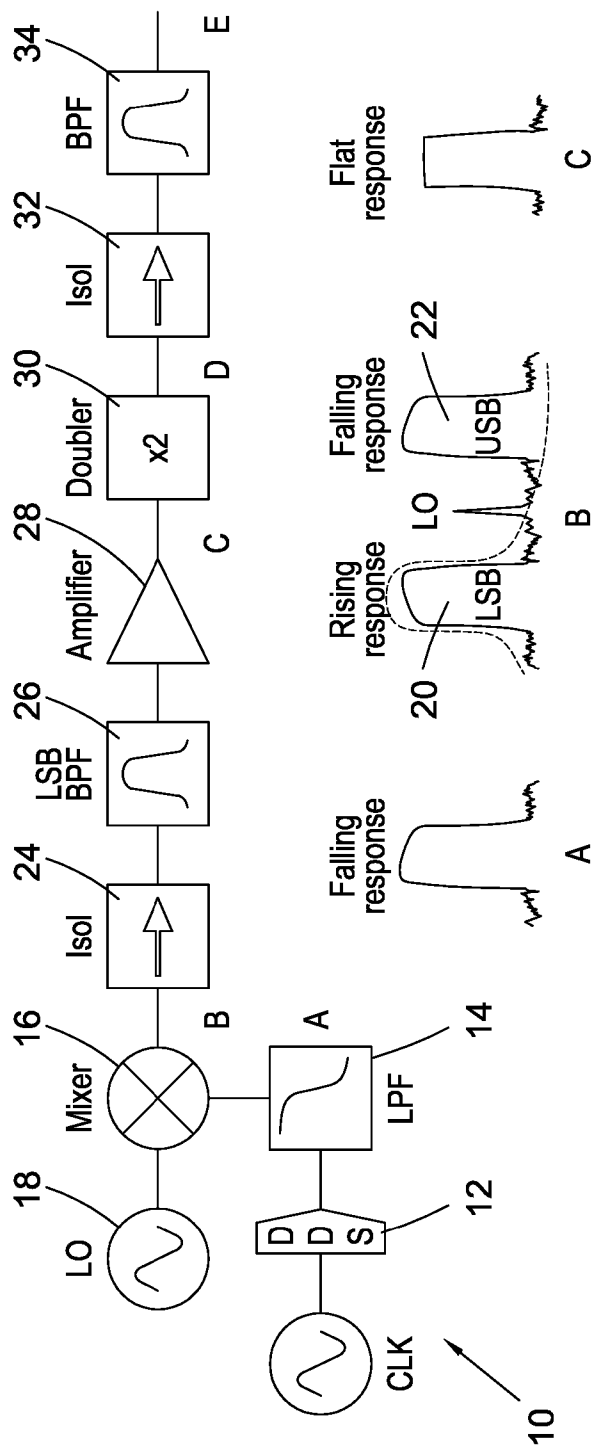


Fig. 1

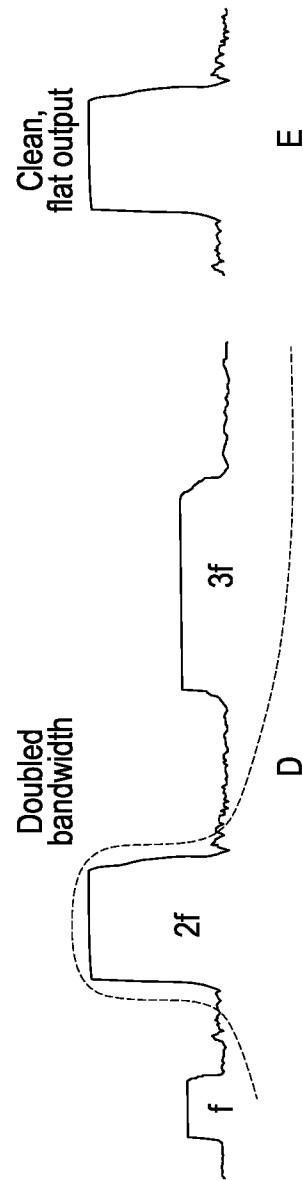


Fig. 2

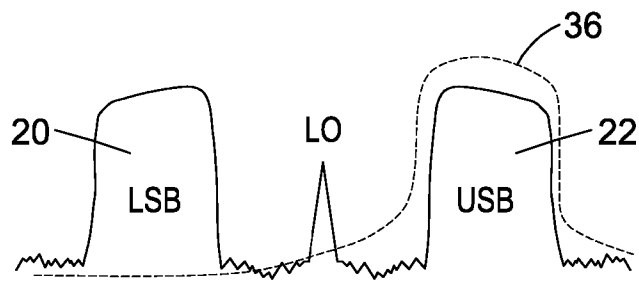


Fig. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2016/054033

A. CLASSIFICATION OF SUBJECT MATTER

INV. G01S7/35 G01S13/34
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/002972 A1 (STIFFLER COLTON RICHARD [US] ET AL) 5 January 2012 (2012-01-05) figures 3a,3c paragraphs [0081], [0086], [0087], [0116]	1-8
X	US 6 825 800 B1 (DUDLEY PETER A [US] ET AL) 30 November 2004 (2004-11-30) figures 8,11,12 column 14, lines 35-60 column 15, lines 33,35 column 16, lines 19-32	1,2,4-6, 8
Y	US 2008/159370 A1 (ATHERTON ADAM T [US]) 3 July 2008 (2008-07-03) figure 10 paragraph [0058]	1-8
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2016/054033

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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