United States Patent

[11] 3,571,932

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[54] **DIGITAL PLANIMETER**
11 Claims, 11 Drawing Figs.

[52] **U.S. Cl.** **33/123, 235/92**
[51] **Int. Cl.** **G01b 7/32, G06g 7/18**
[50] **Field of Search** ..... 33/123, 121, 122; 235/92 (26D), 61.6 (B), 151.3

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Primary Examiner—Robert B. Hull
Attorney—Watson, Cole, Grindle & Watson

ABSTRACT: This invention relates to a planimetry and particularly to planimetric apparatus whereby digital representations of the cursor movement in one of two orthogonal reference coordinates are provided in incremental fashion to register means for accumulation and temporary storage. The movement of the cursor in the other of the orthogonal reference coordinates causes the information in the register to be transferred to a down counter. The down counter is pulsed, by means of clock pulse signals, to a zero condition. Simultaneously the clock pulses are provided to an adder subtracter device which accumulates the pulses until the down counter obtains the zero output condition. Control means are provided such that the pulse information which is entered into the adder/subtracter unit provides the correct updated pulse accumulation which represents the total summation of the incremental information stored in the register and periodically transferred to the down counter. The accumulated information in the adder/subtracter device may be displayed to provide a current indication of the area traversed by the cursor.

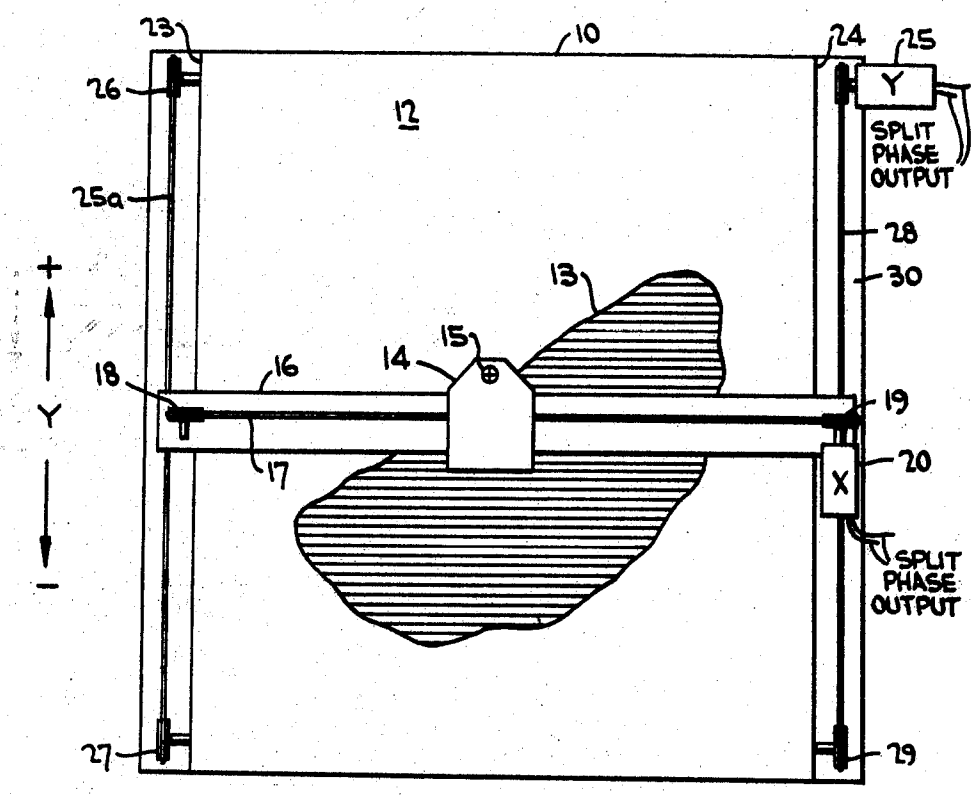


FIG. 1

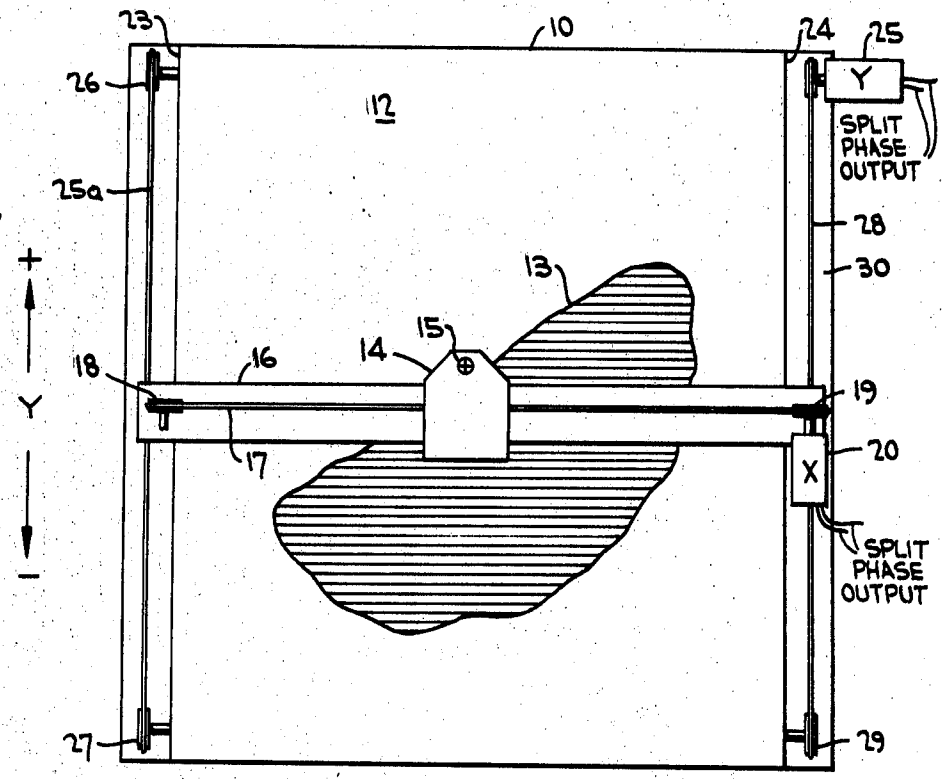


FIG. 2

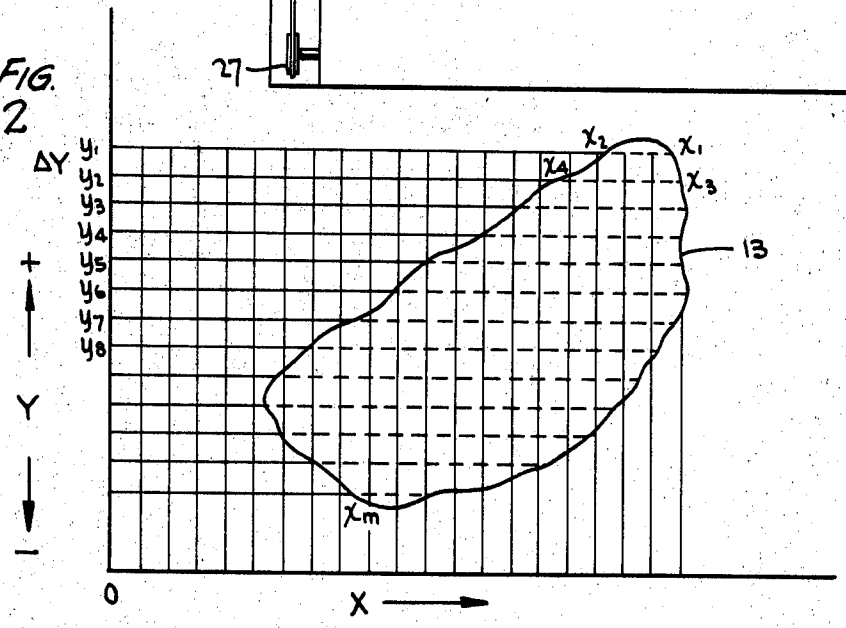
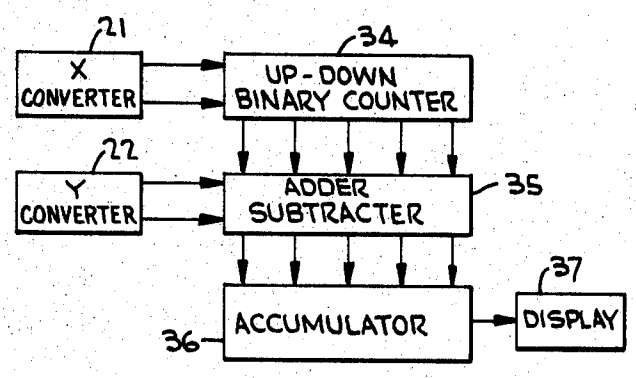


FIG. 3



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FIG. 4

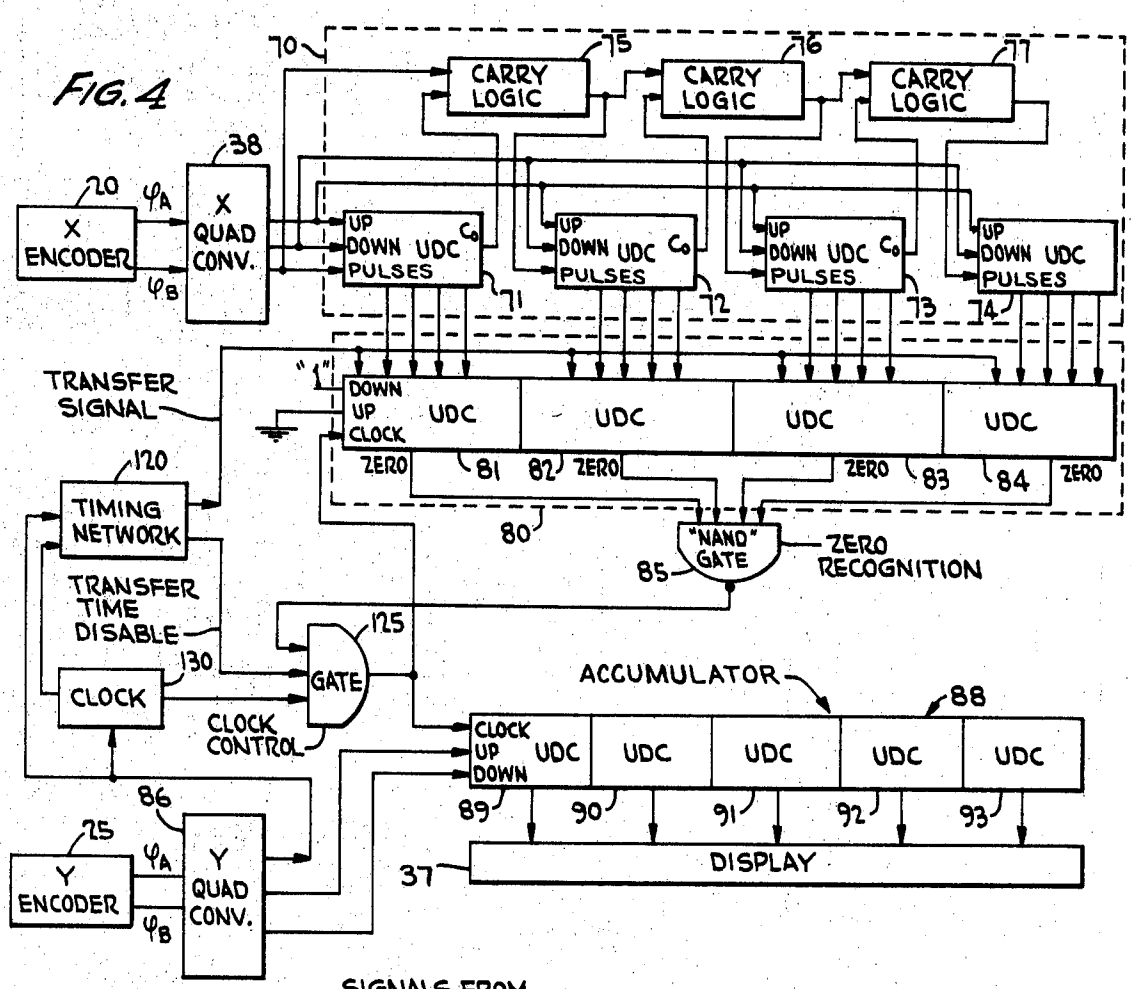


FIG. 5

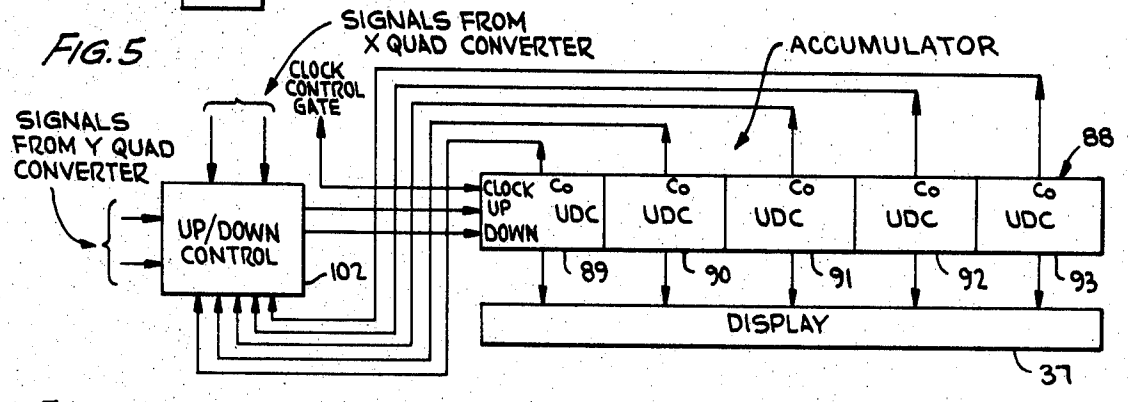
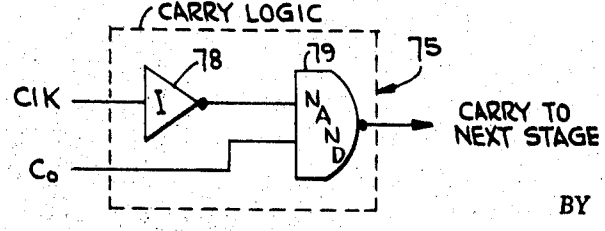


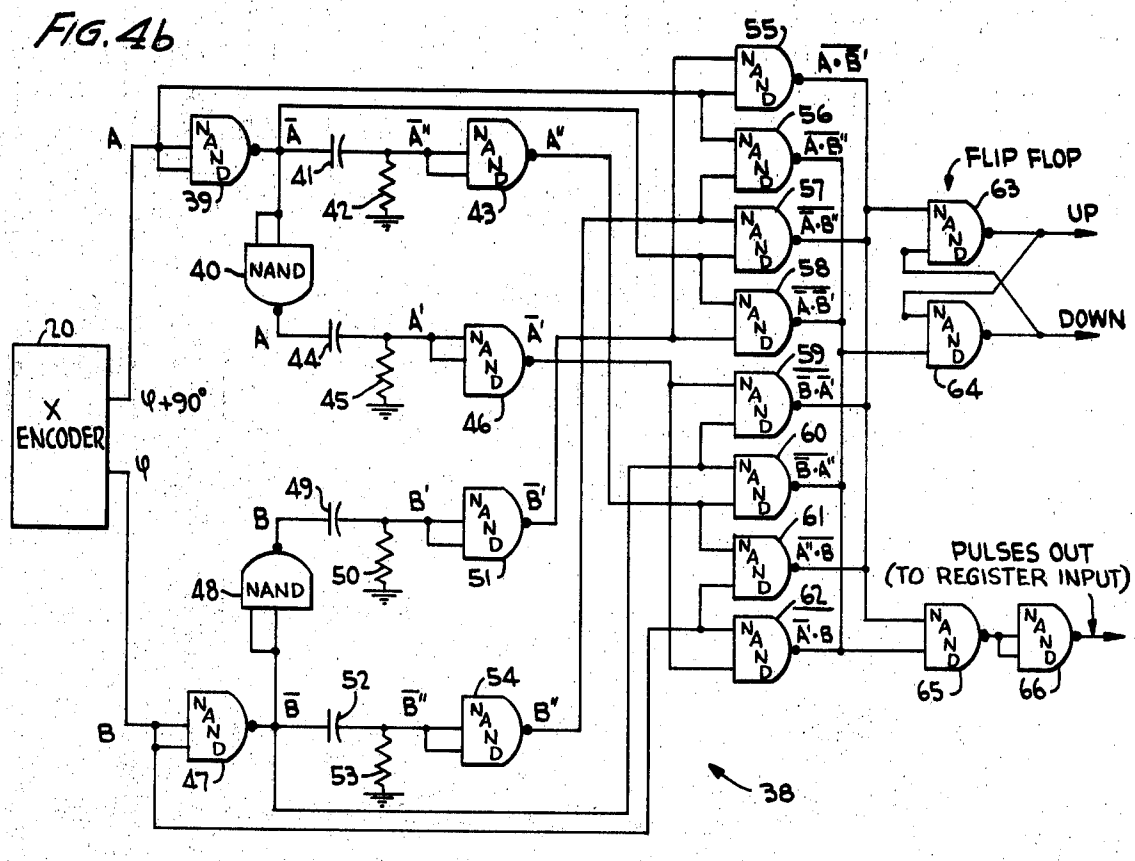
FIG. 4a



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FIG. 4b



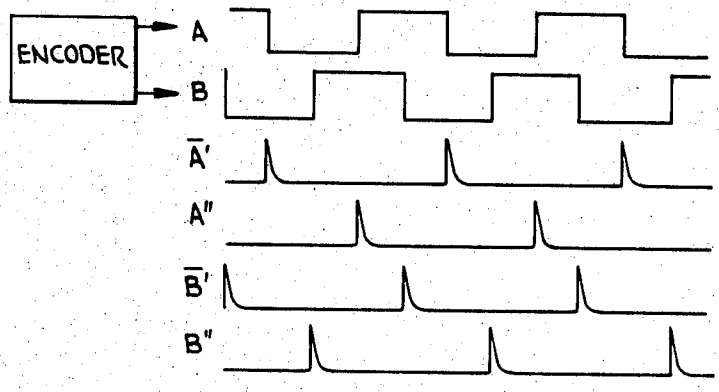


FIG. 4c

$$UP = \overline{A \cdot \overline{B'}} + \overline{\overline{A} \cdot B''} + \overline{\overline{B} \cdot \overline{A'}} + \overline{\overline{A''} \cdot B}$$

$$DOWN = \overline{A \cdot B''} + \overline{\overline{A} \cdot \overline{B'}} + \overline{\overline{B} \cdot A''} + \overline{\overline{A'} \cdot B}$$

$$PULSES\ OUT = \overline{A \cdot \overline{B'}} + \overline{\overline{A} \cdot B''} + \overline{\overline{B} \cdot \overline{A'}} + \overline{\overline{A''} \cdot B} + \overline{A \cdot B''} + \overline{\overline{A} \cdot \overline{B'}} + \overline{\overline{B} \cdot A''} + \overline{\overline{A'} \cdot B}$$

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FIG. 4d

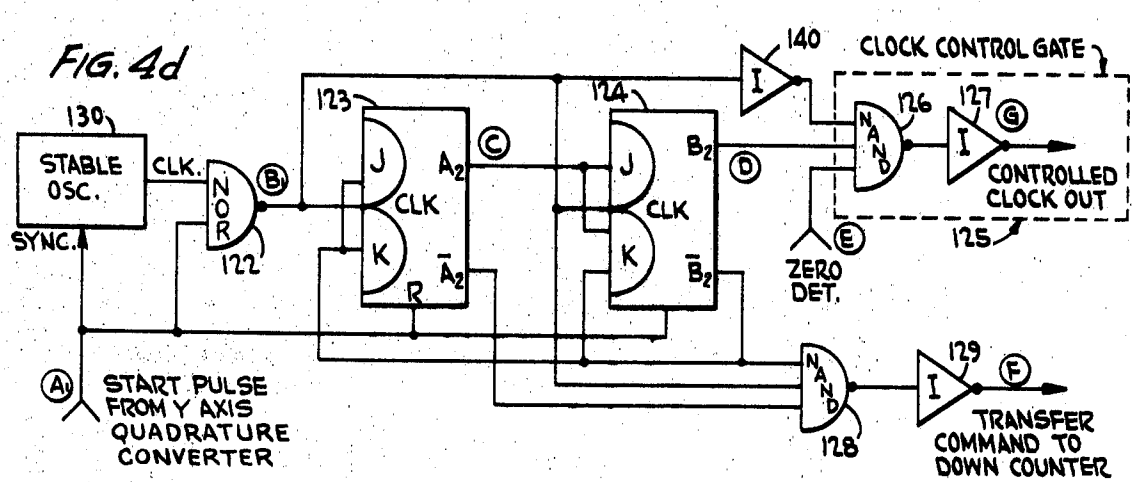
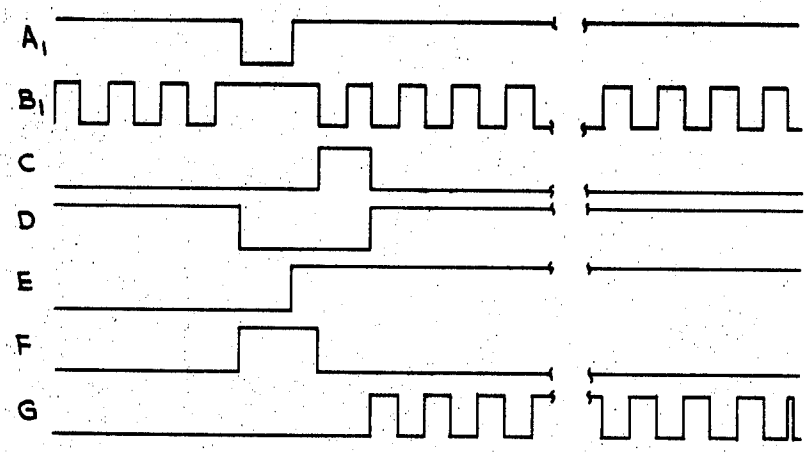


FIG. 4e



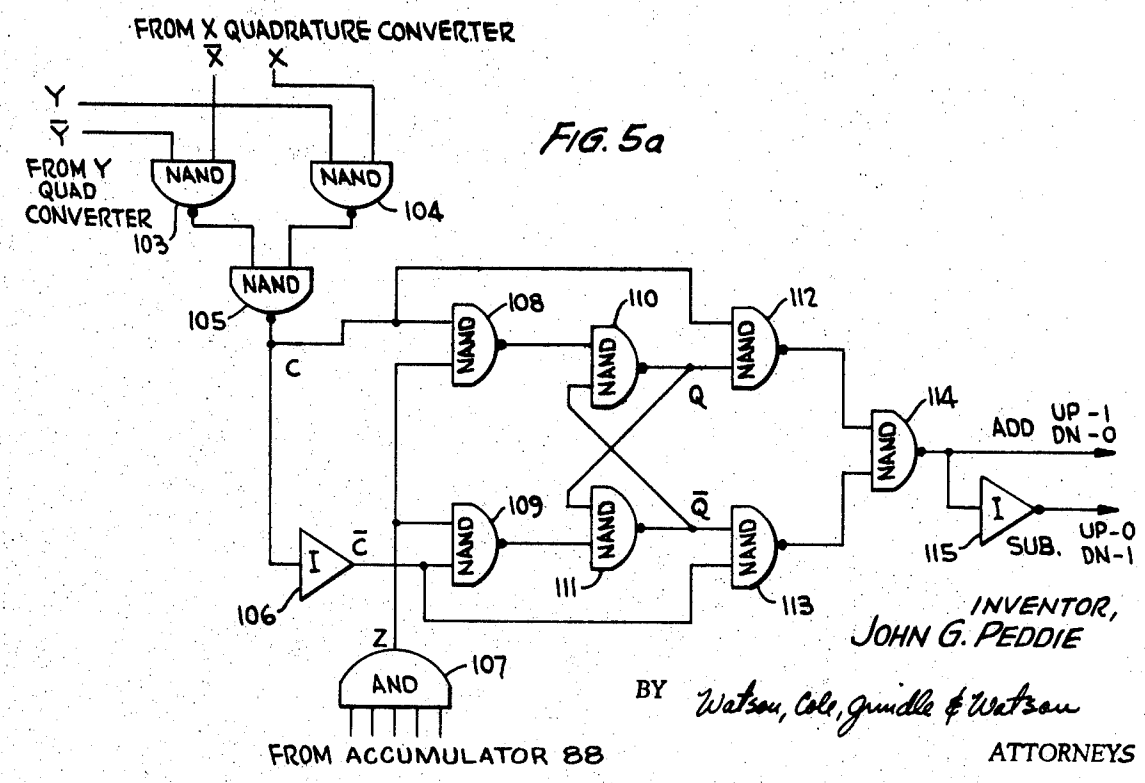


FIG. 5a

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DIGITAL PLANIMETER

The measurement of both regular and irregularly-shaped areas on plane surfaces has long been accomplished using mechanical planimeters such as those originated by Kelvin, Amsler and others and later developed to a high degree of precision and usefulness. Such mechanical integrating instruments are in common use in many civil and mechanical engineering applications. Although these mechanical planimeters are employed frequently in photogrammatic analysis, deliberate and painstaking operation is required to insure even modest accuracy.

Modern photogrammetric processing generally utilizes very rapid scanning and interpretive procedures so that any manual steps within the overall process represent serious time delays. It is desirable that the speed of such slow steps in the determination of areas be increased to be more consistent with automated processing procedures. In addition, it is preferable that the accuracy and reliability of measurements be improved over that obtainable with purely mechanical arrangements. Finally, it would be advantageous to generate information in the form of electrical signals which could be displayed either directly or stored for later use in a computational procedure for determining area measurements.

In well-known graphical techniques, an area to be measured may be divided into parallel strips of unit width and the total area obtained as the product of the unit width and the sum of the lengths of the strips. Various mechanical arrangements have been devised to utilize this apparently simple process, but such arrangements are limited in accuracy by the difficulty of making the strips sufficiently narrow. By use of optical and electronic techniques, however, the measuring increments or "strips" may be made quite small because the formation of the strips is limited only by the resolving capability of lens systems, photographic media and scanning patterns. Similar improvements can be effected, of course, in determining the lengths of the incremental strips and in the summation of the increments to obtain their total value.

For most measurements utilizing rectangular integration methods, the area under a given curve is found merely by the summation of the coordinate values represented by the curve in the coordinate system. In the usual planimetric problem on a map, however, the area of interest is bounded by a closed curve spaced away from the reference axes. Accordingly, the measuring arrangement must utilize the full coordinate values while at the same time providing for the subtraction of the incremental areas which lie outside the boundary curve.

Briefly, in the present invention the boundary enclosing the specified area is traversed by a cursor element which actuates coordinate encoders for the generation of electrical signals representing incremental movements of the cursor element as it is caused to traverse the boundary. The electrical signals are provided to reversible digital counting apparatus, of a unique design, and timing and control means are provided to control the reversible counting apparatus such that the incremental areas are algebraically mounted to obtain the total area traversed by the cursor. The total area may then be displayed. The area to be measured need not be immediately adjacent or in any specific predetermined relationship to the reference axes.

Accordingly, the primary object of this invention is to provide apparatus capable of rapidly and accurately measuring area on graphic media such as maps, photographs and drawings. Another object is to provide apparatus for measuring areas which need not be in adjacent or predetermined relationship to the coordinate reference axes. Still another object is to provide a digital planimeter in which the measured area is indicated immediately in digital format. Yet another object of the invention is to provide a digital planimetric apparatus which can be assembled readily from standard logic elements which are commonly used in data processing equipment. Finally, it is an object of the invention to furnish a planimetric apparatus which is fully compatible and integrable with digital computer processes and apparatus.

These and other objects and novel features of the invention will become apparent in the following description and the related accompanying drawing wherein:

FIG. 1 is a schematic showing the principal elements of the scanning portion of the digital planimeter and their interrelationship;

FIG. 2 is a graphical illustration showing an area to be measured placed upon a system of reference coordinates;

FIG. 3 is a simplified block diagram of one arrangement of logic apparatus required to carry out the invention;

FIG. 4 is a block diagram illustrating one preferred arrangement of the digital logic elements required for implementing the invention of FIG. 3;

FIG. 4*a* represents the implementation of the logic circuitry for performing the carry function;

FIG. 4*b* illustrates the detailed implementation of the quadrature converter circuitry;

FIG. 4*c* shows typical signal waveforms in the quadrature converter circuit;

FIG. 4*d* is a block diagram of the timing network for the digital planimeter;

FIG. 4*e* illustrates typical waveforms at the various points indicated in the timing network shown in FIG. 4*d*;

FIG. 5 is a block diagram representation of the circuitry for controlling the adder/subtractor elements of the invention; and

FIG. 5*a* is a detailed block diagram of the up-down control circuit illustrated in FIG. 5.

Referring to FIG. 1 of the drawing, scanning frame **10** is arranged to hold in fixed relationship the map, photograph or drawing **12** containing an area **13** which is to be measured. A movable cursor assembly **14**, with reticule **15**, is arranged to slide smoothly along horizontal arm **16** and thus transmit its horizontal motion to the X-encoder **20** by means of cable **17** and pulleys **18, 19**. Horizontal arm **16** is also arranged so as to slide smoothly in the vertical direction along guides **23, 24** and to simultaneously actuate Y-encoder **25** by means of cable **28** and pulleys **29, 30**. A similar cable **25***a* and associated pulleys **26, 27** are provided adjacent to guide **23** to provide a balanced and smooth operating motion.

In measuring area **13**, the operator manually moves cursor assembly **14** carefully along the boundary line as observed in reticule **15**. The motions of cursor **14** are transmitted to X-encoder **20** and Y-encoder **25** which generate displacement signals which are utilized in the data recording or area computation circuitry to be described in detail hereinafter.

Referring to the graphical representation of FIG. 2, area **13** may be considered as defined by the boundary x and y coordinates referenced to the zero origin. Thus, if the planimeter index or cursor **14** is placed on the boundary curve at, say, any Y-line, the x-coordinate value may be determined. As cursor **14** traverses the boundary curve it may be assumed that a halt is made at each Y-line, representing an incremental command step, and that the associated x-coordinate value is determined during the halt. In effect, the x-coordinate readings taken at the two boundary intercept points $x1$ and x_2 will furnish the incremental distance (x_1-x_2) which when multiplied by the y-increment step, or Δy, will furnish the small incremental area, $\Delta y\,(x_1-_2)$.

Since the y-increments or command steps are all equal, it can be seen that the order in which x-coordinate values are determined is immaterial in the final summation, provided the boundary curve is traversed carefully and without overlap. Further, it is also evident that the absolute values of $x_1,x2...x_n$ can be used in a defining algorithm if some means is provided for determining when the cursor is moving away from or toward the x-axis. Thus, if y is chosen as the command coordinate, which is to determine the measuring increment, then the x-coordinate value can be defined as positive when y is moving away from the x-axis, and negative when y moves toward the x-axis. More simply, x can be considered positive when the y command value, as defined by the usual x–y coordinate system, is increasing, and x must then be recorded as negative when the y command is decreasing in value.

Using these definitions, an algorithm may be written to show the necessary operational relationship:

$$\text{Area}=h[(x_1)y_1-(x_2)y_1+(x_3)y_2-(x_4)y_2\pm(x_m)y_n\mp(x_{m1})y_n]$$

$h=\Delta y$=increment of y; the command coordinate

Thus, when all values of the y-command coordinate have been traversed and the related x-coordinate values recorded, the total area may be computed by substitution in the algorithm. The proper sign for each x-coordinate value may be determined readily by noting the direction in which y-command has changed since the last halt. The total area is then determined by algebraically summing all the values of the x-coordinate and multiplying this sum by the incremental value of y.

The above-outlined calculations may be automatically computed by the arrangement of apparatus shown in FIG. 3, X-converter 21 is actuated by horizontal movements of cursor 14, shown in FIG. 1, to furnish electrical output signals in digital form to up-down counter 34 comprising sufficient binary (or binary coded) register to permit the desired range of measurement. Various means, which will be described later, may be arranged to supply up-down signals corresponding to increasing or decreasing values of the x-coordinate. The output from up-down counter 34 is transferred to adder/subtractor 35 upon receiving the transfer command from y-converter 22. Whenever cursor 14 moves one increment in the y direction, the adder/subtractor 35 is actuated and acquires the date then accumulated in up-down counter 34 and transfers this data to accumulator 36, where the transferred data is algebraically summed. The total accumulated value may be shown on display 37. This indicated x summation multiplied by the value of the y increment represents the measurement of the desired area.

The simplified representation of FIG. 3 is shown in more detail in FIG. 4 which shows one preferred logic circuit for carrying out the invention. X-encoder 20 and quadrature converter 38 furnish coordinate pulses and sign control signals to the X to register 70 which includes stages 71, 72, 73, 74. Stages 71—74 are interconnected respectively by carry logic circuits 75—77 such that X-register 70 operates as an up-down counter in response to the input signals provided by quadrature converter 38. Binary-coded-decimal format is preferred for compatibility with associated equipment and analysis. Suitable up-down signals, actually representing the sense of either forward or reverse rotation of X-encoder 20, are derived by phase comparison means in quadrature converter 38. Such rotation-direction indicating techniques are well known in the instrumentation art and described in detail in references such as Control Engineer's Handbook, John G. Truxal, Editor, 1958, McGraw-Hill Book Co., New York.

Although various types of up-down counters may be adapted for use in X-register 70, the novel three-input counter disclosed in my previous U.S. application Ser. No. 657,936, filed Aug. 2, 1967, which became U.S. Pat. No. 3,544,773 is especially suitable and preferred. The use of four stages 71, 72, 73 and 74 in X-register 70 is, of course, by way of illustration and additional units may be included to extend the range and accuracy.

Up-down counter stages 71—74 comprising x-register 70 provide means for accumulating instantaneous incremental values of the x-coordinate. In order to automatically compute the area, it is necessary that the instantaneous incremental x-coordinate values be transferred or read out at the sampling or y-increment instants, as determined by the output from Y-encoder 25. Using the previously described graphical illustration, this Y-encoder transfer signal or command occurs at the instant corresponding to the crossing of a Y-line on the graph.

Down counter 80 the operation of which is more fully described below, comprising stages 81—84, is actuated from timing network 120 in response to a command signal from Y-encoder 25 and quadrature converter 86, so as to acquire by transfer the x-coordinate values from X-register 70 at the proper sampling instants. The x-coordinate values must, in turn, be given the proper sign and transferred permanently to accumulator 88 so as to accumulate an updated summation of the x-coordinate values which is shown finally on display 37. This transfer of information is effectively provided to accumulator 88 by utilizing controlled clock signals, from clock 130, to pulse down counter 80 down from the stored x-coordinate value to a zero count, which condition is recognized by zero recognition NAND gate 85. The output of NAND gate 85 disables the clock signal by turning off clock control gate 125.

Simultaneously with the down counting of down counter 80, clock pulses are transmitted to accumulator 88 to effect the algebraic summation with the previously accumulated x count. Accumulator 88 comprises another group of counter stages 89—93 which may be interconnected as shown in my previously mentioned U.S. Pat. application Ser. No. 657,936.

The operation of the apparatus in FIG. 4 may be understood more clearly by the following step-by-step outline:

1. The current x-coordinate pulses from X-encoder 20 are converted into digital form by quadrature converter 38 and temporarily stored in X-register 70.
2. When the y increment or command signal is generated by Y-encoder 25 ("y has crossed a line"), timing network 120 is actuated so as to disable, via clock control NAND gate 125, pulses from clock 130. Simultaneously, the timing network 120 furnishes a transfer command to down counter 80 to accept the count reading from X-register 70.
3. When the X-register count is present in down counter 80, clock 130 starts sending pulses into down counter 80 via clock control gate 125 under control of timing network 120. Simultaneously, clock pulses are sent into accumulator 88 for addition or subtraction as controlled by the "up" or "down" signal from the y quadrature converter 86 and accumulate with the previous count retained therein.
4. The zero output condition of down counter 80 is sensed by zero recognition NAND gate 85 which then stops the clock pulses from clock 130 by disabling clock control gate 125.
5. The clock pulses into accumulator 88 are terminated and the accumulated total count is shown on display 37 as the x-coordinate summation. The accumulated and updated total in accumulator 88 which is displayed by display 37 is the current total area traversed by cursor 14 since the y incremental constant is conveniently selected as unity.

With respect to functioning of down counter 80, it should be noted that the counter stages 81—84 are held permanently in a "down" mode by a logical 1 applied to the "down" input, while the "up" input is permanently connected to logical 0 as represented by the circuit ground. This control configuration is necessitated by the fact that down counter 80 is preferably constructed in accordance with the "Reversible Binary Coded Decimal Synchronous Counter Circuits" as described in my aforementioned pending U.S. Pat. application Ser. No. 657,936. Those skilled in the art will recognize that more conventional down counter circuits can be substituted for that shown in FIG. 4 to accomplish the function of that apparatus.

Carry logic circuit 75 comprises inverter 78 and NAND gate 79 as shown in FIG. 4*a*. The pulse signals from X quadrature converter 38 (FIG. 4) are inverted and logically combined with the carry output signal C_n from counter stage 71. The output of NAND gate 79 is then applied to the input of carry logic circuit 76 along with the carry output from counter stage 71. Carry logic circuits 76 and 77 are similar to carry logic circuit 75 with the exception that for carry logic circuits 76 and 77 the input shown in FIG. 4*a* is replaced by the carry output signal from carry logic circuits 75 and 76, respectively.

An embodiment of the circuitry comprising X quadrature converter 38 is shown in FIG. 4*b*. The operation of the converter will be more easily understood with reference to the signal waveform shown in FIG 4*c*. Quadrature converter 38 is comprised entirely of NAND gate circuit elements, inverter circuits using a NAND gate circuit configuration, and capacitor-resistor networks which serve to provide the necessary dif-

ferentiated pulses. The NAND circuit configuration is for convenience only, since most of the logic elements of the digital planimeter are comprised of such NAND gate elements. Those skilled in the art will recognize that other logic circuitry may also be substituted for that shown in FIG. 4*b* to perform the necessary functions of the quadrature converter circuitry. The two series of output signals from X-encoder **20** are out of phase by 90° as indicated by signal waveforms A and B in FIG. 4*c*. Output signals A and B are provided to inverter gates **39** and **47**, respectively, (which are NAND gate elements having their inputs paralleled to perform an inverter function). The inverted outputs A and B are respectively applied to capacitor-resistor networks **41**, **42** and **52**, **53** to form the indicated output $\overline{A''}$ and $\overline{B''}$. These signals are respectively inverted by inverter circuits **43** and **54** to provide signals A'' and B'' which are shown in FIG. 4*c* in relation to encoder output signals A and B. Simultaneously, the respective outputs from inverter circuits **39**, **47** are provided through inverter circuits **40**, **48** respectively, and then to capacitor-resistor networks **44**, **45** and **49**, **50**, respectively, to provide the indicated outputs A' and B'. The signals A' and B' are then each inverted, respectively, by inverter circuits **46** and **51** to form the indicated outputs $\overline{A'}$ and $\overline{B'}$ which are also shown in FIG. 4*c*. The signals A'', $\overline{A'}$, $\overline{B'}$ and B'', along with the signals $\overline{A}$ and $\overline{B}$ are provided to NAND gate circuits **55**—**62** in the indicated manner so as to be combined to provide the logic signals appearing at the output of NAND gate circuits **55**—**62**. These outputs are then combined according to the logic equations at the bottom of FIG. 4*c* in NAND gate elements **63** and **64** to form the necessary UP, DOWN control signals for register **70** which is shown in FIG. **4**. The pulse output from the X-converter, which is indicative of the movement of the cursor in the X-direction, is formed through NAND gate **65** and inverter **66** in accordance with the logical equation appearing at the bottom of FIG. 4*c*. The UP, DOWN and pulse output signals of the X-converter provide the necessary control signals to properly operate register **70** so as to provide therein an instantaneous accumulation of information which represents the movement of cursor **14** in the X-direction.

The Y-encoder circuitry is similar to that of the X-encoder circuitry just described except that the pulse output signal from the Y-converter is altered such that each pulse output represents a traversal of one unit of the cursor in the *y* coordinate direction. Thus, the Y quadrature converter circuitry may include a counter or divider network such that each pulse output represents one unit of travel of the cursor in the *y* coordinate direction.

The circuitry comprising timing network **120**, clock **130** and clock control gate **125** is shown in FIG. 4*d*. The signals at the indicated points in FIG. 4*d* are shown in FIG. 4*e*. Clock **130** may preferably comprise an oscillator having a sufficiently high oscillation frequency to provide the necessary accuracy of measurement. For example, the oscillator frequency of clock **130** may be five megacycles. The oscillator is synchronized with the output pulse from quadrature converter **86** to form the clock pulses which are provided to NOR **122** along with the pulse output from Y quadrature converter **86**. As shown in FIG. 4*e* the clock pulses B_1 at the output of NOR **122** are controlled by pulses A_1 and provided to clock control gate **125** through inverter **140**. The NOR'd pulses are also provided to the clock inputs of flip-flops **123** and **124**. Flip-flops **123** and **124** are interconnected to provide the indicated signal at D which serves to control the gating of inverted clock pulses B_1 in conjunction with zero detection signal E which is obtained from zero recognition circuit **85** from the zero output condition of counter stages **81**—**84** in down counter **80**. The inverted B_1 clock pulses, along with signal D and zero detection signal E, are provided to the input of NAND gate **126** and the output of NAND gate **126** is inverted by inverter **127** to provide the indicated control clock output signal G. This latter signal is applied, as shown in FIG. **4**, to the clock inputs of the respective counter stages of down counter **80** and also to the respective counter stages of accumulator **88** only when zero detection signal E is at an up level as shown in FIG. 4*e*. The transfer command signal to down counter **80** is formed by providing the indicated signals from flip-flop **123** and **124** to NAND gate **138**. The output of NAND gate **128** is inverted by inverter **129** to form the transfer command signal indicated as signal F. Transfer command signal F indicates the transfer of the accumulated information from register **70** into down counter **80** as described previously.

Although the arrangement described in FIG. **4** is quite reliable and capable of high accuracy when properly instrumented, it is subject to certain operational limitations. For example, to prevent gross errors the operator must take care to move the cursor always in the same direction, clockwise or counterclockwise about the area to be measured when starting a measurement. In addition, the described arrangement requires that the area to be measured extend only in a single quadrant with reference to the origin of the coordinate system. Accordingly, an alternate arrangement is preferred in which all measurements are made essentially automatically and may extend to all four quadrants.

Referring to FIG. **5** of the drawing, up-down control **102** has been added to the previous arrangement to provide quadrant recognition and suitable output control of accumulator **88**. Up-down control **102** is actuated by input signals from X-encoder **20** (via quadrature converter **38**) and Y-encoder **25** (via quadrature converter **86**).

The logical design of up-down control **102** is based on three requirements: (1) the sign of X, from the X-encoder **38**, must be known; (2) the sign of Y, from the Y-encoder **25**, must be known; and (3) the zero or nonzero condition of up-down counter stages **89**—**93**, considered together, must be recognized. Next, it is assumed that the origin (X=0,Y=0) of the coordinate system is located at some point on the boundary of the area to be measured and all up-down counter stages set to zero, after which cursor **14** (FIG. 1) is moved in either direction along the boundary of the area until a Y increment is crossed as indicated by Y-encoder **25**.

Assuming that Z refers to the zero condition of the up-down counter stages **89**—**93**, that "ADD" refers to a logical 1 output, and that "SUBTRACT" refers to a logical 0 output, the following operation is desired when the Y-increment has been detected:

1. ADD, if Z=0 and X=Y.
2. ADD, if Z=0 and $X \neq Y$.
3. SUBTRACT, if $Z \neq 0$ and X did not equal Y when Z was equal to 0, and X=Y.
4. SUBTRACT, if $Z \neq 0$ and X was equal to Y when Z was equal to 0, and X=Y.
5. ADD, if $Z \neq 0$ and X did not equal Y when Z was equal to 0, and $X \neq Y$.
6. ADD, if $Z \neq 0$ and X was equal to Y when Z was equal to 0, and X=Y.

It will be noted that these verbal logic statements describe the quadrantal relationships of the X and Y increments, plus the count condition Z of accumulator **88**.

Referring now to the detailed schematic of FIG. **5***a*, the necessary control logic for up-down control **102** is effected by the interconnected NAND gates and inverters **106**, **115** plus AND gate **107**. In practice, inverters **106**, **115** may be constructed readily from NAND gate circuits by connecting the input leads together. NAND gates **103**, **104** receive the indicated input signals from X-quadrature converter **38** and Y-quadrature converter **86**. Outputs from nAND gates **103**, **104** are provided to NAND gate **105** to effect an EXCLUSIVE OR function. The operation of NAND gates **103**, **104** and **105** is expressed logically as:

$$X\,Y+\overline{X}\,\overline{Y}=C$$
$$X\,\overline{Y}+\overline{X}\,Y=\overline{C}$$

where C is the output condition of NAND gate **105**. The various combinations of X,$\overline{X}$,Y and $\overline{Y}$ reflect the possible quadrantal conditions in the X–Y coordinate system; thus requirements 1 and 2—that the signs of X and Y be known, are satisfied.

The third basic condition—that that the zero or nonzero state of accumulator **88** be known—is satisfied by combining the output of AND gate **107**, which functions as a zero recognition detector or the condition of the stages in accumulator **88**, with C and $\overline{C}$ in NAND gates **108** and **109**, respectively. When the carryouts of counter stages **89**, **90**, **91**, **92** and **93** all are zero, so as to make AND gate **107** have **0** output, the output A from AND gate **107** is combined with C and $\overline{C}$ signals via NAND gates **108** and **109**, and the resulting signals are passed to cross-coupled NAND gates **110** and **111** which supply the necessary memory functions expressed as:

$C\,A=Q$

$\overline{C}\,A=\overline{Q}$

If the memory term is defined as Q_{N11}, where N−1 indicates the condition of the memory, a very general logic expression may be written for the output states corresponding to addition and subtraction:

$ADD=A+\overline{A}\,Q_{N11}$

$SUB=\overline{A}\,Q_{N11}$

Outputs Q and $\overline{Q}$ are combined with C and $\overline{C}$, respectively, in NAND gates **112** and **113**, the outputs of which are logically combined in NAND gate **114**. The three NAND gates **112**, **113** and **114** comprise a two-stage NAND circuit equivalent to the AND-OR function. The output of NAND gate **114**, which constitutes the ADD or $\overline{ADD}$ control signals, as well as the inverted output through inverter **115** which serves as the SUB or $\overline{SUB}$ control, are thus determined by the sign of the X signal from X-encoder **20**, the sign of the Y signal from Y-encoder **25**, and the zero or nonzero output condition of accumulator **88**.

While the complete logic expressions for the ADD and SUBTRACT control functions may be written in expanded form, the following simplified expressions apply with respect to the C and Q variables:

$SUB=C\,\overline{Q}+\overline{C}\,Q=0$

$ADD=C\,Q+\overline{C}\,\overline{Q}=1$

The memory element NAND gates **110** and **111** are set so that the output of **110** is Q and the output of **111** is $\overline{Q}$ when a zero signal is received from AND gate **107**. This condition corresponds to C and $\overline{A}$ inputs to NAND gate **108**, and $\overline{C}$ and $\overline{A}$ inputs to NAND gate **109**, plus subsequent NAND inversion. If inversion of the C input only occurs, the Q memory condition follows the C inversion so that control signal ADD is always received at the output terminal of NAND gate **114**. Because of the Q memory characteristic, however, variables C and $\overline{C}$ occur in opposite sign to Q and $\overline{Q}$ for the SUBTRACT modes.

Output control signals from up-down control **102** are connected to the respective UP and DOWN control terminals on up-down counter stages **89**—**93** to provide fully automatic control for proper accumulation of the count pulses (the connections shown in FIG. **5** are merely illustrative). Forward or "UP" counting occurs when the ADD control signal from output NAND gate **114** is a logical **1**; the invert or logical **0** is applied from inverter **115** to the "DOWN" control terminal. Reverse or "DOWN" counting takes place when the ADD control signal from NAND gate **114** is logical **0** and is inverted so as to appear as a logical **1** at the "DOWN" terminal of up-down counter stages **89**—**93**.

When using the fully automatic arrangement shown in FIGS. **5** and **5***a*, the operator has only to position the cursor **14** (FIG. **1**) on the boundary **13**, reset all up-down counters to establish the origin of the X–Y system, carefully move the cursor **14** around the boundary **13** for one complete traverse, and then read the area on the display **37**. Reversals of direction in the movement of cursor **14** introduce no error into the area indications provided the boundary of area **13** is followed carefully; in fact, excursions from the boundary are permissible provided the motion is carefully retraced.

It will be understood, of course, that the NAND functions are employed for constructional convenience; AND and NOT functions, OR and NOT functions, and NOR functions may be utilized within the scope and intent of the invention. Similarly, positive or negative logic, as well as mixed logic, may be employed without departing from the novelties and advantages of the invention.

The display apparatus illustrated in block diagram form in FIGS. **3** and **4** may comprise any suitable apparatus that will accept digital information and convert that information into a visual set of numbers indicative of the area being traversed by the cursor. For example, a suitable display device would be a series of Nixie tubes arranged to receive the accumulated data in accumulator **88**. The display means could preferably be controlled by the command pulses emitted from the Y quadrature converter such that the area measurement was displayed each time the accumulator unit was updated.

Although preferred embodiments of the invention have been described in such detail as to facilitate reproduction by those skilled in this art, such description is to be considered illustrative rather than limiting for the invention may be altered by the substitution of other components than those described herein without departing from its fundamental concepts and the spirit of the subject invention.

I claim:

1. An area measuring apparatus, comprising:

cursor means for traversing the boundary of a two-dimensional figure forming the area to be measured;

encoding means including first encoding and converter means for generating signals representing the movement of the cursor means along the boundary of the figure only in a first coordinate direction, second encoding and converter means for generating signals representing the movement of the cursor means along the boundary of the figure only in a second coordinate direction, the signals from the second encoding and converter means being command signals produced at each traversal by the cursor means of a unitary distance in the second coordinate direction;

accumulating and registering means for storing the encoder signals and computing the area of the figure, including reversible register means for temporarily storing encoding signals representative of the cursor movement in a first coordinate direction, down counter means for periodically receiving the stored data in the reversible register means and for providing the quantitative value of the stored data, accumulator means for receiving and accumulating pulsed signals representing the quantitative value of the stored data;

control means regulated by the cursor movement in one coordinative direction for generating timing and clock signals to operate the accumulating and registering means; and

display means for indicating instantaneously the accumulated data in the accumulating and registering means representing the area of the measured figure.

2. An area measuring apparatus according to claim **1** wherein the control means further includes clock generating means for providing periodic pulse signals and timing means for generating a transfer signal for transferring data from the reversible register means to the down counter means in response to a command signal from the second encoding and converter means.

3. An area measuring apparatus according to claim **2** wherein the timing means includes gating means for simultaneously transferring the periodic pulse signals to the down counter means and the accumulator means.

4. An area measuring apparatus according to claim **3** wherein the accumulating and registering means further comprises gating means responsive to the zero condition of the down counter means for controlling the timing gating means.

5. An area measuring apparatus according to claim **3** wherein the timing means is responsive to the periodic clock signals and to the command signals from the second encoding and converter means to provide synchronized periodic pulse signals, and comprises means responsive to the synchronized periodic pulse signals for generating additional control signals

for the timing gating means and for generating the transfer signal.

6. An area measuring apparatus according to claim 3 wherein the control means further includes up-down control means responsive to the signals from the first and second encoding and converter means and to the condition of the accumulator means for operating the accumulator means in either an add or a subtract mode.

7. An area measuring apparatus according to claim 6 wherein the up-down control means includes NAND gating means responsive to the signals from the first and second encoding and converter means, AND gating means responsive to the condition of the accumulator means, and means responsive to the output signals from the NAND and AND gating means for generating up and down control signals for operating the accumulator means.

8. An area measuring apparatus for measuring the area of two-dimensional figure, in combination, comprising:

cursor means for traversing the boundary of said figure, accumulating and registering means for computing the area of the two-dimensional figure in response to pulse signals representative of the movement of the cursor means along the boundary of the two-dimensional figure in a first and second coordinate direction;

the accumulating and registering means including reversible register means for storing the pulse signals representing the boundary dimension in the first coordinate direction, down counter means for periodically receiving the stored data in the reversible register means, and accumulator means for receiving and accumulating digital signals representing the quantitative value of the stored data in the reversible counter means;

control means including clock pulse generating means for providing repetitive pulse signals and timing means for

generating a transfer signal to transfer data from the reversible register means to the down counter means in response to the pulse signals representing a unit dimension of the boundary in the second coordinate direction, said control means being regulated by the cursor movement; and

display means for instantaneously indicating the accumulated data in the accumulator means representing the area of the measured figure.

9. An area measuring apparatus according to claim 8 wherein the timing means includes gating means for simultaneously transferring the repetitive pulse signals to the down counter means and the accumulator means.

10. An area measuring apparatus according to claim 9 wherein the accumlating and registering means further comprises gating means responsive to the zero condition of the down counter means for controlling the timing gating means.

11. An area measuring apparatus according to claim 10 wherein the control means further includes up-down control means responsive to the pulse signals representative of the boundaries of the two-dimensional figure and to the condition of the accumulator means for operating the accumulator means in either an add or a subtract mode.

10. An area measuring apparatus according to claim 9 wherein the accumulating and registering means further comprises gating means responsive to the zero condition of the down counter means for controlling the timing gating means.

11. An area measuring apparatus according to claim 10 wherein the control means further includes up-down control means responsive to the pulse signals representative of the boundaries of the two-dimensional figure and to the condition of the accumulator means for operating the accumulator means in either an add or a subtract mode.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,571,932 Dated March 23, 1971

Inventor(s) John G. Peddie

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 20, "register to permit" should read -- register stages to permit --. Column 6, line 65, "nAND" shoul read -- NAND --. Column 7, line 1, "that that the" should rea -- that the --; line 4, "or" should read -- for --; line 14, "Q_{N11}" should read -- Q_{N-1} --; line 18, "ADD = $A+\bar{A}\ Q_{N11}$" shou read -- ADD + $A+\bar{A}\ Q_{N-1}$ --; line 19, "SUB = $\bar{A}\ Q_{N11}$" should read -- SUB = $\bar{A}\ Q_{N-1}$ --.

Signed and sealed this 9th day of November 1971.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Acting Commissioner of Pate