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TEMPERATURE AND BIAS CONTROL OF EDGE RING

BACKGROUND

Field

[0001] Embodiments described herein generally relate to semiconductor device manufacturing, and in particular, to methods and apparatus used to control a processing profile at, and proximate to, the circumferential edge of a substrate during plasma enhanced processing thereof.

Description of the Related Art

[0002] Plasma assisted etching processes are well known and commonly used processes of record (POR) in the manufacture of high-density integrated circuits to pattern a material layer of a substrate by forming openings therein. In a typical plasma assisted etching process, a substrate is positioned on a substrate support disposed in a processing chamber, and a plasma is formed thereabove. Ions from the plasma are then accelerated towards the substrate and openings formed in a mask layer disposed thereon, to etch openings corresponding to the mask layer openings in the material layer disposed beneath the mask surface.

[0003] Often, the substrate support is part of a substrate support assembly which further includes an annular ring, herein an edge ring, disposed on the substrate support proximate to the circumference thereof. The edge ring circumscribes the substrate and protects the dielectric material of the substrate support from erosion otherwise caused by the plasma. Unfortunately, electrical and thermal discontinuities between the edge of the substrate and the portion of the edge ring disposed proximate thereto can cause undesirable processing result variation at the substrate edge. In a plasma assisted etching process, undesirable processing result variation includes non-uniformity of, i.e., differences between, the etched opening profile in openings at the perimeter or edge of the substrate compared to the etched profile of openings in regions of the substrate disposed radially inwardly from the substrate edge or perimeter. Excessive processing result variation across the surface of the edge of the substrate can adversely affect and suppress device yield (the percentage

of devices that conform to performance specifications out of the total number of devices manufactured on the substrate).

[0004] Accordingly, there is a need in the art for apparatus and methods to control processing result variation at the edge of a substrate during plasma assisted processing thereof.

SUMMARY

[0005] Embodiments described herein provide methods and apparatus used to control a processing result profile proximate to a circumferential edge of a substrate during the plasma assisted processing thereof.

[0006] In one embodiment a substrate support assembly features a first base plate and a second base plate circumscribing the first base plate. The first and second base plates each have one or more respective first and second cooling channels disposed therein. The substrate support assembly further features a substrate support disposed on and thermally coupled to the first base plate and a biasing ring disposed on and thermally coupled to the second base plate. Here, the substrate support and the biasing ring are each formed of a dielectric material. The substrate support assembly further includes an edge ring biasing electrode embedded the dielectric material of the biasing ring and an edge ring disposed on the biasing ring.

[0007] In another embodiment, a method of processing a substrate includes heating a substrate support of a substrate support assembly to a first temperature, heating an edge ring circumscribing the substrate support to a second temperature, and positioning a substrate on the substrate support. Here, the substrate support assembly is disposed in a processing volume of a processing chamber and features a first base plate and a second base plate circumscribing the first base plate. The first and second base plates each have one or more respective first and second cooling channels disposed therein. The substrate support assembly further includes the substrate support disposed on and thermally coupled to the first base plate and a

biasing ring disposed on and thermally coupled to the second base plate. The substrate support and the biasing ring are each formed of a dielectric material. The substrate support assembly further includes an edge ring biasing electrode embedded the dielectric material of the biasing ring and the edge ring disposed on the biasing ring. The method further includes flowing a processing gas into the processing volume, igniting and maintaining a plasma of the processing gas, biasing the substrate using a first bias voltage, and biasing the edge ring using a second bias voltage.

[0008] In another embodiment, a processing chamber includes a substrate support assembly disposed in a processing volume of the processing chamber and a computer readable medium having instructions stored thereon for performing a method of processing a substrate when executed by a processor. Here, the substrate support assembly includes a first base plate and a second base plate circumscribing the first base plate. The first and second base plates each have one or more respective first and second cooling channels disposed therein. The substrate support assembly further includes a substrate support disposed on and thermally coupled to the first base plate and a biasing ring disposed on and thermally coupled to the second base plate. Here, the substrate support and the biasing ring are each formed of a dielectric material. The substrate support assembly further includes an edge ring biasing electrode embedded the dielectric material of the biasing ring and an edge ring disposed on the biasing ring. The method of processing the substrate includes heating the substrate support to a first temperature, heating the edge ring circumscribing the substrate to a second temperature, and positioning a substrate on the substrate support. The method further includes flowing a processing gas into the processing volume, igniting and maintaining a plasma of the processing gas, biasing the substrate using a first bias voltage, and biasing the edge ring using a second bias voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0010] Figure 1 is a schematic cross sectional view of a processing chamber featuring a substrate support assembly configured to practice the methods set forth herein, according to one embodiment.

[0011] Figure 2A-2C are schematic cross sectional views of a portion of a substrate support assembly, according other embodiments, which may be used in the plasma processing chamber described in Figure 1.

[0012] Figure 3A-3B are schematic cross sectional views of a portion of a substrate support assembly, according to other embodiments, which may be used in the processing chamber described in Figure 1.

[0013] Figures 4A-4C are close up views of a portion of Figure 1 schematically illustrating various plasma sheath profiles formed using the methods set forth herein.

[0014] Figures 4D-4E are close up views of a portion of Figure 1 schematically illustrating the effect of various edge ring temperatures using the methods set forth herein.

[0015] Figure 5A is a schematic cross sectional view of a portion of a substrate support assembly, according to another embodiment, which may be used in the processing chamber described in Figure 1.

[0016] Figure 5B is a schematic cross sectional view of a portion of a substrate support assembly, according to another embodiment, which may be used in the processing chamber described in Figure 1.

[0017] Figures 6A-6B show comparative measurements of normalized critical dimension (CD) shrinkage proximate to the edges of substrates processed using embodiments of the methods set forth herein.

[0018] Figures 7A-7B show comparative measurements of normalized etch rate proximate to the edges of substrates processed using the same processing conditions set forth respectively in Figures 6A-6B.

[0019] Figure 8 is a flow diagram setting forth a method of processing a substrate according to embodiments described herein.

[0020] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features disclosed in one embodiment may be beneficially incorporated in other embodiments without specific recitation thereof.

DETAILED DESCRIPTION

[0021] Embodiments described herein provide methods and apparatus used to control a processing result profile proximate to a circumferential edge of a substrate during the plasma assisted processing thereof. In particular, the methods and apparatus herein provide for selective electrical biasing and for temperature control of an annular ring, herein an edge ring circumferentially disposed about the surface of the substrate support assembly on which a to be processed substrate will be supported. The biasing and temperature control of the edge ring is independent of the biasing and temperature control of a substrate support having the to be processed substrate disposed thereon.

[0022] Independent biasing and temperature control as between the substrate support and the edge ring enables fine tuning of the processing result profile

proximate to the edge of the substrate. For example, in a plasma assisted etching process the processing results on the substrate proximate to the substrate edge, e.g., within 15 mm of the edge, often deviate from the processing results on the substrate at locations radially inward from the substrate edge. This processing result non-uniformity is often attributable to corresponding discontinuities or changes in the properties of a plasma used to perform a process on the substrate which is formed over the substrate, here where the plane of the major surface of the substrate is processed in a horizontal position. Discontinuities or changes in the properties of the processing plasma include changes in the shape of the plasma region over the substrate and changes in the degree of ionization of processing gases forming the plasma across the plasma. Typically, these discontinuities or changes in the processing plasma are more pronounced in regions disposed above the edge region of the substrate and the edge ring proximate thereto, as compared to regions over the substrate and inwardly of the edge of the substrate. Therefore, the apparatus and methods provided herein enable fine control of both edge ring biasing and edge ring temperature to ameliorate these differences.

[0023] Often previous substrate processing operations, such as material deposition operations, e.g., CVD, PVD, and ALD processes, or material removal operations, e.g., chemical mechanical polishing (CMP) and wet or dry etching processing, may cause a feature profile deviation or material thickness deviation between the center region and the edge regions of the substrate. In such circumstances, the fine control of both edge ring biasing and edge ring temperature enabled by embodiments described herein may be used to compensate for the center-to-edge non-uniformities from the previous substrate processing operations.

[0024] Edge ring biasing facilitates tuning the shape of the plasma in regions disposed above and proximate to the substrate edge by controlling the shape of a plasma sheath, as shown and described in Figures 1 and 4A-4C. Where the plasma sheath curves the trajectories of ions pulled towards the biased substrate are different than the trajectories of ions pulled towards the substrate from a plasma when the sheath is parallel to the substrate surface. Controlling the edge ring

temperature affects the concentration of reactive neutral species, e.g., radicals and activated molecules, in the processing gases, and thus tunes the chemical reactions involving the reactive neutrals, in regions disposed above and proximate to the substrate edge.

[0025] Figure 1 is a schematic cross-sectional view of a plasma processing chamber configured to practice the methods set forth herein, according to one embodiment. In this embodiment, the processing chamber is a plasma etch processing chamber, such as a reactive ion etch (RIE) plasma chamber. In other embodiments, the processing chamber is a plasma-enhanced deposition chamber, for example a plasma-enhanced chemical vapor deposition (PECVD) chamber, a plasma enhanced physical vapor deposition (PEPVD) chamber, or a plasma-enhanced atomic layer deposition (PEALD) chamber. In other embodiments, the processing chamber is a plasma treatment chamber, or a plasma based ion implant chamber, for example a plasma doping (PLAD) chamber, or a physical vapor deposition (PVD) chamber. Herein, the processing chamber includes an inductively coupled plasma (ICP) source electrically coupled to a radio frequency (RF) power supply. In other embodiments, the plasma source is a capacitively coupled plasma (CCP) source, such as a plasma electrode disposed in the processing volume where the plasma electrode is electrically coupled to an RF power supply and capacitively couples energy and power into the plasma in the chamber.

[0026] The processing chamber 100 features a chamber body 101 including a chamber lid 102, one or more sidewalls 103, and a chamber base 104, which collectively define a processing volume 105. The processing volume 105 is fluidly coupled to a processing gas source 106 which delivers processing gases therein. The processing chamber 100 further includes a plasma generator 107 configured to ignite and maintain a plasma 108 of the processing gas(es) introduced into the processing volume through the processing gas source. The plasma generator 107 includes one or more inductive coils 109 disposed proximate to the chamber lid 102 at a location outside of the processing volume 105. The one or more inductive coils 109 are electrically coupled to an RF power supply 110. The plasma generator 107

is used to ignite and maintain the plasma 108 by inductively coupling energy from the inductive coils 109 powered by the RF power supply 110 into the processing gas(es). Here, the processing volume 105 is fluidly coupled to a vacuum source, such as one or more dedicated vacuum pumps to maintain the processing volume 105 at sub-atmospheric pressure and evacuate processing, and other gases, therefrom. Typically, the processing chamber includes a system controller 111 which is used to control the operation of the processing chamber and implement the methods set forth herein.

[0027] Herein, the system controller 111 includes a programmable central processing unit, herein the CPU 112, that is operable with a memory 113 (e.g., non-volatile memory) and support circuits 114. The support circuits 114 are conventionally coupled to the CPU 112 and comprise cache, clock circuits, input/output subsystems, power supplies, and the like, and combinations thereof coupled to the various components of the processing chamber 100, to facilitate control thereof. The CPU 112 is one of any form of general purpose computer processor used in an industrial setting, such as a programmable logic controller (PLC), for controlling various components and sub-processors of the processing chamber 100. The memory 113, coupled to the CPU 112, is non-transitory and is typically one or more of readily available memories such as random access memory (RAM), read only memory (ROM), floppy disk drive, hard disk, or any other form of digital storage, local or remote.

[0028] Typically, the memory 113 is in the form of a computer-readable storage media containing instructions (e.g., non-volatile memory), that when executed by the CPU 112, facilitates the operation of the processing chamber 100. The instructions in the memory 113 are in the form of a program product such as a program that implements the methods of the present disclosure. The program code may conform to any one of a number of different programming languages. In one example, the disclosure may be implemented as a program product stored on computer-readable storage media for use with a computer system. The program(s) of the program

product define functions of the embodiments (including the methods described herein).

[0029] Illustrative computer-readable storage media include, but are not limited to: (i) non-writable storage media (e.g., read-only memory devices within a computer such as CD-ROM disks readable by a CD-ROM drive, flash memory, ROM chips or any type of solid-state non-volatile semiconductor memory) on which information is permanently stored; and (ii) writable storage media (e.g., floppy disks within a diskette drive or hard-disk drive or any type of solid-state random-access semiconductor memory) on which alterable information is stored. Such computer-readable storage media, when carrying computer-readable instructions that direct the functions of the methods described herein, are embodiments of the present disclosure. In some embodiments, the methods described herein, or portions thereof, are performed by one or more application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), or other types of hardware implementations. In some other embodiments, the processes described herein are performed by a combination of software routines, ASIC(s), FPGAs and, or, other types of hardware implementations.

[0030] The processing chamber 100 further includes a substrate support assembly 115 disposed in the processing volume 105. The substrate support assembly 115 is disposed on a support shaft 116 sealingly extending through the chamber base 104, such as being surrounded by a bellows (not shown) in a region below the chamber base 104 or in a region disposed between the substrate support assembly 115 and the chamber base 104. Typically, a substrate 117 is loaded into the processing volume 105 through an opening (not shown) in one of the one or more sidewalls 103 which is conventionally sealed with a door or a valve (not shown) during substrate processing. Transferring of the substrate 117 to and from the substrate support assembly 115 is facilitated by a plurality of lift pins 118 movably disposed therethrough. In a raised position, the lift pins 118 extend above a surface of the substrate support assembly 115 lifting the substrate 117 therefrom and enabling access to the substrate 117 by a robot handler (not shown). In a lowered

position, the upper surfaces (not shown) of the lift pins 118 are flush with, or disposed below, the surface of the substrate support assembly 115 and the substrate 117 rests thereon.

[0031] Here, the substrate support assembly 115 includes a substrate support 119 disposed on, and thermally coupled to, a first base plate 120, and a second base plate 121 circumscribing the first base plate 120. The substrate support 119 is formed from a dielectric material, such as a bulk sintered ceramic material, such as silicon carbide (SiC) or a metal oxide or metal nitride ceramic material, for example aluminum oxide (Al₂O₃), aluminum nitride (AlN), titanium oxide (TiO), titanium nitride (TiN), yttrium oxide (Y₂O₃), mixtures thereof, and combinations thereof. The substrate support 119 is thermally coupled to the first base plate 120 by a thermally conductive adhesive or by mechanical means including a thermally conductive material, such as a thermally conductive and physically conforming gasket or other conductive material, disposed between the first base plate 120 and the substrate support 119. In some embodiments, one or both of the first base plate 120 and the second base plate 121 are formed of a corrosion resistant thermally conductive material, such as a corrosion resistant ceramic or metal, for example aluminum, an aluminum alloy, stainless steel, or aluminum nitride (AlN).

[0032] The substrate support assembly 115 further includes a biasing ring 122 disposed on the second base plate 121 and an edge ring 123 disposed over the biasing ring 122. The biasing ring 122 is typically made of a dielectric material having an electrode embedded therein. The dielectric material can be one or a combination of the ceramic materials which may be used to form the substrate support 119 as set forth above. Typically, the edge ring 123 is formed of a thermally and electrically conductive material, such as silicon, graphite, silicon carbide, or a combination thereof. In some embodiments, the edge ring 123 is thermally coupled to the biasing ring 122 by a thermally conductive material 124, such as a silicone gasket, interposed therebetween. In other embodiments, the thermally conductive material 124 comprises a silicone or acrylic based tape or paste.

[0033] In some embodiments, protective rings 125a-b are disposed between the edge ring 123 and the biasing ring 122 and on the inner and outer circumferential sides of the thermally conductive material 124, to protect the thermally conductive material 124 from processing gas and plasma caused corrosion by preventing exposure thereto. The first protective ring 125a circumscribes the thermally conductive material 124 and is thus disposed proximate to and radially outward therefrom. The second protective ring 125b is disposed radially inward of the thermally conductive material 124 and proximate thereto. Here, the protective rings 125a-b are formed of a processing gas and plasma resistant polymer. Examples of suitable polymers include one or more fluorine-containing polymers (fluoropolymer), such as perfluoroalkoxy (PFA), fluorinated ethylene propylene (FEP), polytetrafluoroethylene (PTFE) commercially available as TEFLON® from DuPont, or combinations thereof.

[0034] In other embodiments, the edge ring 123 is disposed directly on the biasing ring 122 and is in direct contact therewith. Typically, in those embodiments, the interfacial surfaces of one or both of the edge ring 123 and the biasing ring 122 are polished during the manufacturing thereof. The polished interfacial surfaces of the edge ring 123 and the biasing ring 122 result in increased surface contact area relative to unpolished surfaces and thus desirably increased heat transfer rates there between. In some embodiments, the a DC power supply 141 is electrically coupled to an electrode embedded in the biasing ring 122, such as the edge ring biasing electrode 136 or a second electrode (not shown). In those embodiments, the edge ring biasing electrode 136 or the second electrode is used to ensure close contact and thus high thermal transfer rate between the biasing ring 122 and the edge ring 123 by providing a potential between the edge ring 123 and the edge ring biasing electrode or the second electrode which results in an electrostatic (ESC) attraction force therebetween.

[0035] Here, the substrate support 119 includes one or more chucking electrodes 126 embedded in a dielectric material thereof. The one or more chucking electrodes 126 are used to secure the substrate 117 to the substrate support 119 by providing a

potential between the substrate 117 and the chucking electrode(s) 126 which results in an electrostatic (ESC) attraction force therebetween. Here, the one or more chucking electrodes 126 are coupled to a chucking power source 127, such as a DC power supply, which provides a chucking voltage thereto.

[0036] The substrate support assembly 115 is further configured to bias one or both the edge ring 123 and the substrate 117 with respect to the plasma 108 formed thereabove. Typically, the substrate 117 is biased through capacitive coupling with an electrode having a substrate biasing voltage applied thereto. The electrode used to provide the bias may be disposed in or beneath the dielectric material of the substrate support 119. In some embodiments, biasing the substrate 117 comprises applying a substrate biasing voltage to the chucking electrode 126 disposed in the dielectric material of the substrate support 119. In those embodiments, the chucking electrode 126 is electrically coupled to both the chucking power source 127 and the biasing power source 134 (electrical coupling between the biasing power source 134 and the chucking electrode 126 is shown in phantom). In those embodiments, the chucking electrode 126 is used to provide both the substrate bias and the DC chucking potential. In some embodiments, biasing the substrate 117 includes applying a substrate biasing voltage from a biasing power source 134 to the first base plate 120 which is electrically coupled to the biasing power source 134. In other embodiments, biasing the substrate 117 comprises applying a biasing voltage to a substrate biasing electrode (not shown) embedded in the dielectric material of the substrate support 119. When used, a substrate biasing electrode is typically electrically isolated from the chucking electrode 126 by dielectric material of the substrate support 119 disposed therebetween. Typically, the biasing power source 134 provides one or a combination of continuous wave (CW) RF power, pulsed RF power, CW DC power, or pulsed DC power.

[0037] Biasing the edge ring 123, independently of biasing the substrate 117, includes applying an edge ring biasing voltage to an edge ring biasing electrode 136. Here, the edge ring biasing electrode 136 is embedded in the dielectric material of the biasing ring 122 and is electrically coupled to the biasing power source 134

through a tuning circuit 137 disposed therebetween. In other embodiments, the edge ring biasing electrode 136 is electrically coupled to a second biasing power source 140 which is different from the biasing power source 134 (electrical coupling between the edge ring biasing electrode 136 and the second biasing power source 140 is shown in phantom). Independent biasing of the edge ring 123 and the substrate 117 allows fine control of the shape of a plasma sheath 138a proximate to the circumferential edge of the substrate 117. The plasma sheath 138a typically defines a dark-space boundary region disposed between the bulk of the plasma 108 and the surfaces of the substrate 117 and the edge ring 123 facing the plasma 108. Controlling the shape of the plasma sheath 138a is further discussed in the description set forth with respect to Figures 4A-4C below.

[0038] In some embodiments, one or both of the first base plate 120 and the second base plate 121 are formed of a thermally conductive electrically insulating material, such as metal nitride ceramic material, for example aluminum nitride (AlN). Forming one or both of the first and second base plates 120 and 121 of a thermally conductive electrically insulating material desirably prevents or substantially eliminates cross-talk between the edge ring biasing electrode 136 and an electrode used to provide a biasing power the substrate, e.g., a substrate biasing electrode (described above but not shown) or the chucking electrode 126 when the biasing power source 134 is electrically coupled thereto. "Cross-talk" as used herein is the undesirable electrical interference between the powers provided to each of the electrodes which may undesirably interfere with the ability to independently control the biasing powers thereto. Typically, cross-talk results from the capacitive coupling of electrodes and an otherwise electrically conductive base plate or base plates, e.g., aluminum base plates, through the relatively thin dielectric materials of the substrate support or biasing ring disposed therebetween.

[0039] Here, the substrate support assembly 115 further includes one or more first heating elements 128 embedded in the dielectric material of the substrate support 119 and one or more first cooling channels 129 disposed in the first base plate 120. The one or more first heating elements 128 are used to heat the substrate support

119, and thus the substrate 117 disposed thereon, to a desired temperature before processing and to maintain the substrate 117 at a desired temperature during processing. The one or more first cooling channels 129 are fluidly coupled to, and in fluid communication with, a coolant source (not shown), such as a refrigerant source or modified water source having a relatively high electrical resistance. The first base plate 120 is used to regulate the temperature of the substrate support 119, and thus the temperature of a substrate 117 disposed on the substrate support 119, during substrate processing. The first heating element(s) 128 and the coolant flow through the first cooling channels 129 may be used alone or in combination to facilitate fine control of the temperature of the substrate support 119 and thus fine control of the temperature of the substrate 117 disposed thereon.

[0040] The temperature of the edge ring 123 is maintained and controlled independently of the temperature of the substrate 117 using one or both of a second heating element 130 and a second cooling channel 131. In this embodiment, the second heating element 130 comprises a resistive heating element embedded in the dielectric material of the biasing ring 122. The second heating element 130 is used to heat the biasing ring 122, and thus heat the edge ring 123 thermally coupled to the biasing ring 122, to a desired temperature before substrate processing and, in combination with a coolant flowing through the second cooling channel 131, to maintain the edge ring at a desired temperature during substrate processing. Here, the biasing ring 122 is thermally insulated from the substrate support 119 by a first insulator ring 132 interposed therebetween.

[0041] Here, the second cooling channel 131, disposed in the second base plate 121, is fluidly coupled to and in fluid communication with a coolant source (not shown) which may be the same or a different from the coolant source used to deliver cooling fluid to the first cooling channel(s). In embodiments where the same coolant source is used the coolant flowrate through the first and second cooling channels is independently controlled to facilitate independent temperature control of the first and second base plates 120, 121 respectively. Typically, the second base plate 121 is thermally isolated from the first base plate 120 by a second insulator ring 133

interposed therebetween. The first and second insulator rings 132, 133 are typically formed of a material suitable for inhibiting heat transfer between the substrate support 119 and the biasing ring 122 and between the first and second base plates 120 and 121 respectively. Examples of suitable materials which may be used for the thermal insulator rings 132, 133 include PTFE, quartz, silicone, and combinations thereof. In some embodiments, a thermal insulator ring is not used and the first base plate and the second base plate are spaced apart and thermally isolated from one another by a vacuum provided in the space therebetween.

[0042] Here, the substrate support assembly 115 further includes one or more temperature sensors, such as the thermocouple 135, disposed in or proximate to dielectric material of the biasing ring 122. The thermocouple 135 is used to monitor the temperature of the biasing ring 122 and thus the temperature of the edge ring 123 thermally coupled thereto. In some other embodiments, one or both of the substrate support 119 and the edge ring 123 are heated using a dedicated heater therefor disposed therebeneath, such as shown in Figure 2A. In some other embodiments, both the substrate support 119 and the edge ring 123 are disposed on a common baseplate such as shown in Figure 3.

[0043] Figure 2A is a schematic cross-sectional view of a portion of a substrate support assembly 200a, according to one embodiment, which may be used in place of the substrate support assembly 115 in the processing chamber 100 described in Figure 1. Here, a first heater, such as the first heating plate 201 is interposed between the substrate support 119 and the first base plate 120 and a second heater, such as the second heating plate 202, is interposed between the biasing ring 122 and the second base plate 121. The first heating plate 201 is thermally isolated from the second heating plate 202 by the first insulator ring 132 disposed therebetween. The second base plate 121 is thermally isolated from the first base plate 120 by a second insulator ring 133 interposed therebetween.

[0044] Figure 2B is a schematic cross-sectional view of a portion of a substrate support assembly 200b, according to one embodiment, which may be used in place

of the substrate support assembly 115 in the processing chamber 100 described in Figure 1. Here, the substrate support assembly 200a is similar to the substrate support assembly 115 described in Figure 1 and further includes a first electrically insulating plate 203 and a second electrically insulating plate 204. The first electrically insulating plate 203 is interposed between the substrate support 119 and the first base plate 120. The second electrically insulating plate 204 is interposed between the biasing ring 122 and the second base plate 121. Here, the second electrically insulating plate 204 circumscribes the first electrically insulating plate 203 and is thermally isolated therefrom by one or both of the first insulator ring 132 and the second insulator ring 133 interposed therebetween.

[0045] Typically, one or both of the first and second electrically insulating plates 203 and 204 are formed of a thermally conductive electrically insulating material, such as metal nitride ceramic material, for example aluminum nitride (AlN). The electrically insulating plates 203 and 204 desirably prevent or substantially eliminate cross-talk between the edge ring biasing electrode 136 and an electrode used to provide a biasing power to the substrate, e.g., a substrate biasing electrode (described above but not shown) or the chucking electrode 126 when the biasing power source 134 is electrically coupled thereto. In some embodiments, one or both of the electrically insulating plates 203 and 204 have a thickness sufficient to substantially eliminate or significantly reduce capacitive coupling of the respective electrodes disposed there above with the respective base plates disposed there below. For example, in some embodiments, one or both of the electrically insulating plates 203 and 204 have a thickness of more than about 5 mm, such as more than about 10 mm, or for example between about 5 mm and about 50 mm.

[0046] Figure 2C is a schematic cross-sectional view of a portion of a substrate support assembly 200c, according to one embodiment, which may be used in place of the substrate support assembly 115 in the processing chamber 100 described in Figure 1. Here, the substrate support assembly 200c is similar to the substrate support assembly 115 described in Figure 1 and further includes an electrically insulating plate 204 interposed between the second base plate 121 and the biasing

ring 122. The substrate support assembly 200c does not include the electrically insulating plate 203 described in Figure 2B and the first base plate 120 is supported by at least a portion of a facility plate 205. The facility plate 205 provides structural support to the substrate support assembly 200c and may be used with one or any combination of embodiments described herein. In other embodiments, the substrate support assembly may include the electrically insulating plate 203 and not include the electrically insulating plate 204. Including one of the electrically insulating plates and not the other reduces the manufacturing the costs of the substrate support assembly while still reducing or substantially eliminating the cross-talk between biasing electrodes.

[0047] Figure 3A is a schematic cross-sectional view of a portion of a substrate support assembly 300b, according to another embodiment, which may be used in place of the substrate support assembly 115 in the processing chamber 100 described in Figure 1. Here, both the substrate support 119 and the biasing ring 122 are disposed on a common base plate 301. The temperature of the base plate 301 is regulated using one or more cooling channels 302 disposed therein. The one or more cooling channels 302 are fluidly coupled to, and in fluid communication with, a coolant source (not shown), such as a refrigerant source or modified water source having a relatively high electrical resistance. The base plate 301 is used to regulate the temperature of the substrate support 119 and the biasing ring 122, and thus the temperature of a substrate 117 and an edge ring 123 respectively disposed on the substrate support 119 and the biasing ring 122, during substrate processing. Here, the substrate support 119 and the biasing ring 122 are thermally insulated from each other by an insulator ring 303 interposed therebetween. In this embodiment, each of the substrate support 119 and the biasing ring 122 include a respective heating element 128, 130 embedded in the dielectric material thereof. In other embodiments, the substrate support 119 and the biasing ring 122 are heated using heating plates, such as the heating plates 201, 202 shown in Figure 2.

[0048] Typically, the biasing ring 122, and thus the edge ring 123 disposed thereon, is maintained at a desired temperature or within a desired range of

temperatures using measurements provided by the one or more thermocouples 135. The measured temperature(s) are communicated to the system controller 111 which compares the measured temperature(s) to a desired temperature set point or a desired temperature range. If the measured temperature falls below the desired temperature set point or below the desired temperature range the system controller 111 will increase heat flow into the edge ring 123. Typically, heat flow to the edge ring 123 is increased by applying, or increasing, a power provided to a second heating element 130, shown in Figures 1 and 3, or to a second heating plate 202, shown in Figure 2. If the measured temperature rises above the desired temperature set point or above the desired temperature range the system controller 111 will remove heat from the edge ring 123. Typically, heat is removed from the edge ring 123 by turning off or lowering the power applied to the biasing ring 122, changing the coolant flow rate to the second base plate 121, shown in Figures 1 and 2, or the combined base plate, shown in Figure 3A, or a combination thereof. In some embodiments, the substrate support assembly 300a further includes one or both of the first electrically insulating plate 203 and the second electrically insulating plate 204 (shown in Figure 2B) respectively interposed between the base plate 301 and the substrate support 119 or the base plate 301 the biasing ring 122.

[0049] Figure 3B is a schematic cross-sectional view of a portion of a substrate support assembly 300b, according to one embodiment, which may be used in place of the substrate support assembly 115 in the processing chamber 100 described in Figure 1. Here, the substrate support assembly 300b further includes a common electrically insulating plate 304 interposed between the common base plate 301 and the substrate support 119 and biasing ring 122. The electrically insulating plate 304 may be formed of the same material and have the same thickness as described above with respect to the first and second electrically insulating plates 203 and 204.

[0050] Figures 4A-4C are schematic cross sectional views of a portion of the processing chamber 100 shown in Figure 1 respectively illustrating various shapes of plasma sheaths 138a-c proximate to the edge of the substrate 117. Herein, the shapes of the plasma sheaths 138a-c are controlled by adjusting the ratio of biasing

voltages applied to the substrate 117, and to the edge ring 123, using the methods set forth herein. Typically, increasing the bias voltage provided to the edge ring 123 results in relatively thicker plasma sheath 138b above the edge ring 123 when compared to an edge ring 123 having a lower, or no, bias voltage applied thereto.

[0051] In Figure 4A the plasma sheath 138a has a uniform thickness across a region disposed above the substrate 117 and a region disposed above a portion of the edge ring 123 proximate to the substrate 117. The uniform thickness of the plasma sheath 138a facilitates the acceleration of ions from the plasma 108 towards the surface of the substrate 117 in a trajectory 401 which is substantially uniform and orthogonal to the surface of the substrate 117 proximate to the edge thereof.

[0052] In Figure 4B the plasma sheath 138b is thicker in the region disposed above the edge ring 123 than in the region disposed above the substrate 117. As shown in Figure 4B, the plasma sheath 138b bends away from the edge of the substrate 117 in the region disposed there above. Here, the trajectory 401 of ions from the plasma 108 to the edge of the substrate 117 disposed there below is angled towards the edge ring 123. Thus, the ion trajectory 401 proximate to the edge of the substrate in Figure 4B is less focused than in Figures 4A and 4C and the etch rate at proximate to the edge of the substrate is comparatively reduced.

[0053] In Figure 4C the plasma sheath 138c is thinner in the region disposed above the edge ring 123 than in the region disposed above the substrate 117. As shown in Figure 4C the plasma sheath bends towards the edge of the substrate 117 in the region disposed there above. Here, the trajectory 401 of ions from the plasma 108 towards the substrate 117 is angled away from the edge ring 123 around the circumference of the substrate 117. Thus, the ion trajectory 401 proximate to the edge of the substrate in Figure 4C is more focused than in Figures 4A and 4B and the concentration of ions bombarding the substrate, and thus the etch rate, proximate to the edge of the substrate is comparatively increased. By reducing or increasing the focus of the ion trajectory 401 proximate to the edge of the substrate 117 the etch

rate can be tuned to be respectively slower or faster at the edge when compared to the rest of the substrate disposed radially inward therefrom.

[0054] In addition to increasing or decreasing the focus of ions bombarding the substrate surface proximate to the substrate edge, tuning the curvature of the plasma sheath changes the directionality of the openings etched in the material layer(s) thereof. For example, in Figure 4A the trajectories 401 of ions striking the substrate surface proximate to the edge of the substrate are substantially perpendicular thereto and the openings (not shown) formed therefrom will be substantially perpendicular to the substrate surface. In Figures 4B and 4C the trajectories 401 of ions are respectively angled away from or towards the center of the substrate 117 and the resulting openings formed therefrom will be angled accordingly. Thus the angle of the etched openings can be tuned by the edge ring bias power in order to compensate the effects where other chamber components results in feature tilting on the edge of the substrate, such as nonuniform plasma distribution due to plasma source or bias, or edge ring thinning over the useful production lifetime of the substrate support.

[0055] Figures 4D and 4E schematically illustrate the effect of the edge ring temperature on the neutral reactive species concentration above and proximate to the edge of the substrate. Here, the edge ring 123 in Figure 4D is maintained at a lower temperature than the edge ring 123 in Figure 4E. The etch rate profile and polymer deposition profile from locations at the edge of the substrate to locations disposed radially inward therefrom are schematically represented by arrows 405 and 407 respectively. When the edge ring temperature is relatively low (Figure 4D), more polymerizing species 403 tend to deposit on the edge ring 123, resulting in lower concentration of polymerizing species above the edge ring 123 and near the substrate edge. Thus, comparatively less polymer deposits on the substrate edge which results in an edge-high etch rate profile, i.e., an increased etch rate at the edge of the substrate compared to regions disposed radially inward therefrom. On the other hand, when the edge ring temperature is relatively high (Figure 4E), less polymer deposition will occur on the edge ring 123 and there is higher polymerizing species concentration near the substrate edge. Thus, comparatively more polymer

deposits on the substrate edge which results in an edge-slow etch rate profile, i.e., a decreased etch rate at the edge of the substrate compared to regions disposed radially inward therefrom.

[0056] In other embodiments, the high bias power applied on the edge ring can function in part as the elevated edge ring temperature to reduce polymer deposition on the edge ring, thus increasing polymerizing species concentration above the substrate edge. In other embodiments, the bias power applied on the edge ring can be a tuning knob to increase or decrease the sensitivity of the process near the substrate edge to the edge ring temperature.

[0057] Figures 5A and 5B are schematic cross sectional views of a portion of a substrate support assembly according to some embodiments, which may be combined with one or a combination of other embodiments of the substrate support assemblies described herein. In Figure 5A the substrate support assembly 500a may be any one of the substrate support assemblies shown in Figures 1-4 or set forth in the descriptions thereof and further includes an electrically insulating ring 502 made of a dielectric material, such as a quartz or a metal oxide ceramic, disposed on the edge ring 123. Typically, the plasma facing surface of the electrically insulating ring 502 will have a lower etch rate than the plasma facing surface of the edge ring 123 (when the electrically insulating ring 502 is not disposed thereon) and thus will desirably extend the substrate processing lifetime of the substrate support assembly 500a. In other embodiments, the electrically insulating ring 502 is formed of a material that is less likely to generate particles in the chamber for the sake of defect control.

[0058] Figure 5B is a schematic cross sectional view of a portion of a substrate support assembly, according to another embodiment, which may be used in the processing chamber described in Figure 1. In Figure 5B the substrate support assembly 500b may be any one of, or comprise any combination of the features of, the substrate support assemblies shown and described in Figures 1-3. Here, the edge ring 123 extends above a plane of the plasma facing surface of the substrate by

a height H, i.e., the plasma facing surface of the edge ring 123 stands taller than the plasma facing surface of the substrate 117. Typically, if the processing conditions and biasing conditions are the same, the thickness of the sheath disposed above the edge ring will be the same. Assuming the processing conditions and biasing conditions shown in Figure 4A, extending the plasma facing surface of the edge ring 123 above the plane of the plasma facing surface of the substrate 117 will also push the sheath upwards to create a plasma profile resembling the plasma profile of Figure 4B. Thus, extending the plasma facing surface of the edge ring 123 above the plane of the plasma facing surface of the substrate 117 will allow for the formation of the plasma profile of Figure 4B at relatively reduced edge ring biasing power when compared to a coplanar biasing ring and substrate surface configuration. In other embodiments, the edge ring 123 will be recessed from a plane of the surface of the substrate and, for the same processing conditions described in Figure 4A, the resulting plasma profile will more closely resemble the plasma profile of Figure 4C.

[0059] Charts 600a-b of Figures 6A-6B respectively, show comparative measurements of normalized critical dimension (CD) shrinkage proximate to the edges of substrates processed using embodiments of the methods set forth herein. Charts 700a-b of Figures 7A-7B respectively, show comparative measurements of normalized etch rate proximate to the edges of substrates processed using the same processing conditions set forth respectively in Figures 6A-6B.

[0060] CD shrinkage enables the patterning of openings in the surface of a substrate where the openings have a dimension which is less than a lithography defined dimension in a photoresist layer disposed thereabove. Typically, the photoresist layer is formed on a multi-layer mask disposed on the to be etched surface of the substrate to be processed. Openings in the photoresist layer and multi-layer mask are formed by forming a plasma of a processing gas comprising an etchant and a polymerizing gas and exposing a substrate, having the multi-layer mask and the photoresist layer formed thereon, to the plasma. The polymerizing gas forms a polymerized passivation layer on the sidewalls of the openings being etched into the multi-layer stack to decrease the CD of the etched features as they are

formed therein. Thus, the dimensions of the openings formed in the surface of the substrate are reduced, and thus shrunk, when compared to the lithography defined dimensions patterned in the photoresist layer. Typically, the polymerized passivation layer forms faster on a relatively colder surface than that on a warmer surface due to a higher sticking coefficient, and thus absorption, of the polymerizing species on the colder surface.

[0061] In Figures 6A-6B and 7A-7B each of the substrates were processed by forming a plasma of an etchant gas and a polymerizing gas, biasing the substrate, and exposing the substrate to the plasma. Here, the etchant and polymerizing gas included CHF_3 at a flowrate of 100 sccm, CF_4 at 50 sccm, N_2 at 100 sccm, Ar at 100 sccm. The substrates were biased using a biasing power of 0.14 W/cm^2 of substrate surface area and the edge ring bias was varied between about 10 W and about 60 W. Each of the substrates processed had a radius of 150 mm. CD shrinkage, shown in Figures 6A-6B, was measured a plurality of radial locations disposed between about 105 mm and about 145 mm from the center of the substrate. An etch rate example, shown in Figures 7A-7B, was measured at a plurality of radial locations disposed between about 100 mm and about 150 mm from the center of the substrate.

[0062] In Figure 6A the edge ring was biased using a lower bias voltage than the bias voltage applied to the edge ring in Figures 6B. In Figures 6A and 6B respectively, substrates 601a-b, 602a-b, and 603a-b were processed using edge rings maintained at three different temperatures relative to the temperature of a substrate support having the substrate disposed thereon. For substrates 601a,b the temperature of the edge ring was maintained at about 30°C less than the temperature of the substrate support to provide a temperature differential of $\Delta -30^\circ\text{C}$ therebetween. For substrates 602a,b the temperature of the edge ring was maintained at about 40°C more than the temperature of the substrate support to provide a temperature differential of $\Delta +40^\circ\text{C}$ therebetween. For substrates 603a,b the edge ring temperature was maintained at about the same temperature as the substrate support to provide a temperature differential of $\Delta 0^\circ\text{C}$ therebetween.

[0063] In both Figures 6A and 6B decreasing the temperature of the edge ring relative to the substrate 601a,b reduces CD shrinkage at the edge of the substrate compared to CD shrinkage measured at sites disposed radially inward therefrom. In both Figures 6A and 6B increasing the temperature of the edge ring relative to the substrates 602a,b increases CD shrinkage at the edge of the substrate compared to CD shrinkage measured at sites disposed radially inward therefrom. As shown in Figure 6A and 6B, tuning the edge ring temperature is an effective tuning knob to tune the CD profile at the edge of the substrate.

[0064] Notably, the effect of varying the edge ring temperature has a more pronounced effect on both reducing and increasing CD shrinkage at the edge of the substrate when the edge ring is biased using a relatively lower bias voltage, as shown in Figure 6A, than when the edge ring is biased using the higher edge ring bias voltage, as shown in Figure 6B. This suggests that controlled biasing of the edge ring can enlarge or reduce the temperature turning effect of the edge ring by controlling the thickness of the plasma sheath formed there above.

[0065] Figures 7A-7B show comparative measurements of the etch rate example, proximate to the edge of a substrate processed using embodiments of the methods set forth herein. In Figure 7A the edge ring was biased using a lower bias voltage than the bias voltage applied to the edge ring in Figures 7B. Here, the substrates 701a-b, 702a-b, and 703a-b were processed using the same processing conditions respectively set forth for the substrates 601a-b, 602a-b, and 603a-b of Figures 6A and 6B. For substrates 701a,b the temperature of the edge ring was maintained at about 30 °C less than the temperature of the substrate support to provide a temperature differential of $\Delta -30$ °C therebetween. For substrates 702a,b the temperature of the edge ring was maintained at about 40 °C more than the temperature of the substrate support to provide a temperature differential of $\Delta +40$ °C therebetween. For substrates 703a,b the edge ring temperature was maintained at about the same temperature as the substrate support to provide a temperature differential of $\Delta 0$ °C therebetween.

[0066] In both Figures 7A and 7B decreasing the temperature of the edge ring relative to the temperature of the substrates 601a,b generally increases the etch rate measured at the edge of the substrate compared to etch rates measured radially inward therefrom. In both Figures 7A and 7B increasing the temperature of the edge ring relative to the temperature of the substrates 702 a,b decreased the etch rate measured at the edge of the substrate compared to etch rates measured radially inward therefrom.

[0067] Similar to the CD shrinkage measurements set forth in Figures 6A and 6B, the effect of varying the edge ring temperature is more pronounced in both reducing and increasing the etch rate towards the edge of the substrate when the edge ring is biased using a relatively lower bias voltage, as shown in Figure 7A, than when the edge ring is biased using the higher edge ring bias voltage, as shown in Figure 7B. This again suggests that controlled biasing of the edge ring can enlarge or reduce the temperature turning effect of the edge ring by controlling the thickness of the plasma sheath formed there above.

[0068] Figure 8 is a flow diagram setting forth a method 800 of processing a substrate using a substrate support assembly configured according to embodiments described herein. At activity 801 the method includes positioning a substrate on a substrate support assembly disposed in a processing volume of a processing chamber, such as the processing chamber described in Figure 1. Here, the substrate support assembly features a first base plate and a second base plate circumscribing the first base plate. Each of the first and second base plates include one or more first and second channels respectively disposed therein. The substrate support assembly further includes a substrate support disposed on and thermally coupled to the first base plate and a biasing ring disposed on and thermally coupled to the second base plate. Here the substrate support and the biasing ring are each formed of a dielectric material. The biasing ring further includes an edge ring biasing electrode embedded the dielectric material of the biasing ring and an edge ring disposed on the biasing ring.

[0069] At activities 802 and 803 the method 800 includes respectively heating the substrate to a first temperature and heating an edge ring circumscribing the substrate to a second temperature. Typically, the substrate support, and thus the substrate disposed thereon, is heated to the first temperature using a first heater disposed between the substrate support and the first base plate or embedded in the dielectric material of the substrate support. The biasing ring, and thus the edge ring disposed thereon, is heated to the second temperature using a second heater disposed between the biasing ring and the second base plate or embedded in the dielectric material of the biasing ring. In some embodiments, the method 800 further includes maintaining the substrate at a desired temperature or within a desired range of temperatures and maintaining the edge ring at a desired temperature or within a desired range of temperatures. Here, the temperatures of the edge ring and substrate support are controlled independently from one another. Controlling the edge ring temperature enables tuning of the polymerizing species concentration near the edge ring and proximate to the edge of the substrate within the plasma, thus tuning the process profile.

[0070] At activities 804 and 805 the method 800 respectively includes flowing a processing gas into the processing volume of a processing chamber and igniting and maintaining a plasma of the processing gas.

[0071] At activities 806 and 807 the method 800 respectively includes biasing the substrate using a first bias voltage and biasing the edge ring using a second bias voltage. Here, biasing the substrate includes applying the first bias voltage to one of the first base plate, a chucking electrode embedded in the dielectric material of the substrate support, or a biasing electrode embedded in the dielectric material of the substrate support. Biasing the edge ring includes applying the second bias voltage to an edge ring biasing electrode embedded in the dielectric material of the biasing ring.

[0072] At activity 808 the method 800 includes determining a ratio of the first bias voltage and the second bias voltage. At activity 809 the method 800 includes

adjusting the second bias voltage to achieve a target voltage ratio. In some embodiments, the first bias voltage is maintained at a constant voltage while the second bias voltage is adjusted to achieve the target voltage ratio.

[0073] The methods described herein beneficially allow for fine control and tuning of plasma properties in regions disposed above and proximate to the edge of the substrate being processed. Fine control and tuning of the plasma properties allows for fine control and tuning of processing result profiles at the substrate edge. Benefits of embodiments herein further include eliminating or substantially reducing substrate to substrate processing variation otherwise attributable to a steady rise in the temperature of an edge ring not having temperature control after the processing chamber has been sitting idle, e.g., first wafer effect.

[0074] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. A substrate support assembly, comprising:
 - a first base plate having one or more first cooling channels disposed therein;
 - a second base plate circumscribing the first base plate, the second base plate having one or more second cooling channels disposed therein;
 - a substrate support disposed on and thermally coupled to the first base plate;
 - a biasing ring disposed on and thermally coupled to the second base plate, wherein the biasing ring is formed of a dielectric material;
 - an edge ring biasing electrode embedded the dielectric material of the biasing ring; and
 - an edge ring disposed on the biasing ring.
2. The substrate support assembly of claim 1, wherein the second base plate is thermally insulated from the first base plate by a first insulator ring interposed therebetween.
3. The substrate support assembly of claim 2, wherein the biasing ring is thermally insulated from the substrate support by a second insulator ring interposed therebetween.
4. The substrate support assembly of claim 1, further comprising a first heater for heating the substrate support and a second heater for heating the edge ring.
5. The substrate support assembly of claim 4, wherein the second heater is disposed between the biasing ring and the second base plate.
6. The substrate support assembly of claim 4, wherein the second heater is embedded in the dielectric material of the biasing ring.

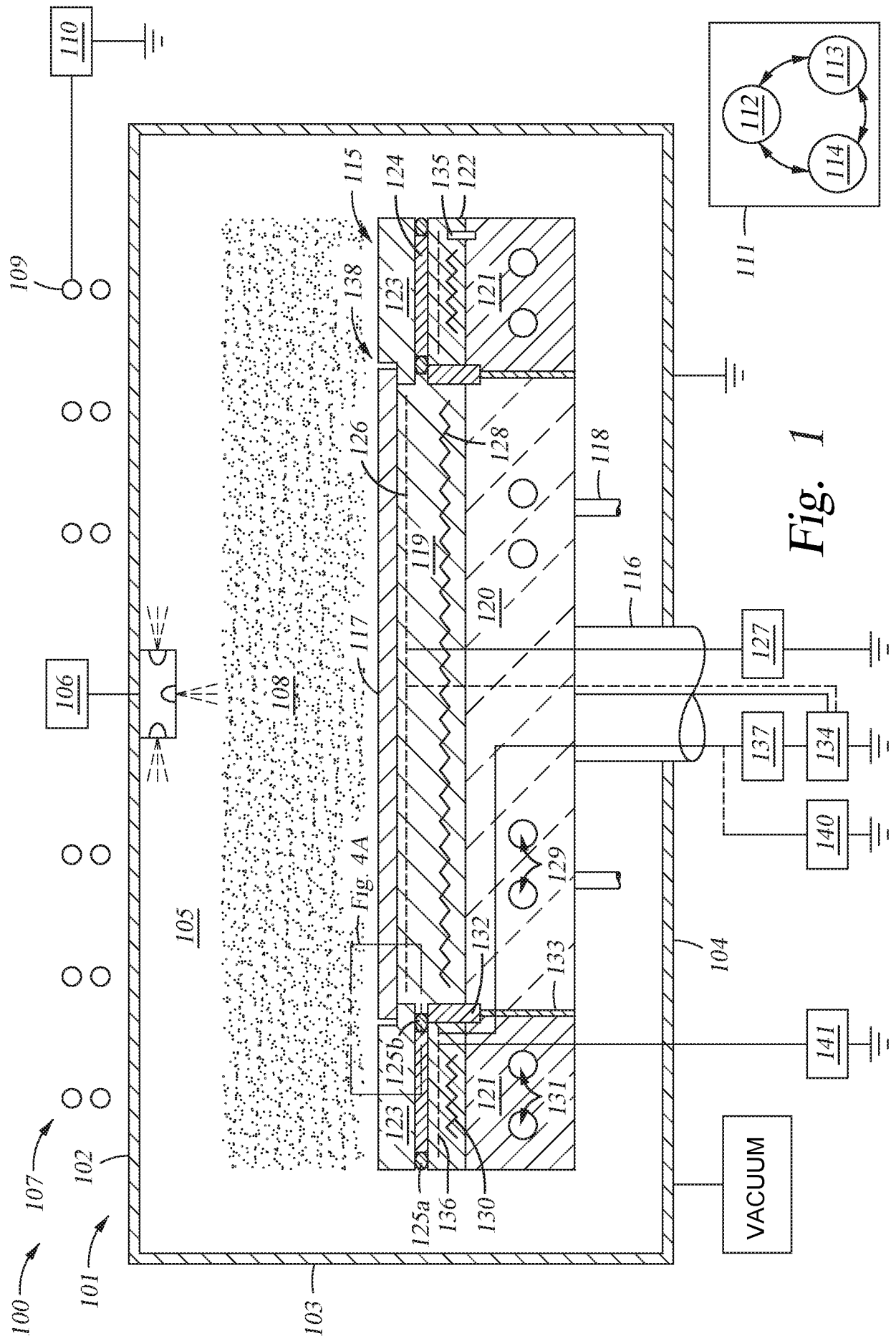
7. A method of processing a substrate, comprising:
- heating a substrate support of a substrate support assembly to a first temperature;
 - heating an edge ring circumscribing the substrate support to a second temperature;
 - positioning the substrate on the substrate support, wherein the substrate support assembly is disposed in a processing volume of a processing chamber and the substrate support assembly comprises:
 - a first base plate having one or more first cooling channels disposed therein;
 - a second base plate circumscribing the first base plate, the second base plate having one or more second cooling channels disposed therein;
 - the substrate support disposed on and thermally coupled to the first base plate;
 - a biasing ring disposed on and thermally coupled to the second base plate, wherein the biasing ring is formed of a dielectric material;
 - an edge ring biasing electrode embedded the dielectric material of the biasing ring; and
 - the edge ring disposed on the biasing ring;
 - flowing a processing gas into the processing volume;
 - igniting and maintaining a plasma of the processing gas;
 - biasing the substrate using a first bias voltage; and
 - biasing the edge ring using a second bias voltage.
8. The method of claim 7, wherein the second base plate is thermally insulated from the first base plate by a first insulator ring interposed therebetween.
9. The method of claim 8, wherein the biasing ring is thermally insulated from the substrate support by a second insulator ring interposed therebetween.

10. The method of claim 7, wherein the substrate support is heated using a first heater and the edge ring is heated using a second heater.
11. The method of claim 10, wherein the second heater is disposed between the biasing ring and the second base plate.
12. The method claim 10, wherein the second heater is embedded in the dielectric material of the biasing ring.
13. A processing chamber, comprising:
a substrate support assembly disposed in a processing volume of the processing chamber, the substrate support assembly comprising:
a first base plate having one or more first cooling channels disposed therein;
a second base plate circumscribing the first base plate, the second base plate having one or more second cooling channels disposed therein;
a substrate support disposed on and thermally coupled to the first base plate;
a biasing ring disposed on and thermally coupled to the second base plate, wherein the biasing ring is formed of a dielectric material;
an edge ring biasing electrode embedded the dielectric material of the biasing ring; and
an edge ring disposed on the biasing ring; and
a computer readable medium having instructions stored thereon for performing a method of processing a substrate when executed by a processor, the method comprising:
heating the substrate support to a first temperature;
heating the edge ring circumscribing the substrate support to a second temperature;
positioning the substrate on the substrate support;
flowing a processing gas into the processing volume;

igniting and maintaining a plasma of the processing gas;
biasing the substrate using a first bias voltage; and
biasing the edge ring using a second bias voltage.

14. The processing chamber of claim 13, wherein the second base plate is thermally insulated from the first base plate by a first insulator ring interposed therebetween.

15. The processing chamber of claim 14, wherein the biasing ring is thermally insulated from the substrate support by a second insulator ring interposed therebetween.



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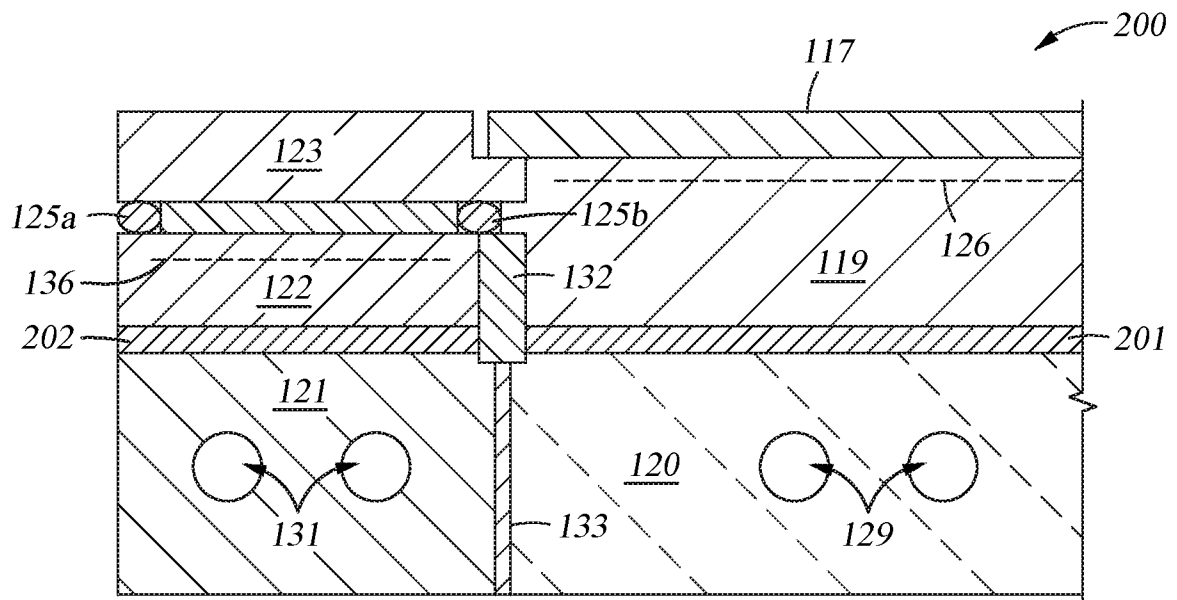


Fig. 2A

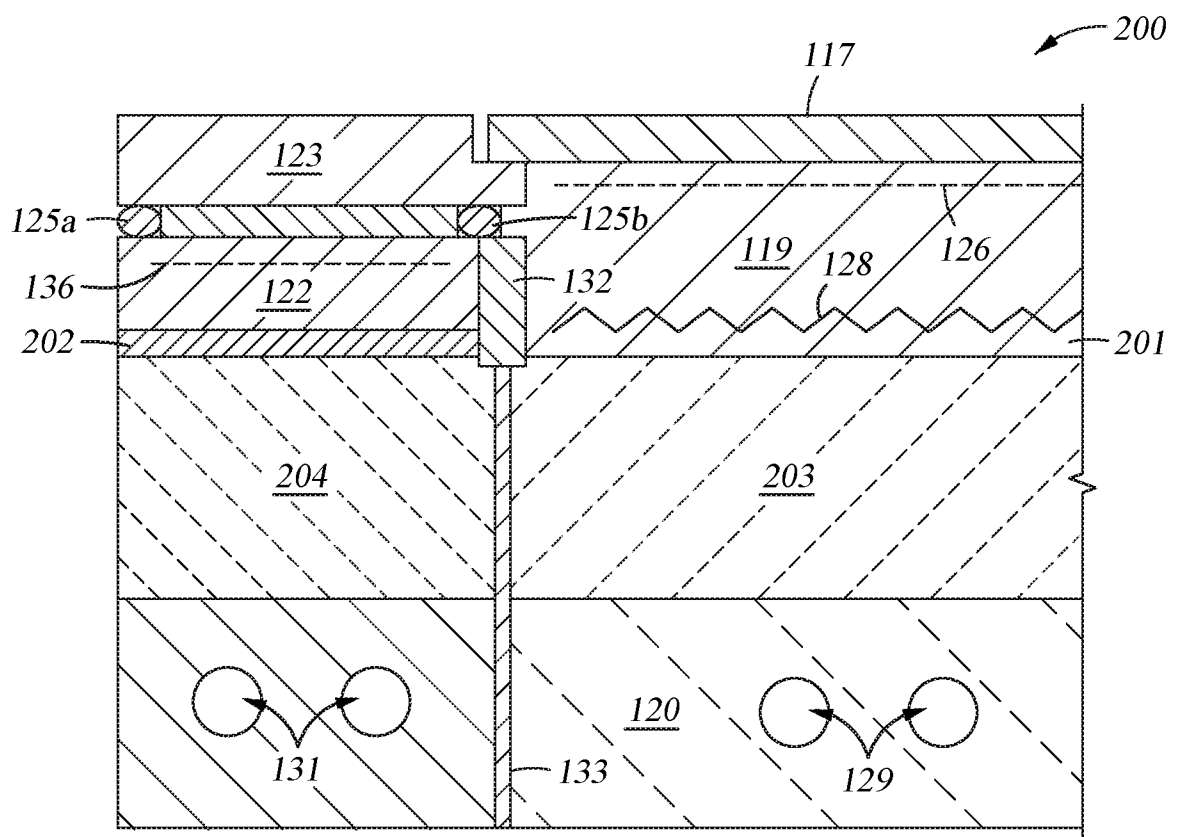
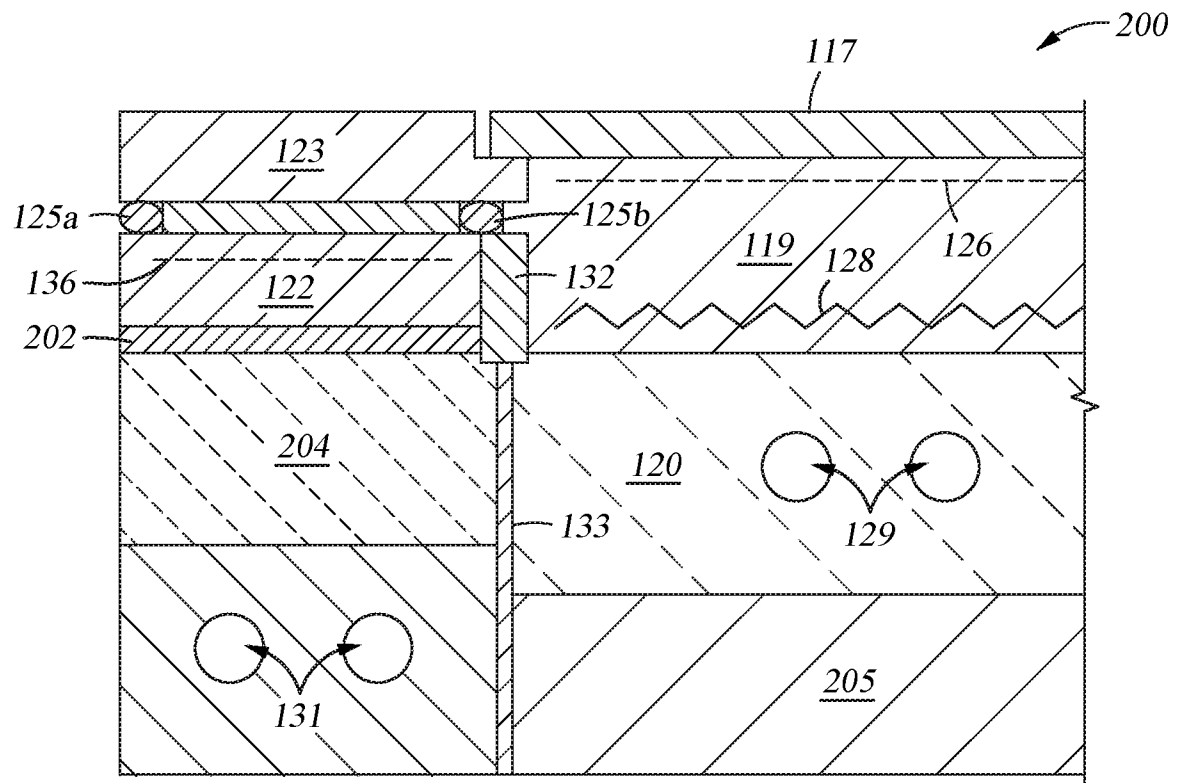


Fig. 2B

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*Fig. 2C*

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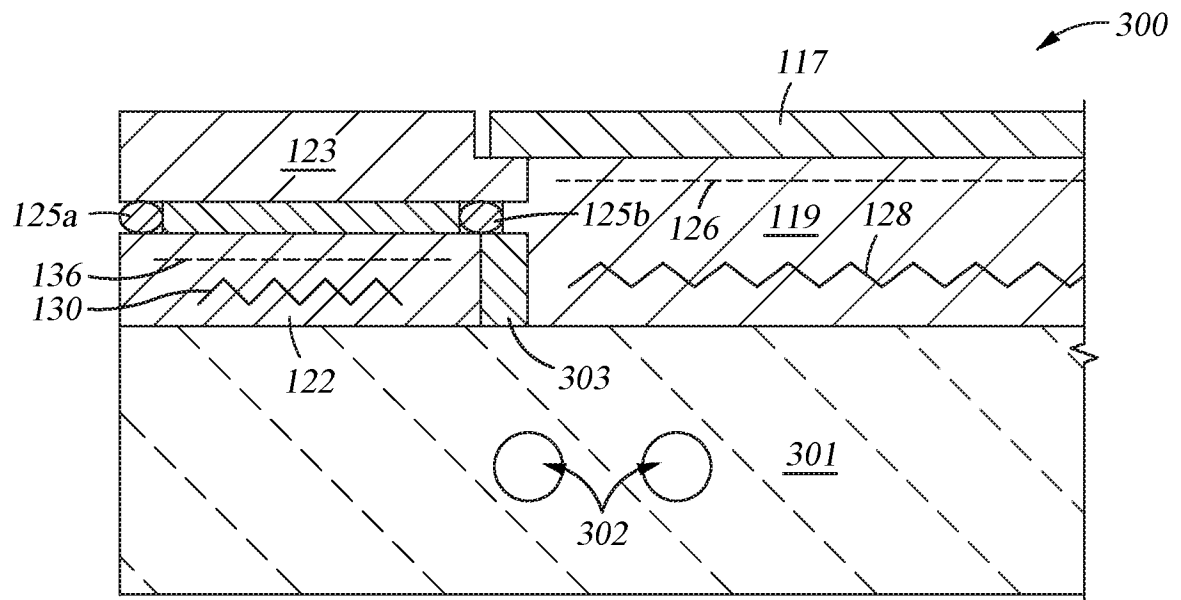


Fig. 3A

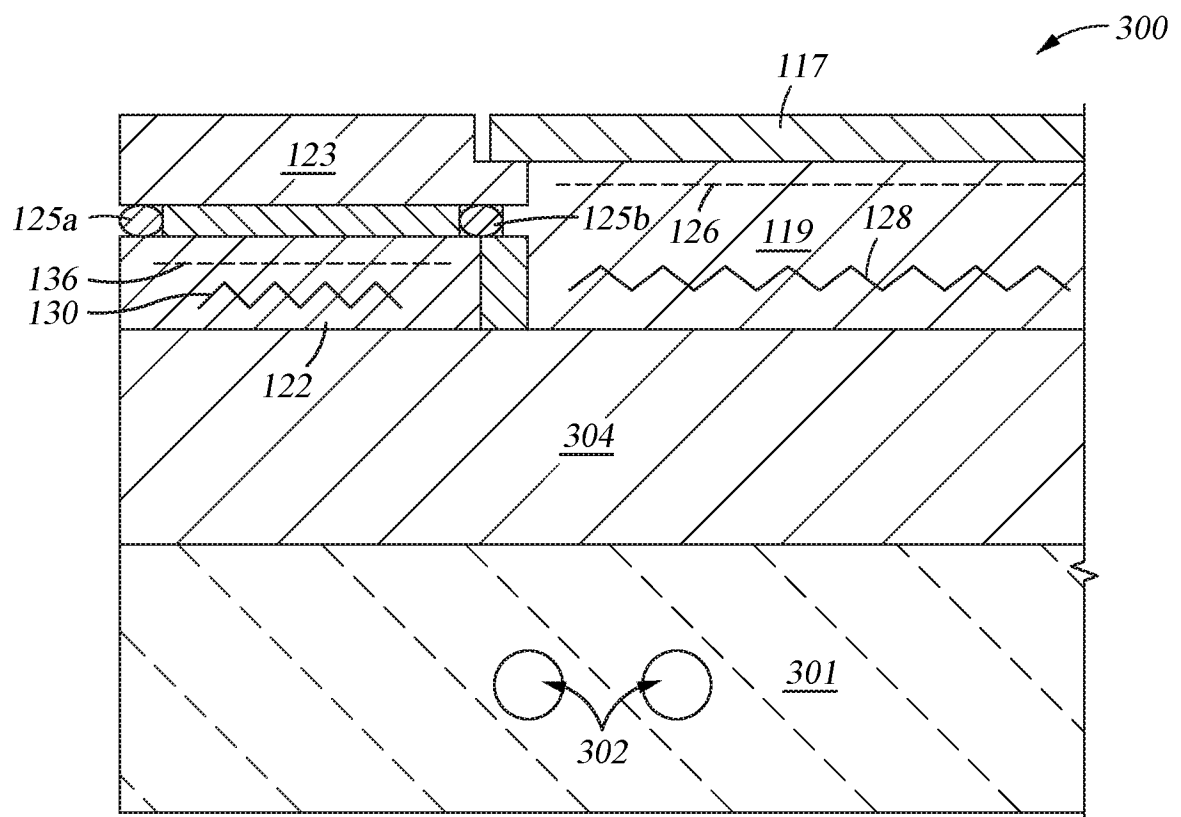
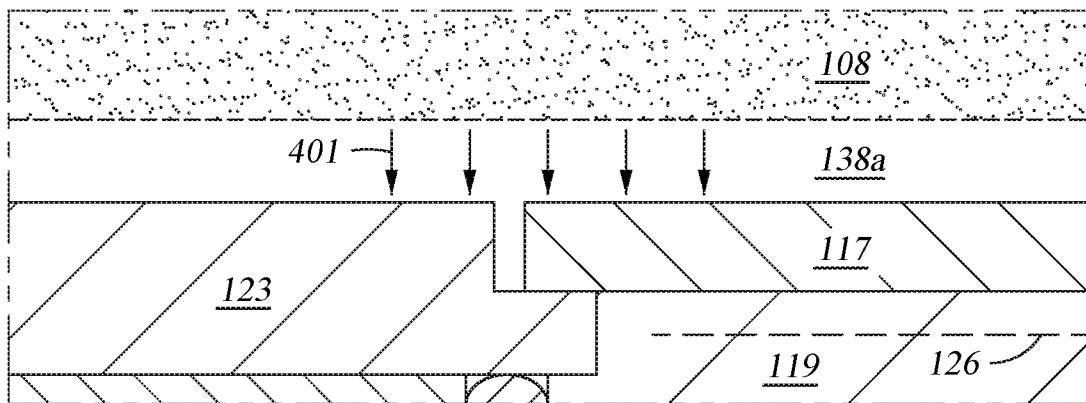
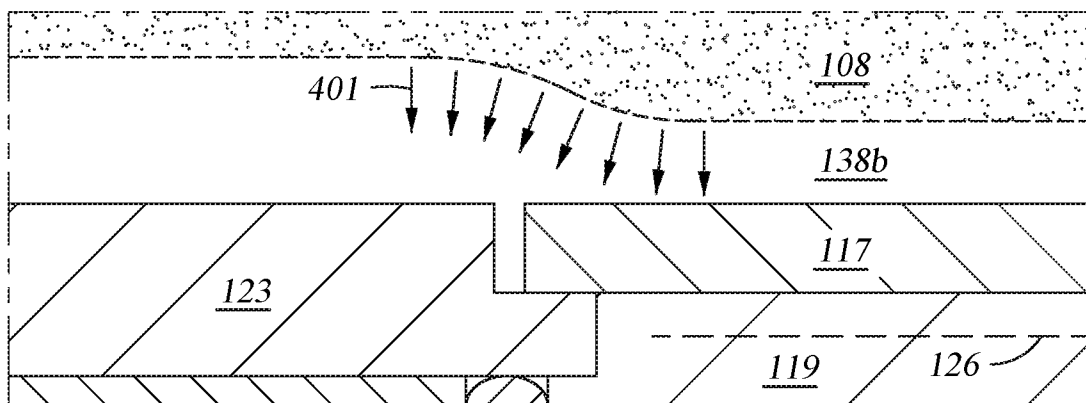
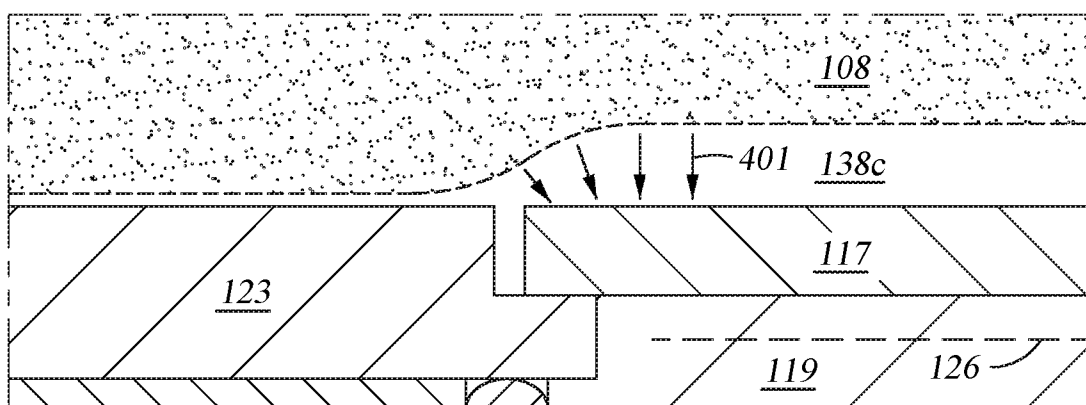


Fig. 3B

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*Fig. 4A**Fig. 4B**Fig. 4C*

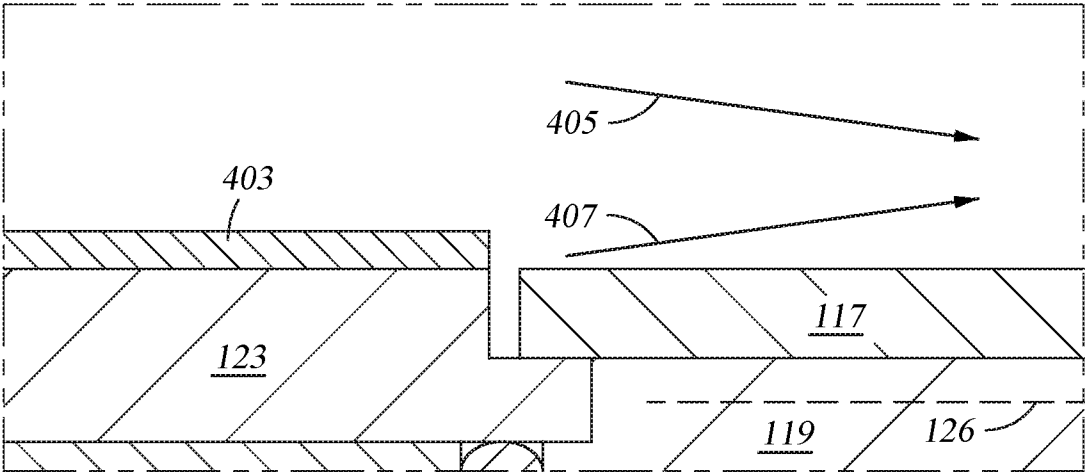


Fig. 4D

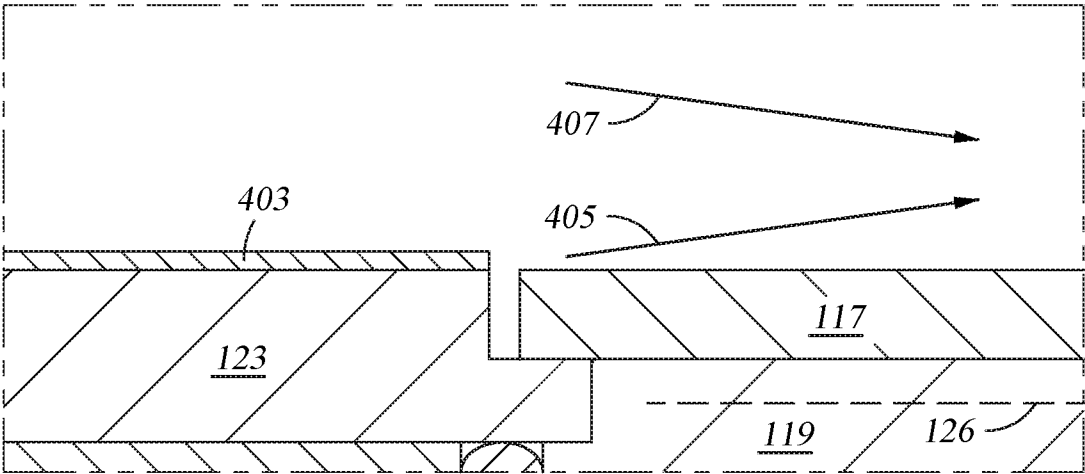


Fig. 4E

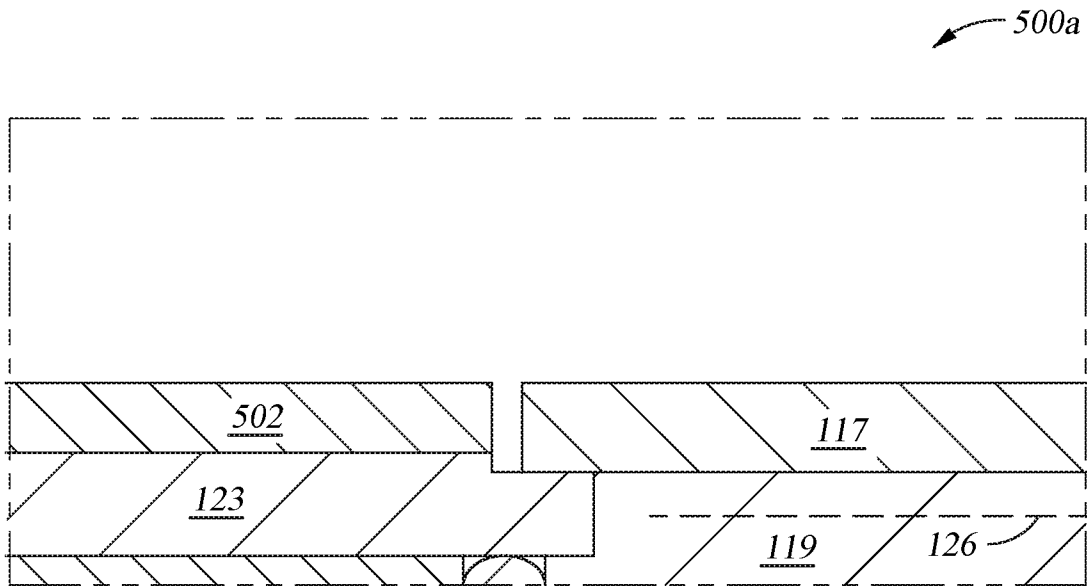


Fig. 5A

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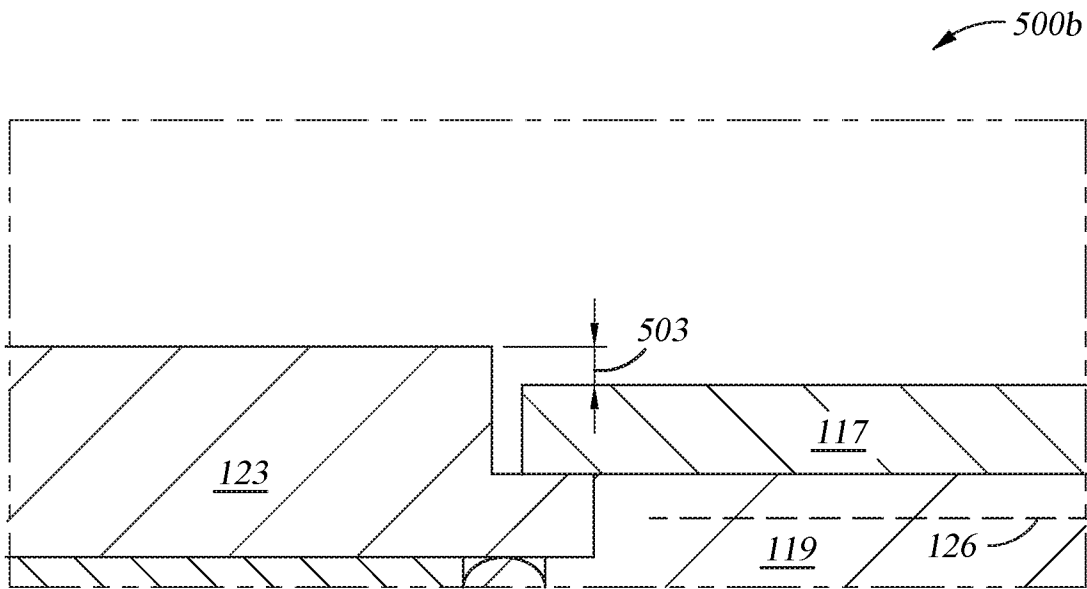
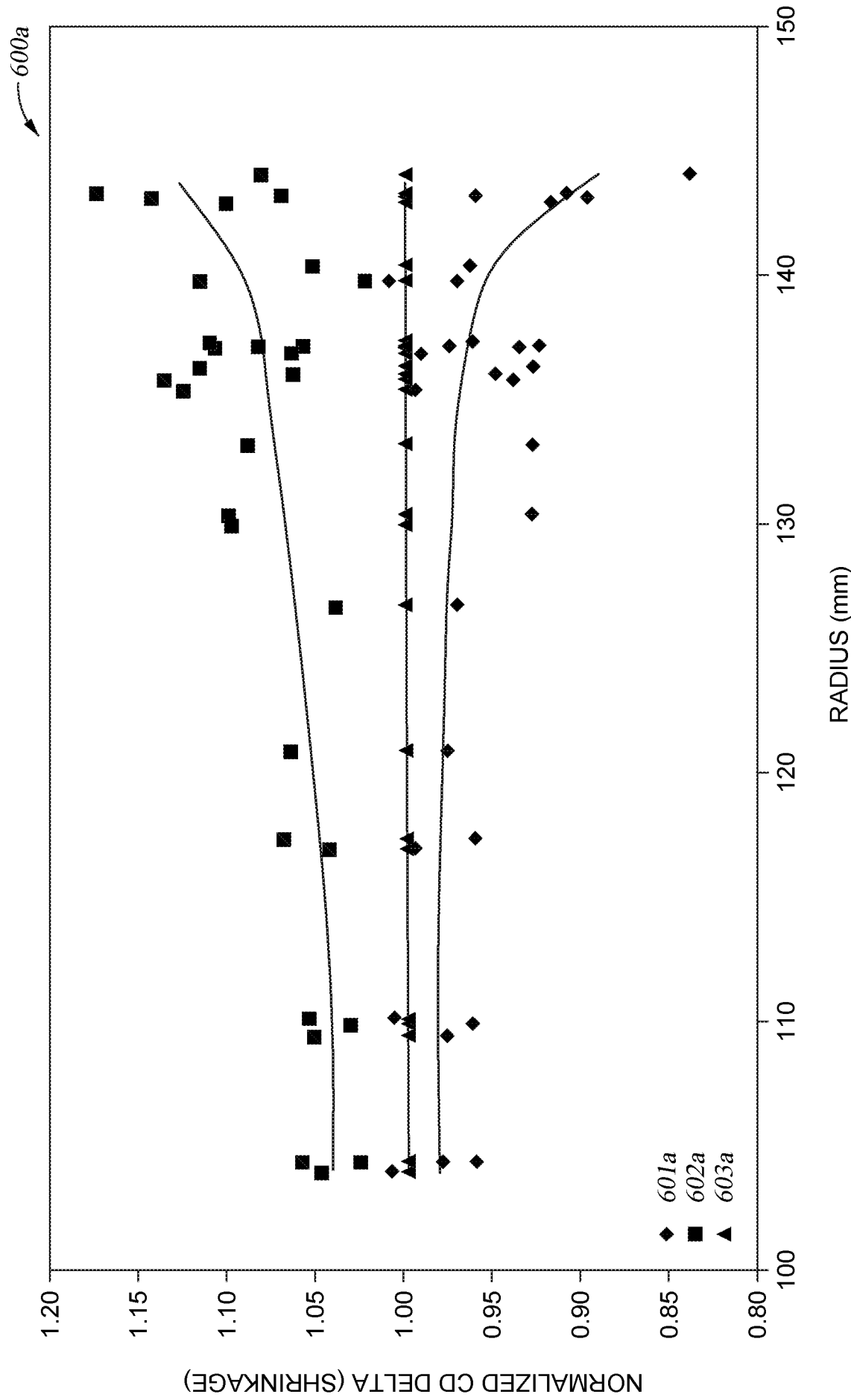


Fig. 5B

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RADIUS (mm)
Fig. 6A

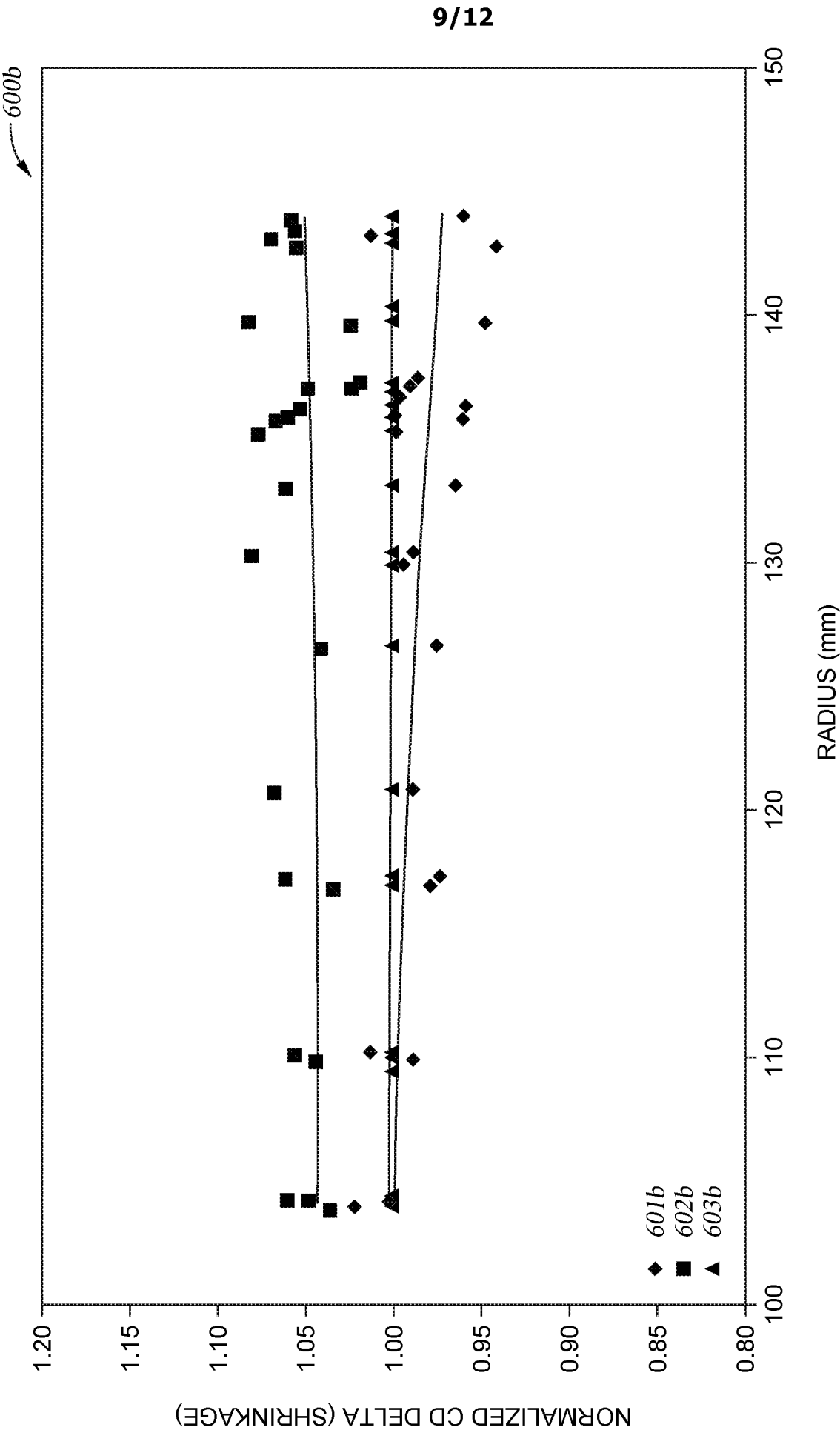


Fig. 6B

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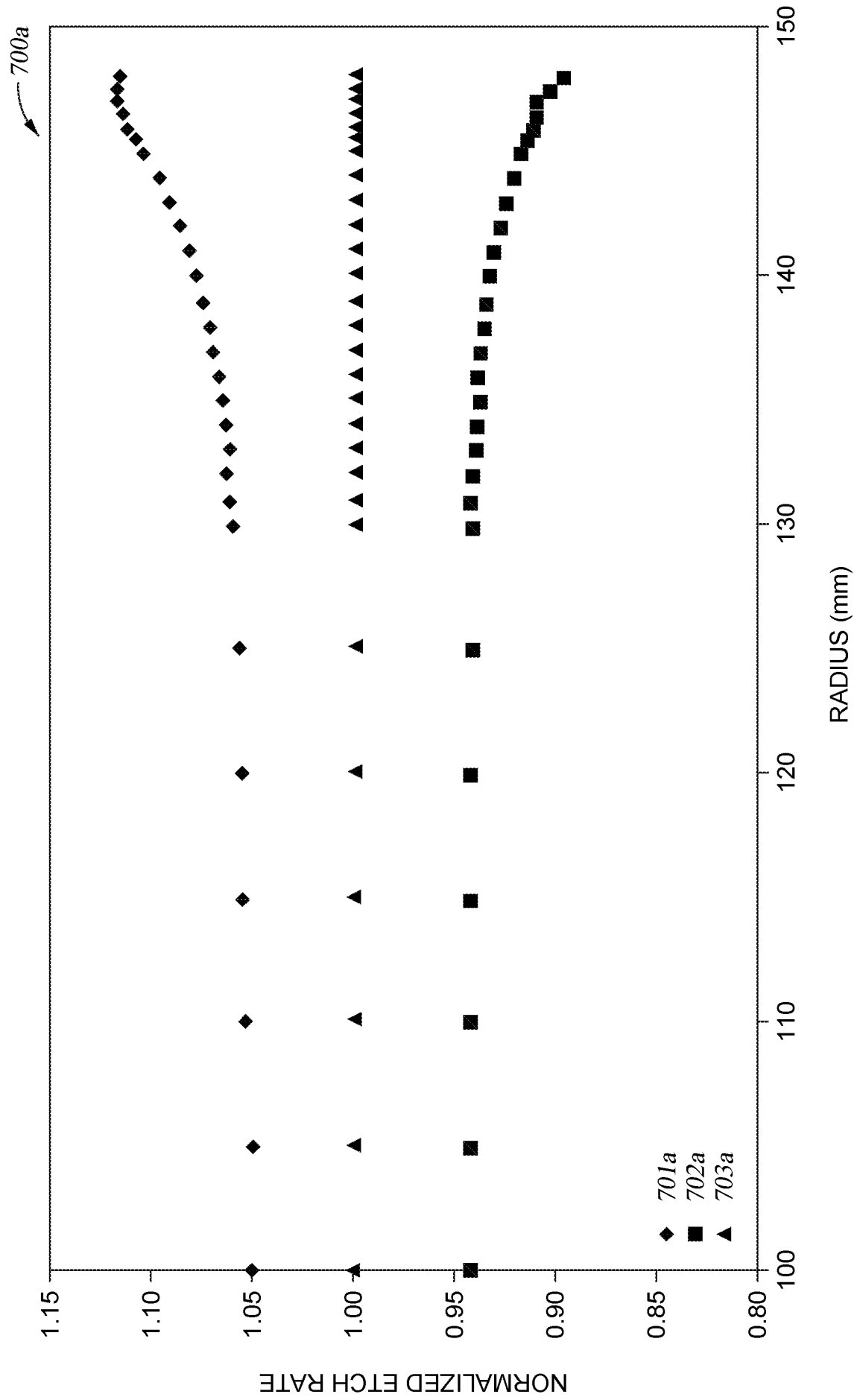


Fig. 7A

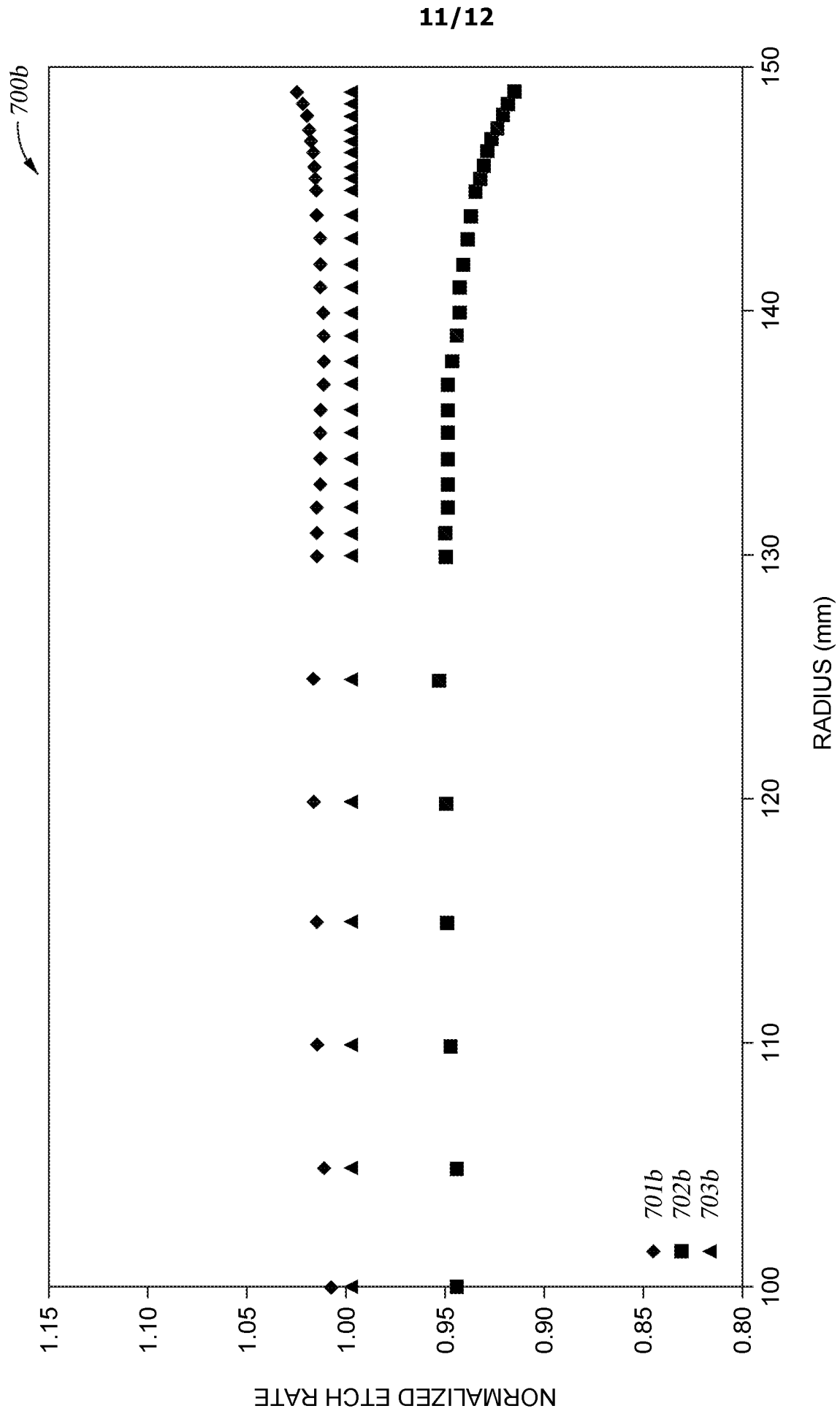
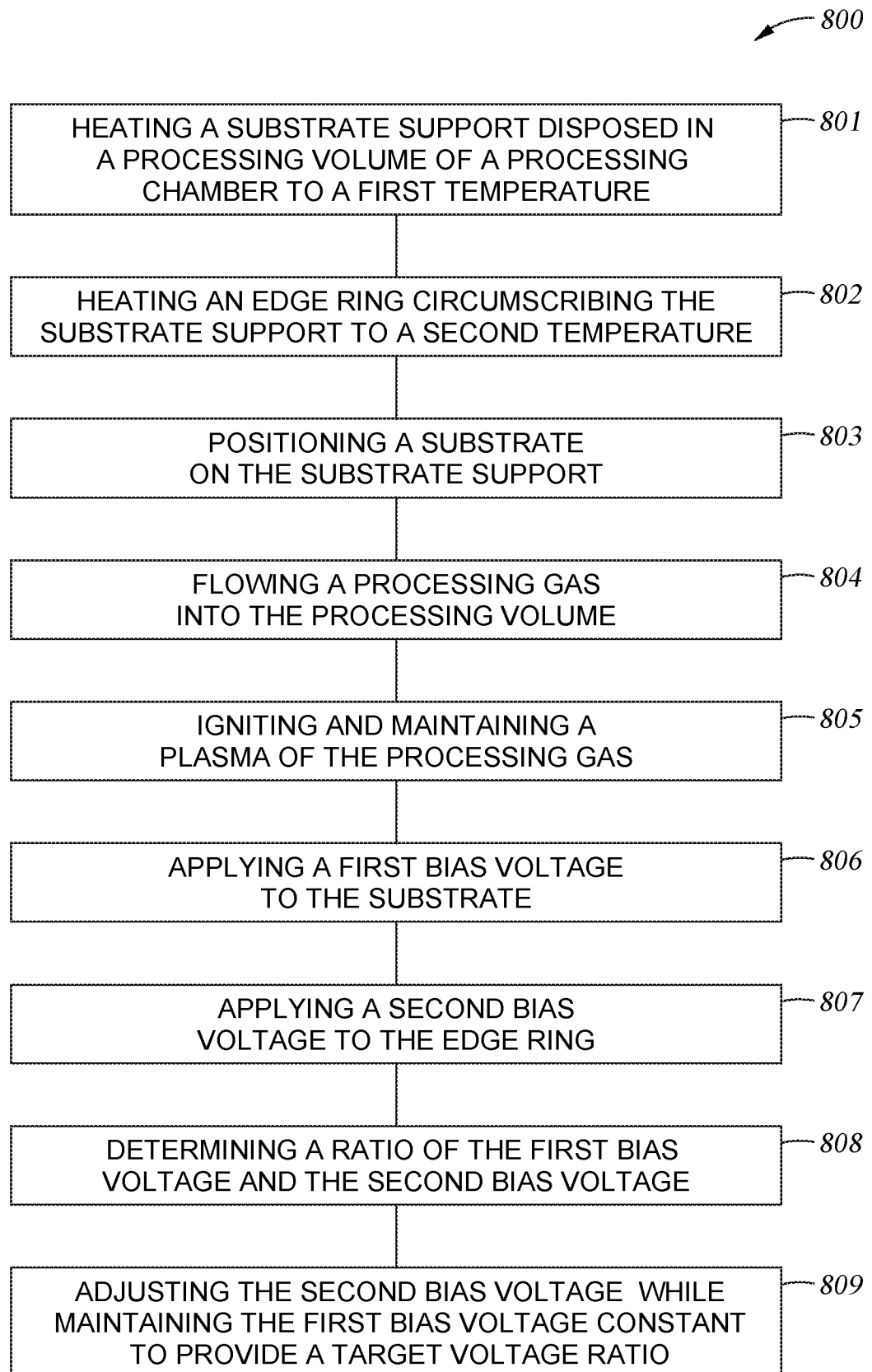


Fig. 7B

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*Fig. 8*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/012503**A. CLASSIFICATION OF SUBJECT MATTER****H01J 37/32(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01J 37/32; H01L 21/3065; H01L 21/48; H01L 21/67; H01L 21/683; H05B 6/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: edge ring, bias, temperature, dielectric material, cooling channel, plasma

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0235063 A1 (LAM RESEARCH CORPORATION) 21 August 2014 See paragraphs 29-44, claims 1-27 and figures 2-6.	1-15
A	US 2017-0053820 A1 (LAM RESEARCH CORPORATION) 23 February 2017 See paragraphs 65-89, claims 1-18 and figures 4A-10.	1-15
A	US 2015-0348813 A1 (APPLIED MATERIALS, INC.) 03 December 2015 See the entire document.	1-15
A	KR 10-2010-0138580 A (SAMSUNG ELECTRONICS CO., LTD.) 31 December 2010 See the entire document.	1-15
A	US 2014-0335698 A1 (LAM RESEARCH CORPORATION) 13 November 2014 See the entire document.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

29 April 2020 (29.04.2020)

Date of mailing of the international search report

29 April 2020 (29.04.2020)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/012503

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