

(43) International Publication Date
20 November 2014 (20.11.2014)

(51) International Patent Classification:
H01L 29/786 (2006.01) *H01L 29/423* (2006.01)
G02F 1/1368 (2006.01) *H01L 29/49* (2006.01)
G09F 9/30 (2006.01) *H01L 51/50* (2006.01)
H01L 21/28 (2006.01) *H05B 33/14* (2006.01)
H01L 29/41 (2006.01)

(72) Inventors: **YAMAZAKI, Shunpei**; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP). **MIYAKE, Hiroyuki**. **OKAZAKI, Kenichi**. **HAYAKAWA, Masahiko**. **MATSUDA, Shinpei**.

(21) International Application Number:
PCT/JP2014/062900

(22) International Filing Date:
8 May 2014 (08.05.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2013-103708 16 May 2013 (16.05.2013) JP

(71) Applicant: SEMICONDUCTOR ENERGY LABORATORY CO., LTD. [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,

[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE

FIG. 1A

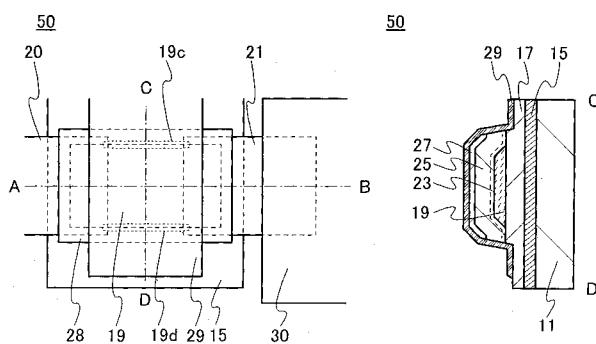


FIG. 1C

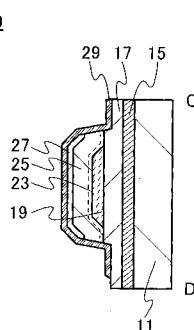
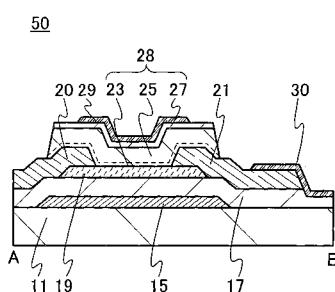


FIG. 1B



(57) Abstract: A semiconductor device which includes an oxide semiconductor and in which formation of a parasitic channel due to a gate BT stress is suppressed is provided. Further, a semiconductor device including a transistor having excellent electrical characteristics is provided. The semiconductor device includes a transistor having a dual-gate structure in which an oxide semiconductor film is provided between a first gate electrode and a second gate electrode; gate insulating films are provided between the oxide semiconductor film and the first gate electrode and between the oxide semiconductor film and the second gate electrode; and in the channel width direction of the transistor, the first or second gate electrode faces a side surface of the oxide semiconductor film with the gate insulating film between the oxide semiconductor film and the first or second gate electrode.



UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

DESCRIPTION

SEMICONDUCTOR DEVICE

5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device having a transistor including an oxide semiconductor film and a method for manufacturing the semiconductor device.

10

BACKGROUND ART

[0002]

Attention has been focused on a technique for forming a transistor using a semiconductor thin film formed over a substrate (also referred to as a thin film transistor (TFT)). Such a transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor has been attracting attention.

20 [0003]

For example, a transistor including an oxide semiconductor containing indium (In), gallium (Ga), and zinc (Zn) as an active layer of the transistor has been disclosed (see Patent Document 1).

[0004]

25 Further, a technique of improving carrier mobility by forming stacked oxide semiconductor layers has been disclosed (see Patent Documents 2 and 3).

[Reference]

[Patent Document]

[0005]

30 [Patent Document 1] Japanese Published Patent Application No. 2006-165528

[Patent Document 2] Japanese Published Patent Application No. 2011-138934

[Patent Document 3] Japanese Published Patent Application No. 2011-124360

DISCLOSURE OF INVENTION

[0006]

In a transistor including an oxide semiconductor film, a large number of defects 5 in the oxide semiconductor film cause poor electrical characteristics of the transistor and cause an increase in the amount of change in threshold voltage due to passage of time or a stress test (e.g., a bias-temperature (BT) stress test).

[0007]

For example, in transistor characteristics (drain current-gate voltage curve 10 (Id-Vg curve)) after application of a gate BT stress (in particular, positive bias) to a transistor formed using an oxide semiconductor, a defect in which drain current is increased gradually at the threshold voltage is caused. This may result from a parasitic channel formed at a side surface of the oxide semiconductor film that overlaps with a gate electrode by a change of the side surface of the oxide semiconductor into n-type. 15 Defects are formed at the side surface of the oxide semiconductor film because of damage due to processing for element isolation, and the side surface of the oxide semiconductor film is polluted by attachment of impurities, or the like. Thus, when stress such as an electric field is applied to the region, an end portion of the oxide semiconductor film is easily activated to be n-type (have low resistance), whereby a 20 parasitic channel is formed.

[0008]

Further, as defects of the oxide semiconductor film, oxygen vacancies are given. For example, in a transistor formed using an oxide semiconductor film including 25 oxygen vacancies, the threshold voltage is likely to shift in the negative direction to have normally-on characteristics. This is because charges are generated owing to oxygen vacancies in the oxide semiconductor film and the resistance is thus reduced. The transistor having normally-on characteristics causes various problems in that malfunction is likely to be caused when a semiconductor device is in operation and that power consumption is increased when a semiconductor device is not in operation. 30 Further, there is a problem in that the amount of change in electrical characteristics, typically in threshold voltage, of the transistor is increased by passage of time or a stress test.

[0009]

One object of one embodiment of the present invention is to provide a semiconductor device which includes an oxide semiconductor and in which formation of a parasitic channel due to a gate BT stress is suppressed. Further, a semiconductor 5 device including a transistor having excellent electrical characteristics is provided.

[0010]

One embodiment of the present invention is a semiconductor device including a transistor having a dual-gate structure in which an oxide semiconductor film is provided between a first gate electrode and a second gate electrode; gate insulating 10 films are provided between the oxide semiconductor film and the first gate electrode and between the oxide semiconductor film and the second gate electrode; and in the channel width direction of the transistor, the first or second gate electrode faces a side surface of the oxide semiconductor film with the gate insulating film between the oxide semiconductor film and the first or second gate electrode.

15 [0011]

Another embodiment of the present invention is a semiconductor device including a transistor. The transistor includes a first gate electrode facing one surface 20 of an oxide semiconductor film; a second gate electrode facing the other surface of the oxide semiconductor film; a first gate insulating film between the oxide semiconductor film and the first gate electrode; a second gate insulating film between the oxide semiconductor film and the second gate electrode; and a pair of electrodes in contact with the oxide semiconductor film. In the channel width direction of the transistor, the first or second gate electrode faces a side surface of the oxide semiconductor film with the first or second gate insulating film between the oxide semiconductor film and the 25 first or second gate electrode.

[0012]

Note that the gate insulating film, the first gate insulating film, or the second gate insulating film may each be isolated from a gate insulating film, a first gate insulating film, or a second gate insulating film formed in an adjacent transistor.

30 [0013]

The gate insulating film, the first gate insulating film, or the second gate insulating film may have a plurality of openings so that the oxide semiconductor film is

provided between the plurality of openings when seen from a direction perpendicular to a surface of any of these films.

[0014]

Furthermore, the first gate electrode may be connected to the second gate
5 electrode.

[0015]

In addition, a conductive film connected to one of the pair of electrodes may be provided. The conductive film serves as a pixel electrode.

[0016]

10 Further, the gate insulating film, the first gate insulating film, or the second gate insulating film may include an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. Note that the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition is an oxide insulating film of which the amount of released
15 oxygen converted into oxygen atoms is greater than or equal to 1.0×10^{18} atoms/cm³, or greater than or equal to 3.0×10^{20} atoms/cm³ in thermal desorption spectroscopy (TDS) analysis.

[0017]

20 When the first or second gate electrode faces a side surface of the oxide semiconductor film with the gate insulating film therebetween in the channel width direction of the transistor, formation of a parasitic channel at the side surface of the oxide semiconductor film and its vicinity is suppressed because of an electric field of the first or second gate electrode. As a result, drain current is drastically increased at the threshold voltage, so that the transistor has excellent electrical characteristics.
25 Further, in the channel width direction of the transistor, the minimum distance between the side surface of the oxide semiconductor film and the second gate electrode is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . In that case, a short circuit between the oxide semiconductor film and the second gate electrode can be prevented, which can increase yield.

30 [0018]

Further, when the gate insulating film, the first gate insulating film, or the

second gate insulating film includes an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition, oxygen contained in the gate insulating film, the first gate insulating film, or the second gate insulating film is transferred to the oxide semiconductor film, which can reduce oxygen 5 vacancies in the oxide semiconductor film. As a result, the transistor has normally-off characteristics. Further, the amount of change in electrical characteristics, typically in threshold voltage, of the transistor due to passage of time or a stress test can be reduced. [0019]

According to one embodiment of the present invention, a semiconductor device 10 which includes an oxide semiconductor and in which formation of a parasitic channel due to a gate BT stress is suppressed can be provided. Further, a semiconductor device including a transistor having excellent electrical characteristics can be provided.

BRIEF DESCRIPTION OF DRAWINGS

15 [0020]

FIGS. 1A to 1C are a top view and cross-sectional views illustrating one embodiment of a transistor.

FIGS. 2A to 2J are cross-sectional views illustrating one embodiment of a method for manufacturing a transistor.

20 FIGS. 3A to 3C are a top view and cross-sectional views illustrating one embodiment of a transistor.

FIGS. 4A to 4C are a top view and cross-sectional views illustrating one embodiment of a transistor.

25 FIGS. 5A to 5C are a top view and cross-sectional views illustrating one embodiment of a transistor.

FIGS. 6A to 6D are cross-sectional views illustrating one embodiment of a method for manufacturing a transistor.

FIGS. 7A and 7B are cross-sectional views illustrating structures of transistors.

30 FIGS. 8A and 8B are graphs each showing current-voltage curves obtained by calculation.

FIGS. 9A and 9B are diagrams showing the calculation results of potentials of a transistor.

FIGS. 10A and 10B are diagrams illustrating models.

FIGS. 11A to 11C are diagrams illustrating models.

FIGS. 12A to 12C are graphs each showing current-voltage curves obtained by calculation.

5 FIGS. 13A to 13C are each a cross-sectional view illustrating one embodiment of a transistor.

FIG. 14 is a cross-sectional view illustrating one embodiment of a transistor.

FIGS. 15A to 15D are a top view and cross-sectional views illustrating one embodiment of a transistor.

10 FIGS. 16A to 16C are diagrams illustrating band structures of transistors.

FIG. 17 shows nanobeam electron diffraction patterns of an oxide semiconductor.

FIGS. 18A to 18C are each a top view illustrating one embodiment of a semiconductor device.

15 FIGS. 19A and 19B are each a cross-sectional view illustrating one embodiment of a semiconductor device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0021]

20 Embodiments of the present invention are described below in detail with reference to drawings. Note that the present invention is not limited to the following description, and it is easily understood by those skilled in the art that the mode and details can be variously changed without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the description in the following embodiments and examples. In addition, in the following embodiments and examples, the same portions or portions having similar functions are denoted by the same reference numerals or the same hatching patterns in different drawings, and description thereof is not repeated.

[0022]

30 Note that in each drawing described in this specification, the size, the film thickness, or the region of each component is exaggerated for clarity in some cases. Therefore, embodiments of the present invention are not limited to such a scale.

[0023]

In addition, terms such as "first", "second", and "third" in this specification are used in order to avoid confusion among components, and the terms do not limit the components numerically. Therefore, for example, the term "first" can be replaced with 5 the term "second", "third", or the like as appropriate.

[0024]

Functions of a "source" and a "drain" are sometimes replaced with each other when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be used to denote the drain and the source, 10 respectively, in this specification.

[0025]

Note that a voltage refers to a difference between potentials of two points, and a potential refers to electrostatic energy (electric potential energy) of a unit charge at a given point in an electrostatic field. Note that in general, a difference between a 15 potential of one point and a reference potential (e.g., a ground potential) is merely called a potential or a voltage, and a potential and a voltage are used as synonymous words in many cases. Thus, in this specification, a potential may be rephrased as a voltage and a voltage may be rephrased as a potential unless otherwise specified.

[0026]

20 In this specification, in the case where an etching step is performed after a photolithography process, a mask formed in the photolithography process is removed.

[0027]

(Embodiment 1)

25 In this embodiment, a semiconductor device that is one embodiment of the present invention and a manufacturing method thereof are described with reference to drawings.

[0028]

A top view and cross-sectional views of a transistor 50 included in a 30 semiconductor device are illustrated in FIGS. 1A to 1C. The transistor 50 illustrated in FIGS. 1A to 1C is a channel-etched transistor. FIG. 1A is a top view of the transistor 50, FIG. 1B is a cross-sectional view taken along dashed-dotted line A-B in FIG. 1A, and FIG. 1C is a cross-sectional view taken along dashed-dotted line C-D in FIG. 1A.

Note that in FIG. 1A, a substrate 11, a gate insulating film 17, an oxide insulating film 23, an oxide insulating film 25, a nitride insulating film 27, and the like are omitted for simplicity.

[0029]

5 The transistor 50 illustrated in FIGS. 1B and 1C includes a gate electrode 15 over the substrate 11; the gate insulating film 17 over the substrate 11 and the gate electrode 15; an oxide semiconductor film 19 overlapping with the gate electrode 15 with the gate insulating film 17 positioned therebetween; a pair of electrodes 20 and 21 in contact with the oxide semiconductor film 19; a gate insulating film 28 over the gate insulating film 17, the oxide semiconductor film 19, and the pair of electrodes 20 and 10 21; and a gate electrode 29 over the gate insulating film 28 and the gate insulating film 17. Further, the gate insulating film 28 includes the oxide insulating film 23, the oxide insulating film 25, and the nitride insulating film 27. Furthermore, an electrode 30 connected to one of the pair of electrodes 20 and 21 (here, the electrode 21) is formed 15 over the gate insulating film 17. Note that the electrode 30 serves as a pixel electrode.

[0030]

In the transistor 50 described in this embodiment, the oxide semiconductor film 19 is provided between the gate electrodes 15 and 29. The gate insulating film 28 that is isolated from a gate insulating film of an adjacent transistor overlaps with the oxide 20 semiconductor film 19. Specifically, in the channel length direction in FIG. 1B, end portions of the gate insulating film 28 are positioned over the pair of electrodes 20 and 21, and in the channel width direction in FIG. 1C, end portions of the gate insulating film 28 are positioned on the outer side of the oxide semiconductor film 19. In the 25 channel width direction in FIG. 1C, the gate electrode 29 faces a side surface of the oxide semiconductor film 19 with the gate insulating film 28 positioned therebetween. As illustrated in FIG. 1C, in the channel width direction, in the case where an interface between the oxide semiconductor film 19 and the gate insulating film 28 is referred to as a first interface and an interface between the gate insulating film 28 and the gate electrode 29 is referred to as a second interface, the minimum distance between the first 30 interface and the second interface is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . In other words, the minimum distance between the side

surface of the oxide semiconductor film 19 and the gate electrode 29 is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . In that case, a short circuit between the gate electrode 29 and the oxide semiconductor film 19 can be prevented, which can increase yield.

5 [0031]

The oxide semiconductor film 19 is formed using typically an In-Ga oxide film, an In-Zn oxide film, an In-M-Zn oxide film (M represents Al, Ga, Y, Zr, La, Ce, or Nd), or the like.

[0032]

10 Defects are formed at an end portion of the oxide semiconductor film processed by etching or the like because of damage due to the processing, and the end portion of the oxide semiconductor film is polluted by attachment of impurities, or the like. Thus, when stress such as an electric field is applied, the end portion of the oxide semiconductor film is easily activated to be n-type (have low resistance). Thus, in this 15 embodiment, end portions of the oxide semiconductor film 19 that overlap with the gate electrode 15 are likely to be n-type. When the n-type end portions are formed between the pair of electrodes 20 and 21 as shown by dashed lines 19c and 19d of FIG. 1A, the n-type regions serve as carrier paths, resulting in formation of a parasitic channel. However, as illustrated in FIG. 1C, when the gate electrode 29 faces the side surface of 20 the oxide semiconductor film 19 with the gate insulating film 28 positioned therebetween in the channel width direction, formation of a parasitic channel at the side surface of the oxide semiconductor film 19 and its vicinity is suppressed because of an electric field of the gate electrode 29. As a result, the transistor has excellent electrical characteristics in which drain current is drastically increased at the threshold voltage.

25 [0033]

Further, an electric field from the outside can be blocked by the gate electrodes 15 and 29; thus, charges of charged particles and the like that are formed between the substrate 11 and the gate electrode 15 and over the gate electrode 29 do not affect the oxide semiconductor film 19. Therefore, degradation due to a stress test (e.g., a 30 negative gate bias temperature (GBT) stress test) can be reduced, and changes in the rising voltages of on-state current at different drain voltages can be suppressed. Note

that this effect is caused when the gate electrodes 15 and 29 have the same potential or different potentials.

[0034]

The BT stress test is one kind of accelerated test and can evaluate, in a short time, change in characteristics (i.e., a change over time) of transistors, which is caused by long-term use. In particular, the amount of change in threshold voltage of the transistor between before and after the BT stress test is an important indicator when examining the reliability of the transistor. As the amount of change in the threshold voltage between before and after the BT stress test is small, the transistor has higher reliability.

[0035]

Next, a specific method of the BT stress test is described. First, initial characteristics of the transistor are measured. Next, the temperature of the substrate over which the transistor is formed (substrate temperature) is set at fixed temperature, the pair of electrodes serving as a source and a drain of the transistor are set at the same potential, and the gate electrode is supplied for a certain period with a potential different from that of the pair of electrodes serving as a source and a drain. The substrate temperature may be determined as appropriate in accordance with the test purpose. Then, the substrate temperature is set at a temperature similar to a temperature when the initial characteristics are measured, and electrical characteristics of the transistor are measured again. As a result, a difference between the threshold voltage in the initial characteristics and the threshold voltage in the electrical characteristics after the BT stress test can be obtained as the amount of change in the threshold voltage.

[0036]

Note that the test in the case where the potential applied to the gate electrode is higher than the potential of the source and the drain is referred to as a positive GBT (+GBT) stress test, and the test in the case where the potential applied to the gate electrode is lower than the potential of the source and the drain is referred to as a negative GBT (-GBT) stress test. A BT stress test with light irradiation is referred to as a GBT photostress test. The test in the case where light irradiation is performed and the potential applied to the gate electrode is higher than the potential of the source and the drain is referred to as a positive GBT photostress test, and the test in the case where

light irradiation is performed and the potential applied to the gate electrode is lower than the potential of the source and the drain is referred to as a negative GBT photostress test.

[0037]

5 With the gate electrodes 15 and 29 having the same potential, the amount of change in the threshold voltage is reduced. Accordingly, variation in electrical characteristics among a plurality of transistors is also reduced. Further, in the oxide semiconductor film 19, a region in which carriers flow is increased in the film thickness direction; thus, the number of transferred carriers is increased. As a result, the on-state
10 current of the transistor 50 is increased and the field-effect mobility is increased. Typically, the field-effect mobility is greater than or equal to $20 \text{ cm}^2/\text{Vs}$.

[0038]

Further, the gate insulating film 28 over the oxide semiconductor film 19 includes an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. Part of oxygen is released by heating from the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. The oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition is an oxide insulating film of which the amount of released oxygen converted into oxygen atoms is
15 greater than or equal to $1.0 \times 10^{18} \text{ atoms/cm}^3$, or greater than or equal to $3.0 \times 10^{20} \text{ atoms/cm}^3$ in TDS analysis.

[0039]

In the case where the gate insulating film 28 includes the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition, part of oxygen contained in the gate insulating film 28 can be transferred to the oxide semiconductor film 19 to reduce oxygen vacancies in the oxide semiconductor film 19.

[0040]

In a transistor formed using an oxide semiconductor film including oxygen vacancies, the threshold voltage is likely to shift in the negative direction to have normally-on characteristics. This is because charges are generated owing to oxygen vacancies in the oxide semiconductor film and the resistance is thus reduced. The

transistor having normally-on characteristics causes various problems in that malfunction is likely to be caused when in operation and that power consumption is increased when not in operation. Further, there is a problem in that the amount of change in electrical characteristics, typically in threshold voltage, of the transistor is 5 increased by passage of time or a stress test.

[0041]

However, in the transistor 50 described in this embodiment, the gate insulating film 28 over the oxide semiconductor film 19 includes an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric 10 composition. Thus, oxygen contained in the gate insulating film 28 can be transferred to the oxide semiconductor film 19 to reduce oxygen vacancies in the oxide semiconductor film 19. As a result, the transistor has normally-off characteristics. Further, the amount of change in electrical characteristics, typically in threshold voltage, of the transistor due to passage of time or a stress test can be reduced.

15 [0042]

Other details of the transistor 50 are described below.

[0043]

There is no particular limitation on the property of a material and the like of the substrate 11 as long as the material has heat resistance enough to withstand at least later 20 heat treatment. For example, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 11. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, a silicon-on-insulator (SOI) substrate, or the like may be used as 25 the substrate 11. Furthermore, any of these substrates further provided with a semiconductor element may be used as the substrate 11. Still alternatively, any of these substrates provided with a semiconductor element may be used as the substrate 11. In the case where a glass substrate is used as the substrate 11, a glass substrate having any of the following sizes can be used: the 6th generation (1500 mm × 1850 mm), the 30 7th generation (1870 mm × 2200 mm), the 8th generation (2200 mm × 2400 mm), the 9th generation (2400 mm × 2800 mm), and the 10th generation (2950 mm × 3400 mm).

Thus, a large-sized display device can be manufactured.

[0044]

Alternatively, a flexible substrate may be used as the substrate 11, and the transistor 50 may be provided directly on the flexible substrate. Alternatively, a 5 separation layer may be provided between the substrate 11 and the transistor 50. The separation layer can be used when part or the whole of a semiconductor device formed over the separation layer is separated from the substrate 11 and transferred onto another substrate. In that case, the transistor 50 can be transferred to a substrate having low heat resistance or a flexible substrate.

10 [0045]

The gate electrode 15 can be formed using a metal element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of these metal elements as a component; an alloy containing these metal elements in combination; or the like. Further, one or more metal elements selected 15 from manganese and zirconium may be used. The gate electrode 15 may have a single-layer structure or a layered structure of two or more layers. For example, a single-layer structure of an aluminum film containing silicon, a two-layer structure in which an aluminum film is stacked over a titanium film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a tantalum nitride film or a tungsten nitride film, a two-layer structure in which a copper film is stacked over a titanium film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given. Alternatively, a film, an alloy film, or a nitride 20 film that contains aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

25 [0046]

The gate electrode 15 can also be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible to have a layered structure formed using the above

light-transmitting conductive material and the above metal element.

[0047]

The gate insulating film 17 can be formed to have a single-layer structure or a stacked-layer structure using, for example, one or more of a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, a gallium oxide film, a Ga-Zn-based metal oxide film, and a silicon nitride film.

[0048]

The gate insulating film 17 may be formed using a high-k material such as hafnium silicate (HfSiO_x), hafnium silicate to which nitrogen is added ($\text{HfSi}_x\text{O}_y\text{N}_z$), hafnium aluminate to which nitrogen is added ($\text{HfAl}_x\text{O}_y\text{N}_z$), hafnium oxide, or yttrium oxide, so that gate leakage current of the transistor can be reduced.

[0049]

The thickness of the gate insulating film 17 is greater than or equal to 5 nm and less than or equal to 400 nm, greater than or equal to 10 nm and less than or equal to 300 nm, or greater than or equal to 50 nm and less than or equal to 250 nm.

[0050]

The oxide semiconductor film 19 is typically an In-Ga oxide film, an In-Zn oxide film, or an In-M-Zn oxide film (M represents Al, Ga, Y, Zr, La, Ce, or Nd).

[0051]

Note that in the case where the oxide semiconductor film 19 is an In-M-Zn oxide film, the proportions of In and M when summation of In and M is assumed to be 100 atomic% are as follows: the atomic percentage of In is greater than or equal to 25 atomic% and the atomic percentage of M is less than 75 atomic%; or the atomic percentage of In is greater than or equal to 34 atomic% and the atomic percentage of M is less than 66 atomic%.

[0052]

The energy gap of the oxide semiconductor film 19 is 2 eV or more, 2.5 eV or more, or 3 eV or more. With the use of an oxide semiconductor having such a wide energy gap, the off-state current of the transistor 50 can be reduced.

[0053]

The thickness of the oxide semiconductor film 19 is greater than or equal to 3 nm and less than or equal to 200 nm, greater than or equal to 3 nm and less than or equal to 100 nm, or greater than or equal to 3 nm and less than or equal to 50 nm.

[0054]

5 In the case where the oxide semiconductor film 19 is an In-M-Zn oxide film (M represents Al, Ga, Y, Zr, La, Ce, or Nd), it is preferable that the atomic ratio of metal elements of a sputtering target used for forming a film of the In-M-Zn oxide satisfy $In \geq M$ and $Zn \geq M$. As the atomic ratio of metal elements of such a sputtering target, $In:M:Zn = 1:1:1$, $In:M:Zn = 1:1:2$, and $In:M:Zn = 3:1:2$ are preferable. Note that the 10 atomic ratios of metal elements in the formed oxide semiconductor film 19 vary from those in the above-described sputtering target, within a range of $\pm 40\%$ as an error.

[0055]

An oxide semiconductor film with low carrier density is used as the oxide semiconductor film 19. For example, an oxide semiconductor film whose carrier 15 density is $1 \times 10^{17} /cm^3$ or lower, $1 \times 10^{15} /cm^3$ or lower, $1 \times 10^{13} /cm^3$ or lower, or $1 \times 10^{11} /cm^3$ or lower is used as the oxide semiconductor film 19.

[0056]

Note that, without limitation to that described above, a material with an appropriate composition may be used depending on required semiconductor 20 characteristics and electrical characteristics (e.g., field-effect mobility and threshold voltage) of a transistor. Further, in order to obtain required semiconductor characteristics of a transistor, it is preferable that the carrier density, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, the interatomic distance, the density, and the like of the oxide semiconductor film 19 be set 25 to be appropriate.

[0057]

Note that it is preferable to use, as the oxide semiconductor film 19, an oxide semiconductor film in which the impurity concentration is low and density of defect states is low, in which case the transistor can have more excellent electrical 30 characteristics. Here, the state in which impurity concentration is low and density of defect states is low (the number of oxygen vacancies is small) is referred to as "highly

purified intrinsic" or "substantially highly purified intrinsic". A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier generation sources, and thus has a low carrier density in some cases. Thus, a transistor including the oxide semiconductor film in which a channel region is formed rarely has a negative threshold voltage (is rarely normally-on). A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has a low density of defect states and accordingly has few carrier traps in some cases. Further, the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has an extremely low off-state current; even when an element has a channel width of 1×10^6 5 μm and a channel length of $10 \mu\text{m}$, the off-state current can be less than or equal to the measurement limit of a semiconductor parameter analyzer, i.e., less than or equal to $1 \times 10^{-13} \text{ A}$, at a voltage (drain voltage) between a source electrode and a drain electrode of 10 from 1 V to 10 V . Thus, the transistor whose channel region is formed in the oxide semiconductor film has a small variation in electrical characteristics and high reliability 15 in some cases. Charges trapped by the trap states in the oxide semiconductor film take a long time to be released and may behave like fixed charges. Thus, the transistor whose channel region is formed in the oxide semiconductor film having a high density of trap states has unstable electrical characteristics in some cases. Examples of the impurities include hydrogen, nitrogen, alkali metal, and alkaline earth metal.

20 [0058]

Hydrogen contained in the oxide semiconductor film reacts with oxygen bonded to a metal atom to be water, and in addition, an oxygen vacancy is formed in a lattice from which oxygen is released (or a portion from which oxygen is released). Due to entry of hydrogen into the oxygen vacancy, an electron serving as a carrier is 25 generated in some cases. Further, in some cases, bonding of part of hydrogen to oxygen bonded to a metal element causes generation of an electron serving as a carrier. Thus, a transistor including an oxide semiconductor that contains hydrogen is likely to be normally on.

[0059]

30 Accordingly, it is preferable that hydrogen be reduced as much as possible as well as the oxygen vacancies in the oxide semiconductor film 19. Specifically, the

hydrogen concentration of the oxide semiconductor film 19, which is measured by secondary ion mass spectrometry (SIMS), is lower than or equal to 2×10^{20} atoms/cm³, lower than or equal to 5×10^{19} atoms/cm³, lower than or equal to 1×10^{19} atoms/cm³, lower than or equal to 5×10^{18} atoms/cm³, lower than or equal to 1×10^{18} atoms/cm³, lower than or equal to 5×10^{17} atoms/cm³, or lower than or equal to 1×10^{16} atoms/cm³.

[0060]

When silicon or carbon that is one of elements belonging to Group 14 is contained in the oxide semiconductor film 19, oxygen vacancies are increased in the oxide semiconductor film 19, and the oxide semiconductor film 19 becomes an n-type film. Thus, the concentration of silicon or carbon (the concentration is measured by SIMS) of the oxide semiconductor film 19 is lower than or equal to 2×10^{18} atoms/cm³, or lower than or equal to 2×10^{17} atoms/cm³.

[0061]

Further, the concentration of alkali metal or alkaline earth metal of the oxide semiconductor film 19, which is measured by SIMS, is lower than or equal to 1×10^{18} atoms/cm³, or lower than or equal to 2×10^{16} atoms/cm³. Alkali metal and alkaline earth metal might generate carriers when bonded to an oxide semiconductor, in which case the off-state current of the transistor might be increased. Therefore, it is preferable to reduce the concentration of alkali metal or alkaline earth metal of the oxide semiconductor film 19.

[0062]

Further, when containing nitrogen, the oxide semiconductor film 19 easily becomes n-type by generation of electrons serving as carriers and an increase of carrier density. Thus, a transistor including an oxide semiconductor that contains nitrogen is likely to be normally on. For this reason, nitrogen in the oxide semiconductor film is preferably reduced as much as possible; the concentration of nitrogen that is measured by SIMS is preferably set to, for example, lower than or equal to 5×10^{18} atoms/cm³.

[0063]

The oxide semiconductor film 19 may have a non-single-crystal structure, for example. The non-single crystal structure includes a c-axis aligned crystalline oxide semiconductor (CAAC-OS) that is described later, a polycrystalline structure, a

microcrystalline structure described later, or an amorphous structure, for example. Among the non-single crystal structure, the amorphous structure has the highest density of defect levels, whereas CAAC-OS has the lowest density of defect levels.

[0064]

5 The oxide semiconductor film 19 may have an amorphous structure, for example. An oxide semiconductor film having an amorphous structure has, for example, disordered atomic arrangement and no crystalline component. Alternatively, an oxide film having an amorphous structure has, for example, an absolutely amorphous structure and has no crystal part.

10 [0065]

Note that the oxide semiconductor film 19 may be a mixed film including two or more of the following: a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure. The mixed film includes, for 15 example, two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure in some cases. Further, the mixed film has a stacked-layer structure of two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline 20 structure, a CAAC-OS region, and a region having a single-crystal structure in some cases.

[0066]

The pair of electrodes 20 and 21 are formed with a single layer or a stack using any of metals such as aluminum, titanium, chromium, nickel, copper, yttrium, zirconium, 25 molybdenum, silver, tantalum, and tungsten and an alloy containing any of these metals as a main component. For example, a single-layer structure of an aluminum film containing silicon, a two-layer structure in which an aluminum film is stacked over a titanium film, a two-layer structure in which an aluminum film is stacked over a tungsten film, a two-layer structure in which a copper film is formed over a copper-magnesium-aluminum alloy film, a two-layer structure in which a copper film is formed over a titanium film, a two-layer structure in which a copper film is formed over a tungsten film, a three-layer structure in which a titanium film or a titanium nitride film,

an aluminum film or a copper film, and a titanium film or a titanium nitride film are stacked in this order, a three-layer structure in which a molybdenum film or a molybdenum nitride film, an aluminum film or a copper film, and a molybdenum film or a molybdenum nitride film are stacked in this order, and the like can be given. Note 5 that a transparent conductive material containing indium oxide, tin oxide, or zinc oxide may be used.

[0067]

The gate insulating film 28 includes the oxide insulating film 23 in contact with the oxide semiconductor film 19, the oxide insulating film 25 in contact with the oxide insulating film 23, and the nitride insulating film 27 in contact with the oxide insulating film 25. The gate insulating film 28 preferably includes at least an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. Here, as the oxide insulating film 23, an oxide insulating film through which oxygen passes is formed. As the oxide insulating film 25, an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition is formed. As the nitride insulating film 27, a nitride insulating film that blocks hydrogen and oxygen is formed.

[0068]

The oxide insulating film 23 is an oxide insulating film through which oxygen passes. Thus, oxygen released from the oxide insulating film 25 over the oxide insulating film 23 can be transferred to the oxide semiconductor film 19 through the oxide insulating film 23. Further, the oxide insulating film 23 also serves as a film that relieves damage to the oxide semiconductor film 19 at the time of forming the oxide insulating film 25 later.

25 [0069]

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 5 nm and less than or equal to 150 nm, or greater than or equal to 5 nm and less than or equal to 50 nm can be used as the oxide insulating film 23. Note that in this specification, a "silicon oxynitride film" refers to a film that contains 30 oxygen at a higher proportion than nitrogen, and a "silicon nitride oxide film" refers to a film that contains nitrogen at a higher proportion than oxygen.

[0070]

Further, it is preferable that the number of defects in the oxide insulating film 23 be small and typically, the spin density of a signal that appears at $g = 2.001$ due to a dangling bond of silicon be lower than or equal to 3×10^{17} spins/cm³ by electron spin resonance (ESR) measurement. This is because if the density of defects in the oxide insulating film 23 is high, oxygen is bonded to the defects and the amount of oxygen that passes through the oxide insulating film 23 is reduced.

[0071]

Further, it is preferable that the number of defects at the interface between the oxide insulating film 23 and the oxide semiconductor film 19 be small and typically, the spin density of a signal that appears at $g = 1.93$ due to an oxygen vacancy in the oxide semiconductor film 19 be lower than or equal to 1×10^{17} spins/cm³, more preferably lower than or equal to the lower limit of detection by ESR measurement.

[0072]

Note that in the oxide insulating film 23, all oxygen that enters the oxide insulating film 23 from the outside is transferred to the outside of the oxide insulating film 23 in some cases. Alternatively, some oxygen that enters the oxide insulating film 23 from the outside remains in the oxide insulating film 23. Further, movement of oxygen occurs in the oxide insulating film 23 in some cases in such a manner that oxygen enters the oxide insulating film 23 from the outside and oxygen contained in the oxide insulating film 23 is transferred to the outside of the oxide insulating film 23.

[0073]

The oxide insulating film 25 is formed in contact with the oxide insulating film 23. The oxide insulating film 25 is formed using an oxide insulating film that contains a higher proportion of oxygen than that of oxygen in the stoichiometric composition. Part of oxygen is released by heating from the oxide insulating film that contains a higher proportion of oxygen than that of oxygen in the stoichiometric composition. The oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition is an oxide insulating film of which the amount of released oxygen converted into oxygen atoms is greater than or equal to 1.0×10^{18} atoms/cm³, or greater than or equal to 3.0×10^{20} atoms/cm³ in TDS analysis.

[0074]

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 30 nm and less than or equal to 500 nm, or greater than or equal to 50 nm and less than or equal to 400 nm can be used as the oxide insulating film 25.

[0075]

5 Further, it is preferable that the number of defects in the oxide insulating film 25 be small and typically, the spin density of a signal that appears at $g = 2.001$ originating from a dangling bond of silicon be lower than 1.5×10^{18} spins/cm³, more preferably lower than or equal to 1×10^{18} spins/cm³ by ESR measurement. Note that the oxide insulating film 25 is provided more apart from the oxide semiconductor film 10 19 than the oxide insulating film 23 is; thus, the oxide insulating film 25 may have higher defect density than the oxide insulating film 23.

[0076]

15 The nitride insulating film 27 has an effect of blocking at least hydrogen and oxygen. Alternatively, the nitride insulating film 27 has an effect of blocking oxygen, hydrogen, water, an alkali metal, an alkaline earth metal, or the like.

[0077]

20 The nitride insulating film 27 is formed using a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, or the like having a thickness of greater than or equal to 50 nm and less than or equal to 300 nm, or greater than or equal to 100 nm and less than or equal to 200 nm.

[0078]

25 Note that instead of the nitride insulating film 27, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like may be provided. As the oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, and a hafnium oxynitride film can be given.

[0079]

30 For each of the gate electrode 29 and the electrode 30, a light-transmitting conductive film is used. As examples of the light-transmitting conductive film, a film of indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide,

indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, indium tin oxide to which silicon oxide is added, or the like can be given.

[0080]

5 Next, a method for manufacturing the transistor 50 illustrated in FIGS. 1A to 1C is described with reference to FIGS. 2A to 2J. FIGS. 2A, 2C, 2E, 2G, and 2I are cross-sectional views in the channel length direction that illustrate steps for manufacturing the transistor 50 illustrated in FIG. 1B. FIGS. 2B, 2D, 2F, 2H, and 2J are cross-sectional views in the channel width direction that illustrate the steps for 10 manufacturing the transistor 50 illustrated in FIG. 1C.

[0081]

As illustrated in FIGS. 2A and 2B, the gate electrode 15 is formed over the substrate 11, and an insulating film 16 to be the gate insulating film 17 is formed over the gate electrode 15. Next, the oxide semiconductor film 19 is formed over the 15 insulating film 16.

[0082]

Here, a glass substrate is used as the substrate 11.

[0083]

20 A method for forming the gate electrode 15 is described below. First, a conductive film is formed by a sputtering method, a CVD method, an evaporation method, or the like. Then, a mask is formed over the conductive film by a photolithography process using a first photomask. Next, part of the conductive film is etched with the use of the mask to form the gate electrode 15. After that, the mask is removed.

25 [0084]

Note that the gate electrode 15 may be formed by an electrolytic plating method, a printing method, an inkjet method, or the like instead of the above formation method.

[0085]

30 Here, a 100-nm-thick tungsten film is formed by a sputtering method. Next, a mask is formed by a photolithography process, and the tungsten film is subjected to dry etching with the use of the mask to form the gate electrode 15.

[0086]

The insulating film 16 is formed by a sputtering method, a CVD method, an evaporation method, or the like.

[0087]

5 In the case where a silicon oxide film, a silicon oxynitride film, or a silicon nitride oxide film is formed as the insulating film 16, a deposition gas containing silicon and an oxidizing gas are preferably used as a source gas. Typical examples of the deposition gas containing silicon include silane, disilane, trisilane, and silane fluoride. As the oxidizing gas, oxygen, ozone, dinitrogen monoxide, nitrogen dioxide, and the like can be given as examples.

[0088]

Moreover, in the case of forming a gallium oxide film as the insulating film 16, a metal organic chemical vapor deposition (MOCVD) method can be employed.

[0089]

15 A formation method of the oxide semiconductor film 19 is described below. An oxide semiconductor film to be the oxide semiconductor film 19 is formed over the insulating film 16. Then, after a mask is formed over the oxide semiconductor film by a photolithography process using a second photomask, the oxide semiconductor film is partly etched using the mask. Thus, the oxide semiconductor film 19 subjected to element isolation as illustrated in FIGS. 2A and 2B is formed. After that, the mask is removed.

[0090]

25 The oxide semiconductor film to be the oxide semiconductor film 19 can be formed by a sputtering method, a coating method, a pulsed laser deposition method, a laser ablation method, or the like.

[0091]

30 In the case where the oxide semiconductor film is formed by a sputtering method, a power supply device for generating plasma can be an RF power supply device, an AC power supply device, a DC power supply device, or the like as appropriate.

[0092]

As a sputtering gas, a rare gas (typically argon), an oxygen gas, or a mixed gas

of a rare gas and oxygen is used as appropriate. In the case of using the mixed gas of a rare gas and oxygen, the proportion of oxygen to a rare gas is preferably increased.

[0093]

Further, a target may be appropriately selected in accordance with the 5 composition of the oxide semiconductor film to be formed.

[0094]

In order to obtain an intrinsic or substantially intrinsic oxide semiconductor film, besides the high vacuum evacuation of the chamber, a highly purification of a sputtering gas is also needed. As an oxygen gas or an argon gas used for a sputtering 10 gas, a gas that is highly purified to have a dew point of -40°C or lower, -80°C or lower, -100°C or lower, or -120°C or lower is used, whereby entry of moisture or the like into the oxide semiconductor film can be prevented as much as possible.

[0095]

Here, a 35-nm-thick In-Ga-Zn oxide film is formed as the oxide semiconductor 15 film by a sputtering method using an In-Ga-Zn oxide target (In:Ga:Zn = 3:1:2). Next, a mask is formed over the oxide semiconductor film, and part of the oxide semiconductor film is selectively etched. Thus, the oxide semiconductor film 19 is formed.

[0096]

20 Next, as illustrated in FIGS. 2C and 2D, the pair of electrodes 20 and 21 are formed.

[0097]

A method for forming the pair of electrodes 20 and 21 is described below. First, a conductive film is formed by a sputtering method, a CVD method, an 25 evaporation method, or the like. Then, a mask is formed over the conductive film by a photolithography process using a third photomask. Next, the conductive film is etched with the use of the mask to form the pair of electrodes 20 and 21. After that, the mask is removed.

[0098]

30 Here, a 50-nm-thick tungsten film and a 300-nm-thick copper film are formed in this order by a sputtering method. Then, a mask is formed over the copper film

through a photolithography process. Next, the copper film is etched by a wet etching method using the mask. Subsequently, the tungsten film is etched by a dry etching method using SF₆, so that a fluoride is formed on a surface of the copper film. The fluoride can reduce diffusion of copper elements from the copper film, resulting in a 5 reduction in the copper concentration in the oxide semiconductor film 19.

[0099]

Next, as illustrated in FIGS. 2E and 2F, an oxide insulating film 22 to be the oxide insulating film 23 and an oxide insulating film 24 to be the oxide insulating film 25 are formed over the oxide semiconductor film 19 and the pair of electrodes 20 and 10 21.

[0100]

Note that after the oxide insulating film 22 is formed, the oxide insulating film 24 is preferably formed in succession without exposure to the air. After the oxide insulating film 22 is formed, the oxide insulating film 24 is formed in succession by 15 adjusting at least one of the flow rate of a source gas, pressure, a high-frequency power, and a substrate temperature without exposure to the air, whereby the concentration of impurities attributed to the atmospheric component at the interface between the oxide insulating films 22 and 24 can be reduced and oxygen in the oxide insulating film 24 can be transferred to the oxide semiconductor film 19; accordingly, the number of 20 oxygen vacancies in the oxide semiconductor film 19 can be reduced.

[0101]

As the oxide insulating film 22, a silicon oxide film or a silicon oxynitride film can be formed under the following conditions: the substrate placed in a treatment chamber of a plasma CVD apparatus that is vacuum-evacuated is held at a temperature 25 higher than or equal to 280 °C and lower than or equal to 400 °C, the pressure is greater than or equal to 20 Pa and less than or equal to 250 Pa, or greater than or equal to 100 Pa and less than or equal to 250 Pa with introduction of a source gas into the treatment chamber, and a high-frequency power is supplied to an electrode provided in the treatment chamber.

30 [0102]

A deposition gas containing silicon and an oxidizing gas are preferably used as the source gas of the oxide insulating film 22. Typical examples of the deposition gas

containing silicon include silane, disilane, trisilane, and silane fluoride. As the oxidizing gas, oxygen, ozone, dinitrogen monoxide, nitrogen dioxide, and the like can be given as examples.

[0103]

5 With the use of the above conditions, an oxide insulating film through which oxygen passes can be formed as the oxide insulating film 22. Further, by providing the oxide insulating film 22, damage to the oxide semiconductor film 19 can be reduced in a later step of forming the oxide insulating film 25.

[0104]

10 As for the oxide insulating film 22, a silicon oxide film or a silicon oxynitride film can be formed as the oxide insulating film 22 under the following conditions: the substrate placed in a treatment chamber of a plasma CVD apparatus that is vacuum-evacuated is held at a temperature higher than or equal to 280 °C and lower than or equal to 400 °C, the pressure is greater than or equal to 100 Pa and less than or 15 equal to 250 Pa with introduction of a source gas into the treatment chamber, and a high-frequency power is supplied to an electrode provided in the treatment chamber.

[0105]

20 Under the above film formation conditions, the bonding strength of silicon and oxygen becomes strong in the above substrate temperature range. Thus, as the oxide insulating film 22, a dense and hard oxide insulating film through which oxygen passes, typically, a silicon oxide film or a silicon oxynitride film of which etching using hydrofluoric acid of 0.5 wt% at 25 °C is performed at a rate of lower than or equal to 10 nm/min, or lower than or equal to 8 nm/min can be formed.

[0106]

25 The oxide insulating film 22 is formed while heating is performed; thus, hydrogen, water, or the like contained in the oxide semiconductor film 19 can be released in the step. Hydrogen contained in the oxide semiconductor film 19 is bonded to an oxygen radical formed in plasma to form water. Since the substrate is heated in the step of forming the oxide insulating film 22, water formed by bonding of oxygen and hydrogen is released from the oxide semiconductor film. That is, when the oxide insulating film 22 is formed by a plasma CVD method, the amount of water and

hydrogen contained in the oxide semiconductor film can be reduced.

[0107]

Further, time for heating in a state where the oxide semiconductor film 19 is exposed can be shortened because heating is performed in a step of forming the oxide insulating film 22. Thus, the amount of oxygen released from the oxide semiconductor film by heat treatment can be reduced. That is, the number of oxygen vacancies in the oxide semiconductor film can be reduced.

[0108]

Note that by setting the pressure in the treatment chamber to be greater than or equal to 100 Pa and less than or equal to 250 Pa, the amount of water contained in the oxide insulating film 23 is reduced; thus, variation in electrical characteristics of the transistor 50 can be reduced and change in threshold voltage can be inhibited.

[0109]

Further, by setting the pressure in the treatment chamber to be greater than or equal to 100 Pa and less than or equal to 250 Pa, damage to the oxide semiconductor film 19 can be reduced when the oxide insulating film 22 is formed, so that the number of oxygen vacancies contained in the oxide semiconductor film 19 can be reduced. In particular, when the film formation temperature of the oxide insulating film 22 or the oxide insulating film 24 that is formed later is set to be high, typically higher than 220 °C, part of oxygen contained in the oxide semiconductor film 19 is released and oxygen vacancies are easily formed. Further, when the film formation conditions for reducing the number of defects in the oxide insulating film 24 that is formed later are used to increase reliability of the transistor, the amount of released oxygen is easily reduced. Thus, it is difficult to reduce oxygen vacancies in the oxide semiconductor film 19 in some cases. However, by setting the pressure in the treatment chamber to be greater than or equal to 100 Pa and less than or equal to 250 Pa to reduce damage to the oxide semiconductor film 19 at the time of forming the oxide insulating film 22, oxygen vacancies in the oxide semiconductor film 19 can be reduced even when the amount of oxygen released from the oxide insulating film 24 is small.

[0110]

Note that when the ratio of the amount of the oxidizing gas to the amount of the deposition gas containing silicon is 100 or higher, the hydrogen content in the oxide

insulating film 22 can be reduced. Consequently, the amount of hydrogen entering the oxide semiconductor film 19 can be reduced; thus, the negative shift in the threshold voltage of the transistor can be inhibited.

[0111]

5 Here, as the oxide insulating film 22, a 50-nm-thick silicon oxynitride film is formed by a plasma CVD method in which silane with a flow rate of 30 sccm and dinitrogen monoxide with a flow rate of 4000 sccm are used as a source gas, the pressure in the treatment chamber is 200 Pa, the substrate temperature is 220 °C, and a high-frequency power of 150 W is supplied to parallel-plate electrodes with the use of a
10 27.12 MHz high-frequency power source. Under the above conditions, a silicon oxynitride film through which oxygen passes can be formed.

[0112]

As the oxide insulating film 24, a silicon oxide film or a silicon oxynitride film is formed under the following conditions: the substrate placed in a treatment chamber of
15 the plasma CVD apparatus that is vacuum-evacuated is held at a temperature higher than or equal to 180 °C and lower than or equal to 280 °C, or higher than or equal to 200 °C and lower than or equal to 240 °C, the pressure is greater than or equal to 100 Pa and less than or equal to 250 Pa, or greater than or equal to 100 Pa and less than or equal to 200 Pa with introduction of a source gas into the treatment chamber, and a
20 high-frequency power of greater than or equal to 0.17 W/cm² and less than or equal to 0.5 W/cm², or greater than or equal to 0.25 W/cm² and less than or equal to 0.35 W/cm² is supplied to an electrode provided in the treatment chamber.

[0113]

25 A deposition gas containing silicon and an oxidizing gas are preferably used as the source gas of the oxide insulating film 24. Typical examples of the deposition gas containing silicon include silane, disilane, trisilane, and silane fluoride. As the oxidizing gas, oxygen, ozone, dinitrogen monoxide, nitrogen dioxide, and the like can be given as examples.

[0114]

30 As the film formation conditions of the oxide insulating film 24, the high-frequency power having the above power density is supplied to the treatment

chamber having the above pressure, whereby the decomposition efficiency of the source gas in plasma is increased, oxygen radicals are increased, and oxidation of the source gas is promoted; therefore, the oxide insulating film 25 contains a higher proportion of oxygen than that of oxygen in the stoichiometric composition. On the other hand, in 5 the film formed at a substrate temperature within the above temperature range, the bond between silicon and oxygen is weak, and accordingly, part of oxygen in the film is released by heat treatment in the later step. Thus, it is possible to form an oxide insulating film that contains a higher proportion of oxygen than that of oxygen in the stoichiometric composition and from which part of oxygen is released by heating. 10 Further, the oxide insulating film 22 is provided over the oxide semiconductor film 19. Accordingly, in the step of forming the oxide insulating film 24, the oxide insulating film 22 serves as a protective film of the oxide semiconductor film 19. Consequently, the oxide insulating film 24 can be formed using the high-frequency power having a high power density while damage to the oxide semiconductor film 19 is reduced.

15 [0115]

Here, as the oxide insulating film 24, a 400-nm-thick silicon oxynitride film is formed by a plasma CVD method in which silane with a flow rate of 200 sccm and dinitrogen monoxide with a flow rate of 4000 sccm are used as the source gas, the pressure in the treatment chamber is 200 Pa, the substrate temperature is 220 °C, and the 20 high-frequency power of 1500 W is supplied to the parallel-plate electrodes with the use of a 27.12 MHz high-frequency power source. Note that a plasma CVD apparatus used here is a parallel-plate plasma CVD apparatus in which the electrode area is 6000 cm², and the power per unit area (power density) into which the supplied power is converted is 0.25 W/cm².

25 [0116]

Next, heat treatment is performed. The heat treatment is performed typically at a temperature of higher than or equal to 150 °C and lower than or equal to 400 °C, higher than or equal to 300 °C and lower than or equal to 400 °C, or higher than or equal to 320 °C and lower than or equal to 370 °C.

30 [0117]

An electric furnace, a rapid thermal anneal (RTA) apparatus, or the like can be

used for the heat treatment. With the use of an RTA apparatus, the heat treatment can be performed at a temperature of higher than or equal to the strain point of the substrate if the heating time is short. Therefore, the heat treatment time can be shortened.

[0118]

5 The heat treatment may be performed under an atmosphere of nitrogen, oxygen, ultra-dry air (air in which a water content is 20 ppm or less, 1 ppm or less, or 10 ppb or less), or a rare gas (argon, helium, or the like). The atmosphere of nitrogen, oxygen, ultra-dry air, or a rare gas preferably does not contain hydrogen, water, and the like.

[0119]

10 By the heat treatment, part of oxygen contained in the oxide insulating film 24 can be transferred to the oxide semiconductor film 19, so that the number of oxygen vacancies contained in the oxide semiconductor film 19 can be reduced. Consequently, the number of oxygen vacancies in the oxide semiconductor film 19 can be further reduced.

15 [0120]

Further, in the case where water, hydrogen, or the like is contained in the oxide insulating films 22 and 24, when the nitride insulating film 26 having a function of blocking water, hydrogen, and the like is formed later and heat treatment is performed, water, hydrogen, or the like contained in the oxide insulating films 22 and 24 are moved 20 to the oxide semiconductor film 19, so that defects are generated in the oxide semiconductor film 19. However, by the heating, water, hydrogen, or the like contained in the oxide insulating films 22 and 24 can be released; thus, variation in electrical characteristics of the transistor 50 can be reduced, and change in threshold voltage can be inhibited.

25 [0121]

Note that when the oxide insulating film 24 is formed over the oxide insulating film 22 while being heated, oxygen can be transferred to the oxide semiconductor film 19 to reduce the oxygen vacancies in the oxide semiconductor film 19; thus, the heat treatment is not necessarily performed.

30 [0122]

Here, heat treatment is performed at 350 °C for one hour in an atmosphere of nitrogen and oxygen.

[0123]

Further, when the pair of electrodes 20 and 21 are formed, the oxide semiconductor film 19 is damaged by the etching of the conductive film, so that oxygen vacancies are generated on the back channel side (the side of the oxide semiconductor film 19 that is opposite to the side facing to the gate electrode 15) of the oxide semiconductor film 19. However, with the use of the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition as the oxide insulating film 24, the oxygen vacancies generated on the back channel side can be repaired by heat treatment. By this, defects contained in the oxide semiconductor film 19 can be reduced, and thus, the reliability of the transistor 50 can be improved.

[0124]

Next, the nitride insulating film 26 is formed by a sputtering method, a CVD method, or the like.

15 [0125]

Note that in the case where the nitride insulating film 26 is formed by a plasma CVD method, the substrate placed in the treatment chamber of the plasma CVD apparatus that is vacuum-evacuated is preferably set to be higher than or equal to 300 °C and lower than or equal to 400 °C, or higher than or equal to 320 °C and lower 20 than or equal to 370 °C, so that a dense nitride insulating film can be formed.

[0126]

In the case where a silicon nitride film is formed by the plasma CVD method as the nitride insulating film 26, a deposition gas containing silicon, nitrogen, and ammonia are preferably used as a source gas. As the source gas, a small amount of 25 ammonia compared to the amount of nitrogen is used, whereby ammonia is dissociated in the plasma and activated species are generated. The activated species cleave a bond between silicon and hydrogen that are contained in a deposition gas containing silicon and a triple bond between nitrogen molecules. As a result, a dense silicon nitride film having few defects, in which a bond between silicon and nitrogen is promoted and a 30 bond between silicon and hydrogen is few can be formed. On the other hand, when the amount of ammonia with respect to nitrogen is large in a source gas, cleavage of a

deposition gas containing silicon and cleavage of nitrogen are not promoted, so that a sparse silicon nitride film in which a bond between silicon and hydrogen remains and defects are increased is formed. Therefore, in a source gas, a flow ratio of the nitrogen to the ammonia is set to be greater than or equal to 5 and less than or equal to 50, or 5 greater than or equal to 10 and less than or equal to 50.

[0127]

Here, in the treatment chamber of a plasma CVD apparatus, a 50-nm-thick silicon nitride film is formed as the nitride insulating film 26 by a plasma CVD method in which silane with a flow rate of 50 sccm, nitrogen with a flow rate of 5000 sccm, and 10 ammonia with a flow rate of 100 sccm are used as the source gas, the pressure in the treatment chamber is 100 Pa, the substrate temperature is 350 °C, and high-frequency power of 1000 W is supplied to parallel-plate electrodes with a high-frequency power supply of 27.12 MHz. Note that the plasma CVD apparatus is a parallel-plate plasma CVD apparatus in which the electrode area is 6000 cm², and the power per unit area 15 (power density) into which the supplied power is converted is 1.7×10^{-1} W/cm².

[0128]

By the above-described steps, the oxide insulating film 22, the oxide insulating film 24, and the nitride insulating film 26 can be formed.

[0129]

20 Next, heat treatment may be performed. The heat treatment is performed typically at a temperature of higher than or equal to 150 °C and lower than or equal to 400 °C, higher than or equal to 300 °C and lower than or equal to 400 °C, or higher than or equal to 320 °C and lower than or equal to 370 °C.

[0130]

25 Next, a mask is formed over the nitride insulating film 26 by a photolithography process using a fourth photomask, and then each of the oxide insulating film 22, the oxide insulating film 24, and the nitride insulating film 26 is partly etched using the mask, so that the gate insulating film 28 including the oxide insulating film 23, the oxide insulating film 25, and the nitride insulating film 27 is 30 formed.

[0131]

The oxide insulating film 22, the oxide insulating film 24, and the nitride insulating film 26 are each etched so that the end portions of the gate insulating film 28 are positioned over the pair of electrodes 20 and 21 in the channel length direction as illustrated in FIG. 2G and the end portions of the gate insulating film 28 are positioned 5 on the outer side of the oxide semiconductor film 19 in the channel width direction as illustrated in FIG. 2H. As a result, the isolated gate insulating film 28 can be formed. In the case where part of the insulating film 16, at least a surface region, is formed using 10 the same material as that of the oxide insulating film 23, the part of the insulating film 16 is also etched in the etching of the oxide insulating film 23. As a result, the gate insulating film 17 having a step is formed.

[0132]

By the etching step, as illustrated in FIG. 2H, in the channel width direction, the minimum distance between the side surface of the oxide semiconductor film 19 and a side surface of the gate insulating film 28 preferably becomes greater than or equal to 15 0.5 μm and less than or equal to 1.5 μm . In that case, a short circuit between the gate electrode 29 and the oxide semiconductor film 19 can be prevented, which can increase yield.

[0133]

Then, as illustrated in FIGS. 2I and 2J, the gate electrode 29 and the electrode 20 30 are formed. A method for forming the gate electrode 29 and the electrode 30 is described below. First, a conductive film is formed by a sputtering method, a CVD method, an evaporation method, or the like. Then, a mask is formed over the conductive film by a photolithography process using a fifth mask. Next, part of the conductive film is etched with the use of the mask to form the gate electrode 29 and the 25 electrode 30. After that, the mask is removed.

[0134]

As illustrated in FIG. 2I, the gate electrode 29 and the electrode 30 are formed so that end portions of the gate electrode 29 are positioned over the gate insulating film 28 in the channel length direction. Further, as illustrated in FIG. 2J, the gate electrode 30 29 and the electrode 30 are formed so that the gate electrode 29 faces the side surface of the oxide semiconductor film 19 with the gate insulating film 28 provided therebetween in the channel width direction, in other words, end portions of the gate electrode 29 are

positioned on the outer side of the end portions of the oxide semiconductor film 19 in the channel width direction.

[0135]

By the above-described process, the transistor 50 can be manufactured.

5 [0136]

In FIGS. 2G and 2H, after the gate insulating film 28 is formed, a mask is formed by a photolithography process, and part of the gate insulating film 17 is etched, so that an opening 28c in which part of the gate electrode 15 is exposed is formed. Then, a gate electrode 29a may be formed so as to be connected to the gate electrode 15 10 in the opening 28c. Accordingly, a transistor 51 in which the gate electrodes 15 and 29a are connected to each other can be fabricated (see FIGS. 3A to 3C). That is, the gate electrodes 15 and 29a can have the same potential.

[0137]

Furthermore, a shape of a transistor 52 in FIGS. 4A to 4C in which an end portion of a gate electrode 29b is positioned on the outer side of the gate electrode 15 in the channel width direction may be employed. Typically, as illustrated in FIG. 4C, in the channel width direction, the end portion of the gate electrode 29b is positioned on the outer side of the end portion of the gate electrode 15.

[0138]

20 In the transistor described in this embodiment, when any of the gate electrodes 29, 29a, and 29b faces the side surface of the oxide semiconductor film 19 with the gate insulating film 28 positioned therebetween in the channel width direction, formation of a parasitic channel at the side surface of the oxide semiconductor film 19 and its vicinity is suppressed because of an electric field of any of the gate electrodes 29, 29a, and 29b. 25 As a result, the transistor has excellent electrical characteristics in which drain current is drastically increased at the threshold voltage.

[0139]

Further, the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition is formed to overlap with the oxide 30 semiconductor film that serves as a channel region, and thus, oxygen in the oxide insulating film can be transferred to the oxide semiconductor film. Consequently, the number of oxygen vacancies in the oxide semiconductor film can be reduced.

[0140]

In this embodiment, an insulating film to be the gate insulating film 28 is formed by a plasma CVD method in which heating is performed at a temperature of higher than or equal to 280 °C and lower than or equal to 400°C. Thus, hydrogen, water, or the like contained in the oxide semiconductor film 19 can be released. Further, in the step, the length of heating time in a state where the oxide semiconductor film is exposed is short, and even when the temperature of the oxide semiconductor film with heat treatment is lower than or equal to 400 °C, it is possible to manufacture a transistor in which the amount of change in threshold voltage is equivalent to that of a transistor subjected to heat treatment at a high temperature. Consequently, the manufacturing cost of a semiconductor device can be reduced.

[0141]

Thus, a semiconductor device which includes an oxide semiconductor and in which formation of a parasitic channel due to a gate BT stress is suppressed can be provided. Further, a semiconductor device including an oxide semiconductor film and having improved electrical characteristics can be obtained.

[0142]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0143]

(Embodiment 2)

In this embodiment, a semiconductor device and a manufacturing method thereof, which are different from those in Embodiment 1, are described with reference to drawings. This embodiment differs from Embodiment 1 in that a protective film is not isolated for each transistor.

[0144]

A top view and cross-sectional views of a transistor 60 included in a semiconductor device are illustrated in FIGS. 5A to 5C. The transistor 60 illustrated in FIGS. 5A to 5C is a channel-etched transistor. FIG. 5A is a top view of the transistor 60, FIG. 5B is a cross-sectional view taken along dashed-dotted line A-B of FIG. 5A,

and FIG. 5C is a cross-sectional view taken along dashed-dotted line C-D of FIG. 5A. Note that in FIG. 5A, the substrate 11, a gate insulating film 31, an oxide insulating film 33, an oxide insulating film 35, a nitride insulating film 37 and the like are omitted for simplicity.

5 [0145]

The transistor 60 illustrated in FIGS. 5B and 5C includes the gate electrode 15 over the substrate 11; the gate insulating film 31 over the substrate 11 and the gate electrode 15; the oxide semiconductor film 19 overlapping with the gate electrode 15 with the gate insulating film 31 positioned therebetween; the pair of electrodes 20 and 10 21 in contact with the oxide semiconductor film 19; a gate insulating film 38 over the gate insulating film 31, the oxide semiconductor film 19, and the pair of electrodes 20 and 21; and a gate electrode 39 over the gate insulating film 38. Further, the gate insulating film 38 includes the oxide insulating film 33, the oxide insulating film 35, and the nitride insulating film 37. Furthermore, an electrode 40 connected to one of 15 the pair of electrodes 20 and 21 (here, the electrode 21) is formed over the nitride insulating film 37. Note that the electrode 40 serves as a pixel electrode.

[0146]

In the transistor 60 described in this embodiment, the oxide semiconductor film 19 is provided between the gate electrodes 15 and 39. The gate insulating film 38 20 includes a plurality of openings. Typically, the gate insulating film 38 includes openings 38a and 38b between which the oxide semiconductor film 19 is positioned in the channel width direction. The openings 38a and 38b are formed also in the gate insulating film 31. The gate insulating film 38 includes an opening 38c in which one 25 of the pair of electrodes 20 and 21 is exposed. In the channel width direction in FIG. 5C, the gate electrode 39 is formed over the gate insulating film 38 and in the openings 38a and 38b formed in the gate insulating films 31 and 38. In the openings 38a and 38b, the gate electrode 15 is connected to the gate electrode 39. The gate electrode 39 faces side surfaces of the oxide semiconductor film 19 at side surfaces of the openings 38a and 38b. Note that as illustrated in FIG. 5C, in the channel width direction, the 30 minimum distance between the side surface of the oxide semiconductor film 19 and each of the side surfaces of the openings 38a and 38b is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . Typically, the distance between the side

surface of the oxide semiconductor film 19 and each of the side surfaces of the openings 38a and 38b that is the closest to the side surface of the oxide semiconductor film 19 is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . In other words, the minimum distance between the side surface of the oxide semiconductor film 19 and the gate electrode 39 is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . In that case, a short circuit between the gate electrode 39 and the oxide semiconductor film 19 can be prevented, which can increase yield.

[0147]

Defects are formed at an end portion of the oxide semiconductor film processed by etching or the like because of damage due to processing, and the end portion of the oxide semiconductor film is polluted by attachment of impurities, or the like. Thus, when stress such as an electric field is applied, the end portion of the oxide semiconductor film is easily activated to be n-type (have low resistance). Thus, in this embodiment, an end portion of the oxide semiconductor film 19 that overlaps with the gate electrode 15 is likely to be n-type. When the n-type end portion is formed between the pair of electrodes 20 and 21, the n-type region serves as a carrier path, resulting in formation of a parasitic channel. However, as illustrated in FIG. 5C, when the gate electrode 39 faces the side surface of the oxide semiconductor film 19 with the gate insulating film 38 positioned therebetween in the channel width direction, formation of a parasitic channel at the side surface of the oxide semiconductor film 19 and its vicinity is suppressed because of an electric field of the gate electrode 39. As a result, the transistor has excellent electrical characteristics in which drain current is drastically increased at the threshold voltage.

[0148]

Further, an electric field from the outside can be blocked by the gate electrodes 15 and 39 that are connected to each other; thus, charges of charged particles and the like that are formed between the substrate 11 and the gate electrode 15 and over the gate electrode 39 do not affect the oxide semiconductor film 19. Therefore, degradation due to a stress test (e.g., -GBT stress test) can be reduced, and changes in the rising voltages of on-state current at different drain voltages can be reduced.

[0149]

With the gate electrodes 15 and 39 that are connected to each other, the amount of change in the threshold voltage is reduced. Accordingly, variation in electrical characteristics among a plurality of transistors is also reduced.

[0150]

5 Moreover, the gate insulating film 38 over the oxide semiconductor film 19 includes an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. Part of oxygen is released by heating from the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. The oxide insulating film containing a higher 10 proportion of oxygen than that of oxygen in the stoichiometric composition is an oxide insulating film of which the amount of released oxygen converted into oxygen atoms is greater than or equal to 1.0×10^{18} atoms/cm³, or greater than or equal to 3.0×10^{20} atoms/cm³ in TDS analysis.

[0151]

15 In the case where the gate insulating film 38 includes the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition, part of oxygen contained in the gate insulating film 38 can be transferred to the oxide semiconductor film 19 to reduce oxygen vacancies in the oxide semiconductor film 19. Consequently, the number of oxygen vacancies in the oxide 20 semiconductor film 19 can be further reduced.

[0152]

25 In a transistor formed using an oxide semiconductor film including oxygen vacancies, the threshold voltage is likely to shift in the negative direction to have normally-on characteristics. This is because charges are generated owing to oxygen vacancies in the oxide semiconductor film and the resistance is thus reduced. The transistor having normally-on characteristics causes various problems in that malfunction is likely to be caused when in operation and that power consumption is increased when not in operation. Further, there is a problem in that the amount of change in electrical characteristics, typically in threshold voltage, of the transistor is 30 increased by passage of time or a stress test.

[0153]

However, in the transistor 60 described in this embodiment, the gate insulating

film 38 over the oxide semiconductor film 19 includes an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition. Accordingly, the number of oxygen vacancies in the oxide semiconductor film 19 can be reduced, and thus the transistor has normally-off characteristics. Further, the amount of change in electrical characteristics, typically in threshold voltage, of the transistor due to passage of time or a stress test can be reduced.

5 [0154]

Other details of the transistor 60 are described below. Descriptions of the structures having the same reference numerals as those of Embodiment 1 are omitted.

10 [0155]

The gate insulating film 31 can be formed using a material similar to that of the gate insulating film 17 described in Embodiment 1 as appropriate.

[0156]

15 The gate insulating film 38 includes the oxide insulating film 33 in contact with the oxide semiconductor film 19, the oxide insulating film 35 in contact with the oxide insulating film 33, and the nitride insulating film 37 in contact with the oxide insulating film 35. Note that the oxide insulating film 33 can be formed using a material similar to that of the oxide insulating film 23 described in Embodiment 1 as appropriate. The oxide insulating film 35 can be formed using a material similar to that of the oxide insulating film 25 described in Embodiment 1 as appropriate. The nitride insulating film 37 can be formed using a material similar to that of the nitride insulating film 27 described in Embodiment 1 as appropriate.

20

[0157]

25 The gate electrode 39 and the electrode 40 can be formed using a material similar to that of the gate electrode 29 and the electrode 30 described in Embodiment 1 as appropriate.

[0158]

30 Next, a method for manufacturing the transistor 60 illustrated in FIGS. 5A to 5C is described with reference to FIGS. 2A to 2F and FIGS. 6A to 6D. FIGS. 6A and 6C are cross-sectional views in the channel length direction that illustrate steps for manufacturing the transistor 60 illustrated in FIG. 5B. FIGS. 6B and 6D are cross-sectional views in the channel width direction that illustrate the steps for

manufacturing the transistor 60 illustrated in FIG. 5C.

[0159]

As in the case of Embodiment 1, through steps of FIGS. 2A to 2F, the gate electrode 15, the insulating film 16, the oxide semiconductor film 19, the pair of electrodes 20 and 21, the oxide insulating film 22, the oxide insulating film 24, and the nitride insulating film 26 are formed over the substrate 11. In the steps, a photolithography process is performed using the first to third photomasks.

[0160]

Next, a mask is formed over the nitride insulating film 26 by a photolithography process using the fourth photomask, and then each of the oxide insulating film 22, the oxide insulating film 24, and the nitride insulating film 26 is partly etched using the mask, so that the gate insulating film 38 including the oxide insulating film 33, the oxide insulating film 35, and the nitride insulating film 37 is formed.

[0161]

In the step, as illustrated in FIG. 6A, each of the oxide insulating film 33, the oxide insulating film 35, and the nitride insulating film 37 is partly etched to form the opening 38c in which the electrode 21, which is one of the pair of electrodes 20 and 21, is exposed in the channel length direction. Further, as illustrated in FIG. 6B, the openings 38a and 38b are formed so that the oxide semiconductor film 19 is positioned therebetween in the channel width direction. In the channel width direction, the minimum distance between the side surface of the oxide semiconductor film 19 and each of the side surfaces of the openings 38a and 38b is preferably greater than or equal to 0.5 μm and less than or equal to 1.5 μm . In that case, a short circuit between the gate electrode 39 and the oxide semiconductor film 19 can be prevented, which can increase yield. Further, the gate insulating film 38 including the openings 38a, 38b, and 38c can be formed.

[0162]

Then, as illustrated in FIGS. 6C and 6D, the gate electrode 39 and the electrode 40 are formed. A method for forming the gate electrode 39 and the electrode 40 is described below. First, a conductive film is formed by a sputtering method, a CVD method, an evaporation method, or the like. Then, a mask is formed over the

conductive film by a photolithography process using the fifth mask. Next, part of the conductive film is etched with the use of the mask to form the gate electrode 39 and the electrode 40. After that, the mask is removed.

[0163]

5 As illustrated in FIG. 6D, in the channel width direction, the gate electrode 39 and the electrode 40 are formed so that the gate electrode 39 faces the side surface of the oxide semiconductor film 19 at each of the side surface of the openings 38a and 38b, in other words, end portions of the gate electrode 39 are positioned on the outer side of the end portions of the oxide semiconductor film 19.

10 [0164]

Through the above-described process, the transistor 60 can be manufactured.

[0165]

15 In the transistor described in this embodiment, when the gate electrode 39 faces the side surface of the oxide semiconductor film 19 at each of the side surfaces of the openings 38a and 38b formed in the gate insulating film 38 in the channel width direction, formation of a parasitic channel at the side surface of the oxide semiconductor film 19 and its vicinity is suppressed because of an electric field of the gate electrode 39. As a result, the transistor has excellent electrical characteristics in which drain current is drastically increased at the threshold voltage.

20 [0166]

Further, the oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition is formed to overlap with the oxide semiconductor film that serves as a channel region, and thus, oxygen in the oxide insulating film can be transferred to the oxide semiconductor film. Consequently, the 25 number of oxygen vacancies in the oxide semiconductor film can be reduced.

[0167]

In this embodiment, an insulating film to be the gate insulating film 28 is formed by a plasma CVD method in which heating is performed at a temperature of higher than or equal to 280 °C and lower than or equal to 400°C. Thus, hydrogen, 30 water, or the like contained in the oxide semiconductor film 19 can be released. Further, in the step, the length of heating time in a state where the oxide semiconductor film is exposed is short, and even when the temperature of the oxide semiconductor film

with heat treatment is lower than or equal to 400 °C, it is possible to manufacture a transistor in which the amount of change in threshold voltage is equivalent to that of a transistor subjected to heat treatment at a high temperature. Consequently, the manufacturing cost of a semiconductor device can be reduced.

5 [0168]

Thus, a semiconductor device which includes an oxide semiconductor and in which formation of a parasitic channel due to a gate BT stress is suppressed can be provided. Further, a semiconductor device including an oxide semiconductor film and having improved electrical characteristics can be obtained.

10 [0169]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0170]

15 (Embodiment 3)

In this embodiment, the electrical characteristics of the transistor having a dual-gate structure described in Embodiments 1 and 2 that includes gate electrodes connected to each other and having the same potential are described with reference to FIGS. 1A to 1C and FIG. 7A to FIG. 12C.

20 [0171]

Note that here a driving method in which the gate electrodes 15 and 29 in FIG. 1A are electrically short-circuited and are supplied with a gate voltage is referred to as dual-gate driving. In other words, in dual-gate driving, the voltage of the gate electrode 15 is always equal to that of the gate electrode 29.

25 [0172]

Here, the electrical characteristics of the transistor were evaluated. FIGS. 7A and 7B illustrate the structures of transistors used for the calculation. Note that device simulation software "Atlas" produced by Silvaco Inc. was used for the calculation.

[0173]

30 A transistor having Structure 1 in FIG. 7A is a dual-gate transistor.

[0174]

In the transistor having Structure 1, an insulating film 203 is formed over a gate

electrode 201, and an oxide semiconductor film 205 is formed over the insulating film 203. A pair of electrodes 207 and 208 are formed over the insulating film 203 and the oxide semiconductor film 205, and an insulating film 209 is formed over the oxide semiconductor film 205 and the pair of electrodes 207 and 208. A gate electrode 213 is formed over the insulating film 209. The gate electrode 201 is connected to the gate electrode 213 at an opening (not illustrated) formed in the insulating films 203 and 209.

[0175]

A transistor having Structure 2 in FIG. 7B is a single-gate transistor.

[0176]

In the transistor having Structure 2, the insulating film 203 is formed over the gate electrode 201, and the oxide semiconductor film 205 is formed over the insulating film 203. The pair of electrodes 207 and 208 are formed over the insulating film 203 and the oxide semiconductor film 205, and the insulating film 209 is formed over the oxide semiconductor film 205 and the pair of electrodes 207 and 208.

[0177]

Note that in the calculation, the work function ϕ_M of the gate electrode 201 was set to 5.0 eV. The insulating film 203 was a 100-nm-thick film having a dielectric constant of 4.1. The oxide semiconductor film 205 was a single-layer In-Ga-Zn oxide film (In:Ga:Zn = 1:1:1). The band gap E_g of the In-Ga-Zn oxide film was 3.15 eV, the electron affinity χ was 4.6 eV, the dielectric constant was 15, the electron mobility was $10 \text{ cm}^2/\text{Vs}$, and the donor density N_d was $3 \times 10^{17} \text{ atoms/cm}^3$. The work function ϕ_{sd} of the pair of electrodes 207 and 208 was set to 4.6 eV. Ohmic junction was made between the oxide semiconductor film 205 and each of the pair of electrodes 207 and 208. The insulating film 209 was a 100-nm-thick film having a dielectric constant of 4.1. Note that defect levels, surface scattering, and the like in the oxide semiconductor film 205 were not considered. Further, the channel length and the channel width of the transistor were 10 μm and 100 μm , respectively.

[0178]

<Reduction in variation in initial characteristics>

As in the case of the transistor having Structure 1, by the dual-gate driving, variation in initial characteristics can be reduced. This is because on account of the

dual-gate driving, the amount of change in the threshold voltage V_{th} , which is one of Id-Vg characteristics, of the transistor having Structure 1 can be small as compared to that of the transistor having Structure 2.

[0179]

5 Here, as one example, a negative shift in the threshold voltage of the Id-Vg characteristics that is caused because a semiconductor film becomes n-type is described.

[0180]

10 The sum of the amount of charges of donor ions in the oxide semiconductor film is Q (C), the capacitance formed by the gate electrode 201, the insulating film 203, and the oxide semiconductor film 205 is C_{Bottom} , and the capacitance formed by the oxide semiconductor film 205, the insulating film 209, and the gate electrode 213 is C_{Top} . The amount of change ΔV of the threshold voltage V_{th} of the transistor having Structure 1 in that case is expressed by Formula 1. The amount of change ΔV of the threshold voltage V_{th} of the transistor having Structure 2 in that case is expressed by
15 Formula 2.

[0181]

[Formula 1]

$$\Delta V = -\frac{Q}{C_{Bottom} + C_{Top}}$$

[0182]

20 [Formula 2]

$$\Delta V = -\frac{Q}{C_{Bottom}}$$

[0183]

As expressed by Formula 1, by the dual-gate driving performed in the transistor having Structure 1, the capacitance between donor ions in the oxide semiconductor film
25 and the gate electrode becomes the sum of C_{Bottom} and C_{Top} ; thus, the amount of change in the threshold voltage is small.

[0184]

FIG. 8A shows the calculation results of the current-voltage curves at drain voltages of 0.1 V and 1 V of the transistor having Structure 1. FIG. 8B shows the calculation results of the current-voltage curves at drain voltages of 0.1 V and 1 V of the 5 transistor having Structure 2. When the drain voltage V_d is 0.1 V, the threshold voltage of the transistor having Structure 1 is -2.26 V and the threshold voltage of the transistor having Structure 2 is -4.73 V.

[0185]

As in the case of the transistor having Structure 1, when the dual-gate driving is 10 employed, the amount of change in the threshold voltage can be small. Thus, variation in electrical characteristics among a plurality of transistors can also be small.

[0186]

15 Note that although a negative shift in the threshold voltage due to the donor ions in the oxide semiconductor film is considered here, a positive shift in the threshold voltage due to fixed charges, mobile charges, or negative charges (electrons trapped by acceptor-like states) in the insulating films 203 and 209 is similarly suppressed, which might reduce the variation.

[0187]

<Reduction in degradation due to -GBT stress test>

20 By the dual-gate driving performed in the transistor having Structure 1, degree of degradation due to a -GBT stress test can be low. Some reasons why the degree of degradation due to the -GBT stress test can be low are described below.

[0188]

25 One of the reasons is that electrostatic stress is not caused on account of the dual-gate driving. FIG. 9A is a diagram in which potential contour lines are plotted in the case where -30 V is applied to each of the gate electrodes 201 and 213 in the transistor having Structure 1. FIG. 9B shows potentials at the cross section A-B in FIG. 9A.

[0189]

30 The oxide semiconductor film 205 is an intrinsic semiconductor, and when a negative voltage is applied to the gate electrodes 201 and 213 and the oxide

semiconductor film 205 is fully depleted, no charge exists between the gate electrodes 201 and 213. With this state, when the same potential is supplied to the gate electrodes 201 and 213, as illustrated in FIG. 9B, the potential of the gate electrode 201 becomes completely equal to that of the gate electrode 213. Since the potentials are equal to 5 each other, electrostatic stress is not caused on the insulating film 203, the oxide semiconductor film 205, and the insulating film 209. As a result, phenomena causing degradation due to the -GBT stress test, such as mobile ions and trap and detrap of carriers in the insulating films 203 and 209, do not occur.

[0190]

10 Another reason is that an external electric field of an FET can be blocked in the case of the dual-gate driving. FIG. 10A illustrates a model in which charged particles in the air are adsorbed on the gate electrode 213 in the transistor having Structure 1 illustrated in FIG. 7A. FIG. 10B illustrates a model in which charged particles in the air are adsorbed on the insulating film 209 in the transistor having Structure 2 illustrated 15 in FIG. 7B.

[0191]

20 As illustrated in FIG. 10B, in the transistor having Structure 2, positively charged particles in the air are adsorbed on a surface of the insulating film 209. When a negative voltage is applied to the gate electrode 201, positively charged particles are adsorbed on the insulating film 209. As a result, as indicated by arrows in FIG. 10B, an electric field of the positively charged particles reaches the interface of the oxide semiconductor film 205 with the insulating film 209, so that a state similar to the state when a positive bias is applied is brought about. As a result, the threshold voltage 25 might shift in the negative direction.

[0192]

30 In contrast, even if positively charged particles are adsorbed on a surface of the gate electrode 213 in the transistor having Structure 1 illustrated in FIG. 10A, as indicated by arrows in FIG. 10A, the gate electrode 213 blocks the electric field of the positively charged particles; thus, the positively charged particles do not affect the electrical characteristics of the transistor. In sum, the transistor can be electrically protected against external charges by the gate electrode 213, leading to suppression of

the degradation due to the -GBT stress test.

[0193]

For the above two reasons, in the transistor operated by the dual-gate driving, the degradation due to the -GBT stress test can be suppressed.

5 [0194]

<Suppression of changes in rising voltages of on-state current at different drain voltages>

Here, in the case of Structure 2, changes in the rising voltages of on-state current at different drain voltages and a cause of the changes are described.

10 [0195]

In a transistor illustrated in FIGS. 11A to 11C, a gate insulating film 233 is provided over a gate electrode 231, and an oxide semiconductor film 235 is provided over the gate insulating film 233. A pair of electrodes 237 and 238 are provided over the oxide semiconductor film 235, and an insulating film 239 is provided over the gate insulating film 233, the oxide semiconductor film 235, and the pair of electrodes 237 and 238.

15 [0196]

Note that in the calculation, the work function ϕ_M of the gate electrode 231 was set to 5.0 eV. The gate insulating film 233 had a stacked-layer structure including a 400-nm-thick film having a dielectric constant of 7.5 and a 50-nm-thick film having a dielectric constant of 4.1. The oxide semiconductor film 235 was a single-layer In-Ga-Zn oxide film (In:Ga:Zn = 1:1:1). The band gap E_g of the In-Ga-Zn oxide film was 3.15 eV, the electron affinity χ was 4.6 eV, the dielectric constant was 15, the electron mobility was 10 cm²/Vs, and the donor density N_d was 1 × 10¹³/cm³. The work function ϕ_{sd} of the pair of electrodes 237 and 238 was set to 4.6 eV. Ohmic junction was made between the oxide semiconductor film 235 and each of the pair of electrodes 207 and 208. The insulating film 239 was a 550-nm-thick film having a dielectric constant of 3.9. Note that defect levels, surface scattering, and the like in the oxide semiconductor film 235 were not considered. Further, the channel length and the channel width of the transistor were 3 μm and 50 μm, respectively.

20 [0197]

Next, models of a transistor illustrated in FIG. 11A in which positively charged particles are adsorbed on a surface of the insulating film 239 are illustrated in FIGS. 11B and 11C. FIG. 11B illustrates an assumed structure in which positive fixed charges are uniformly adsorbed on the surface of the insulating film 239. FIG. 11C illustrates an assumed structure in which positive fixed charges are partly adsorbed on the surface of the insulating film 239.

[0198]

Calculation results of the electrical characteristics of the transistors illustrated in FIGS. 11A to 11C are shown in FIGS. 12A to 12C, respectively.

10 [0199]

In the case where it is assumed that no positive fixed charge is adsorbed on the insulating film 239 in the transistor illustrated in FIG. 11A, the rising voltage at a drain voltage V_d of 1 V approximately corresponds to that at a drain voltage V_d of 10 V as shown in FIG. 12A.

15 [0200]

In contrast, in the case where it is assumed that positive fixed charges are uniformly adsorbed on the insulating film 239 in the transistor illustrated in FIG. 11B, the threshold voltages shift in the negative direction and the rising voltage at a drain voltage V_d of 1 V approximately corresponds to that at a drain voltage V_d of 10 V as shown in FIG. 12B.

[0201]

20 In the case where it is assumed that positive fixed charges are partly adsorbed on the insulating film 239 in the transistor illustrated in FIG. 11C, the rising voltage at a drain voltage V_d of 1 V is different from that at a drain voltage V_d of 10 V as shown in FIG. 12C.

[0202]

25 Since the gate electrode 213 is provided in the transistor having Structure 1, as described in <Reduction in degradation due to -GBT stress test>, the gate electrode 213 blocks the electric field of external charged particles; thus, the charged particles do not affect the electrical characteristics of the transistor. In other words, the transistor can be electrically protected against external charges by the gate electrode 213, and changes in the rising voltages of on-state current at different drain voltages can be suppressed.

[0203]

As described above, in the case where a dual-gate structure is employed and a given voltage is given to each gate electrode, degradation due to a -GBT stress test and changes in the rising voltages of on-state current at different drain voltages can be suppressed. Moreover, in the case where a dual-gate structure is employed and voltages having the same potential are given to each gate electrode, variation in initial characteristics can be reduced, degradation due to a -GBT stress test can be suppressed, and changes in the rising voltages of on-state current at different drain voltages can be suppressed.

10 [0204]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0205]

15 (Embodiment 4)

In any of the transistors described in Embodiments 1 to 3, a base insulating film can be provided between the substrate 11 and the gate electrode 15 as necessary. As a material of the base insulating film, silicon oxide, silicon oxynitride, silicon nitride, silicon nitride oxide, gallium oxide, hafnium oxide, yttrium oxide, aluminum oxide, 20 aluminum oxynitride, and the like can be given as examples. Note that when silicon nitride, gallium oxide, hafnium oxide, yttrium oxide, aluminum oxide, or the like is used as a material of the base insulating film, it is possible to suppress diffusion of impurities such as alkali metal, water, and hydrogen into the oxide semiconductor film 19 from the substrate 11.

25 [0206]

The base insulating film can be formed by a sputtering method, a CVD method, or the like.

[0207]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0208]

(Embodiment 5)

In any of the transistors described in Embodiments 1 to 4, the gate insulating film 17 can have a stacked-layer structure as necessary. Here, structures of the gate insulating film 17 are described using the transistor 50 described in Embodiment 1 with reference to FIGS. 13A to 13C.

[0209]

As illustrated in FIG. 13A, the gate insulating film 17 can have a stacked-layer structure in which a nitride insulating film 17a and an oxide insulating film 17b are stacked in this order from the gate electrode 15 side. When the nitride insulating film 17a is provided over the gate electrode 15, an impurity, typically hydrogen, nitrogen, alkali metal, alkaline earth metal, or the like, can be prevented from moving from the gate electrode 15 to the oxide semiconductor film 19.

[0210]

Further, when the oxide insulating film 17b is provided on the oxide semiconductor film 19 side, density of defect states at the interface between the gate insulating film 17 and the oxide semiconductor film 19 can be reduced. Consequently, a transistor whose electrical characteristics are hardly degraded can be obtained. It is preferable to form, as the oxide insulating film 17b, an oxide insulating film containing a higher proportion of oxygen than that of oxygen in the stoichiometric composition like the oxide insulating film 25. This is because density of defect states at the interface between the gate insulating film 17 and the oxide semiconductor film 19 can be further reduced.

[0211]

As illustrated in FIG. 13B, the gate insulating film 17 can have a stacked-layer structure in which a nitride insulating film 17c with few defects, a nitride insulating film 17d with a high blocking property against hydrogen, and the oxide insulating film 17b are stacked in this order from the gate electrode 15 side. When the nitride insulating film 17c with few defects is provided in the gate insulating film 17, the withstand voltage of the gate insulating film 17 can be improved. Further, when the nitride insulating film 17d with a high blocking property against hydrogen is provided, hydrogen can be prevented from moving from the gate electrode 15 and the nitride

insulating film 17c to the oxide semiconductor film 19.

[0212]

An example of a method for forming the nitride insulating films 17c and 17d illustrated in FIG. 13B is described below. First, as the nitride insulating film 17c, a silicon nitride film with few defects is formed by a plasma CVD method in which a mixed gas of silane, nitrogen, and ammonia is used as a source gas. Then, as the nitride insulating film 17d, a silicon nitride film in which the hydrogen concentration is low and hydrogen can be blocked is formed by switching the source gas to a mixed gas of silane and nitrogen. By such a formation method, the gate insulating film 17 having a stacked-layer structure of nitride insulating films with few defects and a blocking property against hydrogen can be formed.

[0213]

As illustrated in FIG. 13C, the gate insulating film 17 can have a stacked-layer structure in which a nitride insulating film 17e with a high blocking property against an impurity, the nitride insulating film 17c with few defects, the nitride insulating film 17d with a high blocking property against hydrogen, and the oxide insulating film 17b are stacked in this order from the gate electrode 15 side. When the nitride insulating film 17e with a high blocking property against an impurity is provided in the gate insulating film 17, an impurity, typically hydrogen, nitrogen, alkali metal, alkaline earth metal, or the like, can be prevented from moving from the gate electrode 15 to the oxide semiconductor film 19.

[0214]

An example of a method for forming the nitride insulating films 17e, 17c, and 17d illustrated in FIG. 13C is described below. First, as the nitride insulating film 17e, a silicon nitride film with a high blocking property against an impurity is formed by a plasma CVD method in which a mixed gas of silane, nitrogen, and ammonia is used as a source gas. Then, a silicon nitride film with few defects is formed as the nitride insulating film 17c by increasing the flow rate of ammonia. Then, as the nitride insulating film 17d, a silicon nitride film in which the hydrogen concentration is low and hydrogen can be blocked is formed by switching the source gas to a mixed gas of silane and nitrogen. By such a formation method, the gate insulating film 17 having a stacked-layer structure of nitride insulating films with few defects and a blocking

property against an impurity can be formed.

[0215]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0216]

(Embodiment 6)

As for the pair of electrodes 20 and 21 provided in any of the transistors described in Embodiments 1 to 5, it is possible to use a conductive material that is easily bonded to oxygen, such as tungsten, titanium, aluminum, copper, molybdenum, chromium, or tantalum, or an alloy thereof. Thus, oxygen contained in the oxide semiconductor film 19 and the conductive material contained in the pair of electrodes 20 and 21 are bonded to each other, so that an oxygen vacancy region is formed in the oxide semiconductor film 19. Further, in some cases, part of constituent elements of the conductive material that forms the pair of electrodes 20 and 21 is mixed into the oxide semiconductor film 19. Consequently, as illustrated in FIG. 14, low-resistance regions 19a and 19b are formed in the vicinity of regions of the oxide semiconductor film 19 that are in contact with the pair of electrodes 20 and 21. The low-resistance regions 19a and 19b are formed between the gate insulating film 17 and the pair of electrodes 20 and 21 so as to be in contact with the pair of electrodes 20 and 21. Since the low-resistance regions 19a and 19b have high conductivity, contact resistance between the oxide semiconductor film 19 and the pair of electrodes 20 and 21 can be reduced, and thus, the on-state current of the transistor can be increased.

[0217]

Further, the pair of electrodes 20 and 21 may each have a stacked-layer structure of the conductive material which is easily bonded to oxygen and a conductive material which is not easily bonded to oxygen, such as titanium nitride, tantalum nitride, or ruthenium. With such a stacked-layer structure, oxidization of the pair of electrodes 20 and 21 can be prevented at the interface between the pair of electrodes 20 and 21 and the oxide insulating film 23, so that the increase of the resistance of the pair of electrodes 20 and 21 can be inhibited.

[0218]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0219]

5 (Embodiment 7)

In this embodiment, a semiconductor device having a transistor in which the number of defects in an oxide semiconductor film can be further reduced as compared to Embodiments 1 to 6 is described with reference to drawings. The transistor described in this embodiment is different from any of the transistors in Embodiments 1 to 6 in that a multilayer film in which oxide semiconductor films are stacked is provided. Here, details of the transistor are described with reference to Embodiment 1.

[0220]

FIGS. 15A to 15D are a top view and cross-sectional views of a transistor 70 included in the semiconductor device. FIG. 15A is a top view of the transistor 70, FIG. 15B is a cross-sectional view taken along dashed line A-B of FIG. 15A, and FIG. 15C is a cross-sectional view taken along dashed line C-D of FIG. 15A. Note that in FIG. 15A, the substrate 11, the gate insulating film 17, the oxide insulating film 23, the oxide insulating film 25, the nitride insulating film 27, and the like are omitted for simplicity.

[0221]

20 The transistor 70 illustrated in FIG. 15A to 15C includes the gate electrode 15 over the substrate 11; the gate insulating film 17; a multilayer film 47 overlapping with the gate electrode 15 with the gate insulating film 17 positioned therebetween; the pair of electrodes 20 and 21 in contact with the multilayer film 47; the gate insulating film 28 over the gate insulating film 17, the multilayer film 47, and the pair of electrodes 20 and 21; and the gate electrode 29 over the gate insulating film 28 and the gate insulating film 17. Further, the gate insulating film 28 includes the oxide insulating film 23, the oxide insulating film 25, and the nitride insulating film 27. Furthermore, the electrode 30 connected to one of the pair of electrodes 20 and 21 (here, the electrode 21) is formed over the gate insulating film 17. Note that the electrode 30 serves as a pixel electrode.

[0222]

In the transistor 70 described in this embodiment, the multilayer film 47

includes the oxide semiconductor film 19 and an oxide semiconductor film 49a. That is, the multilayer film 47 has a two-layer structure. Further, part of the oxide semiconductor film 19 serves as a channel region. Furthermore, the oxide insulating film 23 is formed in contact with the multilayer film 47. The oxide semiconductor film 49a is provided between the oxide semiconductor film 19 and the oxide insulating film 23. The oxide insulating film 25 is formed in contact with the oxide insulating film 23.

[0223]

The oxide semiconductor film 49a is an oxide film containing one or more elements that form the oxide semiconductor film 19. Thus, interface scattering is unlikely to occur at the interface between the oxide semiconductor films 19 and 49a. Thus, the transistor can have a high field-effect mobility because the movement of carriers is not hindered at the interface.

[0224]

The oxide semiconductor film 49a is typically an In-Ga oxide film, an In-Zn oxide film, or an In-M-Zn oxide film (M represents Al, Ga, Y, Zr, La, Ce, or Nd). The energy at the conduction band bottom of the oxide semiconductor film 49a is closer to a vacuum level than that of the oxide semiconductor film 19 is, and typically, the difference between the energy at the conduction band bottom of the oxide semiconductor film 49a and the energy at the conduction band bottom of the oxide semiconductor film 19 is any one of 0.05 eV or more, 0.07 eV or more, 0.1 eV or more, or 0.15 eV or more, and any one of 2 eV or less, 1 eV or less, 0.5 eV or less, or 0.4 eV or less. That is, the difference between the electron affinity of the oxide semiconductor film 49a and the electron affinity of the oxide semiconductor film 19 is any one of 0.05 eV or more, 0.07 eV or more, 0.1 eV or more, or 0.15 eV or more, and any one of 2 eV or less, 1 eV or less, 0.5 eV or less, or 0.4 eV or less.

[0225]

The oxide semiconductor film 49a preferably contains In because carrier mobility (electron mobility) can be increased.

[0226]

When the oxide semiconductor film 49a contains a larger amount of Al, Ga, Y, Zr, La, Ce, or Nd in an atomic ratio than the amount of In in an atomic ratio, any of the

following effects may be obtained: (1) the energy gap of the oxide semiconductor film 49a is widened; (2) the electron affinity of the oxide semiconductor film 49a decreases; (3) an impurity from the outside is blocked; (4) an insulating property of the oxide semiconductor film 49a increases as compared to that of the oxide semiconductor film 19; and (5) oxygen vacancies are less likely to be generated because Al, Ga, Y, Zr, La, Ce, or Nd is a metal element that is strongly bonded to oxygen.

[0227]

In the case where the oxide semiconductor film 49a is an In-M-Zn oxide film, the proportions of In and M when summation of In and M is assumed to be 100 atomic% are as follows: the atomic percentage of In is less than 50 atomic% and the atomic percentage of M is greater than or equal to 50 atomic%; or the atomic percentage of In is less than 25 atomic% and the atomic percentage of M is greater than or equal to 75 atomic%.

[0228]

Further, in the case where each of the oxide semiconductor films 19 and 49a is an In-M-Zn oxide film (M represents Al, Ga, Y, Zr, La, Ce, or Nd), the proportion of M atoms (M represents Al, Ga, Y, Zr, La, Ce, or Nd) in the oxide semiconductor film 49a is higher than that in the oxide semiconductor film 19. Typically, the proportion of M in the oxide semiconductor film 49a is 1.5 or more times, twice or more, or three or more times as high as that in the oxide semiconductor film 19.

[0229]

Furthermore, in the case where each of the oxide semiconductor films 19 and 49a is an In-M-Zn-based oxide film (M represents Al, Ga, Y, Zr, La, Ce, or Nd), when $\text{In:Zn} = x_1:y_1:z_1$ [atomic ratio] is satisfied in the oxide semiconductor film 49a and $\text{In:Zn} = x_2:y_2:z_2$ [atomic ratio] is satisfied in the oxide semiconductor film 19, y_1/x_1 is higher than y_2/x_2 , or y_1/x_1 be 1.5 or more times as high as y_2/x_2 . Alternatively, y_1/x_1 be twice or more as high as y_2/x_2 . Further alternatively, y_1/x_1 be three or more times as high as y_2/x_2 . In this case, it is preferable that in the oxide semiconductor film, y_2 be higher than or equal to x_2 because a transistor including the oxide semiconductor film can have stable electrical characteristics.

[0230]

In the case where the oxide semiconductor film 19 is an In-M-Zn oxide film (M is Al, Ga, Y, Zr, La, Ce, or Nd) and a target having the atomic ratio of metal elements of $\text{In:}M\text{:Zn} = x_1:y_1:z_1$ is used for forming the oxide semiconductor film 19, x_1/y_1 is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6, and z_1/y_1 is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. Note that when z_1/y_1 is greater than or equal to 1 and less than or equal to 6, a CAAC-OS film to be described later as the oxide semiconductor film 19 is easily formed. Typical examples of the atomic ratio of the metal elements of the target are $\text{In:}M\text{:Zn} = 1:1:1$, $\text{In:}M\text{:Zn} = 1:1:1.2$, and $\text{In:}M\text{:Zn} = 3:1:2$.

[0231]

In the case where the oxide semiconductor film 49a is an In-M-Zn oxide film (M is Al, Ga, Y, Zr, La, Ce, or Nd) and a target having the atomic ratio of metal elements of $\text{In:}M\text{:Zn} = x_2:y_2:z_2$ is used for forming the oxide semiconductor film 49a, x_2/y_2 is preferably less than x_1/y_1 , and z_2/y_2 is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. Note that when z_2/y_2 is greater than or equal to 1 and less than or equal to 6, a CAAC-OS film to be described later as the oxide semiconductor film 49a is easily formed. Typical examples of the atomic ratio of the metal elements of the target are $\text{In:}M\text{:Zn} = 1:3:2$, $\text{In:}M\text{:Zn} = 1:3:4$, $\text{In:}M\text{:Zn} = 1:3:6$, $\text{In:}M\text{:Zn} = 1:3:8$, and the like.

[0232]

Note that a proportion of each atom in the atomic ratio of the oxide semiconductor films 19 and 49a varies within a range of $\pm 40\%$ as an error.

25 [0233]

The oxide semiconductor film 49a also serves as a film that relieves damage to the oxide semiconductor film 19 at the time of forming the oxide insulating film 25 later.

[0234]

30 The thickness of the oxide semiconductor film 49a is greater than or equal to 3 nm and less than or equal to 100 nm, or greater than or equal to 3 nm and less than or

equal to 50 nm.

[0235]

The oxide semiconductor film 49a may have a non-single-crystal structure, for example, like the oxide semiconductor film 19. The non-single crystal structure 5 includes a CAAC-OS that is described later, a polycrystalline structure, a microcrystalline structure described later, or an amorphous structure, for example.

[0236]

The oxide semiconductor film 49a may have an amorphous structure, for example. An amorphous oxide semiconductor film, for example, has disordered 10 atomic arrangement and no crystalline component. Alternatively, an amorphous oxide film is, for example, absolutely amorphous and has no crystal part.

[0237]

Note that the oxide semiconductor films 19 and 49a may each be a mixed film including two or more of the following: a region having an amorphous structure, a 15 region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure. The mixed film has a single-layer structure including, for example, two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal 20 structure in some cases. Further, in some cases, the mixed film has a stacked-layer structure in which two or more of the following regions are stacked: a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure.

25 [0238]

Here, the oxide semiconductor film 49a is provided between the oxide semiconductor film 19 and the oxide insulating film 23. Hence, if trap states are formed between the oxide semiconductor film 49a and the oxide insulating film 23 owing to impurities and defects, electrons flowing in the oxide semiconductor film 19 30 are less likely to be captured by the trap states because there is a distance between the trap states and the oxide semiconductor film 19. Accordingly, the amount of on-state current of the transistor can be increased, and the field-effect mobility can be increased.

When the electrons are captured by the trap states, the electrons become negative fixed charges. As a result, a threshold voltage of the transistor varies. However, by the distance between the oxide semiconductor film 19 and the trap states, capture of the electrons by the trap states can be reduced, and accordingly change in the threshold 5 voltage can be reduced.

[0239]

Impurities from the outside can be blocked by the oxide semiconductor film 49a, and accordingly, the amount of impurities that are transferred from the outside to the oxide semiconductor film 19 can be reduced. Further, an oxygen vacancy is less 10 likely to be formed in the oxide semiconductor film 49a. Consequently, the impurity concentration and the number of oxygen vacancies in the oxide semiconductor film 19 can be reduced.

[0240]

Note that the oxide semiconductor films 19 and 49a are not formed by simply 15 stacking each film, but are formed to form a continuous junction (here, in particular, a structure in which the energy of the bottom of the conduction band is changed continuously between each film). In other words, a stacked-layer structure in which there exist no impurity that forms a defect level such as a trap center or a recombination center at each interface is provided. If an impurity exists between the oxide 20 semiconductor films 19 and 49a that are stacked, a continuity of the energy band is damaged, and the carrier is captured or recombined at the interface and then disappears.

[0241]

In order to form such a continuous energy band, it is necessary to form films 25 continuously without being exposed to the air, with use of a multi-chamber deposition apparatus (sputtering apparatus) including a load lock chamber. Each chamber in the sputtering apparatus is preferably evacuated to be a high vacuum state (to the degree of about 5×10^{-7} Pa to 1×10^{-4} Pa) with an adsorption vacuum evacuation pump such as a cryopump in order to remove water or the like, which serves as an impurity against the oxide semiconductor film, as much as possible. Alternatively, a turbo molecular pump 30 and a cold trap are preferably combined so as to prevent a backflow of a gas, especially a gas containing carbon or hydrogen from an exhaust system to the inside of the chamber.

[0242]

As in a transistor 71 illustrated in FIG. 15D, a multilayer film 48 overlapping with the gate electrode 15 with the gate insulating film 17 provided therebetween, and the pair of electrodes 20 and 21 in contact with the multilayer film 48 may be included.

5 [0243]

The multilayer film 48 includes an oxide semiconductor film 49b, the oxide semiconductor film 19, and the oxide semiconductor film 49a. That is, the multilayer film 48 has a three-layer structure. The oxide semiconductor film 19 serves as a channel region.

10 [0244]

Further, the gate insulating film 17 and the oxide semiconductor film 49b are in contact with each other. That is, the oxide semiconductor film 49b is provided between the gate insulating film 17 and the oxide semiconductor film 19.

[0245]

15 The multilayer film 48 and the oxide insulating film 23 are in contact with each other. The oxide semiconductor film 49a and the oxide insulating film 23 are in contact with each other. That is, the oxide semiconductor film 49a is provided between the oxide semiconductor film 19 and the oxide insulating film 23.

[0246]

20 The oxide semiconductor film 49b can be formed using a material and a formation method similar to those of the oxide semiconductor film 49a.

[0247]

25 It is preferable that the thickness of the oxide semiconductor film 49b be smaller than that of the oxide semiconductor film 19. When the thickness of the oxide semiconductor film 49b is greater than or equal to 1 nm and less than or equal to 5 nm, preferably greater than or equal to 1 nm and less than or equal to 3 nm, the amount of change in threshold voltage of the transistor can be reduced.

[0248]

30 In the transistor described in this embodiment, the oxide semiconductor film 49a is provided between the oxide semiconductor film 19 and the oxide insulating film 23. Hence, if trap states are formed between the oxide semiconductor film 49a and the oxide insulating film 23 owing to impurities and defects, electrons flowing in the oxide

semiconductor film 19 are less likely to be captured by the trap states because there is a distance between the trap states and the oxide semiconductor film 19. Accordingly, the amount of on-state current of the transistor can be increased, and the field-effect mobility can be increased. When the electrons are captured by the trap states, the 5 electrons become negative fixed charges. As a result, a threshold voltage of the transistor varies. However, by the distance between the oxide semiconductor film 19 and the trap states, capture of the electrons by the trap states can be reduced, and accordingly change in the threshold voltage can be reduced.

[0249]

10 Impurities from the outside can be blocked by the oxide semiconductor film 49a, and accordingly, the amount of impurities that are transferred from the outside to the oxide semiconductor film 19 can be reduced. Further, an oxygen vacancy is less likely to be formed in the oxide semiconductor film 49a. Consequently, the impurity concentration and the number of oxygen vacancies in the oxide semiconductor film 19 15 can be reduced.

[0250]

Further, the oxide semiconductor film 49b is provided between the gate insulating film 17 and the oxide semiconductor film 19, and the oxide semiconductor film 49a is provided between the oxide semiconductor film 19 and the oxide insulating film 23. Thus, it is possible to reduce the concentration of silicon or carbon in the 20 vicinity of the interface between the oxide semiconductor film 49b and the oxide semiconductor film 19, the concentration of silicon or carbon in the oxide semiconductor film 19, or the concentration of silicon or carbon in the vicinity of the interface between the oxide semiconductor film 49a and the oxide semiconductor film 25 19. Consequently, in the multilayer film 48, the absorption coefficient derived from a constant photocurrent method is lower than $1 \times 10^{-3} /cm$ or lower than $1 \times 10^{-4} /cm$, and thus density of localized levels is extremely low.

[0251]

A transistor 71 having such a structure includes very few defects in the 30 multilayer film 48 including the oxide semiconductor film 19, thus, the electrical characteristics of the transistor can be improved, and typically, the on-state current can be increased and the field-effect mobility can be improved. Further, in a BT stress test

and a BT photostress test that are examples of a stress test, the amount of change in threshold voltage is small, and thus, reliability is high.

[0252]

<Band structure of transistor>

5 Next, band structures of the multilayer film 47 provided in the transistor 70 illustrated in FIG. 15B and the multilayer film 48 provided in the transistor 71 illustrated in FIG. 15C are described with reference to FIGS. 16A to 16C.

[0253]

10 Here, for example, In-Ga-Zn oxide having an energy gap of 3.15 eV is used as the oxide semiconductor film 19, and In-Ga-Zn oxide having an energy gap of 3.5 eV is used as the oxide semiconductor film 49a. The energy gaps can be measured using a spectroscopic ellipsometer (UT-300 manufactured by HORIBA JOBIN YVON SAS.).

[0254]

15 The energy difference between the vacuum level and the top of the valence band (also called ionization potential) of the oxide semiconductor film 19 and the energy difference between the vacuum level and the top of the valence band of the oxide semiconductor film 49a were 8 eV and 8.2 eV, respectively. Note that the energy difference between the vacuum level and the valence band top can be measured using an ultraviolet photoelectron spectroscopy (UPS) device (VersaProbe manufactured by 20 ULVAC-PHI, Inc.).

[0255]

25 Thus, the energy difference between the vacuum level and the bottom of the conduction band (also called electron affinity) of the oxide semiconductor film 19 and the energy gap therebetween of the oxide semiconductor film 49a were 4.85 eV and 4.7 eV, respectively.

[0256]

FIG. 16A schematically illustrates a part of the band structure of the multilayer film 47. Here, the case where a silicon oxide film is provided in contact with the multilayer film 47 is described. In FIG. 16A, E_{CI1} denotes the energy of the bottom of the conduction band in the silicon oxide film; E_{CS1} denotes the energy of the bottom of the conduction band in the oxide semiconductor film 19; E_{CS2} denotes the energy of the bottom of the conduction band in the oxide semiconductor film 49a; and E_{CI2} denotes

the energy of the bottom of the conduction band in the silicon oxide film. Further, EcI1 and EcI2 correspond to the gate insulating film 17 and the oxide insulating film 23 in FIG. 15B, respectively.

[0257]

5 As illustrated in FIG. 16A, there is no energy barrier between the oxide semiconductor films 19 and 49a, and the energy level of the bottom of the conduction band gradually changes therebetween. In other words, the energy level of the bottom of the conduction band is continuously changed. This is because the multilayer film 10 47 contains an element contained in the oxide semiconductor film 19 and oxygen is transferred between the oxide semiconductor films 19 and 49a, so that a mixed layer is formed.

[0258]

15 As shown in FIG. 16A, the oxide semiconductor film 19 in the multilayer film 47 serves as a well and a channel region of the transistor including the multilayer film 47 is formed in the oxide semiconductor film 19. Note that since the energy of the bottom of the conduction band of the multilayer film 47 is continuously changed, it can be said that the oxide semiconductor films 19 and 49a are continuous.

[0259]

20 Although trap states due to impurities or defects might be formed in the vicinity of the interface between the oxide semiconductor film 49a and the oxide insulating film 23 as shown in FIG. 16A, the oxide semiconductor film 19 can be distanced from the trap states owing to the existence of the oxide semiconductor film 49a. However, when the energy difference between EcS1 and EcS2 is small, an 25 electron in the oxide semiconductor film 19 might reach the trap state across the energy difference. When the electron is captured by the trap state, a negative fixed charge is generated at the interface with the oxide insulating film, whereby the threshold voltage of the transistor shifts in the positive direction. Therefore, it is preferable that the 30 energy difference between EcS1 and EcS2 be 0.1 eV or more, more preferably 0.15 eV or more, because change in the threshold voltage of the transistor is reduced and stable electrical characteristics are obtained.

[0260]

FIG. 16B schematically illustrates a part of the band structure of the multilayer

film 47, which is a variation of the band structure shown in FIG. 16A. Here, a structure where silicon oxide films are provided in contact with the multilayer film 47 is described. In FIG. 16B, EcI1 denotes the energy of the bottom of the conduction band in the silicon oxide film; EcS1 denotes the energy of the bottom of the conduction band in the oxide semiconductor film 19; and EcI2 denotes the energy of the bottom of the conduction band in the silicon oxide film. Further, EcI1 and EcI2 correspond to the gate insulating film 17 and the oxide insulating film 23 in FIG. 15B, respectively.

[0261]

In the transistor illustrated in FIG. 15B, an upper portion of the multilayer film 47, that is, the oxide semiconductor film 49a might be etched in formation of the pair of electrodes 20 and 21. Further, a mixed layer of the oxide semiconductor films 19 and 49a is likely to be formed on the top surface of the oxide semiconductor film 19 in formation of the oxide semiconductor film 49a.

[0262]

For example, when the oxide semiconductor film 19 is an oxide semiconductor film formed with use of, as a sputtering target, In-Ga-Zn oxide whose atomic ratio of In to Ga and Zn is 1:1:1 or In-Ga-Zn oxide whose atomic ratio of In to Ga and Zn is 3:1:2, and the oxide semiconductor film 49a is an oxide semiconductor film formed with use of, as a sputtering target, In-Ga-Zn oxide whose atomic ratio of In to Ga and Zn is 1:3:2, In-Ga-Zn oxide whose atomic ratio of In to Ga and Zn is 1:3:4, or In-Ga-Zn oxide whose atomic ratio of In to Ga and Zn is 1:3:6, the Ga content in oxide semiconductor film 49a is higher than that in the oxide semiconductor film 19. Thus, a GaOx layer or a mixed layer whose Ga content is higher than that in the oxide semiconductor film 19 can be formed on the top surface of the oxide semiconductor film 19.

[0263]

For that reason, even in the case where oxide semiconductor film 49a is etched, the energy of the bottom of the conduction band of EcS1 on the EcI2 side is increased and the band structure shown in FIG. 16B can be obtained in some cases.

[0264]

As in the band structure shown in FIG. 16B, in observation of a cross section of a channel region, only the oxide semiconductor film 19 in the multilayer film 47 is apparently observed in some cases. However, a mixed layer that contains Ga more

than the oxide semiconductor film 19 does is formed over the oxide semiconductor film 19 in fact, and thus the mixed layer can be regarded as a 1.5-th layer. Note that the mixed layer can be confirmed by analyzing a composition in the upper portion of the oxide semiconductor film 19, when the elements contained in the multilayer film 47 are measured by an EDX analysis, for example. The mixed layer can be confirmed, for example, in such a manner that the Ga content in the composition in the upper portion of the oxide semiconductor film 19 is larger than the Ga content in the oxide semiconductor film 19.

[0265]

FIG. 16C schematically illustrates a part of the band structure of the multilayer film 48. Here, the case where silicon oxide films are provided in contact with the multilayer film 48 is described. In FIG. 16C, EcI1 denotes the energy of the bottom of the conduction band in the silicon oxide film; EcS1 denotes the energy of the bottom of the conduction band in the oxide semiconductor film 19; EcS2 denotes the energy of the bottom of the conduction oxide semiconductor film 49a; EcS3 denotes the energy of the bottom of the conduction oxide semiconductor film 49b; and EcI2 denotes the energy of the bottom of the conduction band in the silicon oxide film. Further, EcI1 and EcI2 correspond to the gate insulating film 17 and the oxide insulating film 23 in FIG. 15D, respectively.

[0266]

As illustrated in FIG. 16C, there is no energy barrier between the oxide semiconductor films 49b, 19, and 49a, and the energy level of the bottom of the conduction band gradually changes therebetween. In other words, the energy level of the bottom of the conduction band is continuously changed. This is because the multilayer film 48 contains an element contained in the oxide semiconductor film 19 and oxygen is transferred between the oxide semiconductor films 19 and 49b and between the oxide semiconductor films 19 and 49a, so that a mixed layer is formed.

[0267]

As shown in FIG. 16C, the oxide semiconductor film 19 in the multilayer film 48 serves as a well and a channel region of the transistor including the multilayer film 48 is formed in the oxide semiconductor film 19. Note that since the energy of the bottom of the conduction band of the multilayer film 48 is continuously changed, it can

be said that the oxide semiconductor films 49b, 19, and 49a are continuous.

[0268]

Although trap states due to impurities or defects might be formed in the vicinity of the interface between the oxide semiconductor film 19 and the oxide insulating film 23 and in the vicinity of the interface between the oxide semiconductor film 19 and the gate insulating film 17, as illustrated in FIG. 16C, the oxide semiconductor film 19 can be distanced from the trap states owing to the existence of the oxide semiconductor films 49a and 49b. However, when the energy difference between EcS1 and EcS2 and the energy difference between EcS1 and EcS3 are small, electrons in the oxide semiconductor film 19 might reach the trap state across the energy difference. When the electrons are captured by the trap state, a negative fixed charge is generated at the interface with the oxide insulating film, whereby the threshold voltage of the transistor shifts in the positive direction. Therefore, it is preferable that the energy difference between EcS1 and EcS2 and the energy difference between EcS1 and EcS3 be 0.1 eV or more, more preferably 0.15 eV or more, because change in the threshold voltage of the transistor is reduced and stable electrical characteristics are obtained.

[0269]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0270]

(Embodiment 8)

In this embodiment, one embodiment that can be applied to an oxide semiconductor film in the transistor included in the semiconductor device described in the above embodiment is described.

[0271]

The oxide semiconductor film may include one or more of the following: an oxide semiconductor having a single-crystal structure (hereinafter referred to as a single-crystal oxide semiconductor); an oxide semiconductor having a polycrystalline structure (hereinafter referred to as a polycrystalline oxide semiconductor); an oxide semiconductor having a microcrystalline structure (hereinafter referred to as a

microcrystalline oxide semiconductor), and an oxide semiconductor having an amorphous structure (hereinafter referred to as an amorphous oxide semiconductor). Further, the oxide semiconductor film may be formed of a CAAC-OS film. Furthermore, the oxide semiconductor film may include an amorphous oxide semiconductor and an oxide semiconductor having a crystal grain. Described below are the single-crystal oxide semiconductor, the CAAC-OS, the polycrystalline oxide semiconductor, the microcrystalline oxide semiconductor, and the amorphous oxide semiconductor.

[0272]

10 <Single crystal oxide semiconductor>

The single-crystal oxide semiconductor film has a lower impurity concentration and a lower density of defect states (few oxygen vacancies). Thus, the carrier density can be decreased. Accordingly, a transistor including the single-crystal oxide semiconductor film is unlikely to be normally on. Moreover, since the single-crystal oxide semiconductor film has a lower impurity concentration and a lower density of defect states, carrier traps might be reduced. Thus, the transistor including the single-crystal oxide semiconductor film has small variation in electrical characteristics and accordingly has high reliability.

[0273]

20 Note that when the oxide semiconductor film has few defects, the density thereof is increased. When the oxide semiconductor film has high crystallinity, the density thereof is increased. When the oxide semiconductor film has a lower concentration of impurities such as hydrogen, the density thereof is increased. The single-crystal oxide semiconductor film has a higher density than the CAAC-OS film.

25 The CAAC-OS film has a higher density than the microcrystalline oxide semiconductor film. The polycrystalline oxide semiconductor film has a higher density than the microcrystalline oxide semiconductor film. The microcrystalline oxide semiconductor film has a higher density than the amorphous oxide semiconductor film.

[0274]

30 <CAAC-OS>

The CAAC-OS film is one of oxide semiconductor films having a plurality of crystal parts. The crystal parts included in the CAAC-OS film each have c-axis

alignment. In a plan TEM image, the area of the crystal parts included in the CAAC-OS film is greater than or equal to 2500 nm^2 , greater than or equal to $5\text{ }\mu\text{m}^2$, or greater than or equal to $1000\mu\text{m}^2$. Further, in a cross-sectional TEM image, when the proportion of the crystal parts is greater than or equal to 50 %, greater than or equal to 5 80 %, or greater than or equal to 95 % of the CAAC oxide film, the CAAC oxide film is a thin film having physical properties similar to those of a single crystal.

[0275]

In a transmission electron microscope (TEM) image of the CAAC-OS film, a boundary between crystal parts, that is, a grain boundary is not clearly observed. Thus, 10 in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0276]

According to the TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are 15 arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology reflected by a surface over which the CAAC-OS film is formed (hereinafter, a surface over which the CAAC-OS film is formed is referred to as a formation surface) or the top surface of the CAAC-OS film, and is arranged in parallel to the formation surface or the top surface of the CAAC-OS film. In this specification, a term 20 "parallel" indicates that the angle formed between two straight lines is greater than or equal to -10° and less than or equal to 10° , and accordingly also includes the case where the angle is greater than or equal to -5° and less than or equal to 5° . In addition, a term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100° , and accordingly includes the 25 case where the angle is greater than or equal to 85° and less than or equal to 95° .

[0277]

On the other hand, according to the TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (plan TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the 30 crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0278]

Note that in an electron diffraction pattern of the CAAC-OS film, spots (luminescent spots) having alignment are shown.

[0279]

5 From the results of the cross-sectional TEM image and the plan TEM image, alignment is found in the crystal parts in the CAAC-OS film.

[0280]

10 A CAAC-OS film is subjected to structural analysis with an X-ray diffraction (XRD) apparatus. When the CAAC-OS film is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle (2θ) is around 31° . This peak is derived from the $(00x)$ plane (x is an integer) of the InGaZn oxide crystal, which indicates that crystals in the CAAC-OS film have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS film.

15 [0281]

On the other hand, when the CAAC-OS film is analyzed by an in-plane method in which an X-ray enters a sample in a direction substantially perpendicular to the c-axis, a peak appears frequently when 2θ is around 56° . This peak is derived from the (110) plane of the InGaZn oxide crystal. Here, analysis (ϕ scan) is performed under 20 conditions where the sample is rotated around a normal vector of a sample surface as an axis (ϕ axis) with 2θ fixed at around 56° . In the case where the sample is a single-crystal oxide semiconductor film of InGaZn oxide, six peaks appear. The six peaks are derived from crystal planes equivalent to the (110) plane. On the other hand, in the case of a CAAC-OS film, a peak is not clearly observed even when ϕ scan is 25 performed with 2θ fixed at around 56° .

[0282]

According to the above results, in the CAAC-OS film having c-axis alignment, while the directions of a-axes and b-axes are different between crystal parts, the c-axes are aligned in a direction parallel to a normal vector of a formation surface or a normal 30 vector of a top surface. Thus, each metal atom layer arranged in a layered manner observed in the cross-sectional TEM image corresponds to a plane parallel to the a-b

plane of the crystal.

[0283]

Note that the crystal is formed concurrently with deposition of the CAAC-OS film or is formed through crystallization treatment such as heat treatment. As 5 described above, the c-axis of the crystal is aligned with a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, for example, in the case where a shape of the CAAC-OS film is changed by etching or the like, the c-axis might not be necessarily parallel to a normal vector of a formation surface or a normal vector of the top surface of the CAAC-OS film.

[0284]

Further, the degree of crystallinity in the CAAC-OS film is not necessarily uniform. For example, in the case where crystal growth leading to the CAAC-OS film occurs from the vicinity of the top surface of the film, the degree of the crystallinity in the vicinity of the top surface is higher than that in the vicinity of the formation surface 15 in some cases. Furthermore, when an impurity is added to the CAAC-OS film, the crystallinity in a region to which the impurity is added is changed, and the degree of crystallinity in the CAAC-OS film varies depending on regions.

[0285]

Note that when the CAAC-OS film is analyzed by an out-of-plane method, a 20 peak of 2θ may also be observed at around 36° , in addition to the peak of 2θ at around 31° . The peak of 2θ at around 36° indicates that a crystal part having no c-axis alignment is included in part of the CAAC-OS film. It is preferable that in the CAAC-OS film, a peak of 2θ appear at around 31° and a peak of 2θ do not appear at around 36° .

[0286]

The CAAC-OS film is an oxide semiconductor film having low impurity concentration. The impurity is an element other than the main components of the oxide semiconductor film, such as hydrogen, carbon, silicon, or a transition metal element. In particular, an element that has higher bonding strength to oxygen than a 30 metal element included in the oxide semiconductor film, such as silicon, disturbs the atomic arrangement of the oxide semiconductor film by depriving the oxide

semiconductor film of oxygen and causes a decrease in crystallinity. Further, a heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor film and causes a decrease in crystallinity when it is contained in the oxide semiconductor film. Note that the impurity contained in the oxide semiconductor film might serve as a carrier trap or a carrier generation source.

[0287]

The CAAC-OS film is an oxide semiconductor film having a low density of defect states. In some cases, oxygen vacancies in the oxide semiconductor film serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0288]

The state in which impurity concentration is low and density of defect states is low (the number of oxygen vacancies is small) is referred to as a "highly purified intrinsic" or "substantially highly purified intrinsic" state. A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier generation sources, and thus can have a low carrier density. Thus, a transistor including the oxide semiconductor film rarely has negative threshold voltage (is rarely normally on). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has a low density of defect states, and thus has few carrier traps. Accordingly, the transistor including the oxide semiconductor film has little variation in electrical characteristics and high reliability. Charges trapped by the carrier traps in the oxide semiconductor film take a long time to be released, and might behave like fixed charges. Thus, the transistor that includes the oxide semiconductor film having high impurity concentration and a high density of defect states has unstable electrical characteristics in some cases.

[0289]

With the use of the CAAC-OS film in a transistor, variation in the electrical characteristics of the transistor due to irradiation with visible light or ultraviolet light is small.

[0290]

<Polycrystalline oxide semiconductor>

In an image obtained with a TEM, for example, crystal grains can be found in

the polycrystalline oxide semiconductor film. In most cases, the size of a crystal grain in the polycrystalline oxide semiconductor film is greater than or equal to 2 nm and less than or equal to 300 nm, greater than or equal to 3 nm and less than or equal to 100 nm, or greater than or equal to 5 nm and less than or equal to 50 nm in an image obtained with the TEM, for example. Moreover, in an image obtained with the TEM, a boundary between crystals can be found in the polycrystalline oxide semiconductor film in some cases.

[0291]

The polycrystalline oxide semiconductor film may include a plurality of crystal grains, and alignment of crystals may be different in the plurality of crystal grains. When a polycrystalline oxide semiconductor film is analyzed by an out-of-plane method with use of an XRD apparatus, a single peak or a plurality of peaks appear in some cases. For example, in the case of a polycrystalline IGZO film, a peak at 2θ of around 31° that shows alignment or plural peaks that show plural kinds of alignment appear in some cases.

[0292]

The polycrystalline oxide semiconductor film has high crystallinity and thus has high electron mobility in some cases. Accordingly, a transistor including the polycrystalline oxide semiconductor film has high field-effect mobility. Note that there are cases in which an impurity is segregated at the grain boundary in the polycrystalline oxide semiconductor film. Moreover, the grain boundary of the polycrystalline oxide semiconductor film serves as a defect state. Since the grain boundary of the polycrystalline oxide semiconductor film may serve as a carrier generation source or a trap state, a transistor including the polycrystalline oxide semiconductor film has larger variation in electrical characteristics and lower reliability than a transistor including a CAAC-OS film in some cases.

[0293]

<Microcrystalline oxide semiconductor>

In an image obtained with the TEM, crystal parts cannot be found clearly in the microcrystalline oxide semiconductor in some cases. In most cases, a crystal part in the microcrystalline oxide semiconductor is greater than or equal to 1 nm and less than

or equal to 100 nm, or greater than or equal to 1 nm and less than or equal to 10 nm. A microcrystal with a size greater than or equal to 1 nm and less than or equal to 10 nm, or a size greater than or equal to 1 nm and less than or equal to 3 nm is specifically referred to as nanocrystal (nc). An oxide semiconductor film including nanocrystal is 5 referred to as an nc-OS (nanocrystalline oxide semiconductor) film. In an image obtained with TEM, a crystal grain cannot be found clearly in the nc-OS film in some cases.

[0294]

In the nc-OS film, a microscopic region (for example, a region with a size 10 greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic order. However, there is no regularity of crystal orientation between different crystal parts in the nc-OS film; thus, the orientation of the whole film is not observed. Accordingly, in some cases, the nc-OS film cannot be distinguished from an amorphous 15 oxide semiconductor depending on an analysis method. For example, when the nc-OS film is subjected to structural analysis by an out-of-plane method with an XRD apparatus using an X-ray having a diameter larger than the diameter of a crystal part, a peak that shows a crystal plane does not appear. Further, a halo pattern is shown in an electron diffraction pattern (also referred to as a selected-area electron diffraction 20 pattern) of the nc-OS film obtained by using an electron beam having a probe diameter (e.g., larger than or equal to 50 nm) larger than the diameter of a crystal part. Meanwhile, spots are shown in a nanobeam electron diffraction pattern of the nc-OS film obtained by using an electron beam having a probe diameter (e.g., larger than or equal to 1 nm and smaller than or equal to 30 nm) close to, or smaller than or equal to 25 the diameter of a crystal part. Furthermore, in a nanobeam electron diffraction pattern of the nc-OS film, regions with high luminance in a circular (ring) pattern are observed in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS film, a plurality of spots are shown in a ring-like region in some cases.

[0295]

30 FIG. 17 shows an example of nanobeam electron diffraction performed on a sample including an nc-OS film. The measurement position is changed. Here, the sample is cut in the direction perpendicular to a surface where an nc-OS film is formed

and the thickness thereof is reduced to be less than or equal to 10 nm. Further, an electron beam with a diameter of 1 nm enters from the direction perpendicular to the cut surface of the sample. FIG. 17 shows that, when a nanobeam electron diffraction is performed on the sample including the nc-OS film, a diffraction pattern exhibiting a 5 crystal plane is obtained, but orientation along a crystal plane in a particular direction is not observed.

[0296]

Since the nc-OS film is an oxide semiconductor film having more regularity than the amorphous oxide semiconductor film, the nc-OS film has a lower density of 10 defect states than the amorphous oxide semiconductor film. However, there is no regularity of crystal orientation between different crystal parts in the nc-OS film; hence, the nc-OS film has a higher density of defect states than the CAAC-OS film.

[0297]

15 Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0298]

(Embodiment 9)

In the method for manufacturing any of the transistors described in 20 Embodiments 1 to 8, after the pair of electrodes 20 and 21 are formed, the oxide semiconductor film 19 may be exposed to plasma generated in an oxidizing atmosphere, so that oxygen may be supplied to the oxide semiconductor film 19. Atmospheres of oxygen, ozone, dinitrogen monoxide, nitrogen dioxide, and the like can be given as examples of oxidizing atmospheres. Further, in the plasma treatment, the oxide 25 semiconductor film 19 is preferably exposed to plasma generated with no bias applied to the substrate 11 side. Consequently, the oxide semiconductor film 19 can be supplied with oxygen without being damaged; accordingly, the number of oxygen vacancies in the oxide semiconductor film 19 can be reduced. Moreover, impurities, e.g., halogen such as fluorine or chlorine remaining on a surface of the oxide 30 semiconductor film 19 due to the etching treatment can be removed. The plasma treatment is preferably performed while heating is performed at a temperature higher than or equal to 300 °C. Oxygen in the plasma is bonded to hydrogen contained in the

oxide semiconductor film 19 to form water. Since the substrate is heated, the water is released from the oxide semiconductor film 19. Consequently, the amount of hydrogen and water in the oxide semiconductor film 19 can be reduced.

[0299]

5 Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

[0300]

(Embodiment 10)

10 Although the oxide semiconductor films that are described in the above embodiments can be formed by a sputtering method, such films may be formed by another method, e.g., a thermal CVD method. A metal organic chemical vapor deposition (MOCVD) method or an atomic layer deposition (ALD) method may be employed as an example of a thermal CVD method.

15 [0301]

A thermal CVD method has an advantage that no defect due to plasma damage is generated since it does not utilize plasma for forming a film.

[0302]

20 Deposition by a thermal CVD method may be performed in such a manner that a source gas and an oxidizer are supplied to the chamber at a time, the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, and reaction is caused in the vicinity of the substrate or over the substrate.

[0303]

25 Deposition by an ALD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, source gases for reaction are sequentially introduced into the chamber, and then the sequence of the gas introduction is repeated. For example, two or more kinds of source gases are sequentially supplied to the chamber by switching respective switching valves (also referred to as high-speed valves). For example, a first source gas is introduced, an 30 inert gas (e.g., argon or nitrogen) or the like is introduced at the same time as or after the introduction of the first gas so that the source gases are not mixed, and then a second source gas is introduced. Note that in the case where the first source gas and the inert

gas are introduced at a time, the inert gas serves as a carrier gas, and the inert gas may also be introduced at the same time as the introduction of the second source gas. Alternatively, the first source gas may be exhausted by vacuum evacuation instead of the introduction of the inert gas, and then the second source gas may be introduced.

5 The first source gas is adsorbed on a surface of the substrate to form a first layer; then the second source gas is introduced to react with the first layer; as a result, a second layer is stacked over the first layer, so that a thin film is formed. The sequence of the gas introduction is repeated plural times until a desired thickness is obtained, whereby a thin film with excellent step coverage can be formed. The thickness of the thin film

10 can be adjusted by the number of repetition times of the sequence of the gas introduction; therefore, an ALD method makes it possible to accurately adjust a thickness and thus is suitable for manufacturing a minute FET.

[0304]

15 The variety of films such as the metal film, the oxide semiconductor film, and the inorganic insulating film that are described in the above embodiment can be formed by a thermal CVD method such as a MOCVD method or an ALD method. For example, in the case where an In-Ga-Zn-O film is formed, trimethylindium, trimethylgallium, and dimethylzinc are used. Note that the chemical formula of trimethylindium is $\text{In}(\text{CH}_3)_3$. The chemical formula of trimethylgallium is $\text{Ga}(\text{CH}_3)_3$.

20 The chemical formula of dimethylzinc is $\text{Zn}(\text{CH}_3)_2$. Without limitation to the above combination, triethylindium (chemical formula: $\text{In}(\text{C}_2\text{H}_5)_3$) can be used instead of triethylindium, triethylgallium (chemical formula: $\text{Ga}(\text{C}_2\text{H}_5)_3$) can be used instead of trimethylgallium, and diethylzinc (chemical formula: $\text{Zn}(\text{C}_2\text{H}_5)_2$) can be used instead of dimethylzinc.

25 [0305]

For example, in the case where an oxide semiconductor film, e.g., an In-Ga-Zn-O film is formed using a deposition apparatus employing ALD, an $\text{In}(\text{CH}_3)_3$ gas and an O_3 gas are sequentially introduced plural times to form an In-O layer, a $\text{Ga}(\text{CH}_3)_3$ gas and an O_3 gas are introduced at a time to form a GaO layer, and then a

30 $\text{Zn}(\text{CH}_3)_2$ gas and an O_3 gas are introduced at a time to form a ZnO layer. Note that the order of these layers is not limited to this example. A mixed compound layer such as an In-Ga-O layer, an In-Zn-O layer or a Ga-Zn-O layer may be formed by mixing of

these gases. Note that although an H_2O gas that is obtained by bubbling with an inert gas such as Ar may be used instead of an O_3 gas, it is preferable to use an O_3 gas, which does not contain H. Further, instead of an $In(CH_3)_3$ gas, an $In(C_2H_5)_3$ gas may be used. Instead of a $Ga(CH_3)_3$ gas, a $Ga(C_2H_5)_3$ gas may be used. Furthermore, a $Zn(C_2H_5)_2$ gas may be used.

5

[0306]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments.

10 [0307]

(Embodiment 11)

A semiconductor device (also referred to as a display device) having a display function can be manufactured using the transistor examples of which are shown in the above embodiments. Moreover, some or all of the driver circuits that include the 15 transistor can be formed over a substrate where the pixel portion is formed, whereby a system-on-panel can be obtained. In this embodiment, an example of a display device using the transistor examples of which are shown in the above embodiments is described with reference to FIGS. 18A to 18C and FIGS. 19A and 19B. FIGS. 19A and 19B are cross-sectional views illustrating cross-sectional structures taken along 20 dashed-dotted line M-N in FIG. 18B.

[0308]

In FIG. 18A, a sealant 905 is provided so as to surround a pixel portion 902 provided over a first substrate 901, and the pixel portion 902 is sealed with a second substrate 906. In FIG. 18A, a signal line driver circuit 903 and a scan line driver circuit 904 each are formed using a single crystal semiconductor or a polycrystalline semiconductor over a substrate prepared separately, and mounted in a region different from the region surrounded by the sealant 905 over the first substrate 901. Further, various signals and potentials are supplied to the signal line driver circuit 903, the scan line driver circuit 904, and the pixel portion 902 from flexible printed circuits (FPC) 30 918 and 918b.

[0309]

In FIGS. 18B and 18C, the sealant 905 is provided so as to surround the pixel

portion 902 and the scan line driver circuit 904 that are provided over the first substrate 901. The second substrate 906 is provided over the pixel portion 902 and the scan line driver circuit 904. Thus, the pixel portion 902 and the scan line driver circuit 904 are sealed together with a display element by the first substrate 901, the sealant 905, and the second substrate 906. In FIGS. 18B and 18C, a signal line driver circuit 903 that is formed using a single crystal semiconductor or a polycrystalline semiconductor over a substrate separately prepared is mounted in a region different from the region surrounded by the sealant 905 over the first substrate 901. In FIGS. 18B and 18C, various signals and potentials are supplied to the signal line driver circuit 903, the scan line driver circuit 904, and the pixel portion 902 from an FPC 918.

[0310]

Although FIGS. 18B and 18C each show an example in which the signal line driver circuit 903 is formed separately and mounted on the first substrate 901, one embodiment of the present invention is not limited to this structure. The scan line driver circuit may be separately formed and then mounted, or only part of the signal line driver circuit or part of the scan line driver circuit may be separately formed and then mounted.

[0311]

Note that a connection method of a separately formed driver circuit is not particularly limited, and a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method, or the like can be used. FIG. 18A shows an example in which the signal line driver circuit 903 and the scan line driver circuit 904 are mounted by a COG method. FIG. 18B shows an example in which the signal line driver circuit 903 is mounted by a COG method. FIG. 18C shows an example in which the signal line driver circuit 903 is mounted by a TAB method.

[0312]

The display device includes in its category a panel in which a display element is sealed and a module in which an IC including a controller or the like is mounted on the panel.

[0313]

A display device in this specification refers to an image display device. Further, the display device also includes the following modules in its category: a

module to which a connector such as an FPC or a TCP is attached; a module having a TCP at the tip of which a printed wiring board is provided; and a module in which an integrated circuit (IC) is directly mounted on a display element by a COG method.

[0314]

5 The pixel portion and the scan line driver circuit provided over the first substrate include a plurality of transistors and any of the transistors that are described in the above embodiments can be used. Any of the transistors described in the above embodiments can be applied to a buffer circuit included in the scan line driver circuit.

[0315]

10 As the display element provided in the display device, a liquid crystal element (also referred to as a liquid crystal display element) or a light-emitting element (also referred to as a light-emitting display element) can be used. A light emitting element includes, in its scope, an element whose luminance is controlled by current or voltage, and specifically includes an inorganic electroluminescent (EL) element, an organic EL element, and the like. Further, a display medium whose contrast is changed by an electric effect, such as electronic ink, can be used. FIG. 19A illustrates an example of a liquid crystal display device using a liquid crystal element as the display element and FIG. 19B illustrates an example of a light-emitting display device using a light-emitting element as the display element.

15 [0316]

20 As illustrated in FIGS. 19A and 19B, the display device includes a connection terminal electrode 915 and a terminal electrode 916. The connection terminal electrode 915 and the terminal electrode 916 are electrically connected to a terminal included in the FPC 918 through an anisotropic conductive agent 919.

25 [0317]

The connection terminal electrode 915 is formed using the same conductive film as a first electrode 930, and the terminal electrode 916 is formed using the same conductive film as a pair of electrodes in each of a transistor 910 and a transistor 911.

[0318]

30 Each of the pixel portion 902 and the scan line driver circuit 904 that are provided over the first substrate 901 includes a plurality of transistors. FIGS. 19A and 19B illustrate the transistor 910 included in the pixel portion 902 and the transistor 911

included in the scan line driver circuit 904. In FIG. 19A, an insulating film 924 is provided over each of the transistors 910 and 911, and in FIG. 19B, a planarization film 921 is further provided over the insulating film 924.

[0319]

5 In this embodiment, any of the transistors described in the above embodiments can be used as the transistors 910 and 911 as appropriate. By using any of the transistors described in the above embodiments as the transistors 910 and 911, a display device with high image quality can be fabricated.

[0320]

10 Moreover, FIG. 19B shows an example in which a conductive film 917 is provided over the planarization film 921 so as to overlap with a channel region of an oxide semiconductor film 926 of the transistor 911 for the driver circuit. In this embodiment, the conductive film 917 is formed using the conductive film that is used as the first electrode 930. By providing the conductive film 917 so as to overlap with the 15 channel region of the oxide semiconductor film, the amount of change in the threshold voltage of the transistor 911 between before and after a BT stress test can be further reduced. The conductive film 917 may have the same potential as or a potential different from that of the gate electrode of the transistor 911, and the conductive film 917 can serve as a second gate electrode. The potential of the conductive film 917 20 may be GND, 0 V, in a floating state, or the same potential or substantially the same potential as the minimum potential (Vss; for example, the potential of the source electrode in the case where the potential of the source electrode is a reference potential) of the driver circuit.

[0321]

25 In addition, the conductive film 917 has a function of blocking an external electric field. In other words, the conductive film 917 has a function of preventing an external electric field (particularly, a function of preventing static electricity) from affecting the inside (a circuit portion including the transistor). Such a blocking function of the conductive film 917 can prevent change in electrical characteristics of 30 the transistor due to the influence of an external electric field such as static electricity. The conductive film 917 can be used for any of the transistors described in the above embodiments.

[0322]

In the display panel, the transistor 910 included in the pixel portion 902 is electrically connected to a display element. There is no particular limitation on the kind of the display element as long as display can be performed, and various kinds of display elements can be used.

[0323]

In FIG. 19A, a liquid crystal element 913 that is a display element includes the first electrode 930, a second electrode 931, and a liquid crystal layer 908. Note that an insulating film 932 and an insulating film 933 that serve as alignment films are provided so that the liquid crystal layer 908 is provided therebetween. The second electrode 931 is provided on the second substrate 906 side. The second electrode 931 overlaps with the first electrode 930 with the liquid crystal layer 908 provided therebetween.

[0324]

A spacer 935 is a columnar spacer obtained by selective etching of an insulating film and is provided in order to control the distance between the first electrode 930 and the second electrode 931 (a cell gap). Alternatively, a spherical spacer may be used.

[0325]

Alternatively, a liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is raised. Since the blue phase appears only in a narrow temperature range, a liquid crystal composition in which a chiral material is mixed is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition that includes a liquid crystal showing a blue phase and a chiral material has a short response time of 1 msec or less, and has optical isotropy, which makes the alignment process unneeded and viewing angle dependence small. In addition, since an alignment film does not need to be provided and rubbing treatment is unnecessary, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device in the manufacturing process can be reduced. Thus, the productivity of the liquid crystal display device can be increased.

[0326]

The first substrate 901 and the second substrate 906 are fixed in place by a sealant 925. As the sealant 925, an organic resin such as a thermosetting resin or a photocurable resin can be used.

5 [0327]

Further, the transistor including an oxide semiconductor film used in the above embodiments has excellent switching characteristics. Furthermore, relatively high field-effect mobility is obtained, which enables high-speed operation. Consequently, when the above transistor is used in a pixel portion of a semiconductor device having a 10 display function, high-quality images can be obtained. Since a driver circuit portion and the pixel portion can be formed over one substrate with the use of the above transistor, the number of components of the semiconductor device can be reduced.

[0328]

15 The size of storage capacitor formed in the liquid crystal display device is set considering the leakage current of the transistor provided in the pixel portion or the like so that charges can be held for a predetermined period. By using the transistor including the highly-purified oxide semiconductor film, it is enough to provide a storage capacitor having a capacitance that is 1/3 or less, or 1/5 or less of a liquid crystal capacitance of each pixel; therefore, the aperture ratio of a pixel can be increased.

20 [0329]

In the display device, a black matrix (a light-blocking film), an optical member (an optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member, and the like are provided as appropriate. For example, circular polarization may be obtained by using a polarizing substrate and a retardation substrate.

25 In addition, a backlight, a side light, or the like may be used as a light source.

[0330]

As a display method in the pixel portion, a progressive method, an interlace method, or the like can be used. Further, color elements controlled in a pixel at the 30 time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue, respectively). For example, R, G, B, and W (W corresponds to white), or R, G, B, and one or more of yellow, cyan, magenta, and the like can be used. Further, the sizes of display regions may be different between

respective dots of color elements. One embodiment of the present invention is not limited to the application to a display device for color display but can also be applied to a display device for monochrome display.

[0331]

5 In FIG. 19B, a light-emitting element 963 that is a display element is electrically connected to the transistor 910 provided in the pixel portion 902. Note that although the structure of the light-emitting element 963 is a stacked-layer structure of the first electrode 930, a light-emitting layer 961, and the second electrode 931, the structure is not limited thereto. The structure of the light-emitting element 963 can be
10 changed as appropriate depending on the direction in which light is extracted from the light-emitting element 963, or the like.

[0332]

15 A partition wall 960 can be formed using an organic insulating material or an inorganic insulating material. It is particularly preferable that the partition wall 960 be formed using a photosensitive resin material to have an opening over the first electrode 930 so that a sidewall of the opening has an inclined surface with a continuous curvature.

[0333]

20 The light-emitting layer 961 may be formed to have a single-layer structure or a stacked-layer structure including a plurality of layers.

[0334]

25 A protective film may be formed over the second electrode 931 and the partition wall 960 in order to prevent oxygen, hydrogen, moisture, carbon dioxide, or the like from entering the light-emitting element 963. As the protective film, a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, an aluminum nitride oxide film, a DLC film, or the like can be formed. In addition, in a space that is sealed with the first substrate 901, the second substrate 906, and a sealant 936, a filler 964 is provided and sealed. It is preferable that, in this manner, the light-emitting element be packaged (sealed) with a
30 protective film (such as a laminate film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the light-emitting element is not exposed to the outside air.

[0335]

As the sealant 936, an organic resin such as a thermosetting resin or a photocurable resin, fritted glass including low-melting glass, or the like can be used. The fritted glass is preferable because of its high barrier property against impurities such as water and oxygen. Further, in the case where the fritted glass is used as the sealant 936, as illustrated in FIG. 19B, the fritted glass is provided over the insulating film 924, whereby adhesion of the insulating film 924 to the fritted glass becomes high, which is preferable.

[0336]

As the filler 964, as well as an inert gas such as nitrogen or argon, an ultraviolet curable resin or a thermosetting resin can be used: polyvinyl chloride (PVC), an acrylic resin, polyimide, an epoxy resin, a silicone resin, polyvinyl butyral (PVB), ethylene vinyl acetate (EVA), or the like can be used. For example, nitrogen is used for the filler.

[0337]

If necessary, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate for a light-emitting surface of the light-emitting element. Further, a polarizing plate or a circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment by which reflected light can be diffused by projections and depressions on the surface so as to reduce the glare can be performed.

[0338]

The first electrode and the second electrode (each of which may be called a pixel electrode, a common electrode, a counter electrode, or the like) for applying voltage to the display element may have light-transmitting properties or light-reflecting properties, which depends on the direction in which light is extracted, the position where the electrode is provided, and the pattern structure of the electrode.

[0339]

The first electrode 930 and the second electrode 931 can be formed using a light-transmitting conductive material such as indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide,

indium tin oxide including titanium oxide, ITO, indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0340]

Alternatively, the first electrode 930 and the second electrode 931 can be formed using one or more materials selected from metals such as tungsten (W), molybdenum (Mo), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), cobalt (Co), nickel (Ni), titanium (Ti), platinum (Pt), aluminum (Al), copper (Cu), and silver (Ag); an alloy of any of these metals; and a nitride of any of these metals.

[0341]

The first electrode 930 and the second electrode 931 can be formed using a conductive composition including a conductive macromolecule (also referred to as a conductive polymer). As the conductive high molecule, what is called a π -electron conjugated conductive polymer can be used. For example, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, a copolymer of two or more of aniline, pyrrole, and thiophene or a derivative thereof, and the like can be given.

[0342]

Since the transistor is easily broken owing to static electricity or the like, a protective circuit for protecting the driver circuit is preferably provided. The protection circuit is preferably formed using a nonlinear element.

[0343]

As described above, by using any of the transistors described in the above embodiments, a highly reliable semiconductor device having a display function can be provided.

[0344]

Note that the structures, methods, and the like described in this embodiment can be used as appropriate in combination with any of the structures, methods, and the like described in the other embodiments and examples.

30

REFERENCE NUMERALS

[0345]

11: substrate, 15: gate electrode, 16: insulating film, 17: gate insulating film, 17a: nitride insulating film, 17b: oxide insulating film, 17c: nitride insulating film, 17d: nitride insulating film, 17e: nitride insulating film, 19: oxide semiconductor film, 19a: low-resistance region, 19b: low-resistance region, 19c: dashed line, 19d: dashed line, 5 20: electrode, 21: electrode, 22: oxide insulating film, 23: oxide insulating film, 24: oxide insulating film, 25: oxide insulating film, 26: nitride insulating film, 27: nitride insulating film, 28: gate insulating film, 28c: opening, 29: gate electrode, 29a: gate electrode, 29b: gate electrode, 30: electrode, 31: gate insulating film, 32: oxide semiconductor film, 33: oxide insulating film, 35: oxide insulating film, 37: nitride insulating film, 10 38: gate insulating film, 38a: opening, 38b: opening, 38c: opening, 39: gate electrode, 40: electrode, 47: multilayer film, 48: multilayer film, 49a: oxide semiconductor film, 49b: oxide semiconductor film, 50: transistor, 51: transistor, 52: transistor, 60: transistor, 65: transistor, 70: transistor, 71: transistor, 102: conductive film, 201: gate electrode, 203: insulating film, 205: oxide semiconductor film, 207: electrode, 15 208: electrode, 209: insulating film, 211b: oxide film, 213: gate electrode, 231: gate electrode, 233: gate insulating film, 235: oxide semiconductor film, 237: electrode, 238: electrode, 239: insulating film, 901: substrate, 902: pixel portion, 903: signal line driver circuit, 904: scan line driver circuit, 905: sealant, 906: substrate, 908: liquid crystal layer, 910: transistor, 911: transistor, 913: liquid crystal element, 915: connection terminal electrode, 916: terminal electrode, 917: conductive film, 918: FPC, 919: anisotropic conductive agent, 921: planarization film, 924: insulating film, 925: sealant, 926: oxide semiconductor film, 930: electrode, 931: electrode, 932: insulating film, 933: insulating film, 935: spacer, 936: sealant, 960: partition wall, 961: light-emitting layer, 963: light-emitting element, 964: filler

25

This application is based on Japanese Patent Application serial No. 2013-103708 filed with Japan Patent Office on May 16, 2013, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a transistor comprising:

5 a first gate electrode;

a first gate insulating film over the first gate electrode;

a first oxide semiconductor film over the first gate insulating film;

a source electrode and a drain electrode over the first oxide semiconductor film;

10 a second gate insulating film over the first oxide semiconductor film, the source electrode, and the drain electrode; and

a second gate electrode over the second gate insulating film,

wherein the first oxide semiconductor film is located between the first gate electrode and the second gate electrode,

15 wherein the second gate electrode comprises a first region and a second region that face each other in a channel width direction of the transistor,

wherein the first oxide semiconductor film is located between the first region and the second region of the second gate electrode,

wherein the first oxide semiconductor film comprises indium and zinc, and

20 wherein the first oxide semiconductor film comprises a crystalline region.

2. The semiconductor device according to claim 1, wherein the second gate electrode is in contact with a side surface of the second gate insulating film.

25 3. The semiconductor device according to claim 1, wherein a side surface of the first oxide semiconductor film faces the second gate electrode in the channel width direction of the transistor.

30 4. The semiconductor device according to claim 1, wherein the second gate electrode is in contact with the first gate insulating film.

5. The semiconductor device according to claim 1, wherein the second gate

insulating film is in contact with the first gate insulating film.

6. The semiconductor device according to claim 1, wherein the second gate electrode is electrically connected to the first gate electrode through a contact hole provided in the first gate insulating film.

7. The semiconductor device according to claim 1,
wherein the second gate electrode is electrically connected to the first gate electrode through a first contact hole and a second contact hole each provided in the first gate insulating film, and

wherein the first oxide semiconductor film is located between the first contact hole and the second contact hole.

8. The semiconductor device according to claim 1, wherein an outline of the first oxide semiconductor film is located inside an outline of the first gate electrode.

9. The semiconductor device according to claim 1, wherein the second gate insulating film comprises:

a first oxide insulating film;
a second oxide insulating film over the first oxide insulating film; and
a nitride insulating film over the second oxide insulating film.

10. The semiconductor device according to claim 1,

wherein the transistor comprises:

a second oxide semiconductor film over the first gate insulating film; and
a third oxide semiconductor film over the first oxide semiconductor film,
wherein the first oxide semiconductor film is located between the second oxide semiconductor film and the third oxide semiconductor film,

wherein the source electrode and the drain electrode is located over the third oxide semiconductor film, and

wherein each of the first oxide semiconductor film, the second oxide semiconductor film, and the third oxide semiconductor film comprises indium, gallium, and zinc.

11. The semiconductor device according to claim 1, wherein the transistor is provided over a substrate.

5 12. A display device comprising:
a pixel portion comprising:
a transistor comprising:
a first gate electrode;
a first gate insulating film over the first gate electrode;
10 a first oxide semiconductor film over the first gate insulating film;
a first electrode and a second electrode over the first oxide semiconductor film;
a second gate insulating film over the first oxide semiconductor film, the first electrode, and the second electrode; and
15 a second gate electrode over the second gate insulating film; and
a third electrode electrically connected to the first electrode,
wherein the first oxide semiconductor film is located between the first gate electrode and the second gate electrode,
wherein the second gate electrode comprises a first region and a second region that
20 face each other in a channel width direction of the transistor,
wherein the first oxide semiconductor film is located between the first region and the second region of the second gate electrode,
wherein the first oxide semiconductor film comprises indium and zinc, and
wherein the first oxide semiconductor film comprises a crystalline region.

25 13. The display device according to claim 12, wherein the second gate electrode is in contact with a side surface of the second gate insulating film.

30 14. The display device according to claim 12, wherein a side surface of the first oxide semiconductor film faces the second gate electrode in the channel width direction of the transistor.

15. The display device according to claim 12, wherein the second gate electrode is in contact with the first gate insulating film.

16. The display device according to claim 12, wherein the second gate insulating film 5 is in contact with the first gate insulating film.

17. The display device according to claim 12, wherein the second gate electrode is electrically connected to the first gate electrode through a contact hole provided in the first gate insulating film.

10

18. The display device according to claim 12, wherein the second gate electrode is electrically connected to the first gate electrode through a first contact hole and a second contact hole each provided in the first gate insulating film, and

15 wherein the first oxide semiconductor film is located between the first contact hole and the second contact hole.

19. The display device according to claim 12, wherein an outline of the first oxide semiconductor film is located inside an outline of the first gate electrode.

20

20. The display device according to claim 12, wherein the second gate insulating film comprises:

a first oxide insulating film;
a second oxide insulating film over the first oxide insulating film; and
25 a nitride insulating film over the second oxide insulating film.

21. The display device according to claim 12,

wherein the transistor comprises:

30 a second oxide semiconductor film over the first gate insulating film; and

a third oxide semiconductor film over the first oxide semiconductor film,
wherein the first oxide semiconductor film is located between the second oxide semiconductor film and the third oxide semiconductor film,

wherein the first electrode and the second electrode is located over the third oxide semiconductor film, and

wherein each of the first oxide semiconductor film, the second oxide semiconductor film, and the third oxide semiconductor film comprises indium, gallium, and zinc.

5

22. The display device according to claim 12, wherein the transistor is provided over a substrate.

10 23. The display device according to claim 12, comprising a liquid crystal layer over the third electrode.

24. The display device according to claim 23, comprising a fourth electrode over the liquid crystal layer.

15 25. The display device according to claim 12, comprising:
a light-emitting layer over the third electrode; and
a fourth electrode over the light-emitting layer.

FIG. 1A

1/19

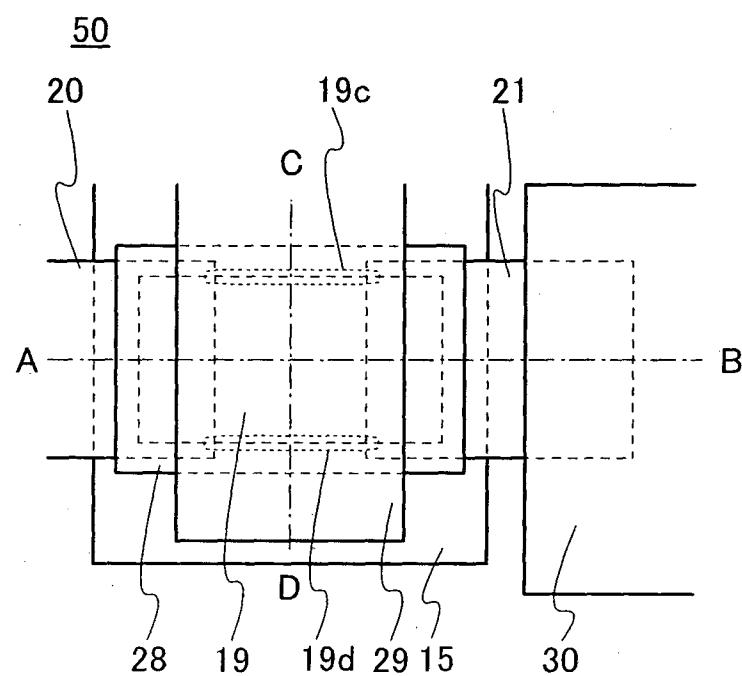


FIG. 1C

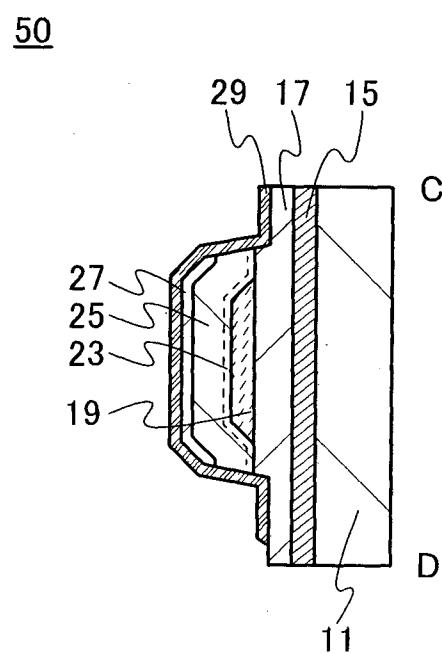
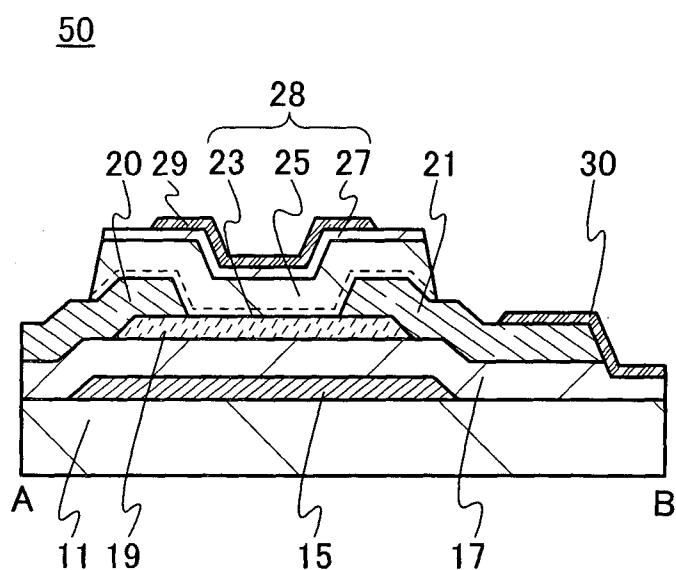


FIG. 1B



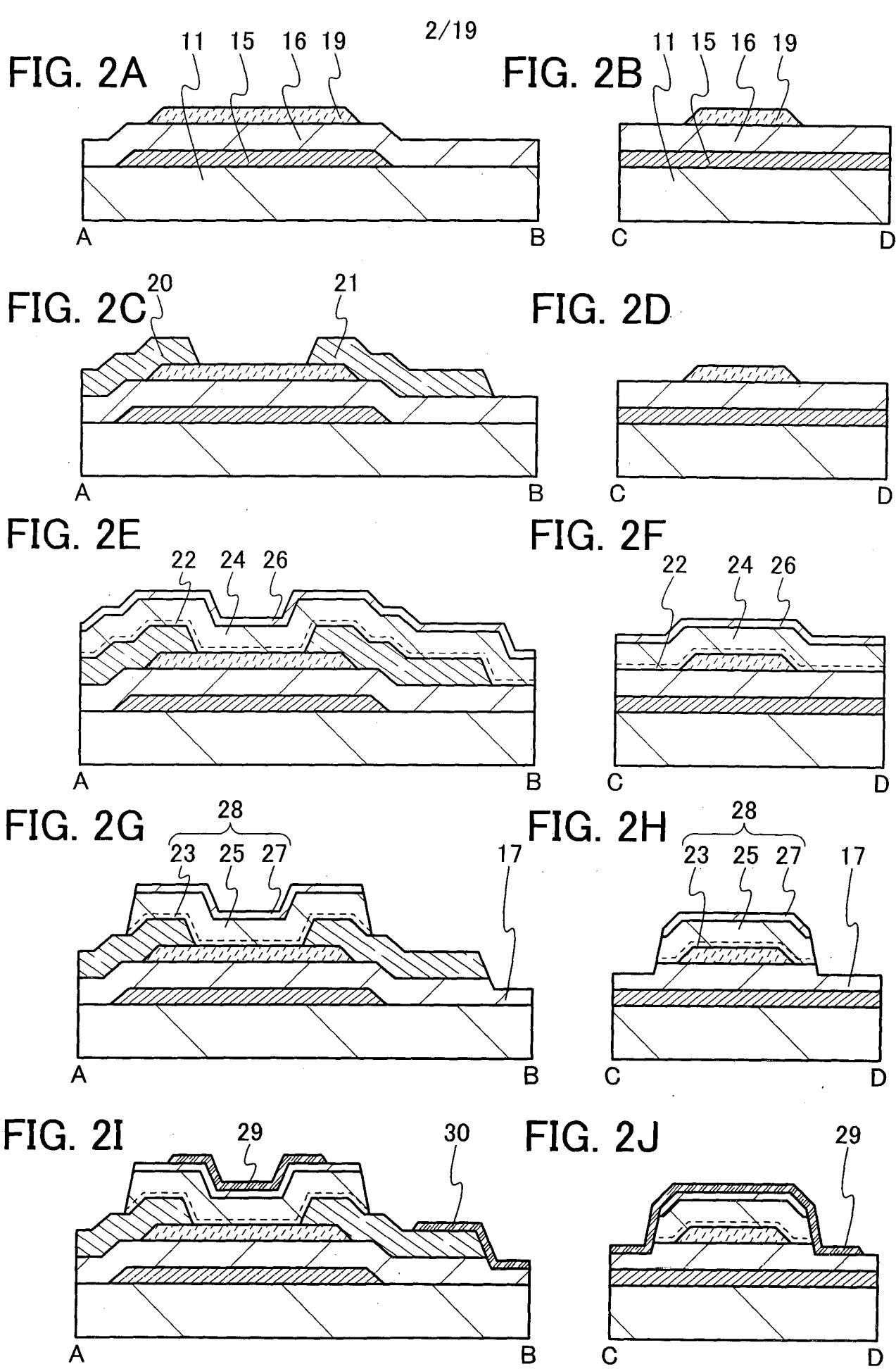


FIG. 3A

3/19

FIG. 3C

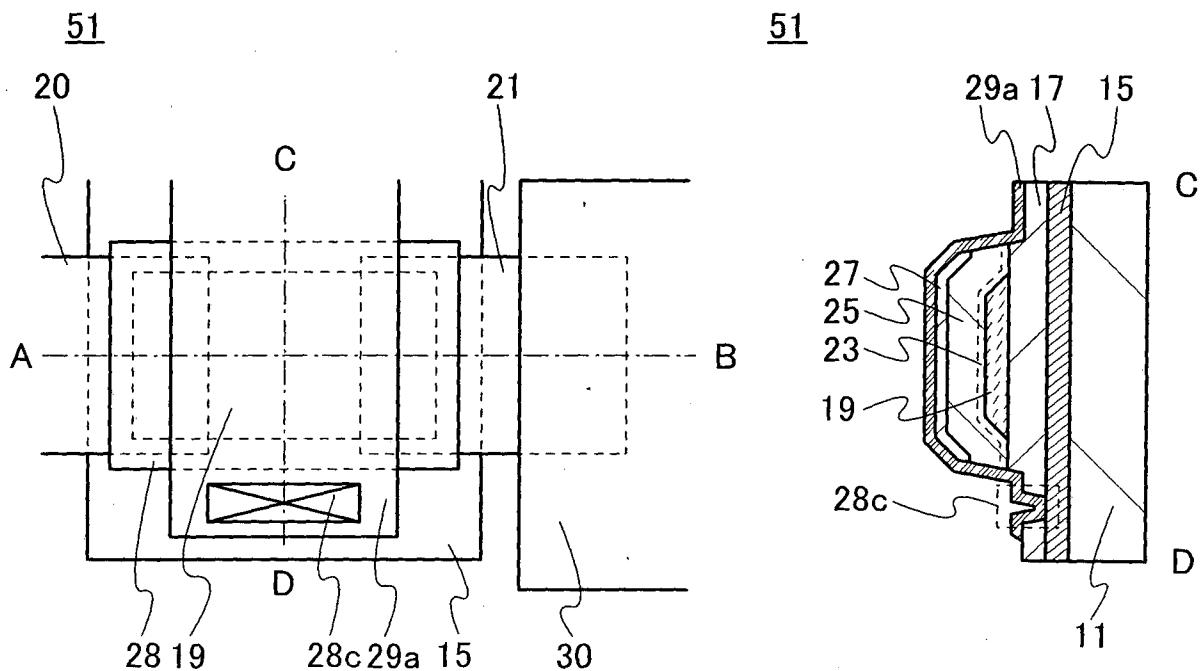
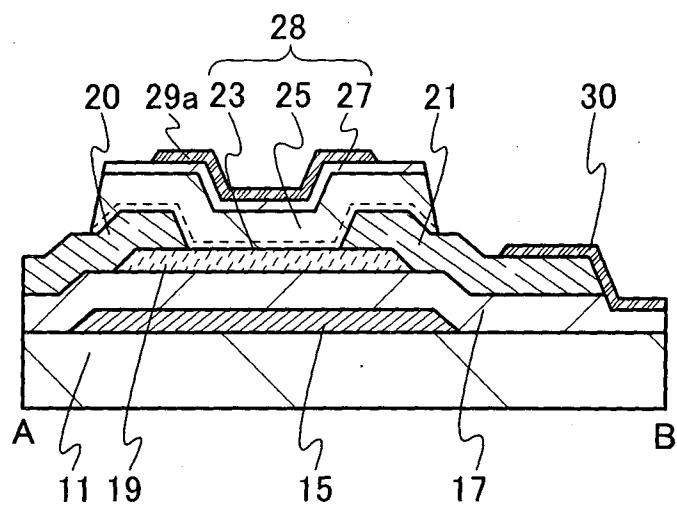


FIG. 3B

51



4/19

FIG. 4A

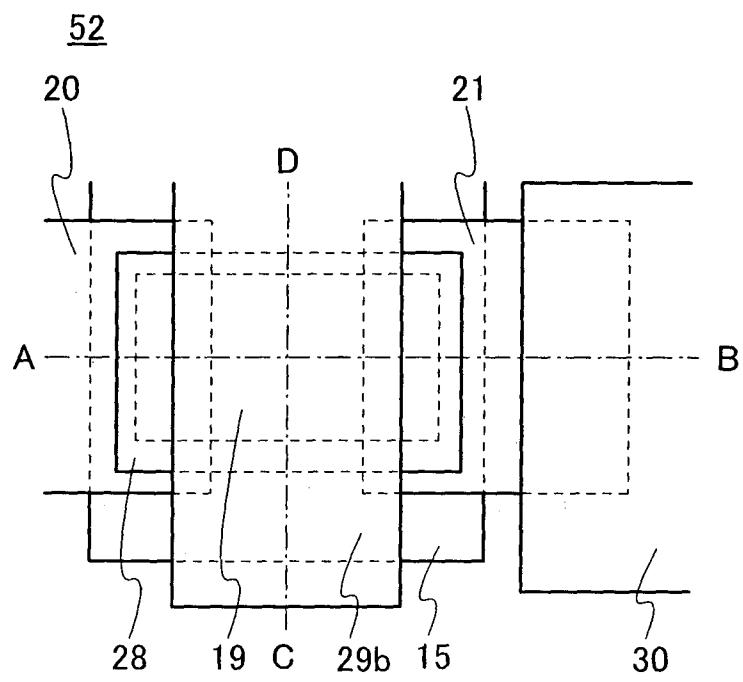


FIG. 4C

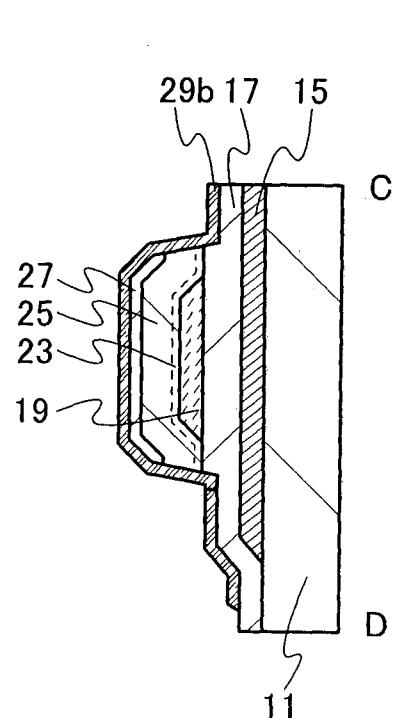


FIG. 4B

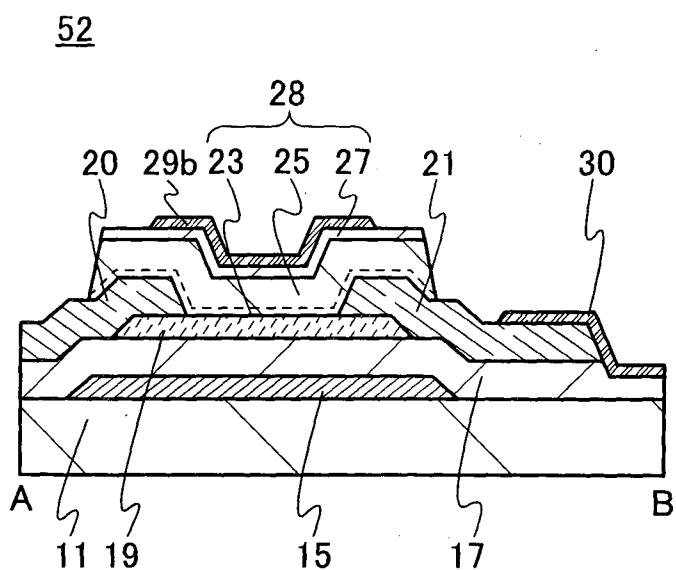


FIG. 5A

5/19

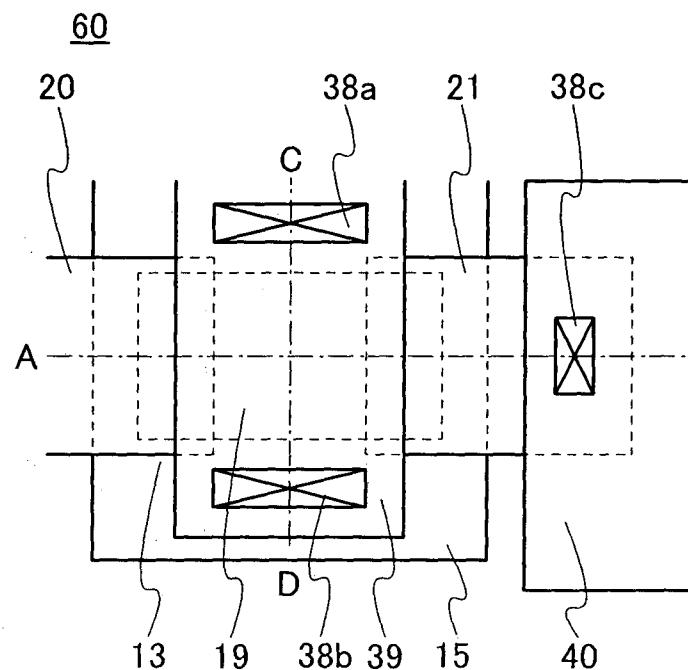


FIG. 5C

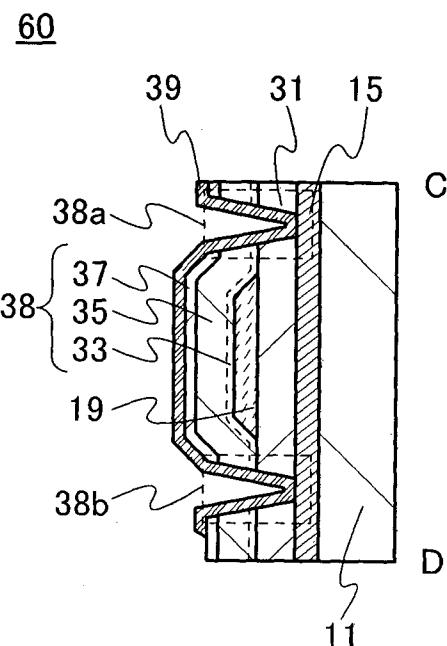


FIG. 5B

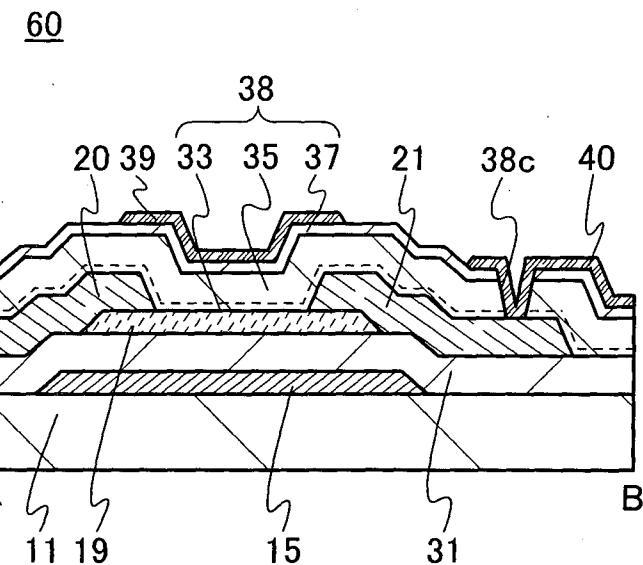
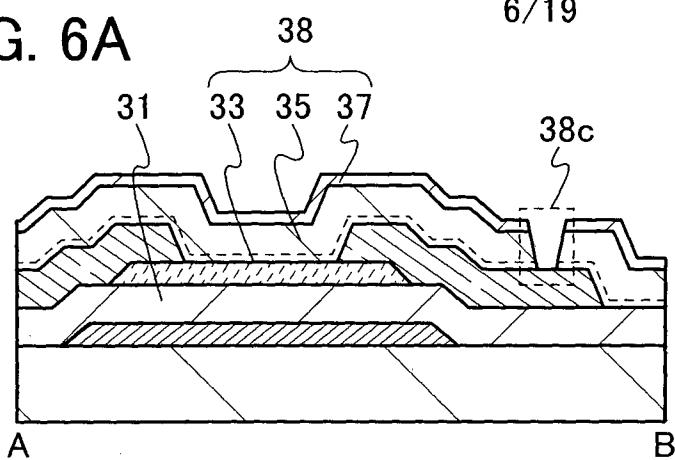
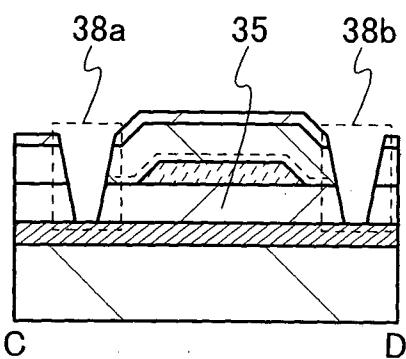
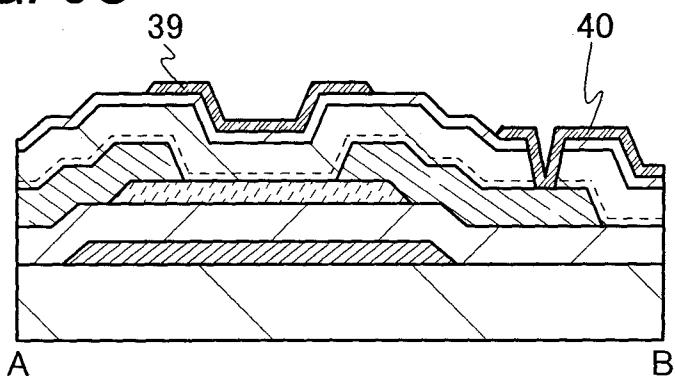
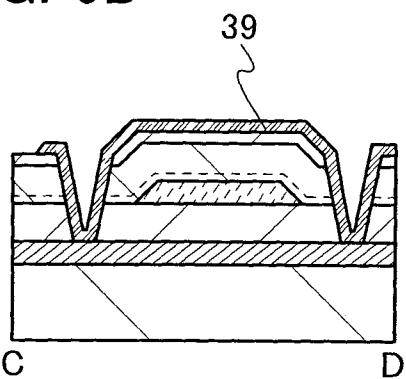


FIG. 6A**FIG. 6B****FIG. 6C****FIG. 6D**

7/19

FIG. 7A

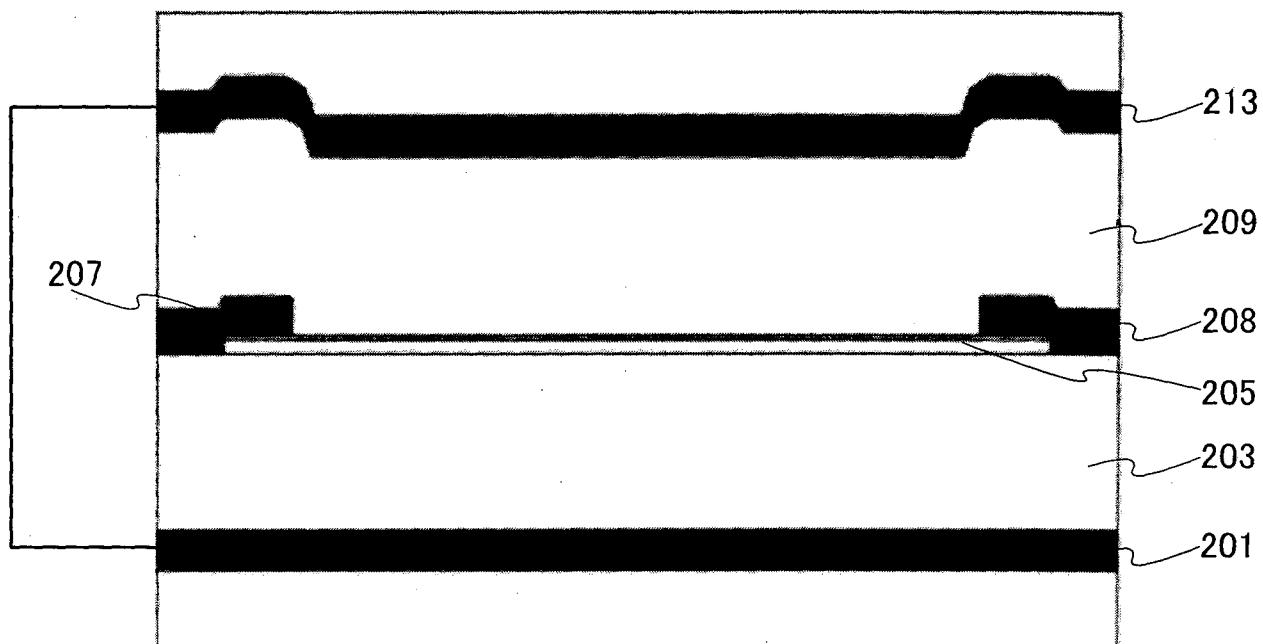
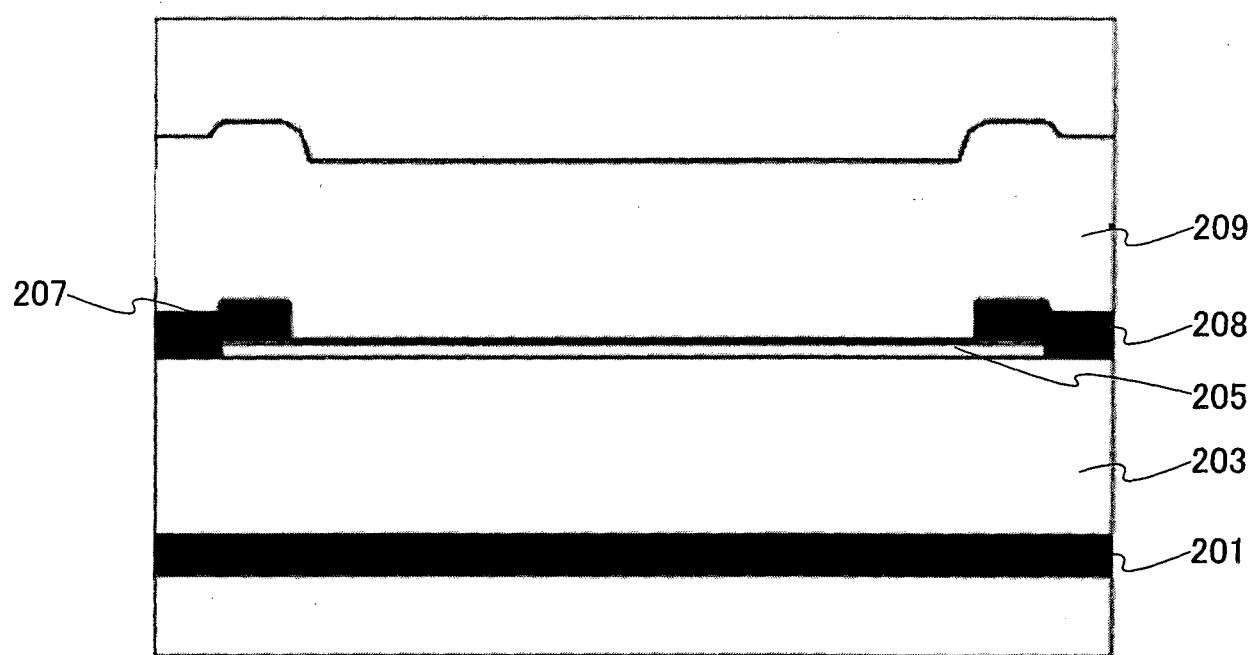


FIG. 7B



8/19

FIG. 8A

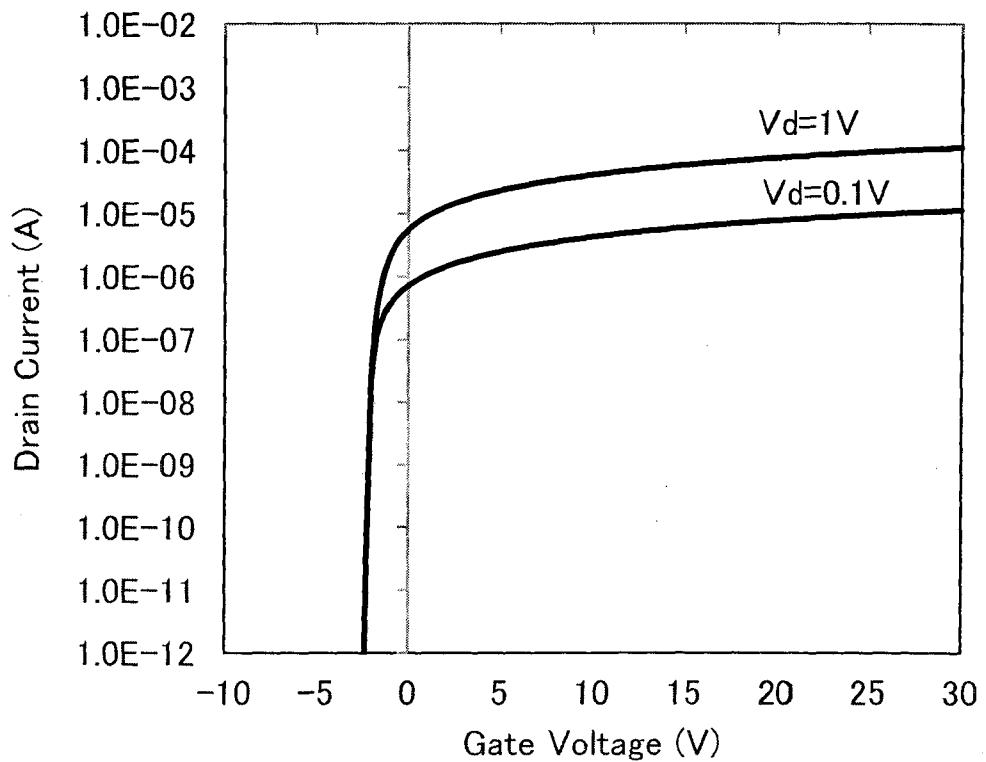
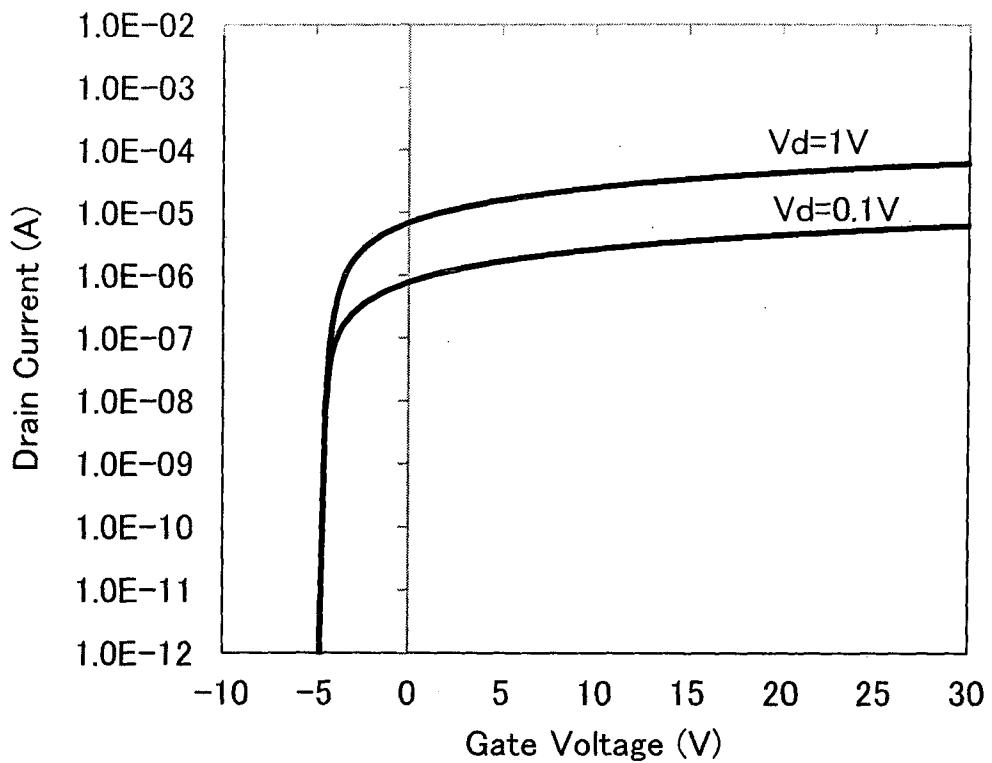


FIG. 8B



9/19

FIG. 9A

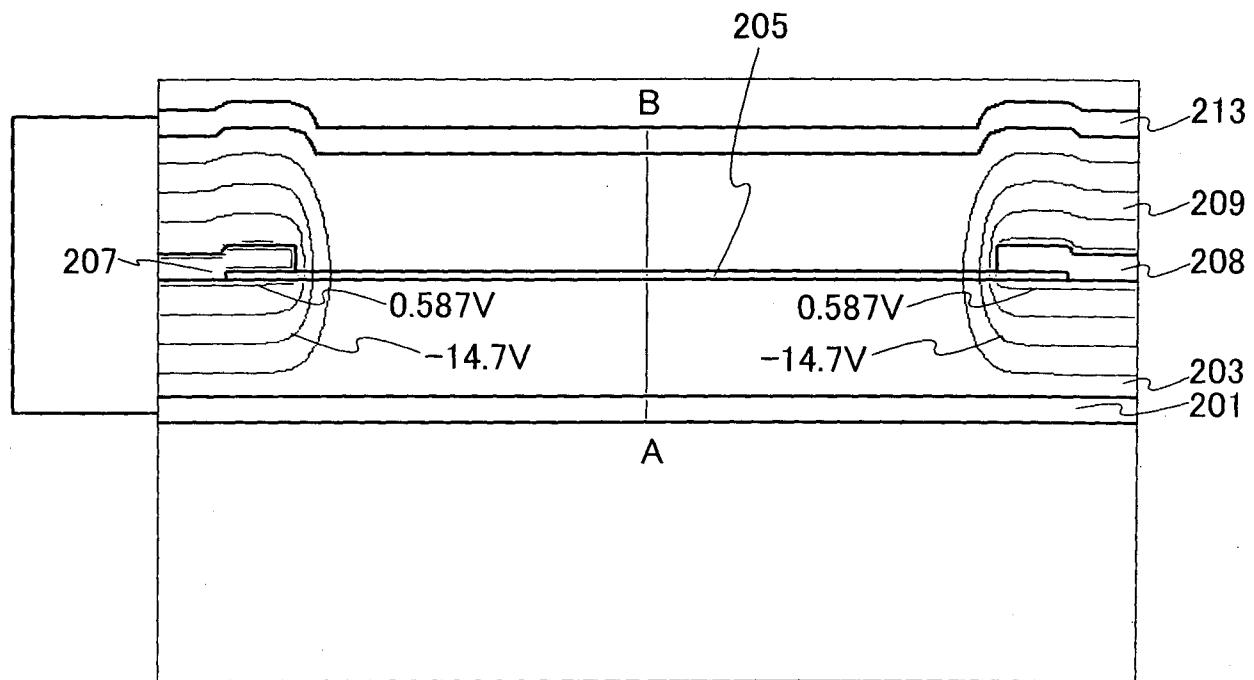
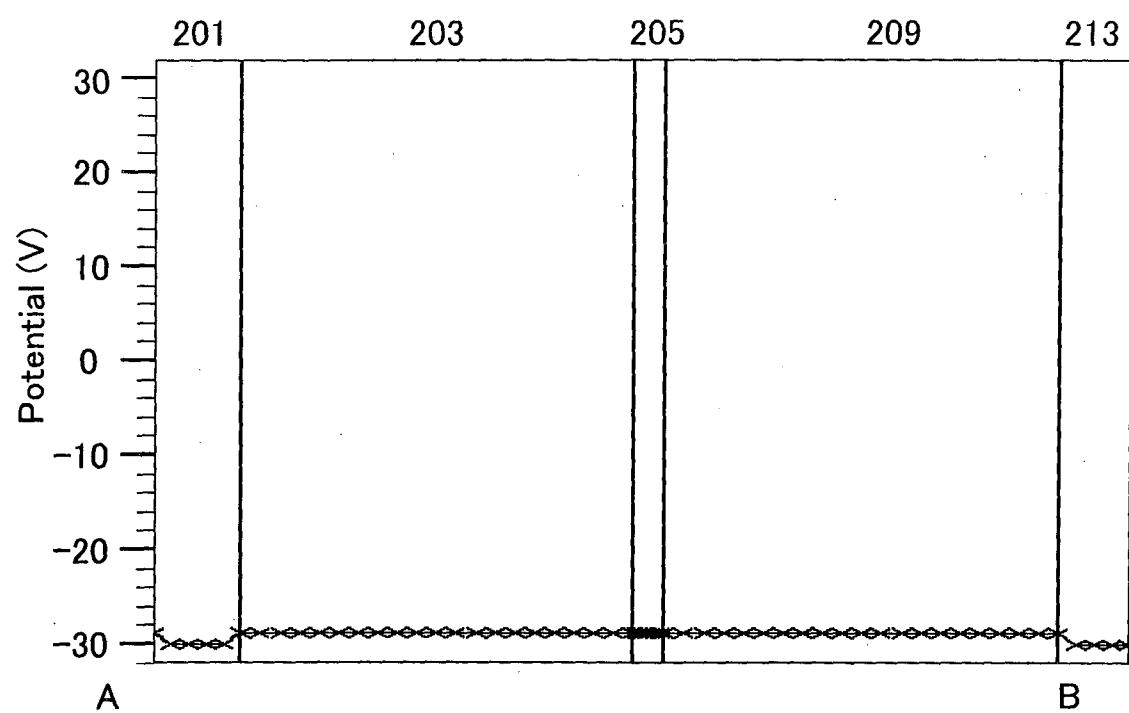


FIG. 9B



10/19

FIG. 10A

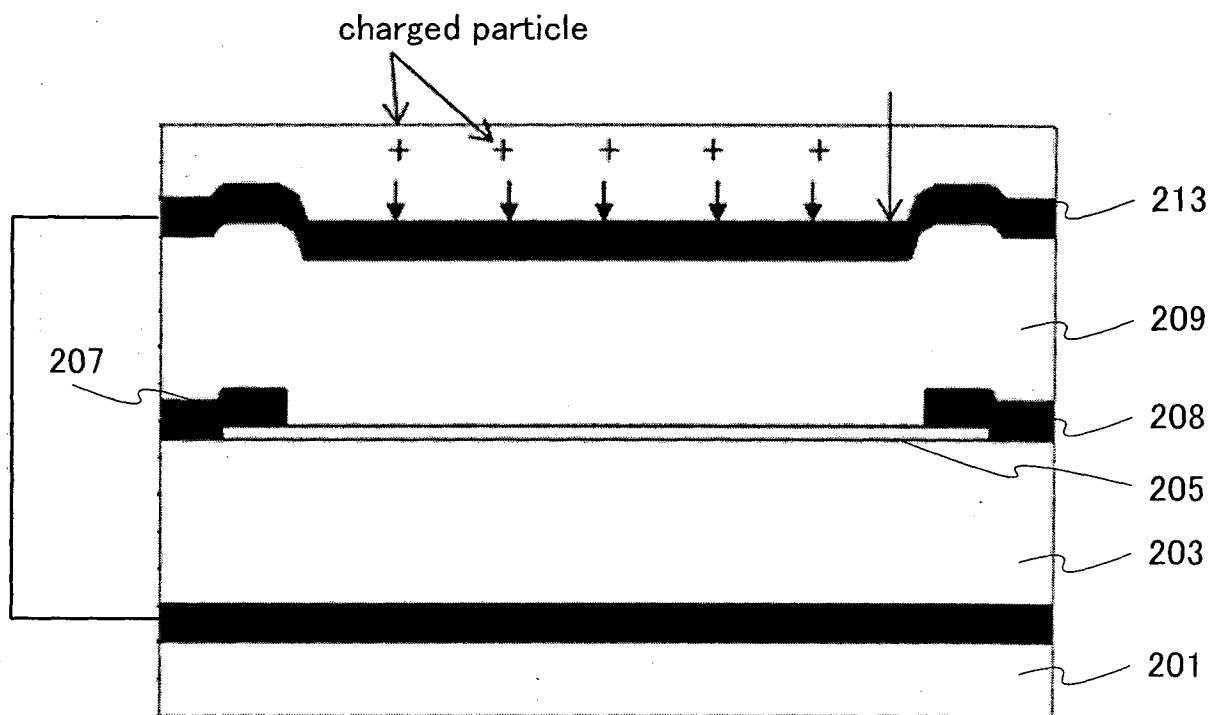
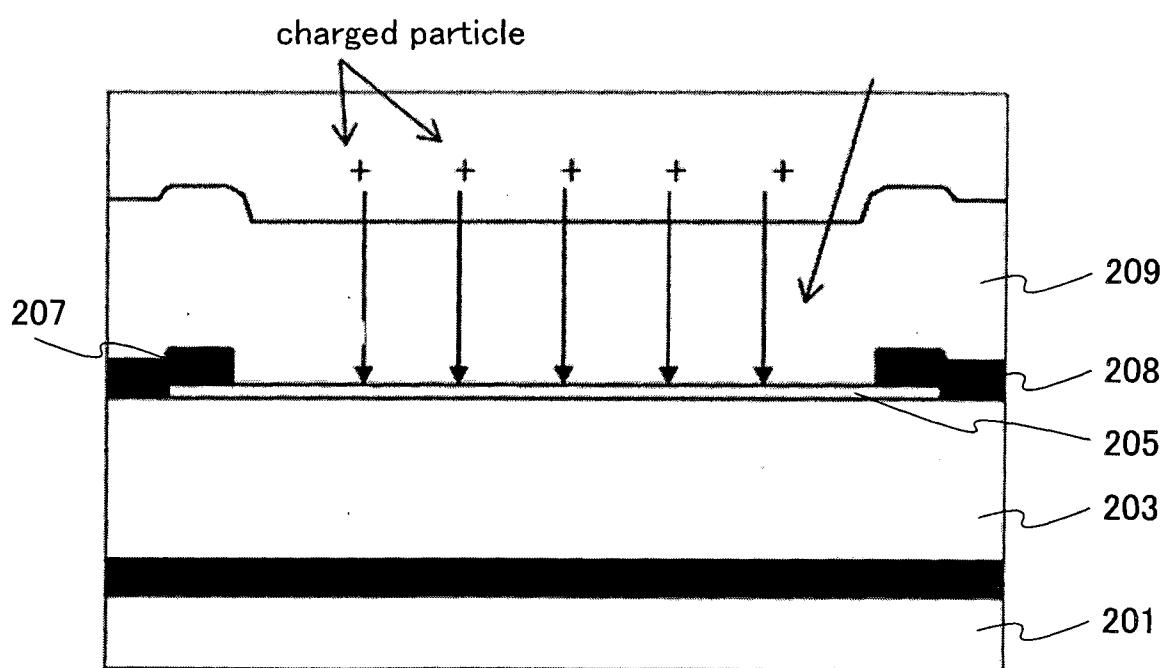


FIG. 10B



11/19

FIG. 11A

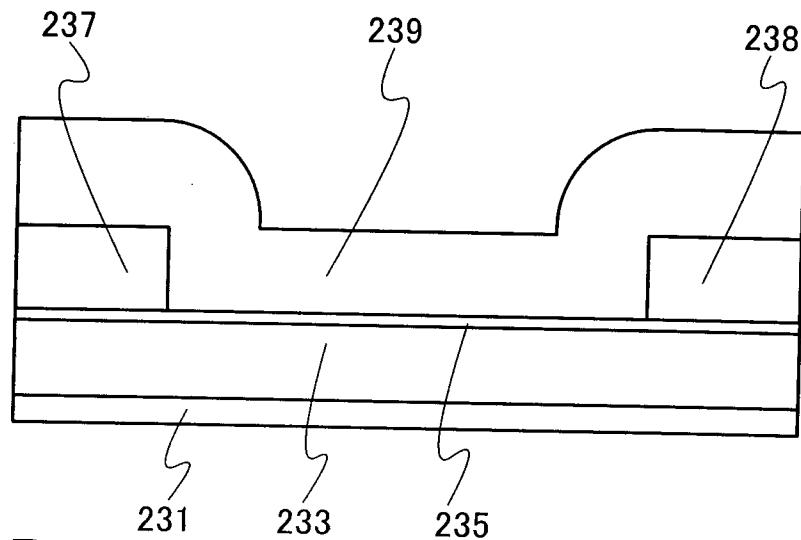


FIG. 11B

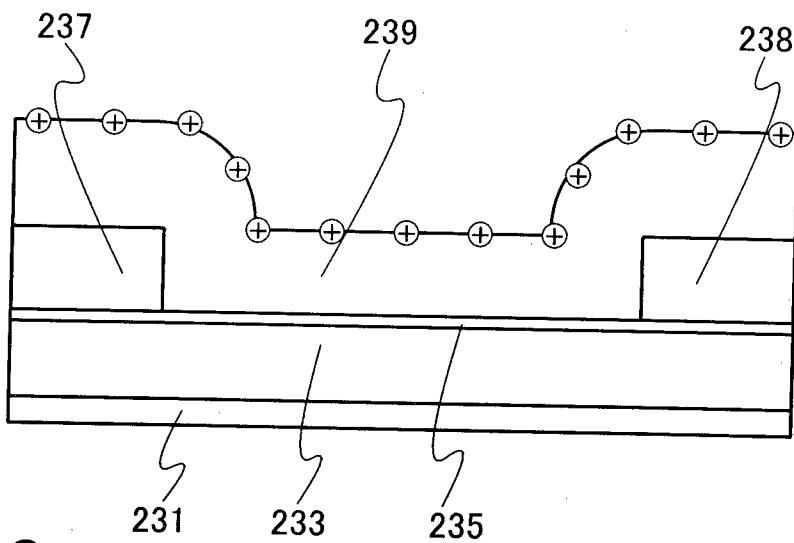


FIG. 11C

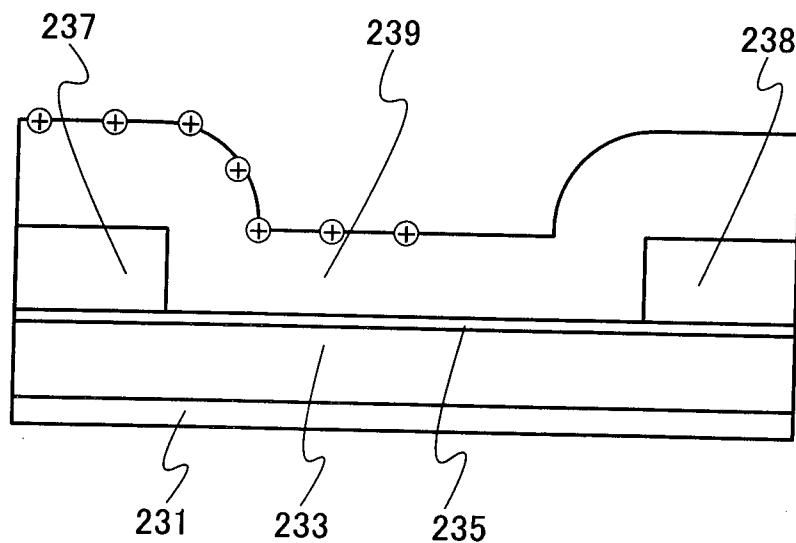


FIG. 12A

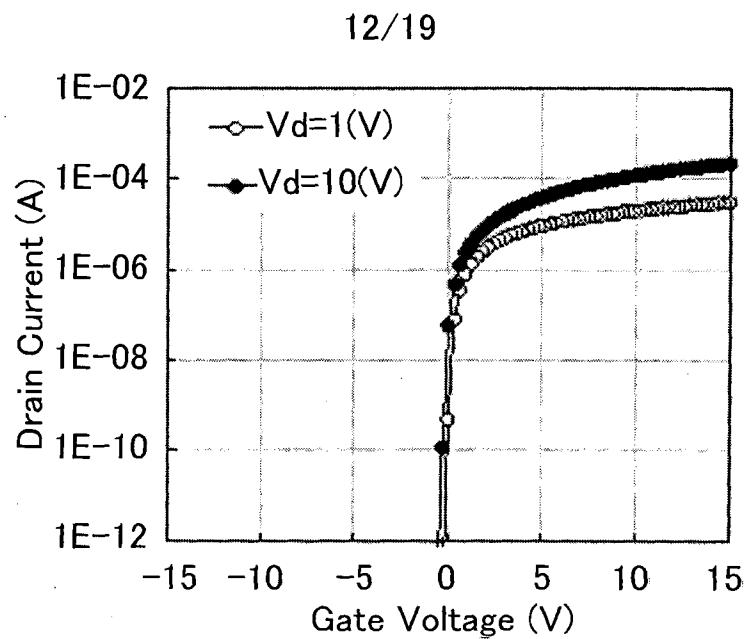


FIG. 12B

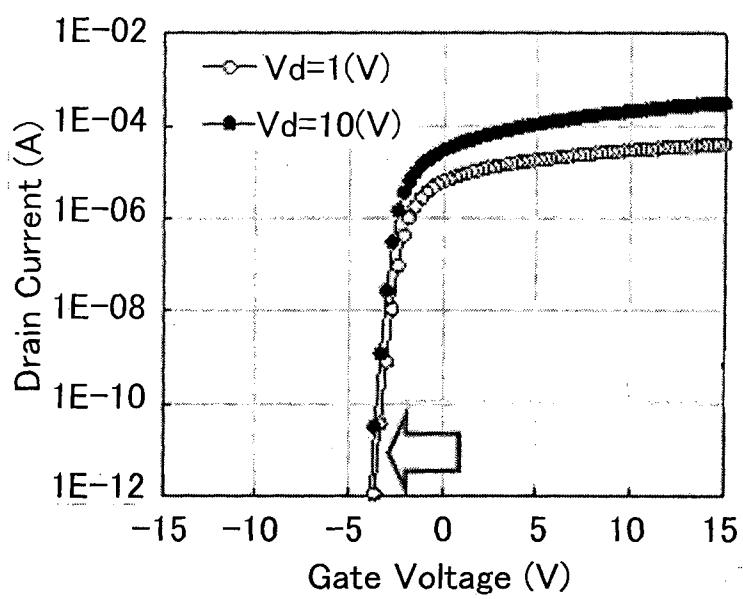
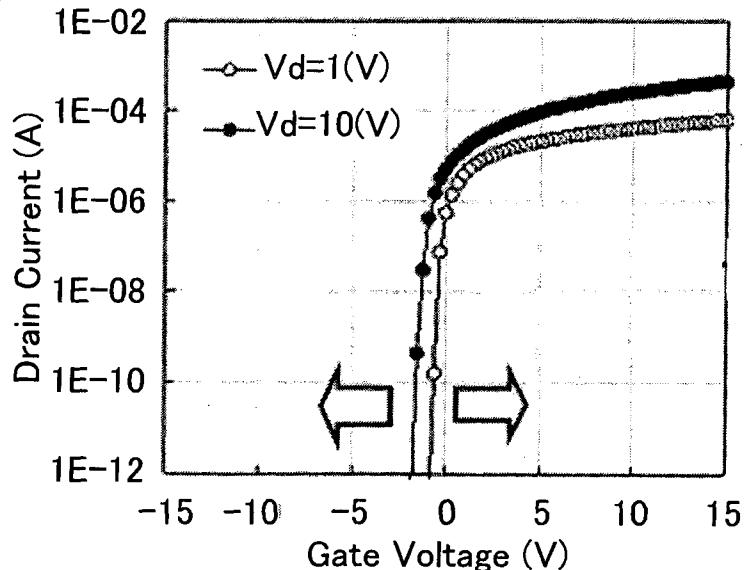


FIG. 12C



13/19

FIG. 13A

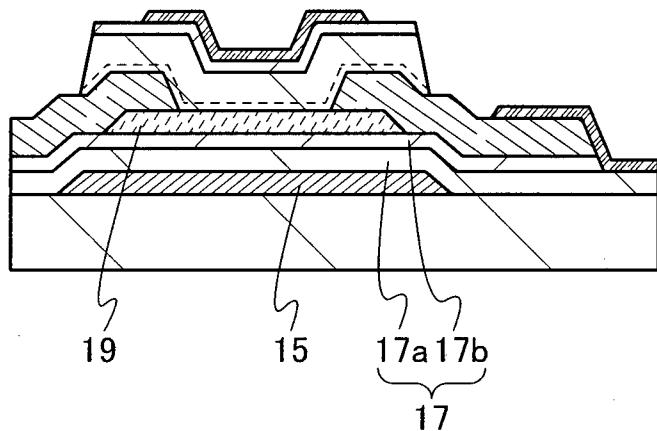


FIG. 13B

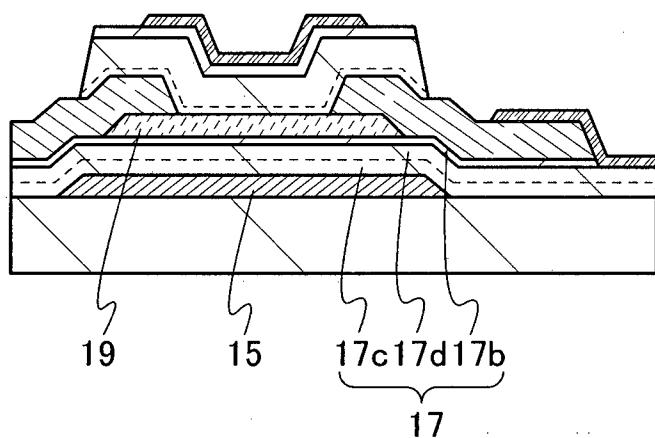
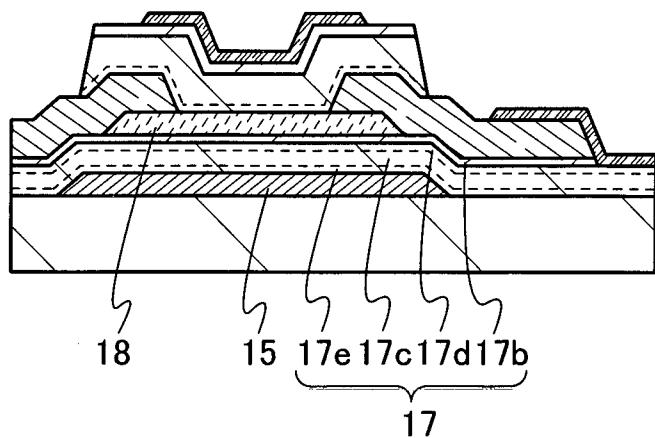
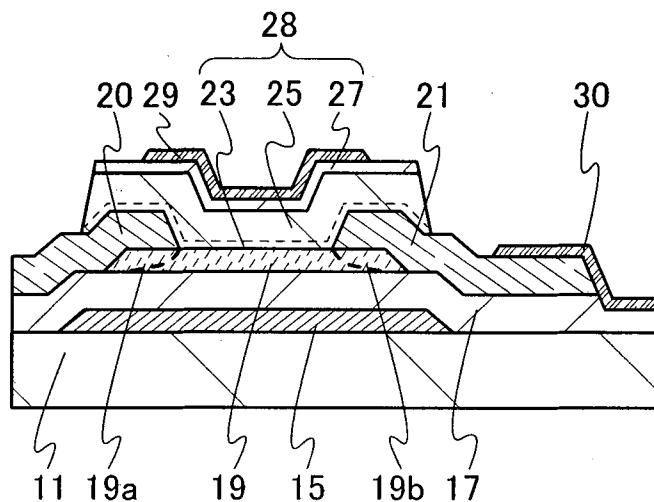


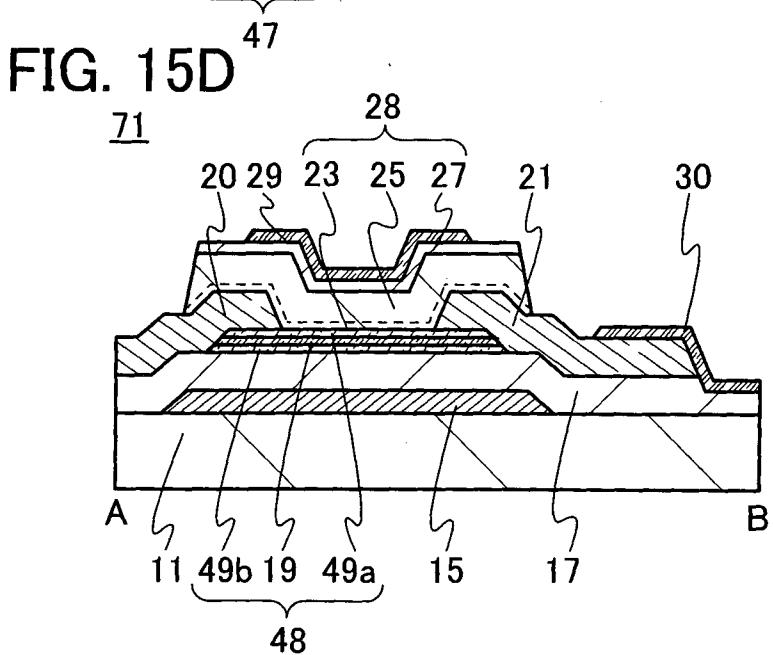
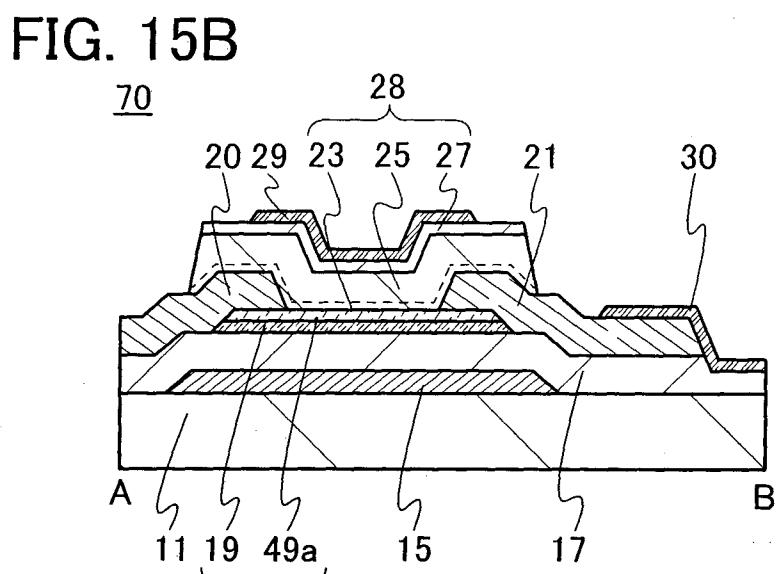
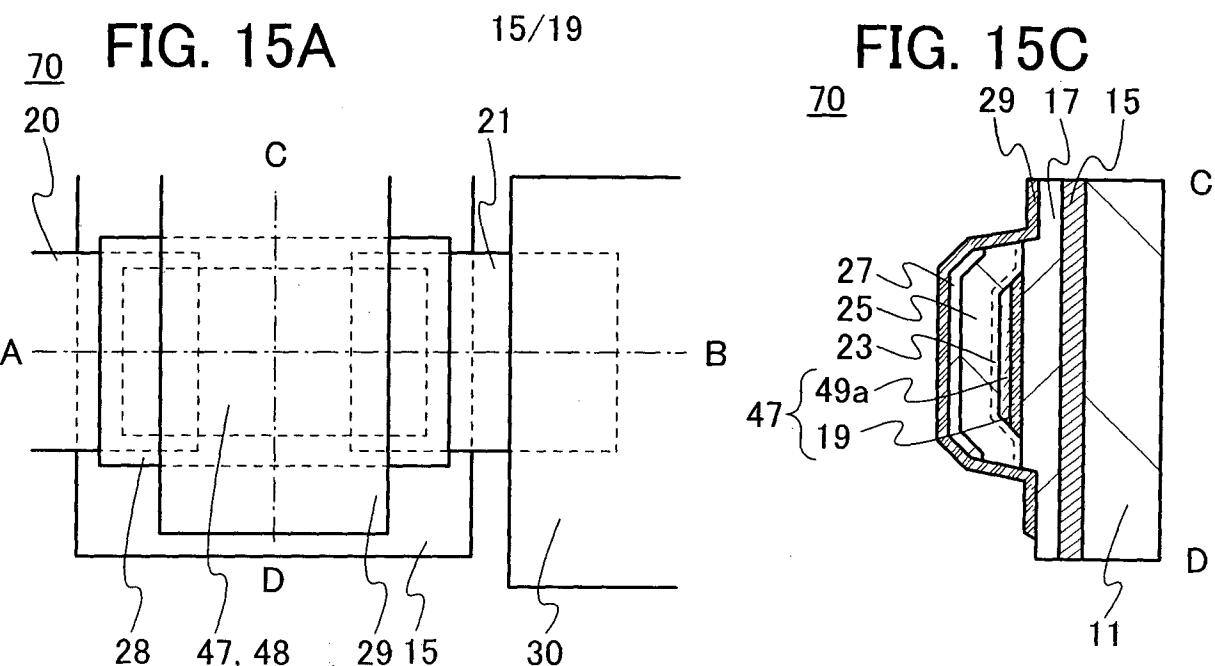
FIG. 13C



14/19

FIG. 14





16/19

FIG. 16A

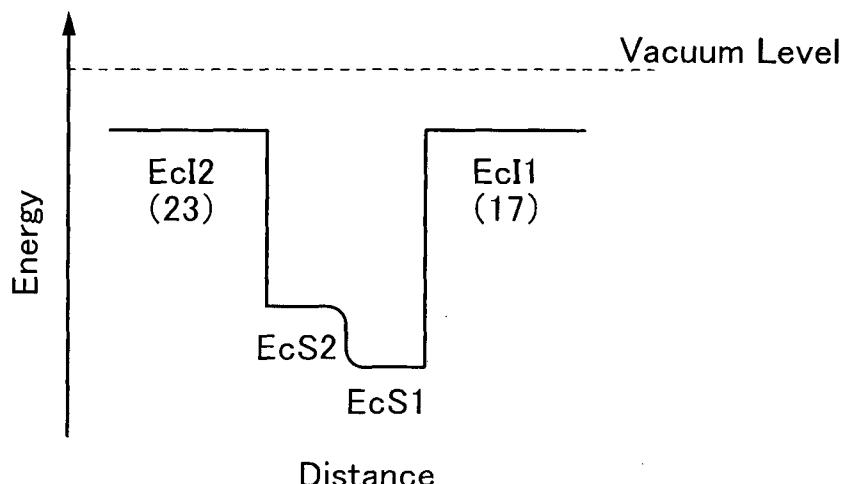


FIG. 16B

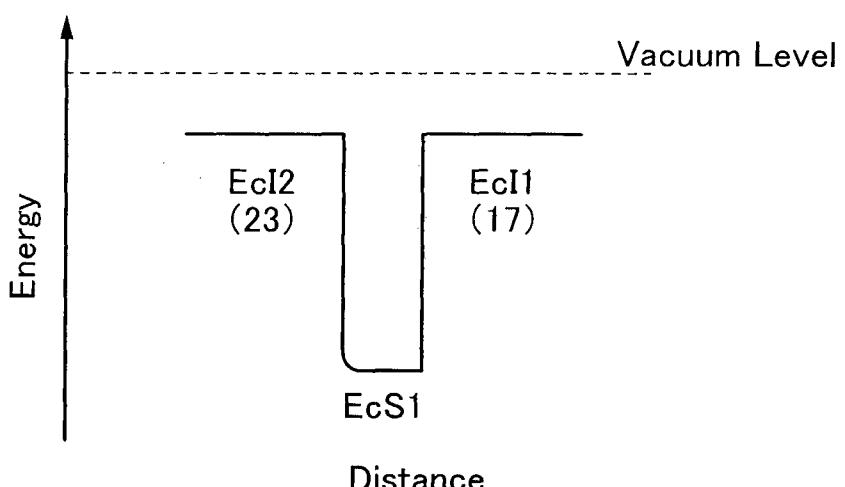


FIG. 16C

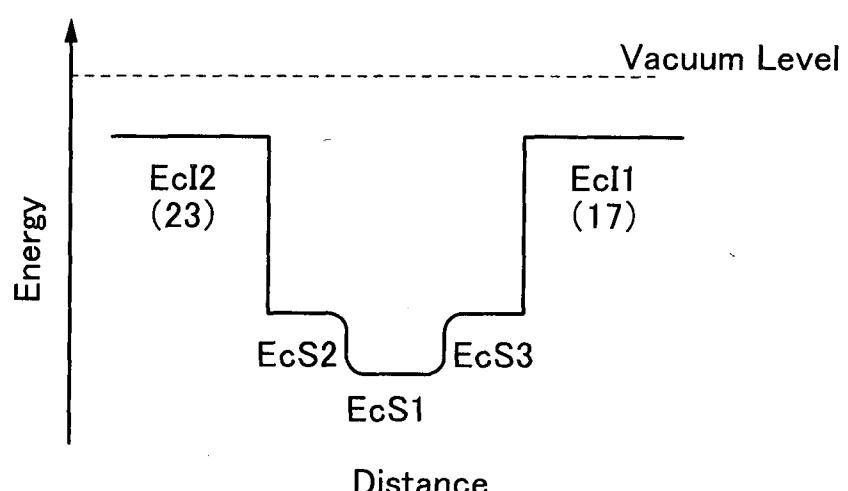
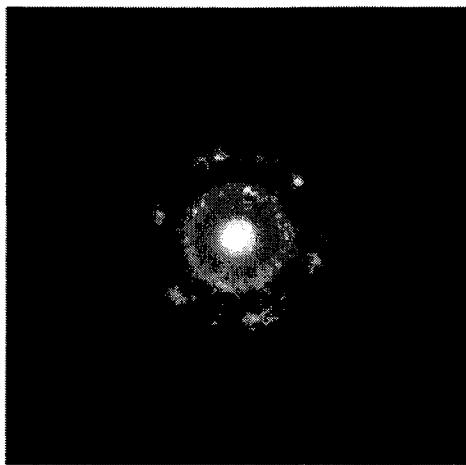
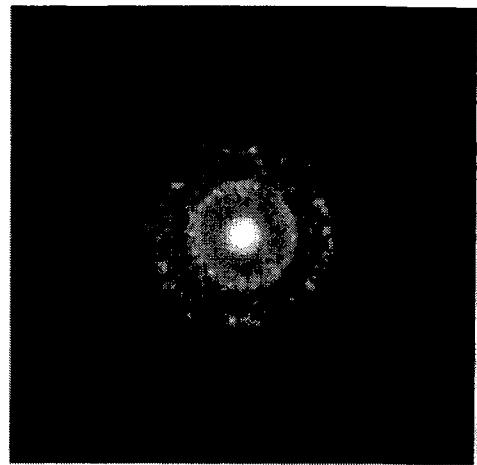


FIG. 17

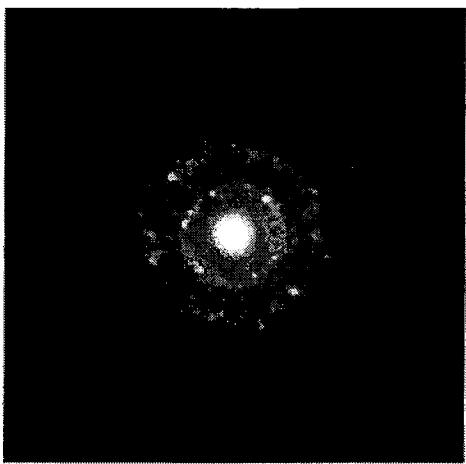
17/19



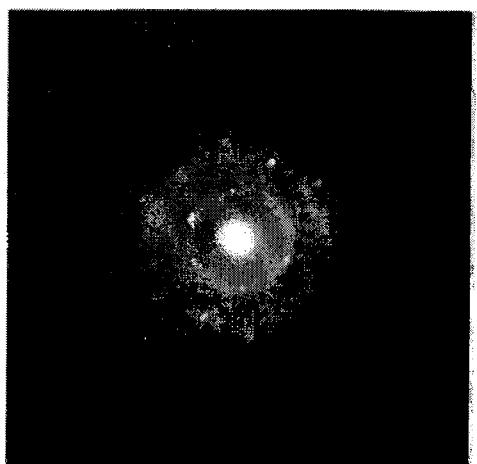
nc-OS measurement position 1



nc-OS measurement position 3



nc-OS measurement position 2



nc-OS measurement position 4

FIG. 18A

18/19

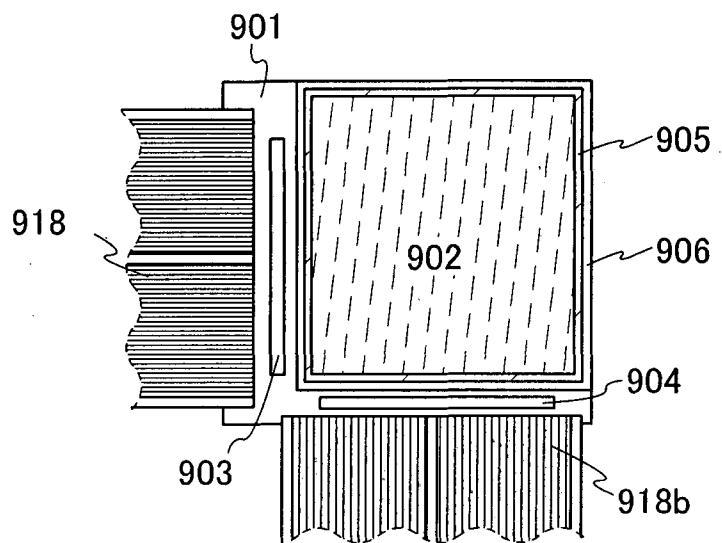


FIG. 18B

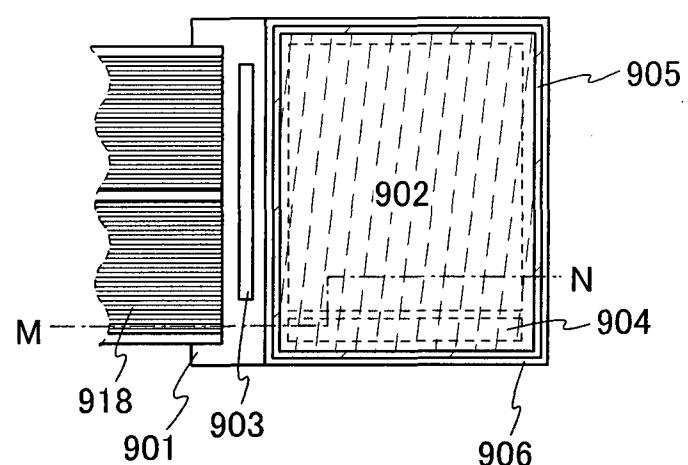
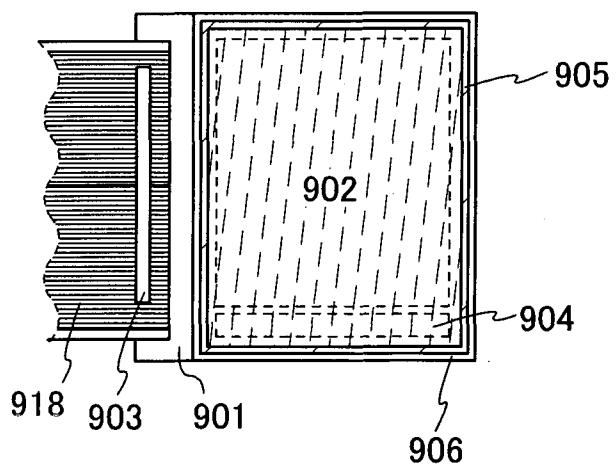


FIG. 18C



19/19

FIG. 19A

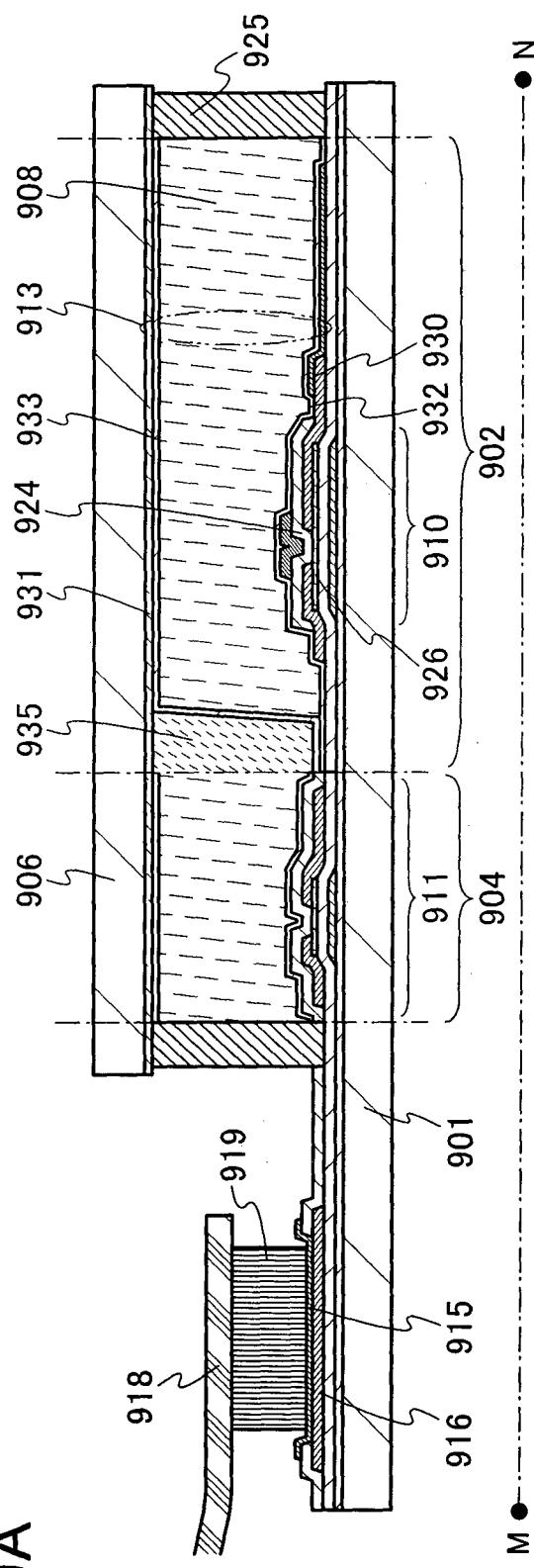
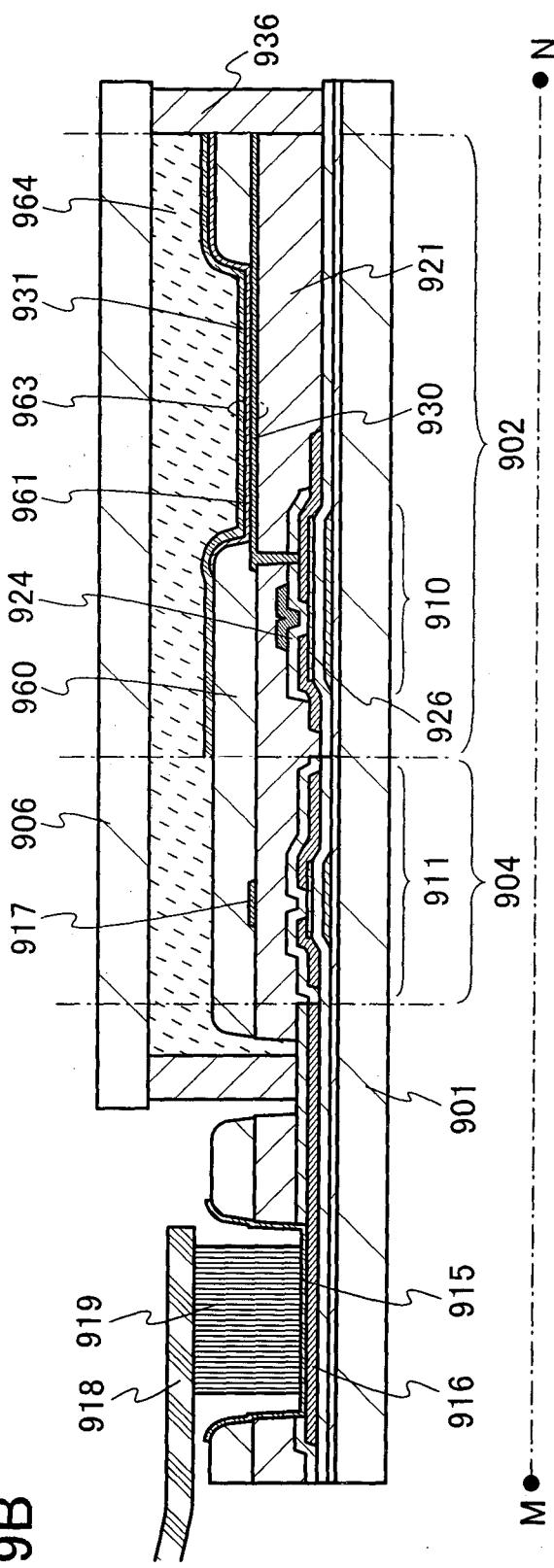


FIG. 19B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2014/062900

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, G02F1/1368, G09F9/30, H01L21/28, H01L29/41, H01L29/423, H01L29/49, H01L51/50, H05B33/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996

Published unexamined utility model applications of Japan 1971-2014

Registered utility model specifications of Japan 1996-2014

Published registered utility model applications of Japan 1994-2014

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2011/096263 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.08.11,	1-7, 11-18, 22-25
Y	Par. Nos. [0024]-[0102], [0196], Figs. 1-3 & JP 2011-181913 A & US 2011/0193077 A1 & KR 10-2012-0117914 A & TW 201342622 A	8-10, 19-21
Y	US 2010/0264412 A1 (YAMAZAKI, Shunpei) 2010.10.21, Par. No. [0112], Fig. 10 & JP 2010-267955 A & CN 101866952 A & KR 10-2010-0114842 A & TW 201108417 A	8, 19

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

25.07.2014

Date of mailing of the international search report

05.08.2014

Name and mailing address of the ISA/JP

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer

WATAHIKI, Takashi

5F 2934

Telephone No. +81-3-3581-1101 Ext. 3516

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2014/062900

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2011/135987 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.11.03, Par. Nos. [0128]-[0139], Figs. 1, 5 & JP 2011-249788 A & US 2011/0269266 A1 & TW 201205684 A	9, 20
Y	US 2013/0009209 A1 (YAMAZAKI, Shunpei) 2013.01.10, Par. Nos. [0068]-[0116], Fig. 1 & JP 2013-38400 A	10, 21

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2014/062900

CLASSIFICATION OF SUBJECT MATTER

H01L29/786 (2006. 01) i, G02F1/1368 (2006. 01) i, G09F9/30 (2006. 01) i,
H01L21/28 (2006. 01) i, H01L29/41 (2006. 01) i, H01L29/423 (2006. 01) i,
H01L29/49 (2006. 01) i, H01L51/50 (2006. 01) i, H05B33/14 (2006. 01) i