United States Patent

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[54] **PROBABILITY-GENERATING SYSTEM AND GAME FOR USE THEREWITH**
13 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** **273/138A**
[51] **Int. Cl.** **A63b 71/06**
[50] **Field of Search** .... 273/138 (A)

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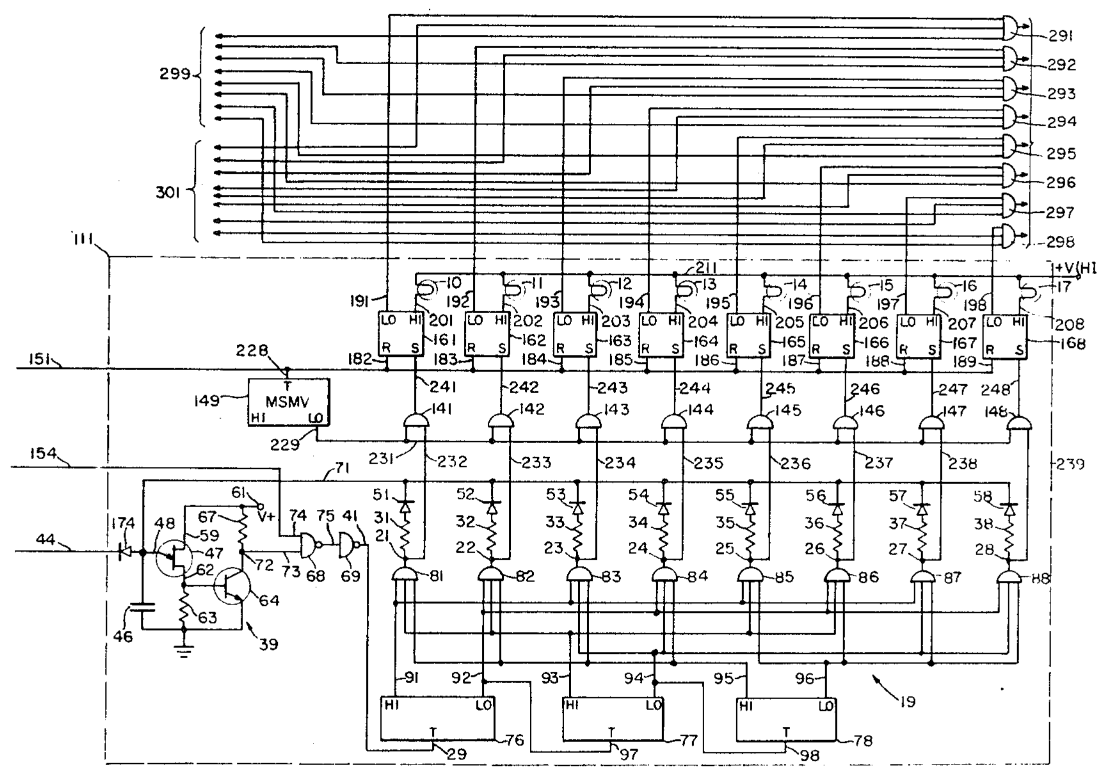
ABSTRACT: In order to select an event at random from a set of possible events, wherein each event has a preselected and different probability of being selected, an electrical circuit is provided for generating a continuous cyclic succession of electrical output signals each corresponding to one event in which the time duration of each signal is individually controlled and preset to provide a different time portion of the total combined time duration of all of the output signals and means are provided for interrupting this continuous train of output signals at an arbitrary point in time, whereby the output signal occurring at the time of this interruption is sensed and the event associated therewith is accordingly selected. Furthermore, a series of these circuits is disclosed in combination with a set of visual monitors for symbolically displaying the selection of events to provide a game for amusement and entertainment in which each event and combinations thereof is assigned a winning or losing value.



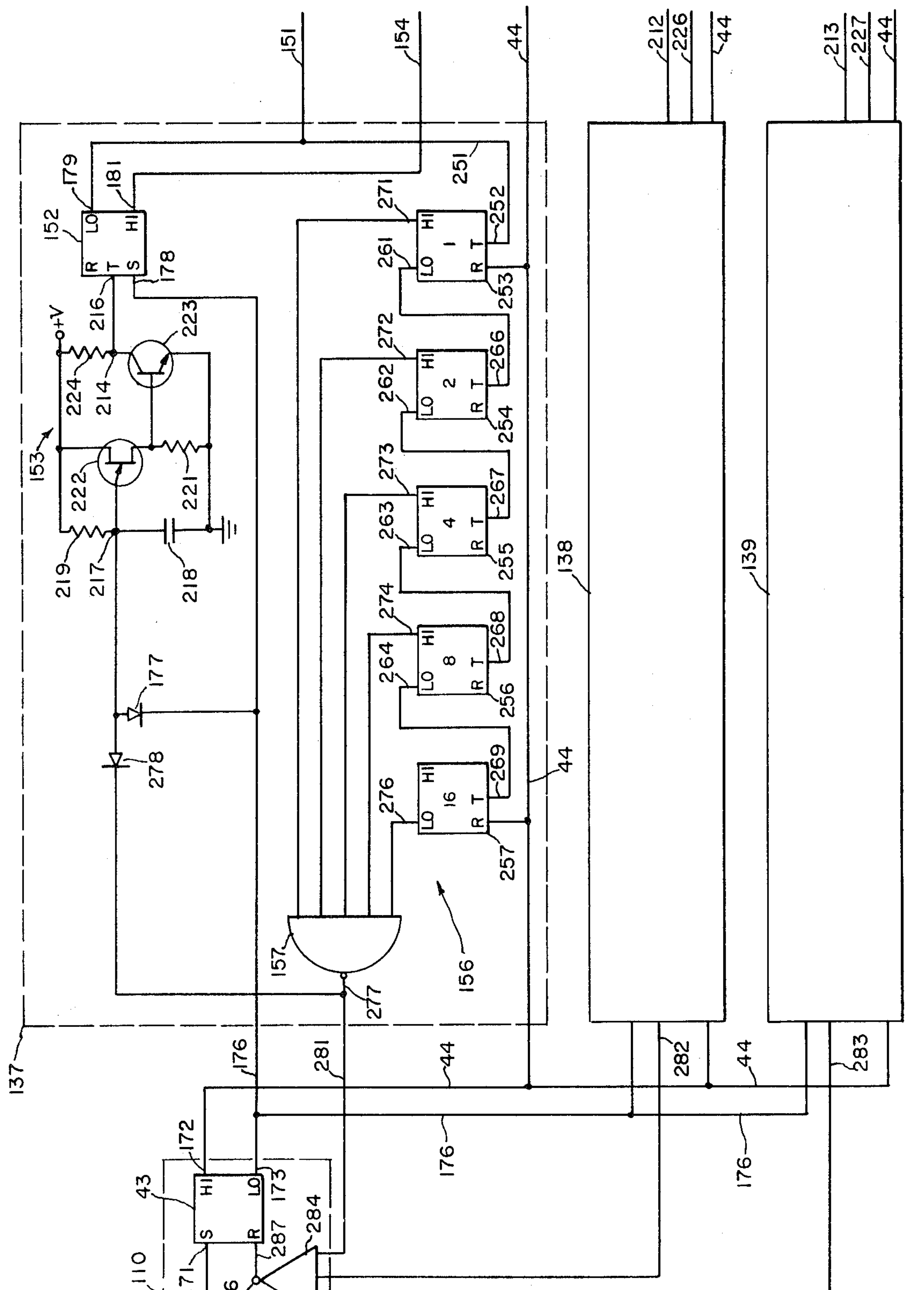


FIG. 1

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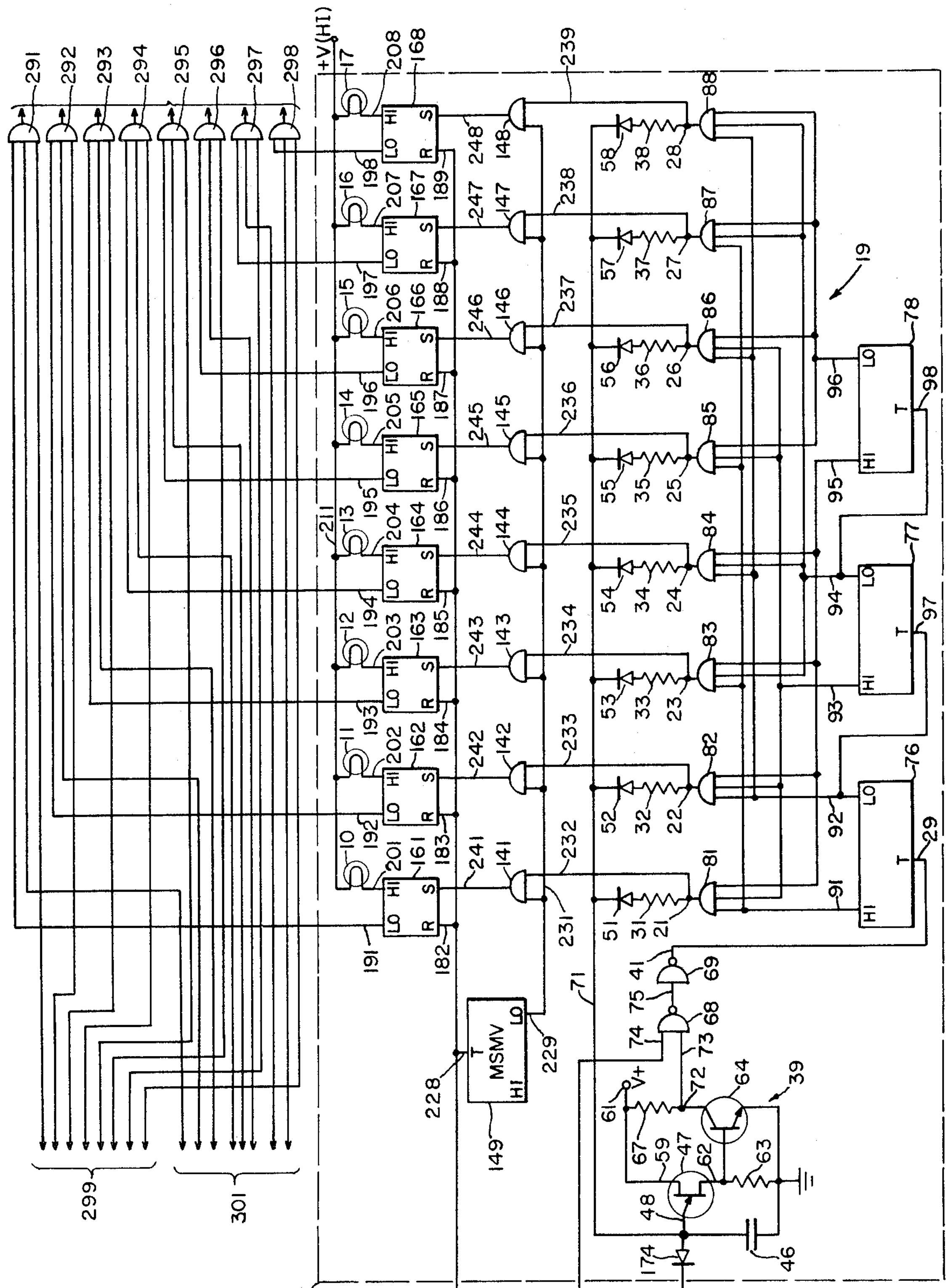

FIG. 2

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FIG. 3

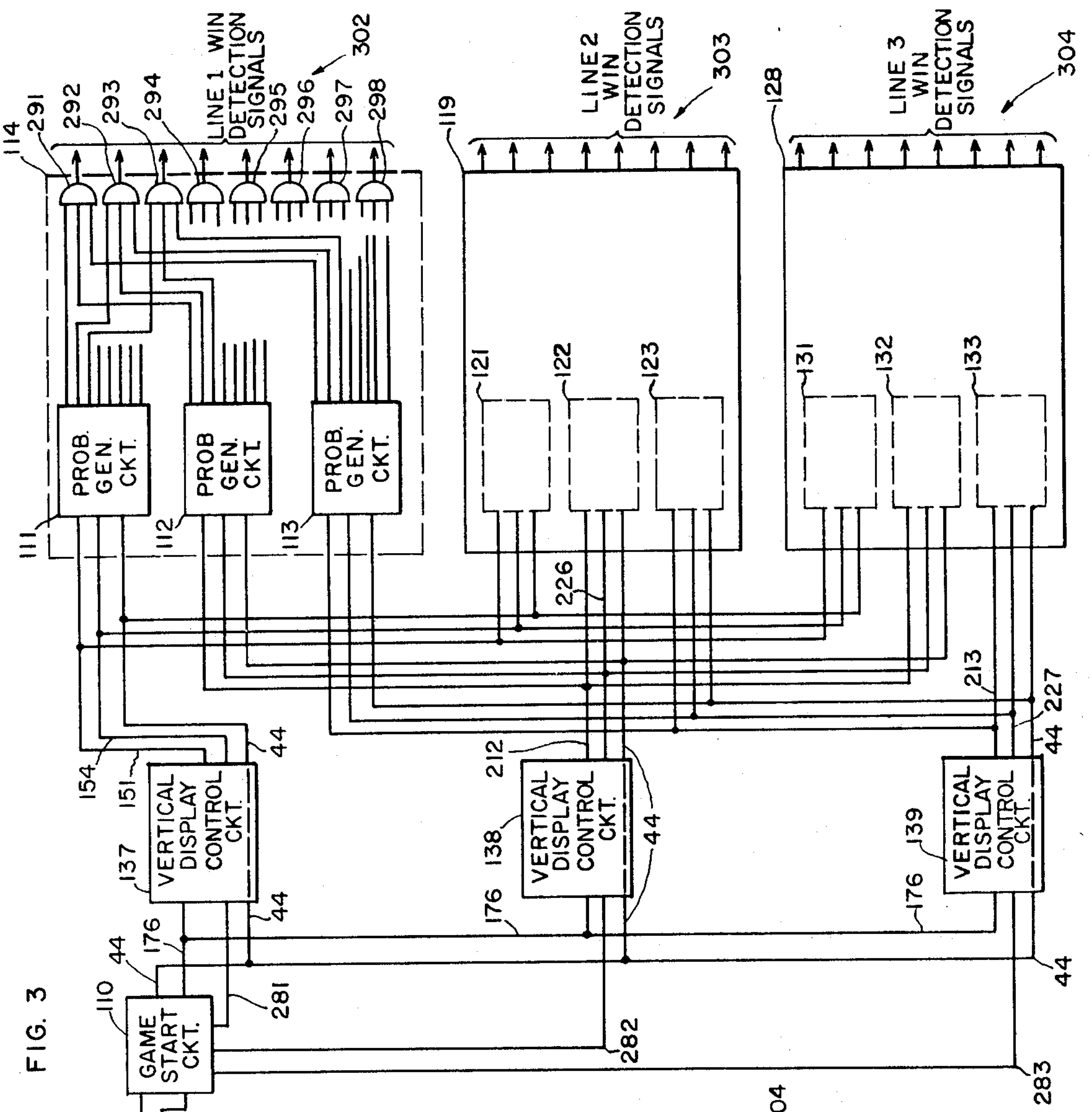


FIG. 4

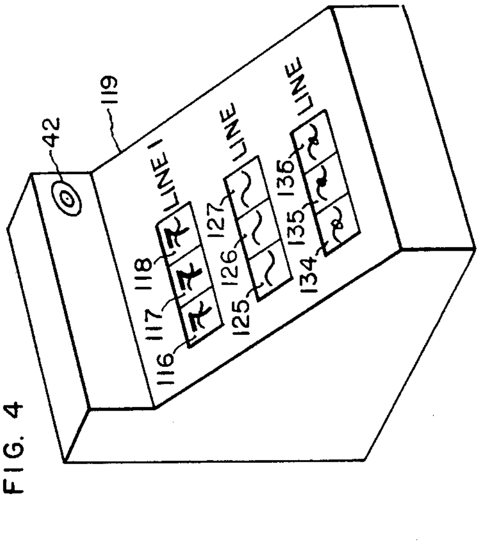
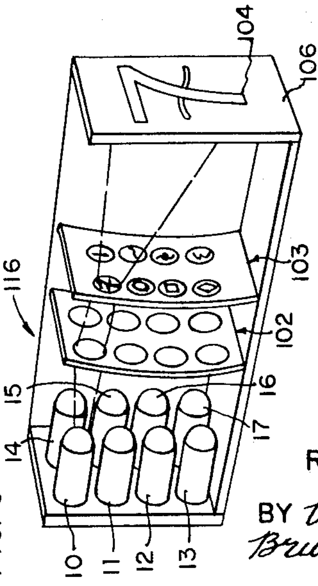


FIG. 5



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PROBABILITY-GENERATING SYSTEM AND GAME FOR USE THEREWITH

The present invention relates to method and apparatus for generating events having predetermined probabilities of occurrence and to game devices using such method and apparatus for games of amusement and entertainment.

The simulation of event occurrence by selecting an event from a field or set of possible events and controlling the probabilities or likelihood that any given event will be selected, is useful in the testing or use of certain game apparatus. Additionally, means for providing such simulation and probability control has valuable applications in the study of mathematics and statistics and in the statistical sampling of various data. While there exists a number of methods and apparatus for generating and controlling the probability of occurrence of events, they have been found to involve one or more disadvantages in their operation such as restrictions on their ability to provide a wide range of probabilities and to closely control these probabilities. For example, in game apparatus designed to provide the foregoing generation and selection of events and control of the probability of such selections, mechanical mechanisms are predominantly employed, but have been found limited or disadvantageous in a number of respects. These include short lifetime due to the frictional wear on the mechanical parts thus requiring constant repair or replacement and limitations on the ability to generate a wide range or spectrum of probabilities. The latter disadvantage or limitation is dictated by the impracticability of constructing larger and more precise mechanisms which might provide an increase in probability range. Attempts have been made to overcome these disadvantages, by employing various types of electrical circuits for simulating the operation of mechanical game apparatus and to thereby avoid the life-limiting frictional and mechanical wear. However, electronic or electrical circuits heretofore known have likewise been restricted in probability range, in this case due to the large number of expensive electrical components and extensive and intricate electrical wiring required to expand the available probability spectrum.

To appreciate the desirability of providing an extended probability spectrum, reference is made to a typical game situation. Given a set of four possible events designated as events A, B, C and D having the respective probabilities of occurrence of 1/10, 2/10, 3/10 and 4/10. Here, the probability spectrum is limited to a minimum probability of occurrence of one in ten for event A. In assigning game values to each event, the enjoyment of the game is maximized when the value of each event is approximately inversely proportional to the probability of its occurrence. Thus, event A is likely to be assigned a value of 9, B a value of 8, C a value of 7, and D a value of 6. It would be possible to assign event A a value of 100, leaving the remaining event values the same, however it is apparent that this would attenuate the enjoyment and excitement of the game by effectively decreasing the worth of scoring events B, C and D. On the other hand, assume that it is possible to expand the probability spectrum to provide event A with a 1 in 100 chance of occurrence while leaving the probability for events B, C and D the same. If such were the case, it is possible and in fact desirable to assign event A with a value of 100 and thereby not only preserve the effective worth of the lower valued events due to their substantially more frequent occurrence but also heighten the excitement of the game in view of the anticipation of scoring a very large value upon the occasional occurrence of event A, thereby enhancing the interest, amusement and enjoyment of game play.

It is noted in regard to the foregoing, that existing mechanical game apparatus and electrical simulations thereof, operate on a general principle of providing a plurality of individual mechanical or electrical states through which the apparatus may be rapidly cycled and eventually brought to rest in one of these states. The probability of the apparatus stopping in each state is generally equal. In order to provide a probability spectrum, each event of the game play is assigned or provided with one or more of the apparatus states. That is, several states are combined such that the occurrence of any one of such combined states provides the occurrence of a single common event of the game. Accordingly, the most likely event will be assigned the most number of states of the apparatus while the least likely event may be assigned only a single apparatus state. It will be apparent that this principle of operation limits the probability spectrum strictly to the number of available apparatus states. That is, the minimum probability that the machine can provide is one over the number of states. In order to increase the probability spectrum, it is obviously necessary to increase the number of states provided by the apparatus, yet such a provision has been found entirely impractical due to attendant increase in size, cost and complexity of the apparatus.

In view of the foregoing, it is an object of the present invention, to provide method and apparatus for the production and control of event occurrence probability, having a heretofore unobtainable large probability spectrum and to accomplish this objective in a relatively simple and low-cost manner.

It is another object of the present invention to provide an electrical circuit for generating and controlling the probability of event occurrence characterized by its capability of providing an extended probability range while employing only a few number of components for compact size and low-cost construction.

It is a further object of the present invention to provide a game apparatus of the type characterized, having an unusually large available probability range for greater versatility and diversification in scheduling winning events or combinations thereof, and thereby substantially enhancing the enjoyment, excitement and amusement of the game play.

It is another object of the present invention to provide such a game apparatus employing electronic control circuitry requiring a relatively few number of components all of which may be arranged in a housing of convenient compact size, consuming very little power, and operating reliably over long periods of substantially continuous use.

The invention possesses other objects and features of advantage, some of which with the foregoing will be set forth in the following description of the preferred form of the invention which is illustrated in the drawings accompanying and forming part of this specification. It is to be understood, however, that variations in the showing made by the drawings and description may be adopted within the scope of the invention as set forth in the claims.

IN THE DRAWINGS:

FIG. 1 is a combined schematic and block diagram of a portion of the control circuitry of the game apparatus of the invention;

FIG. 2 is a schematic diagram of a preferred embodiment of the probability-generating circuit of the present invention;

FIG. 3 is an overall block diagram of the control and probability-generating circuitry of a preferred embodiment of the game apparatus constructed in accordance with the present invention, which employs a combination of several of the basic circuits shown in FIGS. 1 and 2;

FIG. 4 is a perspective view of an assembled game apparatus housing the circuitry shown by FIG. 3 and employing a series of visual monitors representing the operation of such circuitry; and

FIG. 5 is an exploded perspective view of one of the visual monitors shown generally in FIG. 4, partially cut away for an interior view thereof.

In general, the present invention provides a novel method for generating a plurality of events which taken together form a given event set, and in response to an external control signal select an arbitrary one of such events wherein the probability of selecting each event is preprogramed. The uniqueness of the present method for accomplishing this result is best illustrated by means of the electrical circuitry shown in FIGS. 1 and 2, in which the various structural features and arrangements also embody the present invention. In this case, each of the above noted events is represented by an electrical signal in which a series of such event signals comprise a set of events. In the circuit embodiment of FIG. 2, each of the signals representing one event is sensed and displayed by one of lamps 10, 11, 12, 13, 14, 15, 16 and 17 wherein energization of any one of these lamps provides a symbolic display of the particular electrical signal and the event corresponding thereto which has been selected by operation of the circuit. In order to generate these events, make particular selection thereof and control the probabilities of such selections, the invention comprises in general a recycling electrical pulse counter indicated at 19 providing a succession of electrical counting states evidenced by the successive appearance of electrical signals at outputs 21, 22, 23, 24, 25, 26, 27 and 28 thereof. In operation, counter 19 is responsive at an input 29 thereof to the receipt of a series of electrical pulses to successively energize outputs 21 through 28, wherein a transition of the counter between states occurs upon receipt of each input pulse. Connected between outputs 21—28 and input 29 is a timing circuit, in this instance embodied by resistors 31, 32, 33, 34, 35, 36, 37 and 38 and an astable [free-running] multivibrator device 39 providing means responsive to each of outputs 21 through 28 of counter 19 to issue a pulse at an output 41 to input 29 and thereby advance the output state of the counter. Moreover, device 39 together with resistors 31 through 38 provide a timing operation by which a pulse will be issued to input 29 only after counter 19 has rested in any one of its given states for a time period individually preselected for that state. In other words, each of outputs 21 through 28 representing one of the counting states of counter 19 operates through its respective one of resistors 31 through 38 to cause astable device 39 to issue a pulse to input 29 for advancing the state of counter 19 only after a preset time delay dependent upon the state in which the counter is in, prior to the issuance of such pulse. Accordingly, counter 19 in response to device 39 continuously cycles through each of its counting states causing signals to appear in succession at outputs 21, 22, 23, 24, 25, 26, 27, 28 and back to output 21 to repeat the same cyclic sequence. Furthermore, by virtue of the operation of device 39 in conjunction with the values of resistors 31 through 38, the time duration of the signals occurring at each of the counter outputs may be selected to have a duration different than that of each of the remaining outputs such that during a continuing cyclic succession of counting states, each state will occupy a different time portion of the total lapsed time for a full cycle of states and thus the signals appearing at outputs 21 through 28 will likewise appear for differing lengths of time.

At this point in the operation, the circuitry of FIG. 2 has provided for the generation of a set of events, eight in this case, each event corresponding to the signal appearing at one of outputs 21 through 28 and for controlling the probability of selecting any one of the possible eight events. The actual event selection, takes place by interrupting the sequence of input pulses to input 29 of counter 19 at an arbitrary point in time [that is, at random] or by otherwise disabling the self-sustained cyclic operation of counter 19 and device 39. Upon such interruption the instantaneous condition of counter 19 is held in abeyance such that one of outputs 21 through 28 and the event corresponding thereto may be monitored. In this instance, and with reference to FIG. 1, such means for interrupting counter 19 is provided by a control switch 42 which, upon closure, actuates a set-reset bistable multivibrator 43 causing astable device 39 to be momentarily disabled via a line 44 connected therebetween. When device 39 thereby responds to operation of switch 42, the instantaneous state in which counter 19 is found will be momentarily sustained and the output signal from the corresponding one of outputs 21 through 28 may be sensed and monitored by energization of the associated one of lamps 10 through 17. Since the probability that counter 19 will be in any particular state when switch 42 is operated is directly dependent upon the foregoing preselected time duration of that state, the likelihood of selecting such event is precisely predictable and uniquely controlled.

It is noted that the probability of selecting any given event in the foregoing circuit operation is not limited or restricted by the total number of states which the apparatus provides, in this instance eight. That is, the probability control is dependent on the preselected time duration in which each state resides while the apparatus is continuously cycling through each of these states in succession. Accordingly, the probability range may be greatly extended between the least likely and most likely event occurrence by merely adjusting the time durations of the states corresponding thereto to be substantially different. By minimizing the required number of electrical states of the circuit and nevertheless greatly extending the available probability spectrum, the value of this circuitry and its method of operation to applications in mathematics, statistics and game devices is substantially enhanced.

Also it will be apparent that the operation of counter 19 in conjunction with astable device 39, provides for the selection of events, in which the probability of such selection and thus occurrence, corresponds to a true probability function. That is, for a finite number of selections, each being provided by the interruption of the otherwise self-sustained cyclic load of counter 19 and device 39, certain events may occur more frequently or less frequently than dictated by the expected probability of occurrence of such events for an infinite number of event selections. In this regard, it is noted that the full cycle time for counter 19 operating in response to time controlling resistors 31—38 and device 39 is preferrably less than the expected time interval between consecutive closures of switch 42. This design criteria provides that counter 19 will run through all of its states one or more times between consecutive actuations of switch 42, such that all of the possible event or switching states of counter 19 are available for selection each time. Such an operation will insure that the selections or occurrences conform to the above-noted true probability spectrum.

In the presently preferred embodiment of the probability selection circuit of FIG. 2, astable multivibrator device 39 together with output resistors 31 through 38 provide a particularly unique and convenient arrangement for controlling the time delay of each of the counter states. In general, the timing operation is provided by employing each of resistors 31 through 38 in individual succession as the resistive compliment of an RC timing network wherein the capacitance of such networks if provided by a single capacitor 46 so as to form a plurality of separate and different RC time constants for controlling the period of oscillation of astable multivibrator device 39. For this purpose, device 39 comprises a unijunction transistor 47 having an emitter electrode 48 connected to a junction of capacitor 47 with each of resistors 31 through 38 through a set of blocking diodes 51 through 58. A first base 59 of transistor 47 is connected to V+ at terminal 61 while a second base 62 is connected through a biasing resistor 63 and to a transistor driver 64. An output signal is developed between the collector electrode of transistor driver 64 and a biasing resistor 67 therefor which is applied to one input of a NAND gate 68 which responds thereto and issues a signal to output 41 through an inverter 69. In operation, as each of outputs 21 through 28 is energized with a positive voltage in succession, current is conducted through an associated one of resistors 31 through 38 and diodes 51 through 58 to develop a charge across capacitor 46 over a common line 71. When the charge relative to ground across capacitor 46 reaches a threshold value at emitter 48, transistor 47 switches to provide a low impedance path between emitter 48 and second base 62 such as to discharge capacitor 46 across resistor 63. The threshold value of charge potential required for this operation of unijunction transistor 47 is determined by the intrinsic standoff ratio thereof. Transistor driver 64 responds to the voltage pulse developed across resistor 63 and collector 72 thereof switches from HI to LO, wherein HI refers to the relatively high voltage logic state and LO refers to a relatively low voltage logic state. A first input 73 of NAND gate 68 accordingly switches from HI to LO in response to transistor driver 64 and with a second input 74 at a HI logic state at this time, gate 68 responds by switching from LO to HI at an output 75 thereof. This operation follows from the standard logic provided by NAND gate in which the output thereof will be low only when all of the gate inputs are HI and with any one or more inputs LO the gate output will be HI. Invertor 69 merely provides a logic state inversion between output 75 of gate 68 and output 41 which is connected to input 29 of counter 19. Thus, upon each switching operation of unijunction transistor 47 in response to a threshold charge reached by capacitor 46 there is issued to input 29 of counter 19 a pulse having a logic state transition from HI to LO. After capacitor 46 is discharged pursuant to this switching characteristic, unijunction transistor 47 automatically and quickly returns to a normal condition in which the impedance between emitter 48 and the second base 62 is very high permitting capacitor 46 to be recharged and the sequence repeated.

As an example of the self-sustained and continuous operation of this portion of the circuit, let it be assumed that counter 19 is in a first state in which output 21 exhibits a logical HI state, in this instance evidenced by a relatively high positive voltage. Immediately upon entering this first state, current flow occurs through resistor 31 and forward biased diode 51 over line 71 charging capacitor 46 which, upon reaching the above noted threshold value, causes a switching operation resulting in the issuance of a pulse or logic state transition from HI to LO at input 29 of counter 19. Counter 19 responds thereto and advances to a second counting state in which output 22 is in a HI logic condition. In the meantime, capacitor 46 has been discharged and unijunction transistor 47 returned to its normal "off" condition. With output 22 now providing a relatively high positive voltage, current flows through resistor 32 and diode 52 over line 71 to charge capacitor 46 repeating the above operation and causing counter 19 to again advance its counting state whereby output 23 is driven to a high logic state. This sequence continues through outputs 24 through 28 and returns to output 21 whereupon another cycle is initiated such that counter 19 is in this sense a recycling counter responsive to successive pulses received at its input 29. As only one of outputs 21 through 28 is HI at a time, only one of resistors 31 through 38 at any time is effective for charging capacitor 46. In this regard, diodes 51 through 58 serve to prevent current from flowing from one of outputs 21 through 28 which is HI to the remaining such outputs, all of which are LO.

Thus, in order to individually preset the time portion in which each of the states of counter 19 remains during a complete counting cycle, the values of resistors 31 through 38 are selected to provide different impedance values to thereby regulate the amount of charging current issued to capacitor 46 and thus regulating the time lapse required for charging capacitor 46 to the threshold switching potential above noted. For example, if resistor 31 were selected to have an impedance one one-hundredth as large as resistor 32, then output 21 would be high one one-hundredth of the time compared with that of output 22. In programming a desired probability range, i.e., selecting the relative time durations of each of outputs 21 through 28, it is merely necessary to select a suitable time period for completion of a full cycle of counting states. (The successive advancement of counter 19 through eight states in this case corresponds to a full cycle.) Using such a full-cycle time period, which is preferably less than a second and most advantageous at around 10 to 15 milliseconds, a composite impedance may be calculated to simulate all of resistors 31 through 38 taken together to this desired full-cycle period. Then, for example, assuming a value of one meg. ohms for this composite resistance, each of the values of resistors 31 through 38 is calculated to provide a fraction or proportion of one meg. ohms in accordance with the desired probability of selection for each counting state or event. Thus, a typical probability spectrum might provide that output 21 has a 50 percent probability of being selected, output 22 a 17 percent probability, output 33 a 15 percent probability, output 34 a 10 percent, output 36 a 5 percent, output 37 a 2 percent, and output 38 a 1 percent. From this schedule, the values of resistors 31 through 38 may be selected to respectively equal 500 K (K=1000) ohms, 170 K ohms, 150 K ohms, 100 K ohms, 50 K ohms, 20 K ohms, and 10 K ohms.

By virtue of this preferred circuitry arrangement, in which the plurality of RC delay or timing networks is provided by a single capacitor 46 together with a plurality of separate resistors 31 through 38, extremely precise control is obtained over the proportional and relative time spans for each electrical state of counter 19. That is, as the single capacitor 46 is common to all of the effectively different RC networks, the timing operation is dependent only on the individual values of resistors 31 through 38, which may be selected within close tolerances and which do not exhibit substantial variation in impedance over long periods of time. Thus, even though it may be difficult to control the capacity value of capacitor 46, the precision and stability of the impedances of resistors 31 through 38 allow accurate and reliable control over the probabilities of signal or event selection.

As shown in FIG. 2, counter 19 is most advantageously provided by a binary counter portion, consisting in this instance of bistable multivibrators 76, 77 and 78 and a logic decoding matrix or circuit, here provided by a plurality of three input AND gates 81, 82, 83, 84, 85, 86, 87 and 88. Utilizing three such multivibrators 76, 77, and 78 in this case provides a total of eight possible binary states in response to pulses received at input 29 of multivibrator 76 wherein AND gates 81 through 88 decode these binary states to provide a plurality of individual or separate outputs 21 through 28, each such output corresponding to one binary count state. Outputs 91, 92, 93, 94, 95 and 96 of multivibrator 76—78, are shown with Hi and LO designations in FIG. 2 corresponding to the condition of multivibrator 76—78 in a first binary counting state. The various inputs of AND gates 81—88 are connected in a known manner to receive outputs 91—96 such as to successively and exclusively drive each of outputs 21—28 of the AND gates HI in accordance with predetermined combinations of the voltage conditions [HI or LO] of the outputs from multivibrator 76—78. Output 92 of multivibrator 76 is connected to a trigger input 97 of multivibrator 77 and output 94 thereof is in turn connected to a trigger input 98 of multivibrator 78 such that the multivibrators are interconnected to continuously cycle through the various binary counting states in response to pulses received at input 29 of multivibrator 76. In operation, each of trigger inputs 29, 97 and 98 (also designated in FIG. 2 as T) is responsive to input signal transitions from HI to LO, which in the case of input 29 is provided by output 41 in response to discharge of capacitor 46 by unijunction transistor 47. By virtue of the preferred binary structure and operation of counter 19, together with the timing circuit means provided by resistor 31—38 and astable device 39, only a relatively few number of components is employed to achieve an unusually large and thus advantageous probability range. When a number of these basic probability-generating circuits are combined, as in the case of several useful applications, the advantages of small size and low power consumption made possible by the minimal number of components, are apparent.

With reference to FIGS. 1, 2 and 3, the circuitry thus far described is employed by the present invention as a portion of the control circuitry for a game apparatus. For this purpose, each of lamps 10 through 17, which as mentioned above may be energized in response to the selection of an associated output event signal from counter 19, is arranged in a rearview projector 116 best shown in FIG. 5. Projector 116 is comprised of a lens system 102, a film system 103 and a rearview screen 106 for responding to energization of any one of lamps 10—17 to display a preselected symbol 104 on screen 106. The projector is constructed such that the source of light from each of lamps 10 through 17 when individually energized is directed through a single lens of lens system 102 and a single film of film system 103 to project a desired symbol 104. In this manner, means are provided for rapid, convenient visual monitoring of a signal output selected from counter 19 corresponding to one of the possible events. Furthermore, according to game play, each of the event symbols displayed by projector 116 pursuant to operation of the circuit shown in FIG. 2 is assigned a particular value or worth, whereupon the occurrence of higher valued event symbols pursuant to a selection made by actuating switch 42 of FIG. 1 will result in successful or winning game play. In this regard, in order to enhance the excitement and amusement of the game, the higher valued event symbols are preferably associated with lower probabilities of occurrence as controlled by the selection of resistors 31—38 of FIG. 1, each being associated with one event symbol as above discussed.

A preferred embodiment of the game apparatus pursuant to the present invention is provided by employing a plurality of probability generating circuits, each one being identical to circuit 111 shown in FIG. 2, and furthermore providing a corresponding plurality of projectors of the type shown in FIG. 5, one projector being associated with each such probability generating circuit. Such an embodiment of the present invention is best illustrated in FIGS. 3 and 4, wherein each of probability-generating circuits 111, 112, and 113 is combined in a first line control circuit 114 for operating respectively projectors 116, 117 and 118 mounted in a game housing 119 as shown in FIG. 4. In a similar manner, a second line control circuit 119 shown in FIG. 3 includes probability-generating circuits 121, 122 and 123 (shown in Phantom) for controlling projectors 125, 126 and 127 again shown in FIG. 4. A third line control circuit 128 similarly provides probability control circuits 131, 132 and 133 (shown in phantom) for operating projectors 134, 135 and 136. As will be described in further detail, each of the probability-generating circuits of line control circuits 114, 119 and 128 provides for concurrent event symbol generation and selection in response to each game play which is initiated by actuating switch 42 of a start circuit 130 (see FIGS. 1 and 3). Furthermore, the occurrence of certain combinations of events, as visually represented by the displayed symbols of projectors 116—118, etc., may be electrically sensed in a predetermined fashion such that game play can be dependent not only on the occurrence of individual events from one of the probability-generating circuits as described in regard to FIG. 2 for circuit 111, but may also depend upon the simultaneous occurrence of selected combinations of particular events, each being selected from several separate event sets. For example, a win may require that projectors 116 and 117 and 118 of line 1 provide the concurrent display of three identical symbols such as shown in FIG. 4. If such a composite event occurs, this will mean that each of the recycling counters of probability-generating circuits 111—113 corresponding to counter 19 of circuit 111 as shown in FIG. 2 will have interrupted their counting sequence at corresponding event states. As will be described herein, the combination of electrical output signals corresponding to the winning combination of symbols displayed by the projectors may be detected, and in response thereto provide an output signal for rewarding or recording the score of the successful play. Furthermore, by virtue of the minimal number of components required for the probability-generating circuits, it has been possible as shown in FIG. 4 to provide three sets of games (corresponding to lines 1, 2 and 3) combined in a single compact housing 119 in which each game set is comprised of three projectors representing three separate sets of possible events. Each of the game lines, lines 1, 2 and 3, may be played separately or any two of the three games played concurrently or, as described herein, all three games may be played concurrently for maximum amusement and game interest.

While the preferred provision for monitoring each of the event states by projectors 116—118, 15—127 and 134—136 may be provided by merely connecting each set of lamps for each projector to the output terminals of each associated counter circuit, such as connecting lamps 10—17 of projector 116 shown in FIG. 5 directly to outputs 21—28 of counter 19 for circuit 111 shown in FIG. 2, it has been found that such an arrangement may be unsatisfactory due to the preferred high-speed cycling of counter 19 and due to the large power consumption which would result from continuously turning the monitor light sources on and off during sustained cycling of each associated counter. For this purpose, electrical gating means are connected between outputs 21 through 28 of counter 19 and lamps 10—17 of probability generating circuit 111 to permit the lamps to respond to the output counter states only during a short pretimed period of each game play. The gating means in this instance are provided by AND gates 141, 142, 143, 144, 145, 146, 147 and 148 together with a monostable multivibrator device 149 as shown in FIG. 2. Monostable multivibrator 149 is connected over a line 151 to the vertical display control circuit 137 shown in FIG. 1 for responding to the operation of a bistable multivibrator 152 which in turn is initially responsive to the switching state of multivibrator device 43 of circuit 110.

The pulse source for driving counter 19 through its cyclic states during the above-noted timed display period is provided by a free-running astable multivibrator device indicated at 153 of circuit 137 which supplies a sequence of driving pulses through multivibrator 152, over a line 154 to circuit 111 shown in FIG. 2 and particularly to input 74 of NAND gate 68 for driving counter 19. A binary counting unit indicated at 156 of FIG. 1 provides for counting the number of pulses issued by multivibrator 152 in response to free running multivibrator 153 during the game play display period and in response to a preset maximum pulse count. Binary counter 156 operates to terminate the display period by actuating a NAND gate 157. To provide for storing and thus sustaining visual display of the selected event symbols by projectors 116—118, etc., each of the probability-generating circuits is provided with a series of set-reset bistable devices such as devices 161, 162, 163, 164, 165, 166, 167 and 168 for circuit 111 as shown in FIG. 2. With reference to FIG. 3, each set of three probability-generating circuits, such as circuits 111—113, is provided with a separate vertical display control circuit 137, 138, and 139. The details of each of these identical circuits are shown for control circuit 137 of FIG. 1 wherein each such circuit functions to provide a simulated flashing display of the various possible event symbols provided by projectors 116—118, 125—127 and 134—136 during the game play. In general this is accomplished by driving each of the counters corresponding to counter 19 of circuit 111, shown in FIG. 2 for each of probability circuits 111—113 and 121—123 and 131—133, through a slow counting sequence for several full counting cycles in which the various output lamps such as lamps 10—17 of circuit 111, are successively pulsed. In response thereto each of the projectors of the game apparatus shown in FIG. 4 flashes each of the possible event symbols in close succession. Furthermore, control circuits 137—139 are adjusted to provide different flash display periods associated with each vertical column of projectors as arranged in game housing 119 of FIG. 4. For example, vertical display circuit 137 is jointly connected to probability-generating circuits 111, 121 and 131 respectfully associated with projectors 116, 125 and 134 such that the flashing display period of this left hand column of projectors will last for a given period of time determined by circuit 137. On the other hand, the column of projectors comprised of projector 117, 126 and 135 will have a flashing display period different from that of the left-hand column and is controlled by vertical display circuit 138 connected for joint operation of probability-generating circuits 112, 122 and 132. Similarly, the right-hand column of projectors as arranged in FIG. 4 will have still a different flashing display period determined by control circuit 139 operating circuits 113, 123 and 133. As will be described herein, at the termination of such display periods, the projectors provide a sustained display of the particular event symbols selected therefor to indicate to the player the value of his score, if any. Accordingly, the time periods of control circuits 137—139 are adjusted such that the left-hand column has the shortest flashing display period, the center column of projectors a slightly longer flashing display period and the right-hand column of projectors being provided with the longest display duration. In this manner, the excitement of the game is increased as the player must wait for each column of projectors to come to rest in sequence from left to right in order that he may determine whether the play has been successful.

Considering now the complete operating sequence of the circuits shown in FIGS. 1, 2 and conjunction with the game device shown in FIG. 4, the order of circuitry operation is as follows. Initially, and prior to game play, each of probability-generating circuits 111—113 and 121—123 and 131—133 is in a mode of operation in which its associated recycling counter, such as counter 19 of circuit 111 of FIG. 2, is in a continuous free-running variable-timing condition as above described. At the same time, the lamps of each of projectors 116—118 and 125—127 and 134—136 are electrically disengaged from the outputs of each counter by gating means, such as AND gates 141—148 as shown in FIG. 2 for circuit 111. Furthermore, the last selected signal event or counting state obtained from each counter is stored by set-reset bistable devices such as devices 161—168 providing for operation and storage of an associated one of lamps 10—17 for projector 116 and circuit 111 in this instance.

The game is initiated when manually operated switch 42 is closed causing a set input 171 of bistable device 43 to go from LO to HI. In response thereto, device 43 changes state, with a normally high output 172 switching LO and a normally LO output 173 switching HI. The signal transition at output 172 of device 43 is extended over a line 44 and jointly each of control circuits 137—139 and probability-generating circuits 111-—113, etc., to terminate the cycling operation of each of the recycling counters such as counter 19 of circuit 111 as shown in FIG. 2. This is accomplished, as shown in FIG. 2, by applying the LO logic signal to a diode 174 having its cathode connected to line 44 and its anode joined to emitter 48 of unijunction transistor 47 of astable device 39, thus inhibiting the response of device 39 to the outputs of counter 19. As above mentioned, the free-running and variable-timing operation of device 39 is now interrupted whereby counter 19 is disposed in one of its counting states as represented by one of outputs 21—28 exhibiting a HI logic signal. At this operating stage, an event has thereby been selected from each of the counters corresponding to counter 19 for circuits 111—113 and 121-—123 and 131—133.

At this same time, the logical state transition from LO to HI at output 173 of device 43 is extended over a line 176 to the cathode of a diode 177 for initiating operation of free-running device 153 and to a set input 178 of bistable multivibrator 152, both of vertical control circuit 137. Line 176 is likewise connected to corresponding components of identical control circuits 138 and 139 which for the purpose of simplification are illustrated in block diagram form in FIG. 1. In response to this operation, multivibrator 152 switches state, causing a normally LO output 179 thereof to go HI and a normally HI output 181 to go LO, wherein these logic signal transitions are extended over lines 151 and 154 respectively to probability-generating circuit 111 of FIG. 2.

Each of bistable devices 161—168 as shown in FIG. 2 for circuit 111 and like sets of devices for each of the other probability-generating circuits 111, 121 and 131 as shown in FIG. 3, respond to the LO to HI transition at output 179 of multivibrator 152 at reset inputs 182—189 to assume a normal state in which outputs 191—198 are LO and outputs 201—208 are HI. Since one side of lamps 10—17 is jointly connected via a common line 211 to V+ [HI], these lamps are turned on only when an associated one of outputs 201—208 goes LO. Thus, the initial switching transition of multivibrator 152 in response to closure of game start switch 42 causes all of lamps 10—17 of circuit 111 and projector 116 to be initially turned off. Likewise, lines 212 and 213 respectively of circuits 138 and i39 corresponding to line 151 of circuit 137 provide an initial LO to HI signal transition jointly in response to closure of switch 42 thereby causing all of the projector lamps associated with probability-generating circuits 111—113 and 121—123 and 131—133 to turn off at this stage of operation.

Concurrently therewith, diode 177 as shown in FIG. 1 is immediately reverse biased as output 173 of device 43 goes HI in response to closure of switch 42, permitting circuit 153 to enter upon a free-running switching mode of operation in which an output 214 thereof issues a continuous train of pulses to a trigger input 216 of multivibrator 152. Specifically, the switching of diode 177 to a reversed biased mode allows a junction 217 of device 153 to assume a positive voltage with respect to ground by charging of a capacitor 218 connected to a unijunction transistor 222. The principle of operation of astable device 153 is similar to that described for astable device 39 of FIG. 2 except for the employment of a single permanently connected charge current regulating resistor 219 which provides a constant switching period for device 153 as opposed to the variable switching period of device 39 as discussed in regard to FIG. 2. A driving transistor 223 together with a biasing resistor 224 is responsive to the periodic pulse output provided across a resistor 221 to issue the aforementioned pulse train at output 214.

As noted above, the constant period pulse output of device 153 provides for driving each of the counters corresponding to counter 19 of each of probability-generating circuits 111, 121 and 131 at a relatively slow rate through a predetermined number of full counting state cycles in which the projector lamps corresponding thereto are sequentially flashed for a game display effect. This constant period relatively low frequency pulse train drive is provided at output 181 of multivibrator 152 in response to HI to LO logic state transitions received at trigger input 216 from output 214 of device 153. The pulse train thus provided at output 181 is extended over line 154 to an input 74 of NAND gate 68 of FIG. 2 whereupon it is applied to input 29 of counter 19 and through identical circuit arrangements found in probability-generating circuits 111, 121 and 131 as shown in FIG. 3. Likewise, multivibrator outputs from circuits 138 and 139 as shown in FIGS. 1 and 3 corresponding to output 181 of circuit 137 are extended over lines 226 and 227 respectively to probability circuits 112, 122, 132 and circuits 113, 123, 133 respectively.

The operation of each of the recycling counters of each of the probability-generating circuits is essentially identical, and thus will be described in detail in regard to probability generating circuit 111 shown in FIG. 2. In response to the initial output signal transition provided at output 181 of multivibrator 152 which is extended over line 154 to NAND gate 68, counter 19 advances one state beyond the originally selected event signal state pursuant to interruption of device 39 on closure of switch 42. For example, assume that counter 19 pursuant to interruption of device 39 is stopped in its first counting state corresponding to output 21 thereof exhibiting a HI signal condition. Soon thereafter, output 181 of multivibrator 152 (FIG. 1) goes from HI to LO also in response to closure switch 42 causing output 75 of NAND gate 68 to go from LO to HI, whereupon inverter 69 causes input 29 of counter 19 and specifically the input of bistable multivibrator 76 to go from HI to LO advancing counter 19 to a second state in which output 22 thereof is HI. Also, immediately following this, astable device 153 of FIG. 1 is activated and issues a series of pulses through multivibrator 152 over line 154 as above discussed causing counter 19 to progressively advance through each of its counting states similar to its operation in response to device 39, except in this instance exhibiting a constant period of rest in each state and a substantially slower cycling rate.

During this operating stage, lamps 10—17 are connected through AND gates 141—148 in the following manner for responding to the cyclic state transitions of counter 19. Line 151 is connected to a trigger input 228 of monostable multivibrator 149 which has a normally low output 229 jointly connected to one of the pair of inputs to each of AND gates 141—148 over a line 231. The remaining input of each of gates 141—148 is connected individually to one of outputs 21—28 of counter 19 over lines 232, 233, 234, 235, 236, 237, 238 and 239. Normally, output 229 is in a LO logic condition and thus AND gates 141—148 prevent communication of the signals emitted at outputs 21 through 28 from reaching set inputs 241, 242, 243, 244, 245, 246, 247 and 248 of bistable devices 161—168 respectively. However, as switch 42 is closed at the start of the game, trigger input 228 of monostable multivibrator 149 periodically responds to each HI to LO signal transition of multivibrator 152 provided over line 151 to issue short duration HI going pulse at output 229. Each of these HI pulses momentarily gates each of AND gates 141—148 to pass the instantaneous signal condition at outputs 21—28 of counter 19 to set inputs 241—248 of bistable devices 161—168. In response to each gating signal one of devices 161—168 is switched from a normal reset condition in which its associated one of outputs 191—198 is LO and the associated one of outputs 201—208 is HI to a set condition in which the logic states are reversed. Also, at a time between each gating pulse issued at output 229 of multivibrator 149, all of devices 161—168 are switched to their reset condition by LO to HI signal transistions from multivibrator 152 received at reset inputs 182—188. Thus, each of devices 161—168 is successively switched to its set condition in response to the states of counter 19 in which associated lamps 10— 17 are energized, thereby providing a rapid successive flashing display of all of the event symbols carried by projector 116 as best shown in FIG. 5 and including lamps 10—17. Similarly, each of probability-generating circuits 112—113 and 121—123 and 131—133 and vertical control circuits 138 and 139 as shown in FIG. 3 concurrently provide this operation causing each of projectors 116—118 and 125—127 and 134—136 as shown in FIG. 4 to project in rapid succession each of its symbols.

To provide means for terminating this display period, output 179 of multivibrator 152 as shown in FIG. 1 is also extended over a line 251 to a trigger input 252 of a first in line bistable device 253 of binary counter 156. Counter 156 comprises in addition to device 253, devices 254, 255, 256 and 257. Each of the normally LO outputs 261, 262, 263 and 264 is connected to the trigger input of the next in line binary device, in this instance comprising trigger inputs 266, 267, 268 and 269 respectively. Normally HI outputs 271, 272, 273 and 274 of devices 253—256 and a normally LO output 276 of device 257 are individually connected to a corresponding number of inputs of NAND gate 157 for detecting a predetermined maximum count at an output 277 thereof. That is, counter 156 together with gate 157 responds to a preselected number of input pulses received over line 251 from multivibrator 152, in this instance 16 such pulses, to issue at output 277 a logic state transition from HI to LO. Upon such an occurrence, a diode 278 connected with its cathode to output 277 and its anode to junction 217 is responsive thereto to assume a forward bias condition essentially shorting junction 217 to ground and terminating the free-running operation of astable device 153.

At the end of the display period, which occurs when counter 156 reaches the aforementioned preselected maximum pulse count of those pulses issued by multivibrator 152 to counter 19, one of lamps 10 through 17, corresponding to an initially selected state of counter 19, is energized and sustained in such a condition until the next game is played. For this purpose, the maximum pulse count provided by counter 156 is selected to cause counter 19 to cycle through one or more full cyclic states such that upon termination of the display period counter 19 has returned to the initially selected event state thereof. For example, assume that astable device 39 is interrupted when counter 19 is in a first state in which output 21 is HI. Immediately thereafter multivibrator 152, also in response to closure of switch 42, switches states and issues a pulse over line 154 causing counter 19 to advance one state and causing counter 156 to receive a pulse over line 251 causing it to register a first count. Thereafter, free running astable device 153 takes over and issues a succession of pulses over lines 154 and 251 concurrently causing both counters 19 and 156 to advance in counting states. By selecting counter 156 to have a maximum pulse count equal to a multiple of the total number of states provided by counter 19, in this instance 16 and eight respectively, astable device 153 will drive counter 19 through one or more full cycle counts (in this example two full cycles) before counter 156 disables device 153 via NAND gate 157 and diode 278 stopping counter 19 in its initially selected output state, in this instance output 21.

By this arrangement, the circuitry of FIGS. 1 and 2 has been greatly simplified by employing counter 19 for two separate purposes, one purpose being for probability generation and event selection in which it operates in conjunction with astable device 39 and a second purpose for cycling lamps 10 through 17 through a display sequence in which counter 19 operates in conjunction with astable device 153 and counter 156. It has been mentioned that during the display period, counter 19 is advanced through its states at a relatively slow rate as compared with its normal cycling time in conjunction with astable device 39. For this purpose, it has been found to be preferable to adjust free-running device 153 to have a switching period of around 50 to 60 milliseconds, thus permitting sufficient time to turn lamps 10—17 on and off in succession during the display sequence. It is noted that this switching period is substantially slower than the average switching period of astable device 39, the latter of which is on the order of 10 —13 millisecond/eight counting states or about 1.5 millisec.

As noted above, it is desirable to have the display periods for each vertical column of projectors as seen in FIG. 4 last for different times, specifically wherein the left-hand column of projectors terminates the flashing display period first, then the center column of projectors and finally the right-hand column of projectors. For this purpose, vertical display control circuit 137 has been selected in this instance to have its counter 156 provide a maximum of 16 counts before disabling astable device 153 and terminating the display period for probability-generating circuits 111, 121 and 131 as seen in FIG. 3 respectively associated with projectors 116, 125 and 134 as shown in FIG. 4. Vertical display control circuit 138 on the other hand is provided with a counter corresponding to counter 156 having a maximum count of 24 such as to allow probability-generating circuits 112, 122 and 132 to generate a longer display period for associated projectors 117, 126 and 135 occupying the center column. Similarly, vertical control circuit 139 is provided with a counter corresponding to counter 156 having a total count maximum of 32 causing probability-generating circuits 113, 123 and 133 to drive projectors 118, 127 and 136 through the longest display period.

Furthermore, in order to avoid too large a pulse power drain on the power supply (not shown) for operating the circuit of FIG. 3, it is preferred that each of the free-running astable devices, such as device 153, for each of circuits 137—139 be provided with slightly different switching periods such that the lamps for each column of projectors as shown in FIG. 4 are not turned on and off in unison.

At the end of each display period the bistable devices corresponding to devices 161—168 of circuit 111, shown in FIG. 2 for each of the probability-generating circuits of FIG. 3, respond to the instantaneous output state in which the associated recycling counter, corresponding to counter 19 of FIG. 2, comes to rest. This will correspond to the initially selected state of such counter provided by closure of switch 42 when operated to initiate a game. By this operation, one of devices 161—168 will be disposed by a selected one of outputs 21—28 in a set condition pursuant to a pulse received at an associated one of set inputs 241—249 via the gating operation of AND gates 141—148. Accordingly, the selected signal event is stored by devices 161—168 and sustains the selected event lamp in an on condition for continuous displayed projection of the symbol corresponding thereto by an associated projector shown in FIG. 4. After the display sequence of all of the probability-generating circuits and associated projectors has terminated, start circuit **110** is restored to its original normal condition for responding to a subsequent closure of switch **42** and the start of another game.

To provide this termination of game play and restoration of the circuit for a subsequent game, the output of each NAND gate from control circuits **137—139**, such as output **277** of NAND gate **157** of control circuit **137**, is fed over lines **281**, **282** and **283** respectively to a three input NOR gate **284** as shown in FIG. **1**. As each of lines **281'283** go LO in response to the termination of display periods associated with each of circuits **137—i39**, the corresponding inputs to NOR gate **284** sequentially go LO and when all such inputs exhibit a LO condition an output **286** of gate **284** goes HI in accordance with standard NOR logic. Output **286** is connected to a reset input **287** of bistable device **43**. Thus, after all of the display periods associated with vertical control circuits **137** through **i39** terminate, input **287** is driven HI resetting device **43** to its initial normal condition in which output **172** is HI and output **173** is LO.

While the player will be able to observe whether he has achieved a winning combination of event occurrences, as seen from the displayed symbols provided by projectors **116—118** and **125—127** and **134—136** of FIG. **4**, it is many times desirable to electrically detect winning combinations and, in response thereto, to provide an electrical signal for operating a scoring device or, if desired, rewarding the player with a prize, or the like. For this purpose, and with reference to FIG. **2**, each of the normally low outputs **191—198** of bistable devices **161—168** is individually connected to one input of a plurality of AND gates **291—298**. Furthermore, the remaining pair of inputs of each of these AND gates is connected as indicated at **299** and **301** to separate corresponding outputs of other probability-generating circuits identical to those shown in FIG. **2**. Accordingly, if pursuant to game play, all three inputs of one of AND gates **291—298** go HI pursuant to a preselected combination of event signals, each of the three signals being taken from one of eight outputs in this instance of each probability-generating circuit, then an output from such AND gate will issue a HI signal indicating that a winning combination has been registered. This signal may in turn be used for actuating a number of output devices, such as a scoring apparatus, which accumulates consecutive scores registered for several plays. This circuit arrangement is also illustrated in FIG. **3**, wherein AND gates **291—298** are responsive to the combined outputs of probability-generating circuits **111—113** of a first line control circuit **114**. Second and third line control circuits, **119** and **128** in this instance, are similarly provided with a series of win combination detecting AND gates (not shown) such that winning combinations along the horizontal projector rows as shown in FIG. **4** for lines **1**, **2** and **3** may be detected. At variance with this arrangement, it will be appreciated that any number of winning detection circuit arrangements may be provided and accordingly a wide variety of game plans may be designed. For example, it is possible to combine the output win detection signals indicated at **302**, **303** and **304** from circuits **114**, **119** and **128** respectively into a compounded win detection circuit, using logic components similar to or the same as those of AND gates **291—298**, to provide a game play which is dependent upon the occurrence of certain combinations of symbols on all of lines **1**, **2** and **3**.

While the circuitry of the invention illustrated in FIGS. **1** and **2** has been shown in terms of generalized logic symbols for the purpose of convenience, it will be appreciated that there are a number of available devices for accomplishing these basic logic and switching functions. For example, AND gates **141—148** and **291—298** are conveniently and economically provided by appropriate diode matrix logic as is well known in the art. In a similar manner, each of bistable devices **161—168** may be provided by a simple SCR circuit biased to provide bistable state operation as required for storing electrical signals in accordance with the foregoing disclosure.

I claim:

1. Apparatus for generating a set of possible events and selecting an event therefrom at random, wherein each such event may have an individual predetermined probability of being selected comprising,

a recycling electrical pulse counter providing a succession of electrical counting states at an output thereof in response to electrical pulses received at an input thereof wherein each said state is designated as one of said events,

timing circuit means connected to said counter and responsive to said counter output being in each state for a time duration selected for that state to issue one said pulse to said counter input advancing the state thereof comprising an astable multivibrator having a plurality of RC timing networks for providing a corresponding plurality of switching periods therefor and having an output connected to said counter input for issuing one said pulse thereto after each said switching period, and means connected to said counter output and being responsive in succession to each said state thereof to effectively connect a separate one of said networks to said multivibrator, and

means for interrupting the advancement of said counter at random whereby the one of said states occurring at such interruption represents a selection of a corresponding one of said events.

2. The apparatus defined in claim **1**, wherein said counter output is provided by a set of separate outputs each for issuing a signal representing one of said counter states, said RC networks being formed by a single capacitor connected to said multivibrator and a plurality of resistors individually connected at one of their ends to said set of outputs and a plurality of diodes individually connected between the other ends of said resistors and said capacitor and being responsive to said signals appearing in succession at said separate outputs to effectively connect an associated one of said resistors to said capacitor.

3. The apparatus defined in claim **2**, said counter comprising a plurality of bistable devices interconnected to provide a sequence of binary count states, a decoding circuit connected to said devices and having a plurality of output terminals providing said set of separate counter outputs each issuing an electrical signal in response to one of said binary count states.

4. The apparatus defined in claim **1**, said astable multivibrator comprising a unijunction transistor having first and second electrical conditions and being connected and responsive to each of said RC networks in succession to switch between its first and second condition to issue one of said series of pulses to said counter input.

5. The apparatus defined in claim **1**, for use as a game of amusement and further comprising,

electrically operated monitor means for visually displaying a representative symbol of each said event, said monitor means being connected to said counter output and responsive to each state thereof to display a symbol corresponding to the event associated with that counter state.

6. The apparatus defined in claim **5**, and

bistable means connected to said monitor means for operating and storing each display symbol thereof,

gating means connected between counter and bistable means for setting said bistable means in response to said counter output, said gating means being connected to and operated by said means for interrupting the advancement of said counter such that the states appearing at said counter output upon such interruption is passed by said gating means to and for setting said bistable means to store and display an associated one of said symbols.

7. The apparatus defined in claim **6**, and pulse generator and cooperating timeout counter means for driving said counter through one or more full cycles of counting states in response to said means for interrupting advancement of said counter by said timing circuit means such that said monitor means and bistable means are responsive to said counter output through said gating means to momentarily display each said symbol in succession and thereafter store and display the symbol selected by the counter state occurring upon said interruption.

8. The apparatus defined in claim 6, wherein said means for interrupting advancement of said counter states comprised, a bistable switching means having first and second states and means for disposing said switching means in its second state; said timing circuit means being connected to said switching means and responsive to the second state thereof to interrupt the issuance of said pulses to said counter input, said pulse generator means having an output connected to said counter input and being connected to and operated by said switching means in its second state to issue a succession of pulses at its output, said timeout counter being connected between said pulse generator output and said switching means and being responsive to a predetermined number of pulses issued by said generator means to dispose said switching means in its first state.

9. The apparatus defined in claim 8, wherein the time duration between consecutive pulses issued by said pulse generator means is substantially greater than the average time duration between consecutive pulses issued by said timing circuit.

10. The apparatus defined in claim 5, wherein said game of amusement is based on simultaneous occurrence of certain combinations of events, each such event being selected from one of a plurality of event sets, and

one said counter and circuit means and monitor means for each said event set, said means for interrupting counter advancement being jointly connected to each said circuit means for generally simultaneous interruption of pulses therefrom to dispose each associated said counter in one of its states providing a selected event from each said event set.

11. The apparatus defined in claim 10, and output gating means connected to said outputs of said counters and responsive to the occurrence of predetermined combinations of individual counter states and the events corresponding thereto to issue an electrical control signal whereby the occurrence of certain event combinations may be electrically detected.

12. Method of generating a set of events and selecting an event therefrom at random, wherein each such event has an individually preset probability of being selected, the steps comprising, initiating a self-sustaining recycling pulse counter through a continuous succession of counting states, wherein each said state is designated as one of said events and wherein said counter is provided with an input for receiving a series of pulses thereat each pulse advancing said counter one state and a set of outputs each for issuing a signal representing one of said states,

advancing said pulse counter through said states in response to each counter output by issuing one said pulse to said counter input,

controlling the time periods in which said counter is in each of its states and adjusting said time period for at least one said state to be different from said periods for the remaining states, interrupting at random the advancement of said counter such that the one of said states occurring thereupon provides the selection of the corresponding one of said events, and

displaying said randomly selected event.

13. The method defined in claim 12, wherein the summation of time periods for all of said counter states is less than 1 second, and said step of interrupting comprises interrupting said series of pulses by means adapted for manual operation.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,580,581 Dated May 25, 1971

Inventor(s) Richard C. Raven

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 5, line 69, after "together to", insert --provide--.

Column 6, line 35, change "Hi" to --HI--.

Column 7, line 72, change "15" to --125--.

Column 9, line 9, after "1, 2", insert --and 3--.

Column 9, line 74, change "i39" to --139--.

Column 13, line 9, change "281'283" to --281-283--.

Column 13, line 11, change "i39" to --139--.

Column 13, line 17, change "i39" to --139--.

Signed and sealed this 28th day of December 1971.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Acting Commissioner of Patents

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