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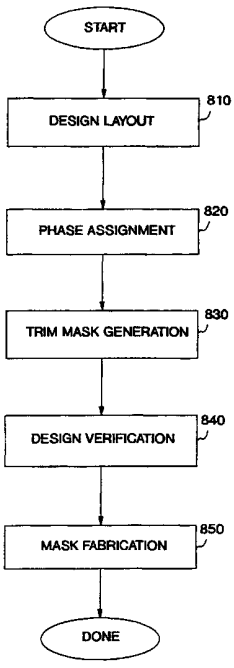
(54) Title: METHOD AND APPARATUS FOR DETERMINING PHASE SHIFTS AND TRIM MASKS FOR AN INTEGRATED CIRCUIT



(57) Abstract: A method and apparatus for deep sub-micron layout optimization is described. Components of an integrated circuit (IC) design (e.g., gates) can be identified and manufactured using a phase shifting process to improve circuit density and/or performance as compared to a circuit manufactured without using phase shifting processes. In one embodiment, a first mask (e.g., a phase shift mask) is generated that includes the component to be manufactured using the phase shifting process. A second mask (e.g., a trim mask) is also generated to further process the structure created using the first mask. Both masks are defined based on a region (e.g., a diffusion region) in a different layer of the integrated circuit layout than the structure (e.g., the gate) being created with the phase shifting process.

WO 01/23961 A1

METHOD AND APPARATUS FOR DETERMINING PHASE SHIFTS AND TRIM MASKS FOR AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The invention relates to integrated circuit processing. More particularly, the invention relates to optical correction for deep sub-micron (<0.25 μm) integrated circuit processes.

BACKGROUND OF THE INVENTION

As integrated circuits (ICs) become more dense, the widths of lines and components, as well as the separation between lines becomes increasingly smaller. Currently, deep sub-micron (<0.25 μm) processes are being used. However, with deep sub-micron processes, silicon yield is affected by several factors including reticle/mask pattern fidelity, optical proximity effects, and diffusion and loading effects during resist and etch processing. Typical problems include line-width variations that depend on local pattern density and topology and line end pullback.

Figure 1a is an exemplary deep sub-micron design layout. Figure 1a represents the intended layout; however, because of the physics of deep sub-micron processing the resulting circuit is different than the design layout. **Figure 1b** is an uncorrected structure based on the design of Figure 1a.

In the structure of Figure 1b, line widths vary based on topology and density, which can detrimentially affect speed and accuracy of operation. Line edges are also shortened and rounded, which can break connections and cause circuit failure. U.S. Patent No. 5,858,580 issued to Wang, et al. ("the '580 patent") discloses a method an apparatus for reducing gate width from an original size to a reduced size that can be a sub-micron dimension.

The '580 patent reduces gate sizes from a first manufacturing process having a first minimum realizable dimension to a second manufacturing process having a second minimum realizable dimension. The second minimum realizable dimension is less than the first minimum realizable dimension. However, the '580 patent requires an

integrated circuit layout to be laid out for a first process and then shrunk for use with a second process. What is needed is improved deep sub-micron processing that can operate on an original circuit layout.

SUMMARY OF THE INVENTION

A method and apparatus for generating a phase shifting mask and a trim mask for integrated circuit manufacture is described. A first mask is generated that defines a first region in a first layer of the integrated circuit. The first region is based, at least in part, on a region in a second layer of the integrated circuit. A second mask is generated that defines a second region in the first layer of the integrated circuit. The second region is also based, at least in part, on the region in the second layer of the integrated circuit. The second mask also removes artifacts generated by the first mask.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example, and not by way of limitation in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1a is an exemplary deep sub-micron design layout.

Figure 1b is an uncorrected structure based on the design of Figure 2a.

Figure 2 is one embodiment of an integrated circuit processing arrangement.

Figure 3 is a design layout having two gates over a diffusion region.

Figure 4 is the design layout of Figure 3 with line segment indications used to generate phase shift and trim masks according to one embodiment of the invention.

Figure 5 is a phase shifting mask for the layout of Figure 3 according to one embodiment of the invention.

Figure 6 is a trim mask for the layout of Figure 3 according to one embodiment of the invention.

Figure 7 is a resulting circuit based on the layout of Figure 3.

Figure 8 is a flow diagram for generating phase shift and trim masks according to one embodiment of the invention.

Figure 9 is a flow diagram for generating phase shift and trim masks according to one embodiment of the invention.

Figure 10 illustrates an EDA tool incorporated with the simulation tool of the present invention in accordance with one embodiment is shown.

Figure 11 illustrates one embodiment of a computer system suitable for use to practice the present invention.

DETAILED DESCRIPTION

A method and apparatus for generating a phase shifting mask and a trim mask for integrated circuit manufacture is described. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

Methods and apparatuses for deep sub-micron layout optimization are described. Components of an integrated circuit (IC) design (e.g., gates) can be identified and manufactured using a phase shifting process to improve circuit density and/or performance as compared to a circuit manufactured without using phase shifting processes. In one embodiment, a first mask (e.g., a phase shift mask) is generated that includes the component to be manufactured using the phase shifting process. A second

mask (e.g., a trim mask) is also generated to further process the structure created using the first mask. Both masks are defined based on a region (e.g., a diffusion region) in a different layer of the integrated circuit layout than the structure (e.g., the gate) being created with the phase shifting process.

Figure 2 is one embodiment of an integrated circuit processing arrangement. The arrangement of Figure 2 is suitable for use with the invention and can be used as described below to reduce component sizes. The general uses of the components of Figure 2 are known in the art. Modifications are described in greater detail below. For example, specific reticle and/or mask configurations and modifications can be used with the remaining components of Figure 2.

Light source 200 provides light towards wafer 230. Mask/reticle 210 blocks light for certain predetermined portions of wafer 230. Stepper scanner 220 directs the patterns of mask/reticle 210 to one of multiple integrated circuits being developed on wafer 230.

Figure 3 is a design layout having two gates over a diffusion region. The layout of Figure 3 is used herein to describe the invention. However, the usefulness of the invention is not limited to the design of Figure 3.

Diffusion region 310 can be used, for example, to provide a collector and an emitter for a transistor. Diffusion region 310 can be provided in any manner known in the art. For example, diffusion region 310 can be provided by ion implantation.

Metal (or polysilicon) region 300 provides electrical connectivity between components. For example, metal region 300 provides two gates across diffusion region 310 and a connection for the two gates to another device (not shown in Figure 3). Metal region 300 can be made, for example, of aluminum, copper, etc.

Figure 4 is the design layout of Figure 3 with line segment indications used to generate phase shift and trim masks according to one embodiment of the invention. In one embodiment, the line segments are used to define a region of a phase shift mask. In alternative embodiments, offsets from the line segments are used to define the phase shift mask.

Line segments 405 and 445 are beyond the ends of diffusion region 310. Line segments 400 and 430 correspond to the center of the gates of metal region 300. Line

segments 415, 410, 435 and 440 connect the respective end line segments (i.e., 405 and 445) and gate line segments (i.e., 400 and 430). Line segments 420 and 425 connect the gate line segments. In alternative embodiment, the gate line segments are not centered in the gates of metal region 300.

In one embodiment, the line segments of Figure 4 are offset from the boundaries of diffusion region 310 by a predetermined amount. In one embodiment, the offset is greater than $\frac{0.25\lambda}{NA}$, where λ is the wavelength of the light used and NA is the numerical aperture used. Thus, the offset is greater than the width of the gates. The line segments of Figure 4 indicate the dimensions of a phase shifted region manufactured over diffusion region 310 as described in greater detail below. By defining the phase shifted region based on diffusion region 310, the phase shifting mask can be more easily defined than if the phase shifting mask is defined based on a gate or other region to be generated using phase shifting techniques.

Figure 5 is a phase shifting mask for the layout of Figure 3 according to one embodiment of the invention. In the embodiment described with respect to Figure 5, the line segments described with respect to Figure 4 are used to define the phase shifting mask to generate gates according to the invention.

Line segments 400, 405, 410 and 415 define a first region of exposure for a phase shifting mask. Line segments 430, 435, 440 and 445 define a second region of exposure for the phase shifting mask. In an alternative embodiment, offsets from the line segments of Figure 5 are used to define the first and second regions of exposure.

Line segments 400, 405, 410 and 415 and line segments 430, 435, 440 and 445 define phase shifting regions within the phase shifting mask. In one embodiment, the line segments define a region that phase shifts light by 180 degrees while the neighboring regions do not shift the light. Alternatively, the region(s) external to the line segments can be 180 degree phase shifted regions and the internal regions can be zero degree phase shifted regions.

Other phase shifted and non-phase shifted regions can also be included in the phase shifting mask. In alternative embodiments, phase shifting other than zero degrees and 180 degrees can be used. The phase shift mask can also be used to provide

additional structure for the metal layer other than the gates, or other regions, created using phase shifting techniques.

Figure 6 is a trim mask for the layout of Figure 3 according to one embodiment of the invention. The trimming regions eliminate the artifacts that are generated by the phase shifting mask that are not part of the transistor gate to be manufactured.

The trimming regions corresponding to the phase shifting regions of the phase shifting mask are defined by line segments 500, 505, 510 and 515 and by line segments 530, 535, 540 and 454. In one embodiment, the line segments that define the trimming regions are at a predetermined offset from the corresponding line segments that define the phase shifting regions. Other structural regions (not shown in Figure 6) can also be included in the trimming mask.

Figure 7 is a resulting circuit based on the layout of Figure 3. Diffusion region 310 is the same size as the layout of Figure 3. In one embodiment, the two transistor gates over diffusion region 310 have a reduced dimension as compared to the original circuit layout of Figure 3. In one embodiment, the connection between the gates has a reduced dimension. Thus, some or all of the metal or polysilicon region 700 has a reduced dimension as compared to the circuit layout of Figure 3.

Figure 8 is a flow diagram for generating phase shift and trim masks according to one embodiment of the invention. A design layout is generated and/or accessed at 810. The design layout can be, for example, a GDS-II description of the circuit to be manufactured. Other layout formats can also be supported.

The design layout is accessed at 810. In one embodiment, the design layout is a circuit description in GDS-II format; however, other formats can also be used. The design layout describes the circuit design from which masks and/or reticles are designed to realize the circuit described by the design layout.

Phase assignments are made based on the design layout at 820. In one embodiment, the phase assignments are made to create gate structures having dimensions that are less than the minimum realizable dimension of the integrated circuit manufacturing process to be used.

The phase assignments are made, as described above, based on a circuit structure in a circuit layer other than the layer for which the phase shifted processing is

to be used. For example, if phase shifting is to be used to create gate structures, the phase assignments for the gate structures are made based on the diffusion region over which the gate structure is to be manufactured. A phase shifting mask is generated based on the phase assignments.

A trim mask is generated at 830. The trim mask functions to remove artifacts created by the phase shifting mask. In one embodiment, the trim mask is based on the same circuit structure as the phase shifting mask. The trim mask can also define structure other than the structures created using the two mask phase shifting process described herein. For example, the trim mask can define metal or other connecting structures between the gate regions created using the phase shifting mask and the trim mask.

Design verification is performed at 840. In one embodiment, design verification is performed after phase assignments are made. Typically, design verification includes design rule checking and/or electrical continuity checking, which is referred to as layout versus schematic (LVS) checking. In one embodiment, artificial gate widths are used for design verification purposes because the physical gate width generated by the layout of the phase shifting mask can cause conventional design verifications to fail. Modifications to the design are made, if necessary, based on the design verification to match the original layout topology allowing conventional LVS checks to be executed. The multiple masks used to fabricate the integrated circuit are fabricated at 850.

Figure 9 is a flow diagram for generating phase shift and trim masks according to one embodiment of the invention. The embodiment of Figure 9 performs design verification prior to phase assignments. In this embodiment, the reduced gate widths do not cause the design verification to fail.

The design layout is accessed at 910. As described above, the layout can be in GDS-II format, or any other appropriate format. The design layout is used for design verification at 920. Because the design verification is performed on the original design layout, the reduced dimensions provided by the dual-mask phase shifting fabrication described above does not cause the design verification to fail.

Phase assignment is provided at 930. In one embodiment, the phase assignment is performed based on circuit structure in a different circuit layer than the layer for

which the phase mask is to be used. A trim mask is generated, at 940, for the circuit layer corresponding to the phase assignment described above. The appropriate masks are fabricated at 950.

Figure 10 illustrates an EDA tool incorporated with the simulation tool of the present invention in accordance with one embodiment is shown. As illustrated, EDA tool suite 1000 includes simulation tool 1002 incorporated with the teachings of the present invention as described earlier. Additionally, EDA tool suite 1000 includes other tool modules 1004. Examples of these other tool modules 1002 include but not limited to synthesis module, layout verification module and so forth.

Figure 11 illustrates one embodiment of a computer system suitable for use to practice the present invention. As shown, computer system 1100 includes processor 1102 and memory 1104 coupled to each other via system bus 1106. Coupled to system bus 1106 are non-volatile mass storage 1108, such as hard disks, floppy disk, and so forth, input/output devices 1110, such as keyboard, displays, and so forth, and communication interfaces 1112, such as modem, LAN interfaces, and so forth. Each of these elements perform its conventional functions known in the art.

In particular, system memory 1104 and non-volatile mass storage 1108 are employed to store a working copy and a permanent copy of the programming instructions implementing the above described teachings of the present invention. System memory 1104 and non-volatile mass storage 1106 may also be employed to store the IC designs. The permanent copy of the programming instructions to practice the present invention may be loaded into non-volatile mass storage 1108 in the factory, or in the field, using distribution source/medium 1114 and optionally, communication interfaces 1112. Examples of distribution medium 1114 include recordable medium such as tapes, CDROM, DVD, and so forth. In one embodiment, the programming instructions are part of a collection of programming instructions implementing EDA tool 1000 of Fig. 10. The constitution of elements 1102-1114 are well known, and accordingly will not be further described.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader

spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method of generating a set of masks for integrated circuit manufacture, the method comprising:

generating a first mask to define a first region in a first layer of the integrated circuit, the first region based, at least in part, on a region in a second layer of the integrated circuit;

generating a second mask to define a second region in the first layer of the integrated circuit, the second region based, at least in part, on the region in the second layer of the integrated circuit, the second mask further to remove artifacts generated by the first mask.

2. The method of claim 1 wherein the first region is generated by destructive light interference.

3. The method of claim 1 wherein the first mask includes phase shifting elements to define the first region.

4. The method of claim 1 wherein the second mask further defines additional structural elements in the first integrated circuit layer.

5. The method of claim 1 wherein the region in the second layer of the integrated circuit is a diffusion region.

6. The method of claim 1 wherein the second mask does not include phase shifting elements.

7. The method of claim 1 wherein the first mask and the second mask define a transistor gate.

8. The method of claim 1 wherein the second mask retains a topology of an original integrated circuit layout.

9. An apparatus for generating a set of masks for integrated circuit manufacture, the apparatus comprising:

means for generating a first mask to define a first region in a first layer of the integrated circuit, the first region based, at least in part, on a region in a second layer of the integrated circuit;

means for generating a second mask to define a second region in the first layer of the integrated circuit, the second region based, at least in part, on the region in the second layer of the integrated circuit, the second mask further to remove artifacts generated by the first mask.

10. The apparatus of claim 9 wherein the first region is generated by destructive light interference.

11. The apparatus of claim 9 wherein the first mask includes means for phase shifting to define the first region.

12. The apparatus of claim 9 wherein the second mask further comprises defining additional structural elements in the first integrated circuit layer.

13. The apparatus of claim 9 wherein the region in the second layer of the integrated circuit is a diffusion region.

14. The apparatus of claim 9 wherein the second mask does not include phase shifting elements.

15. The apparatus of claim 9 wherein the first mask and the second mask define a transistor gate.

16. The apparatus of claim 9 wherein the second mask retains a topology of an original integrated circuit layout.

17. A machine-readable medium having stored thereon sequences of instructions that when executed by one or more processors cause an electronic device to:

generate a first mask definition that defines a first region in a first layer of the integrated circuit, the first region based, at least in part, on a region in a second layer of the integrated circuit;

generate a second mask definition that defines a second region in the first layer of the integrated circuit, the second region based, at least in part, on the region in the second layer of the integrated circuit, the second mask further to remove artifacts generated by the first mask.

18. The machine-readable medium of claim 17 wherein the first region is generated by destructive light interference.

19. The machine-readable medium of claim 17 wherein the first mask includes phase shifting elements to create the first region.

20. The machine-readable medium of claim 17 wherein the sequences of instructions that generate the second mask further comprise sequences of instruction that define additional structural elements in the first integrated circuit layer.

21. The machine-readable medium of claim 17 wherein the region in the second layer of the integrated circuit is a diffusion region.

22. The machine-readable medium of claim 17 wherein the second mask does not include phase shifting elements.

23. The machine-readable medium of claim 17 wherein the first mask and the second mask define a transistor gate.

24. The machine-readable medium of claim 17 wherein the second mask retains a topology of an original integrated circuit layout.

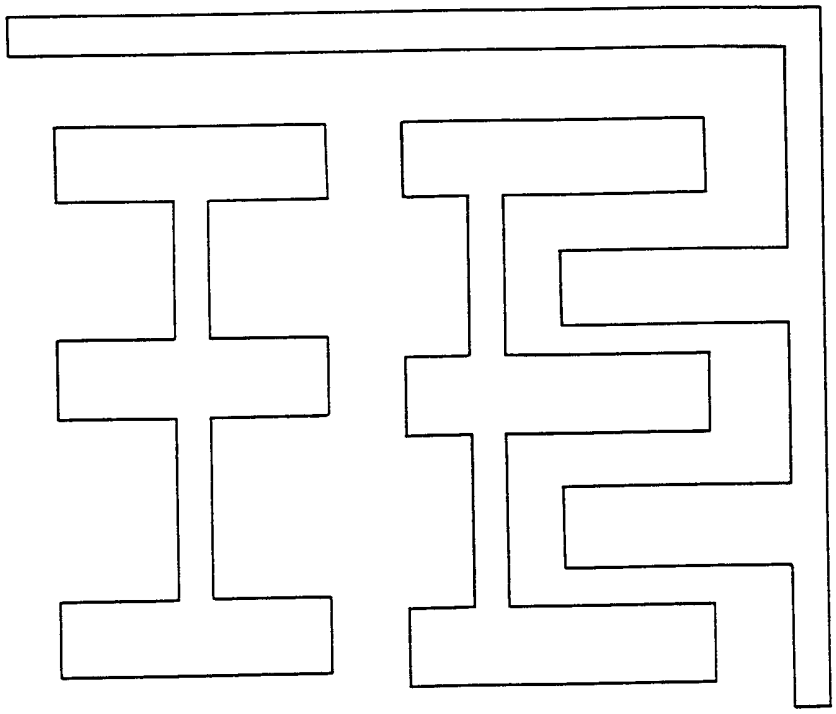


FIG. 1a

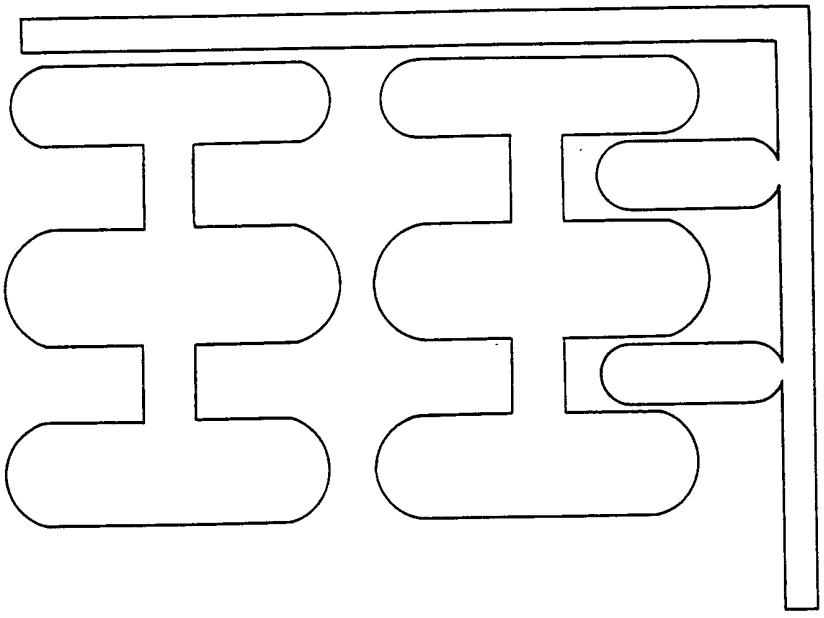
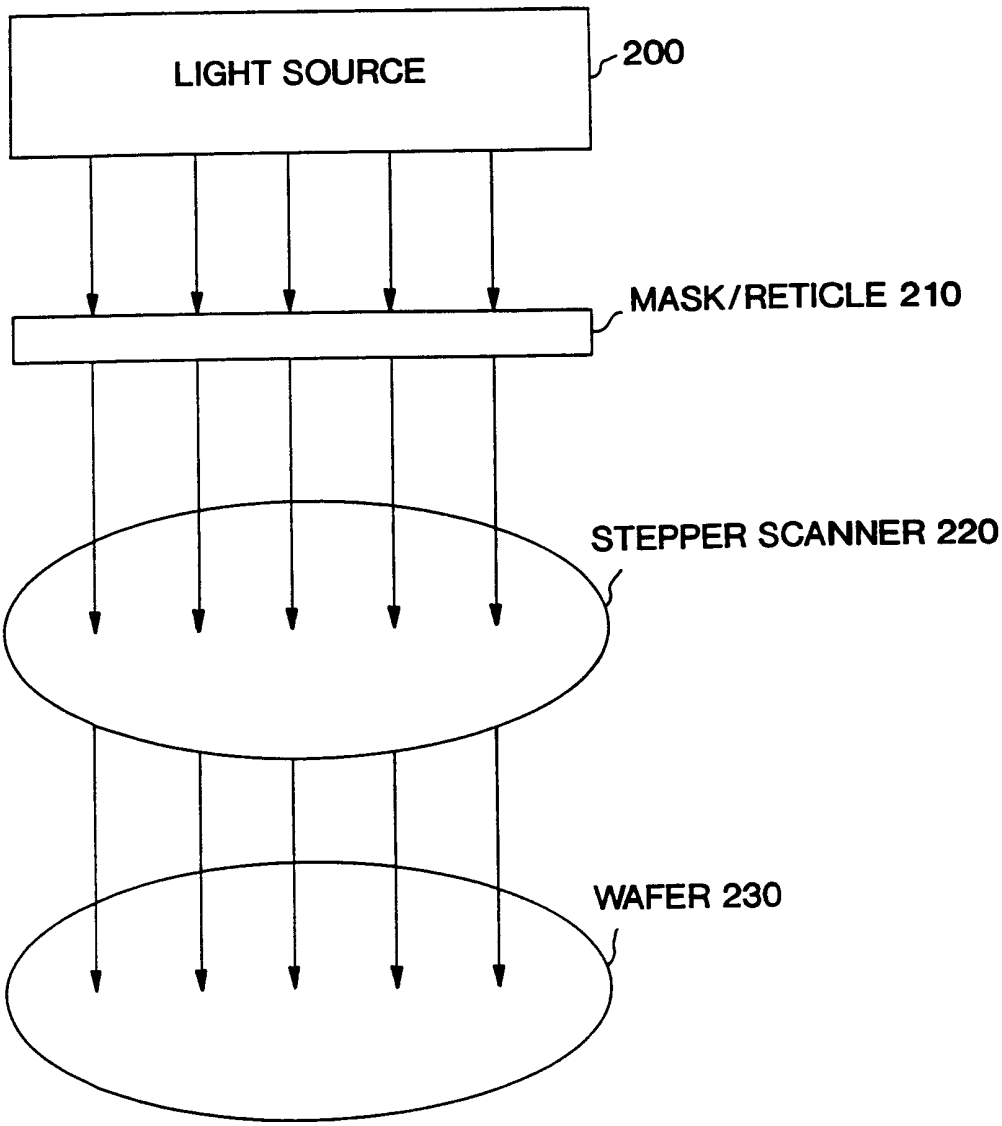


FIG. 1b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MASK/RETICLE 210
STEPPER SCANNER 220
WAFER 230

FIG. 2

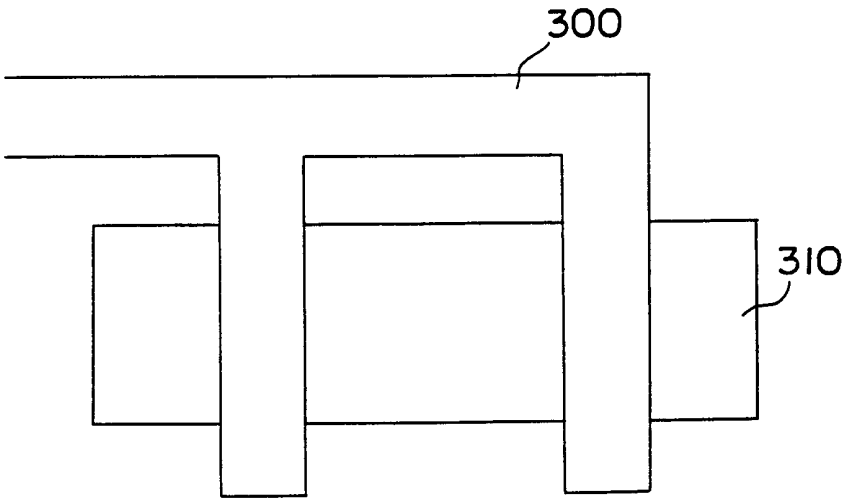


FIG. 3

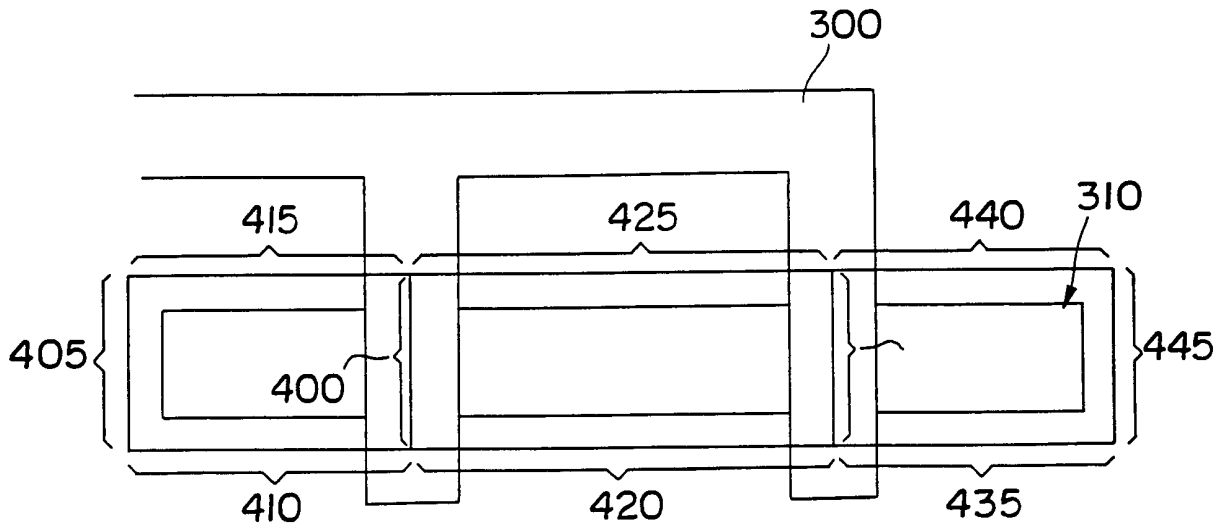
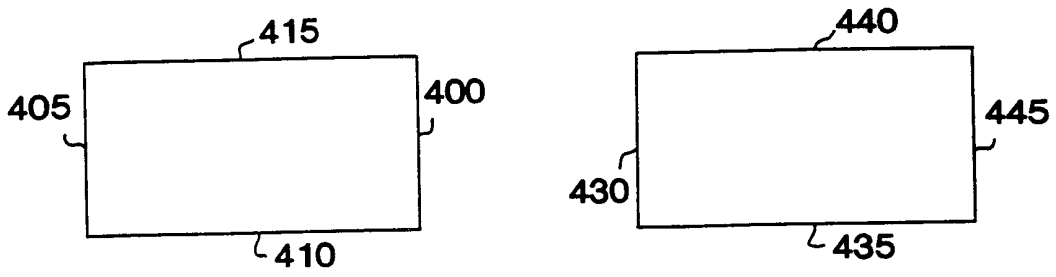


FIG. 4


415
405
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410
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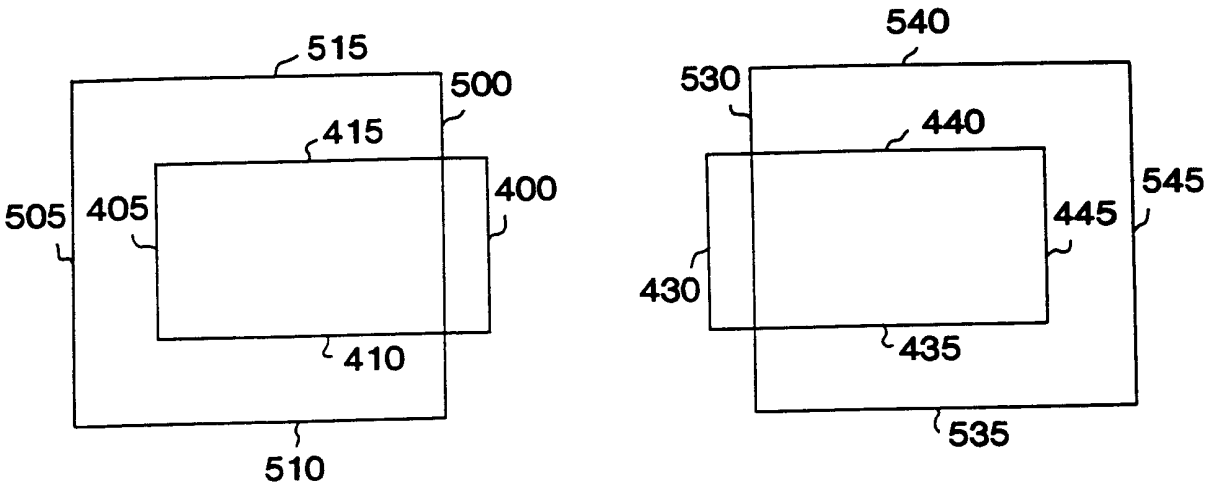
445
430
435

FIG. 5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435
535

FIG. 6

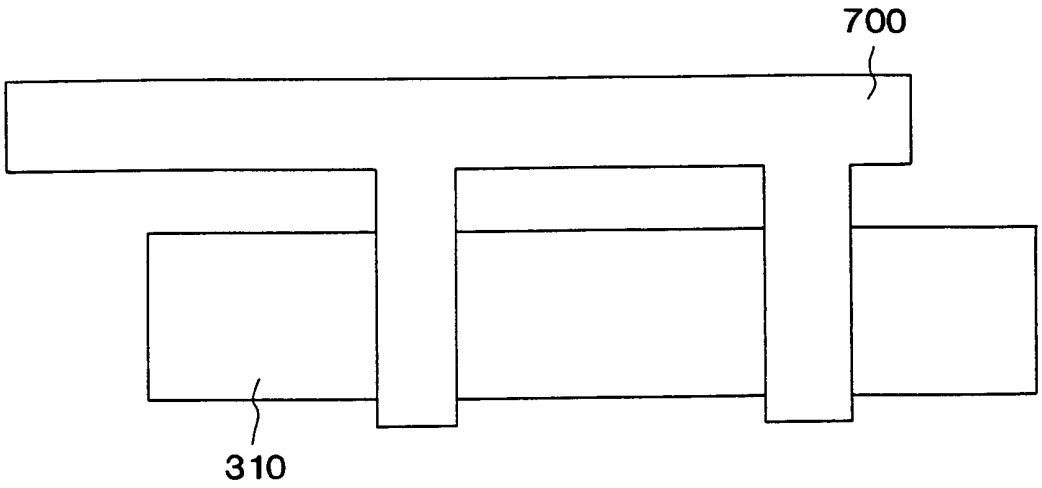
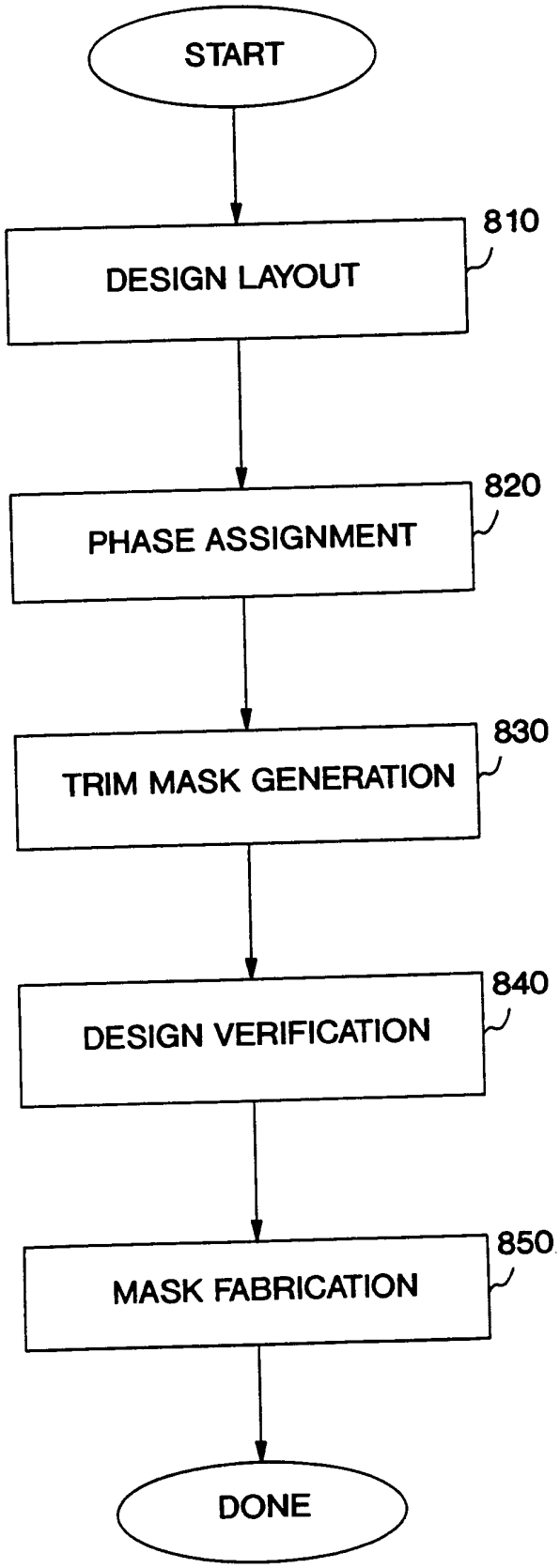


FIG. 7


START
DESIGN LAYOUT
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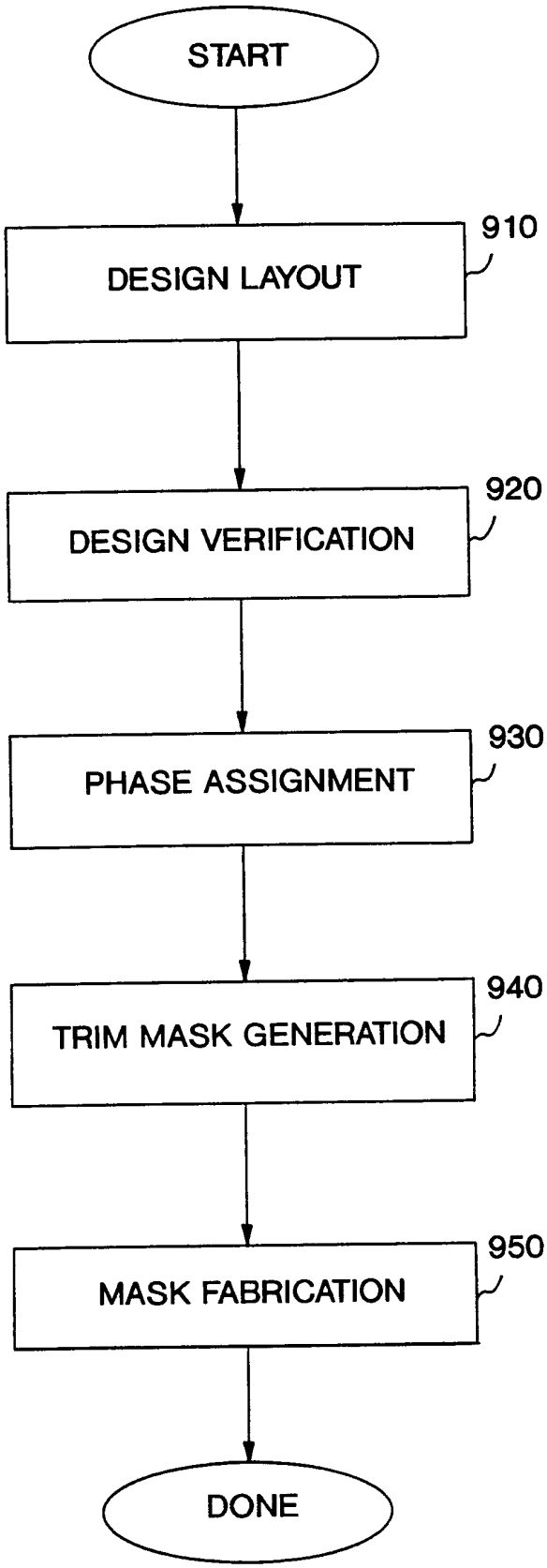
PHASE ASSIGNMENT
820
TRIM MASK GENERATION
830
DESIGN VERIFICATION
840
MASK FABRICATION
850
DONE

FIG. 8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DESIGN VERIFICATION
920
PHASE ASSIGNMENT
930
TRIM MASK GENERATION
940
MASK FABRICATION
950
DONE

FIG. 9

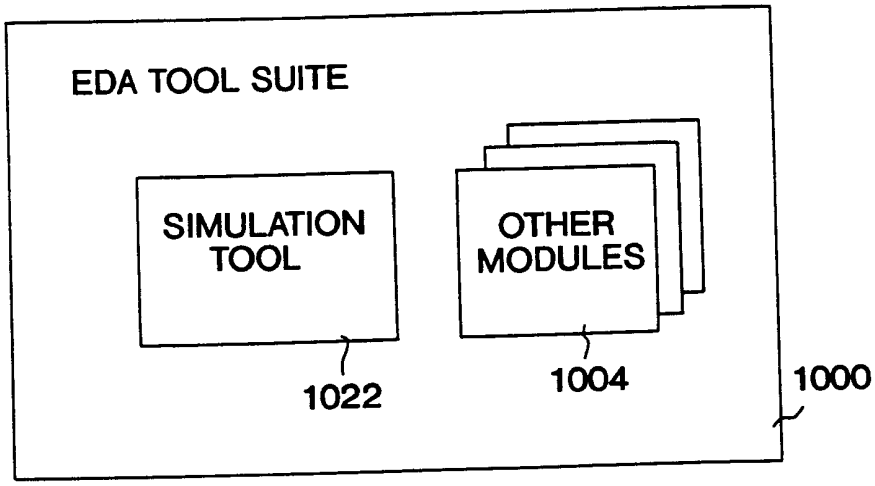
EDA TOOL SUITE
SIMULATION TOOL
OTHER MODULES
1022
1004
1000

FIG. 10

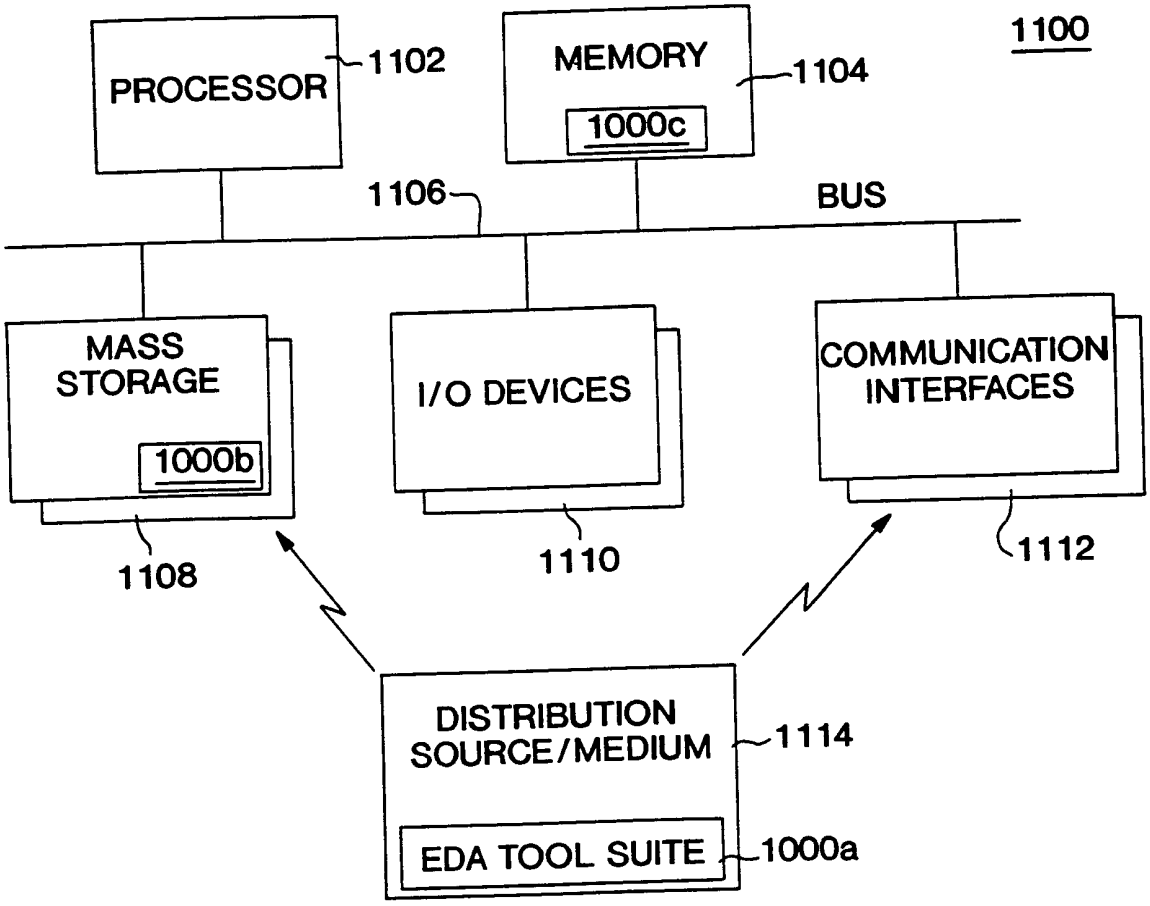
1100
PROCESSOR
1102
MEMORY
1104
1000c
1106
BUS
MASS STORAGE
1000b
I/O DEVICES
COMMUNICATION INTERFACES
1108
1110
1112
DISTRIBUTION SOURCE/MEDIUM
1114
EDA TOOL SUITE
1000a

FIG. 11

INTERNATIONAL SEARCH REPORT

Interr nal Application No
PCT/US 00/20606

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G03F1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, IBM-TDB, COMPENDEX, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 698 916 A (ADVANCED MICRO DEVICES INC) 28 February 1996 (1996-02-28)	1-3, 5-11, 13-19, 21-24
Y	column 6 -column 7	4,12,20
Y	GB 2 333 613 A (SONY CORP) 28 July 1999 (1999-07-28) page 7	4,12,20
A	US 5 858 580 A (WANG YAO-TING ET AL) 12 January 1999 (1999-01-12) cited in the application	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 January 2001	01/02/2001

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