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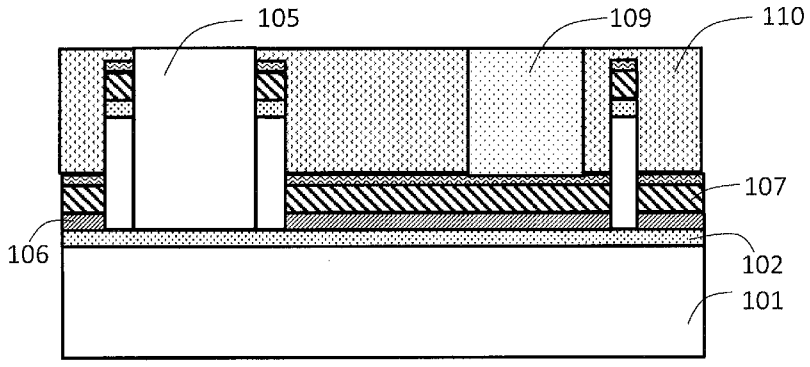


FIG. 7B

(57) Abstract: A solid state battery may comprise: a substrate; a first current collector deposited on the surface of the substrate; an insulating mesa deposited on the cathode current collector, the insulating mesa defining a boundary of an active area of the solid state battery, the insulating mesa forming a continuous wall around the active area; and a stack of active device layers within the boundary, the stack comprising a cathode layer, an electrolyte layer and a second current collector layer; wherein a height of the insulating mesa is greater than a thickness of the stack of active device layers. The insulating mesa may further define a boundary of a contact area of the first current collector, the insulating mesa forming a continuous wall around the first contact area, and further comprising a first conductive mesa for providing electrical contact to the first current collector.

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METHOD AND APPARATUS FOR FABRICATING BATTERY WITH MESA STRUCTURES AND BATTERY COMPRISING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/153,771 filed April 28, 2015, incorporated in its entirety herein.

TECHNICAL FIELD

[0002] Embodiments relate to solid state thin or thick film battery devices and methods and apparatuses for fabricating the same.

BACKGROUND OF THE RELATED ART

[0003] Maskless fabrication techniques have been considered advantageous in the field of solid state thin or thick film battery devices because they can enable high volume manufacturing, improving efficiencies and lowering costs. Some conventional maskless fabrication techniques use laser ablation to define cell boundaries and form contact areas such as a cathode pad area. However, in the process of forming a contact area such as a cathode pad area, control of laser ablation to stop before the thin bottom cathode layer is very difficult and can result in yield loss. Femtosecond lasers may provide a more controlled removal of surface layers, however this is at the expense of longer processing time. Clearly, there is a need for improved maskless thin or thick film battery fabrication techniques that avoid these limitations.

SUMMARY

[0004] According to some embodiments, a solid state battery may comprise: a substrate; a first current collector deposited on the surface of the substrate; an insulating mesa deposited on the cathode current collector, the insulating mesa defining a boundary of an active area of the solid state battery, the insulating mesa forming a continuous wall around the active area; and a stack of active device layers within the boundary, the stack comprising a cathode layer, an electrolyte layer and a second current collector layer; wherein a height of the insulating mesa is greater than a thickness of the stack of active device layers.

[0005] According to some embodiments, a method of fabricating a solid state battery may comprise: providing a substrate; depositing a first current collector layer on the substrate; forming an insulating mesa on the first current collector layer, the insulating mesa defining a boundary of an active area of the solid state battery, the insulating mesa forming a continuous wall around the active area; and depositing a stack of active device layers within the boundary, the stack comprising a cathode layer, an electrolyte layer and a second current collector layer; wherein a height of the insulating mesa is greater than a thickness of the stack of active device layers.

[0006] According to some embodiments, an apparatus for fabricating a solid state battery may comprise: a first system for blanket depositing a first current collector layer on a substrate; a second system for forming an insulating mesa structure defining a boundary of an active area of the solid state battery, the insulating mesa forming a continuous wall around the active area; and a third system for blanket depositing a cathode layer, an electrolyte layer and an second current collector layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] These and other aspects and features of the present disclosure will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the disclosure in conjunction with the accompanying figures, wherein:

[0008] FIGS. 1A & 1B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing mesa structures, defining the battery active area and cathode contact area, formed on a current collector layer, according to some embodiments;

[0009] FIGS. 2A & 2B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing a cathode contact mesa formed on the cathode contact area of FIGS. 1A & 1B, according to some embodiments;

[0010] FIGS. 3A & 3B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing a stack of battery layers blanket deposited on the structure of FIGS. 2A & 2B, according to some embodiments;

[0011] FIGS. 4A & 4B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing removal of the stack of battery layers off the cathode contact mesa of the structure of FIGS. 3A & 3B, according to some embodiments;

[0012] FIGS. 5A & 5B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing anode contact mesas formed on the anode current collector of FIGS. 4A & 4B, according to some embodiments;

[0013] FIGS. 6A & 6B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing an encapsulation layer blanket deposited on the structure of FIGS. 5A & 5B, according to some embodiments;

[0014] FIGS. 7A & 7B are a top view and a cross-sectional view (section X-X) of a representation of a process for fabricating a solid state battery structure, showing partial removal of the encapsulation layer to expose the cathode and anode contact mesas of the structure of FIGS. 6A & 6B, according to some embodiments;

[0015] FIG. 8 is a schematic illustration of a cluster tool for TFB (thin film battery) fabrication, according to some embodiments;

[0016] FIG. 9 is a representation of a TFB fabrication system with multiple in-line tools, according to some embodiments; and

[0017] FIG. 10 is a representation of an in-line tool of FIG. 9, according to some embodiments.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] The present disclosure will now be described in detail with reference to the drawings, which are provided as illustrative examples of the disclosure so as to enable those skilled in the art to practice the disclosure. Notably, the figures and examples below are not meant to limit the scope of the present disclosure to a single embodiment, but other embodiments are possible by way of interchange of some or all of the described or illustrated elements. Moreover, where certain elements of the present disclosure can be partially or fully implemented using known components, only those portions of such known components that are necessary for an understanding of the present disclosure will be described, and detailed descriptions of other portions of such known components will be omitted so as not to obscure

the disclosure. Embodiments described as being implemented in software should not be limited thereto, but can include embodiments implemented in hardware, or combinations of software and hardware, and vice-versa, as will be apparent to those skilled in the art, unless otherwise specified herein. In the present specification, an embodiment showing a singular component should not be considered limiting; rather, the disclosure is intended to encompass other embodiments including a plurality of the same component, and vice-versa, unless explicitly stated otherwise herein. Moreover, applicants do not intend for any term in the specification or claims to be ascribed an uncommon or special meaning unless explicitly set forth as such. Further, the present disclosure encompasses present and future known equivalents to the known components referred to herein by way of illustration.

[0019] Embodiments herein will be particularly described in connection with thin film solid state battery devices. However, those skilled in the art will understand how to extend the described examples to thick film battery devices and fabrication techniques therefor. Herein the term thin film is used to refer to films with thicknesses less than 25.4 microns, and the term thick film is used to refer to films with a thickness greater than or equal to 25.4 microns. Note that the method of applying a thin film can be via a spin coating method, spray coating method, a vapor condensation method (as for parylene coating), PVD (physical vapor deposition) or CVD (chemical vapor deposition) coating method, etc., whereas the method of applying a thick film usually uses a different set of tools and methods, such as dip coating, painting, doctor blading, litho or gravure printing, etc. A thin film solid state battery herein refers to a battery in which all component films are thin films (not accounting for mesa structure thickness), and a thick film solid state battery herein refers to a battery in which one or more of the component films is a thick film.

[0020] FIGS. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 6A, 6B, 7A & 7B are top views and cross-sectional views of an example method of fabricating a thin film solid state battery according to some embodiments.

[0021] FIGS. 1A & 1B are a top view and a cross-sectional view of a representation of a process for fabricating a solid state battery structure, according to some embodiments, showing mesa structures 103 & 104, defining a battery active area and a cathode contact area, respectively, formed on a cathode current collector layer 102 formed on a substrate 101,

[0022] Processing starts by preparing and cleaning the substrate 101. The substrate material may be glass, and in embodiments may be silicon, mica, ceramic, metal, rigid material, flexible material, plastic / polymer, etc. Furthermore, in embodiments the substrate

material may include alumina, low temperature co-fired ceramic (LTCC), aluminum nitride, FR4 glass-reinforced epoxy laminate sheets, etc. It should be noted that the substrate material can be a silicon wafer with integrated circuits. The battery cell(s) can be built on these silicon wafers as part of a 3D integration process. Moreover, a blanket die patterning assistant layer (e.g. a layer of a-Si, μc-Si, or $LiCoO_2$), a substrate encapsulation layer, an adhesion layer, a crystallinity seeding layer or a lattice matching layer can also optionally be deposited over the substrate surface prior to deposition of a current collector layer.

[0023] After preparing the substrate, a cathode current collector layer 102 (e.g. Ti/Au) is blanket deposited on the substrate 101. In embodiments, this is done by PVD, and the resulting layer is about 500 Angstroms to 5000 Angstroms thick.

[0024] Next, an insulating mesa or dam pattern 103 is deposited on the substrate surface to define the battery active area boundary, the insulating mesa forming a continuous wall around the active area. This can be accomplished by a dispensing method, jetting method, screen printing method, assembly stack up method or lithographic method. In some embodiments, the dam or mesa material is a particle loaded polymer, in which case, the deposition of the liquid polymer or paste can be followed by a curing step using UV, radiation or thermal energy, for example. In some embodiments, the dam or mesa material can be LTCC, which can withstand a subsequent high temperature annealing step in later processing. Suitable annealing or curing techniques known to those skilled in the art can be used following the deposition of these materials.

[0025] It should be noted that although FIGS. 1A & 1B only show the boundary of a single battery, it should be apparent that this step can include depositing a pattern that defines the boundaries of a plurality, and possibly hundreds, of batteries, depending on the battery type, substrate dimensions, whether the process is 2D or 3D, etc. According to certain aspects, the process of the present disclosure provides better electrical isolation between micro batteries patterned on the same substrate. Furthermore, the process of the present disclosure also helps to avoid a yield debug issue where a network of multiple electrical battery stack shorts can pull down the global open circuit voltage.

[0026] Next, as shown in FIGS. 2A & 2B, a conducting mesa material 105 is deposited on the cathode current collector 102 within the corner cathode pad area of the battery, as defined by mesas 103 and 104, which will form an electrical contact to the cathode current collector layer. In embodiments, the conducting material is a low viscosity ink such as a conductive silver ink. In other embodiments, materials such as silver paste can be used.

The deposition of the conducting material can be accomplished by a dispensing method, jetting method, screen printing method, assembly stack up method or lithographic method, and can be followed by a suitable anneal or cure as required.

[0027] Next, as shown in FIGS. 3A & 3B, TFB stack layers are blanket deposited and annealed as required. In this example, a cathode layer 106 (e.g. $LiCoO_2$ (LCO)) is blanket deposited over the previously deposited cathode current collector layer 102 and thermally annealed at about 500 to 700 degrees C. An electrolyte layer 107 (e.g. LiPON) is blanket deposited over the cathode layer. In embodiments, an anode layer (not shown) (e.g. Li, Si) is optionally blanket deposited over the electrolyte layer. In these and other embodiments, finally an anode current collector ACC layer 108 (e.g. TiO_2/Cu) is blanket deposited over the anode layer or electrolyte layer.

[0028] Furthermore, in embodiments a mesa material is chosen which shrinks when annealed, such that the width of the mesa wall may be reduced in width by 18%, for example, during a 600 to 700 degrees C anneal (typical anneal for LCO). This type of shrinkage could result in the mesa wall pulling away from a deposited LCO cathode – layer 106 in FIG. 3B – which would allow for a subsequent deposition of electrolyte, such as LiPON – layer 107 in FIG. 3B – to cover the edge of the LCO layer and reduce the occurrence of shorting. Mesa materials that exhibit this extent of shrinkage when annealed include ceramic pastes, and other materials comprising particulates in a binder.

[0029] It should be noted that, according to certain aspects, the relatively small area of the cathode pad area in comparison to the overall area of the stack is made possible by the deposited mesa or dam structure and yields benefits in the completed battery device. For example, all of the active layers of the battery device can occupy the remaining area outside the defined cathode pad area, improving the overall capacity of the battery device as opposed to battery devices formed using conventional maskless fabrication techniques. In one example, the overall area of the battery device is about $1x10^{-2}$ cm^2, and the area of the cathode pad area is about $4x10^{-4}$ cm^2. (Note that the cathode pad area is shown covering a much larger fraction of the battery area in the figures, than would be the case in an actual device – the figures are representative of the device and some features have been drawn larger than they would be in an actual device simply for ease and clarity of illustration. The same comment applies also to thicknesses of layers and other features.)

[0030] Next, as shown in FIGS. 4A & 4B, laser ablation or a mild mechanical abrasion planarization process is performed to remove the stack of layers – cathode, electrolyte and anode current collector – from the top of the conductive mesa structure 105.

[0031] Next, as shown in FIGS. 5A & 5B, additional conductive mesa structures 109 can optionally be formed on top of the anode current collector 108 to provide electrical contact pad areas for the anode. These conductive mesa structures can be formed similarly to the mesa structure for the cathode, and can comprise similar materials as described above. Moreover, although not necessarily to scale, FIG. 5B illustrates aspects of the embodiments, in which the relatively tall conductive mesas provide good cathode (and optionally anode) packaging and assembly connections. For example, the active battery layers – cathode, electrolyte and anode current collector – can be about 10 microns thick, while the conductive mesas can be formed to be about 20 to 500 microns high, depending on the battery application. As should also be apparent, according to aspects of embodiments, the height of the conductive mesas is greater than a thickness of the deposited battery layers – cathode, electrolyte and anode current collector.

[0032] Next, as shown in FIGS. 6A & 6B, an encapsulation layer 110 is deposited over the entire device. The encapsulation layer can comprise one or more layers of polymer materials such as parylene, epoxy, etc. and/or other encapsulating layers. These layer(s) may have built-in in-situ thermal or UV anneal or cure processes, as needed. The encapsulation layer in embodiments can be 10 to 20 microns in thickness, and can be thicker to provide adequate surface planarization if needed. Parylene can be deposited by a room temperature vapor condensation process, in a vacuum chamber. Epoxies and other polymers are usually applied via a process method such as spin coating, dip coating, powder coating etc. to achieve adequate surface planarization and an effective moisture/gas permeation barrier.

[0033] Next, as shown in FIGS. 7A & 7B, the encapsulation layer 110 is partially removed to expose the tops of the conductive mesas which form battery pad contact areas for the cathode, and optionally anode. A laser ablation process may be used for partial removal of the encapsulation layer.

[0034] FIG. 8 is a schematic illustration of a processing system 800 for fabricating a TFB device having mesa structures according to some embodiments of the present disclosure. The processing system includes a standard mechanical interface (SMIF) 803 to a cluster tool 801 equipped with a reactive plasma clean (RPC) chamber 802 and process chambers 811, 812, 813 and 814, which may be utilized in the blanket deposition steps described above. A

glovebox 804 may also be attached to the cluster tool if needed. The glovebox can store substrates in an inert environment (for example, under a noble gas such as He, Ne or Ar), which is useful after alkali metal/alkaline earth metal deposition, if used. An ante chamber 805 to the glovebox may also be used if needed – the ante chamber is a gas exchange chamber (inert gas to air and vice versa) which allows substrates to be transferred in and out of the glovebox without contaminating the inert environment in the glovebox. (Note that a glovebox can be replaced with a dry room ambient of sufficiently low dew point as such is used by lithium foil manufacturers.) The process chambers 811, 812, 813 and 814 can be configured for process steps for manufacturing thin film battery devices which may include: deposition of a cathode layer (e.g. $LiCoO_2$ by RF sputtering); deposition of an electrolyte layer (e.g. RF sputtering of Li_3PO_4 in N_2); deposition of an alkali metal or alkaline earth metal; and possibly the deposition and annealing of insulating and conductive mesa structures. Examples of suitable cluster tool platforms include display cluster tools. It is to be understood that while a cluster arrangement has been shown for the processing system 800, a linear system may be utilized in which the processing chambers are arranged in a line without a transfer chamber so that the substrate continuously moves from one chamber to the next chamber.

[0035] FIG. 9 shows a representation of an in-line fabrication system 900 with multiple in-line tools 910, 920, 930 and 940, although more tools may be used than are shown in the illustrative figure, according to some embodiments. In-line tools may include tools for depositing all the active layers and mesa structures of a TFB device according to embodiments. Furthermore, the in-line tools may include pre- and post-conditioning chambers. For example, tool 910 may be a pump down chamber for establishing a vacuum prior to the substrate moving through a vacuum airlock 915 into a deposition tool 920. Some or all of the in-line tools may be vacuum tools separated by vacuum airlocks 915. Note that the order of process tools and specific process tools in the process line will be determined by the particular TFB device fabrication method being used – specific examples of which are provided above. Furthermore, substrates may be moved through the in-line fabrication system oriented either horizontally or vertically.

[0036] In order to illustrate the movement of a substrate through an in-line fabrication system such as shown in FIG. 9, in FIG. 10 a substrate conveyer 950 is shown with only one in-line tool 910 in place. A substrate holder 955 containing a substrate 1010 (the substrate holder is shown partially cut-away so that the substrate can be seen) is mounted on the

conveyer 950, or equivalent device, for moving the holder and substrate through the in-line tool 910, as indicated. An in-line platform for processing tool 910 may in some embodiments be configured for vertical substrates, and in some embodiments configured for horizontal substrates.

[0037] An apparatus for forming thin film batteries according to some embodiments may comprise: a first system for blanket depositing a first current collector layer on a substrate; a second system for forming an insulating mesa structure defining a boundary of an active area of the solid state battery, the insulating mesa forming a continuous wall around the active area; and a third system for blanket depositing a cathode layer, an electrolyte layer and an second current collector layer. Furthermore, the insulating mesa may further define a boundary of a contact area of the first current collector, the insulating mesa forming a continuous wall around the contact area, and the apparatus may further comprise a fourth system for depositing a first conductive mesa on the contact area. Furthermore, the apparatus may comprise a fifth system for removing the cathode layer, the electrolyte layer and the second current collector layer off the top surface of the first conductive mesa. Furthermore, the apparatus may comprise a sixth system for depositing an encapsulation layer over the second current collector. Furthermore, the apparatus may comprise a seventh system for depositing a second conductive mesa on the second current collector. The systems may be cluster tools, in-line tools, stand-alone tools, or a combination of one or more of the aforementioned tools. Furthermore, the systems may include some tools which are common to one or more of the other systems.

[0038] The insulating mesa structures in embodiments provide a structural support for stacking battery cells – the mesa walls being taller than the thickness of the active device layers, provide protection to the active area of each battery cell.

[0039] Although the present disclosure has been particularly described with reference to solid state batteries with electrical connection to both cathode and anode from a top surface, in other embodiments solid state batteries may be fabricated on electrically conductive substrates, and electrical connection to the bottom current collector may be made through the substrate, in which case the battery can be fabricated without the insulating mesa wall 104 and conductive mesa 105 of FIGS. 2A & 2B.

[0040] Although the present disclosure has been particularly described with reference to solid state batteries fabricated with cathode on the bottom (closer to the substrate) and

anode on the top, in some embodiments solid state batteries may be fabricated with anode on the bottom (closer to the substrate) and cathode on the top.

[0041] Although the present disclosure has been particularly described with reference to some embodiments thereof, it should be readily apparent to those of ordinary skill in the art that changes and modifications in the form and details may be made without departing from the spirit and scope of the disclosure. It is intended that the appended claims encompass such changes and modifications.

WHAT IS CLAIMED IS:

1. A solid state battery comprising:

a substrate;

a first current collector deposited on the surface of said substrate;

an insulating mesa deposited on said cathode current collector, said insulating mesa defining a boundary of an active area of said solid state battery, said insulating mesa forming a continuous wall around said active area; and

a stack of active device layers within said boundary, said stack comprising a cathode layer, an electrolyte layer and a second current collector layer;

wherein a height of said insulating mesa is greater than a thickness of said stack of active device layers.

2. The solid state battery of claim 1, wherein said insulating mesa further defines a boundary of a contact area of said first current collector, said insulating mesa forming a continuous wall around said first contact area, and further comprising a first conductive mesa for providing electrical contact to said first current collector, wherein said first conductive mesa is deposited on said contact area, and wherein a height of said first conductive mesa is greater than a thickness of said stack of active device layers.

3. The solid state battery of claim 1, further comprising a second conductive mesa deposited on said second current collector, for making electrical contact to said second current collector.

4. The solid state battery of claim 1, further comprising an encapsulation layer over said stack of active device layers.

5. The solid state battery of claim 1, wherein said stack of active device layers further comprises an anode layer.

6. The solid state battery of claim 1, wherein said solid state battery is a thin film solid state battery.

7. A method of fabricating a solid state battery comprising:

providing a substrate;

depositing a first current collector layer on said substrate;

forming an insulating mesa on said first current collector layer, said insulating mesa defining a boundary of an active area of said solid state battery, said insulating mesa forming a continuous wall around said active area; and

depositing a stack of active device layers within said boundary, said stack comprising a cathode layer, an electrolyte layer and a second current collector layer;

wherein a height of said insulating mesa is greater than a thickness of said stack of active device layers.

8. The method of claim 7, wherein said insulating mesa further defines a boundary of a contact area of said first current collector, said insulating mesa forming a continuous wall around said contact area, and further comprising, before said depositing said stack of active device layers, depositing a first conductive mesa on said contact area, for providing electrical contact to said first current collector, wherein a height of said first conductive mesa is greater than a thickness of said stack of active device layers.

9. The method of claim 7, further comprising, after said depositing said stack of active device layers, removing said stack of active device layers from a top surface of said first conductive mesa.

10. The method of claim 7, further comprising depositing a second conductive mesa on said second current collector, for making electrical contact to said second current collector.

11. The method of claim 7, further comprising depositing an encapsulation layer over said stack of active device layers.

12. An apparatus for fabricating a solid state battery comprising:

a first system for blanket depositing a first current collector layer on a substrate;

a second system for forming an insulating mesa structure defining a boundary of an active area of said solid state battery, said insulating mesa forming a continuous wall around said active area; and

a third system for blanket depositing a cathode layer, an electrolyte layer and an second current collector layer.

13. The apparatus of claim 12, wherein said insulating mesa further defines a boundary of a contact area of said first current collector, said insulating mesa forming a continuous wall around said contact area, and further comprising a fourth system for depositing a first conductive mesa on said contact area.

14. The apparatus of claim 13, further comprising a fifth system for removing said cathode layer, said electrolyte layer and said second current collector layer off a top surface of said first conductive mesa.

15. The apparatus of claim 12, wherein said apparatus comprises in-line processing systems.

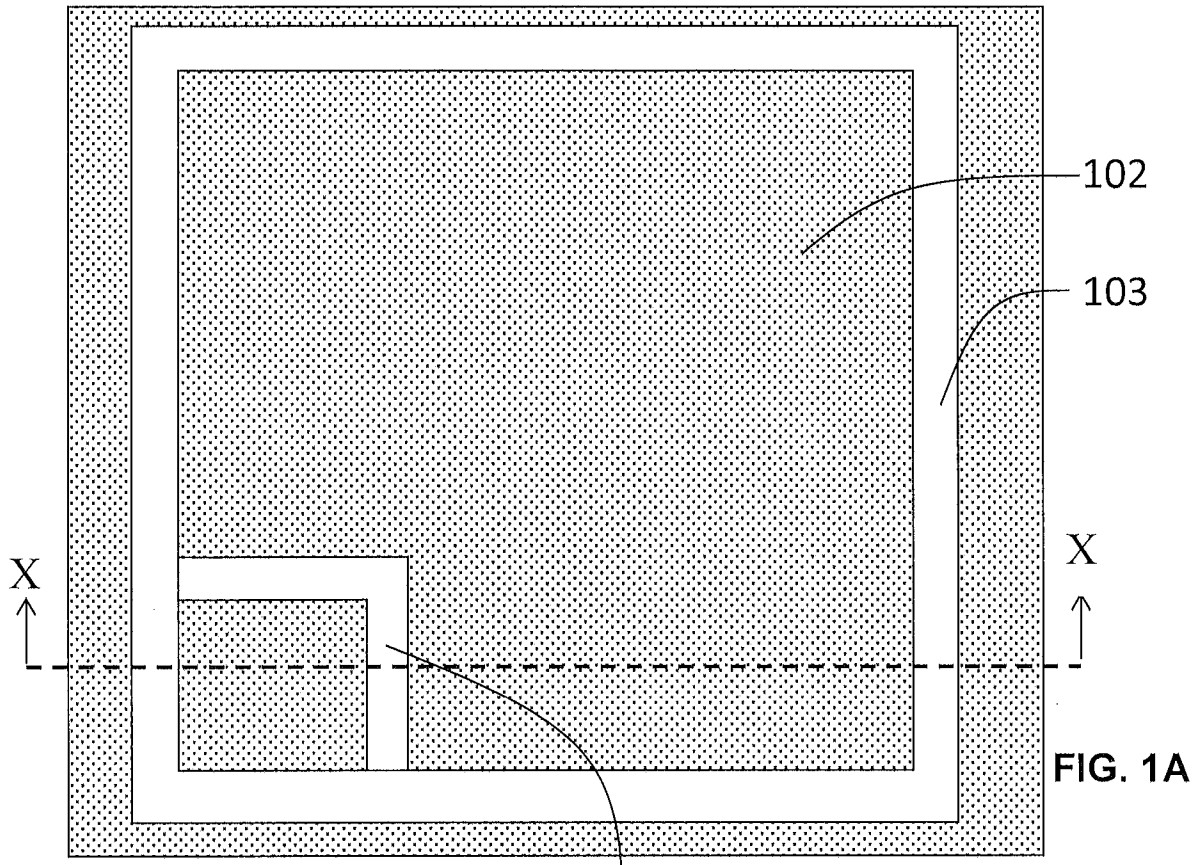


FIG. 1A

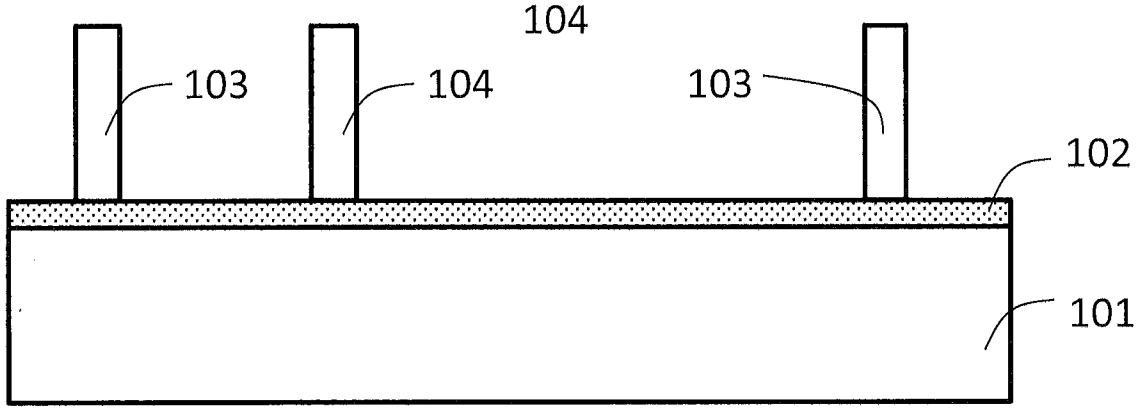


FIG. 1B

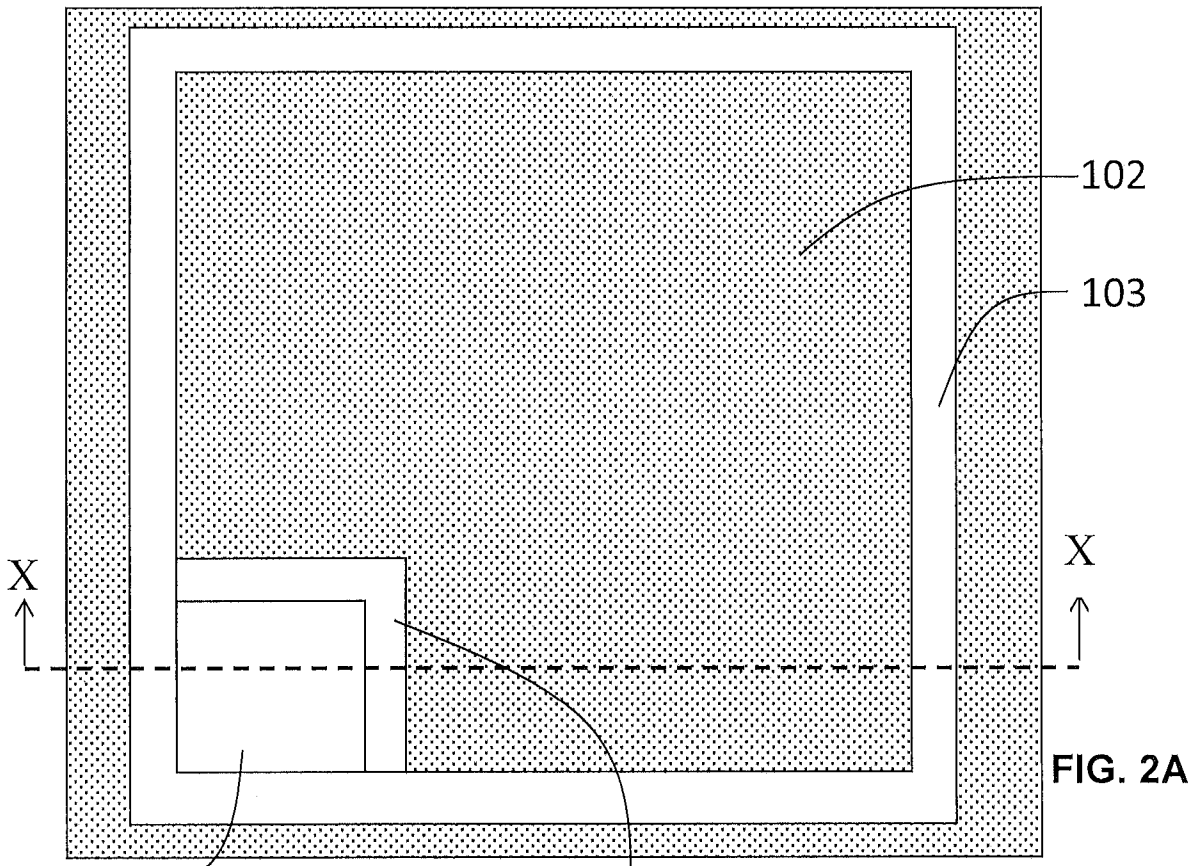


FIG. 2A

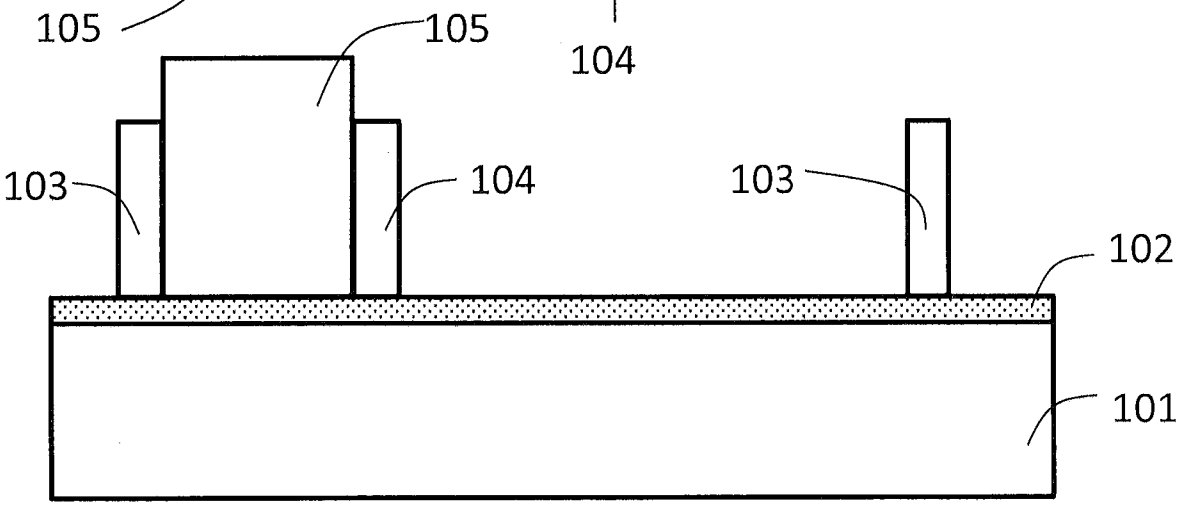


FIG. 2B

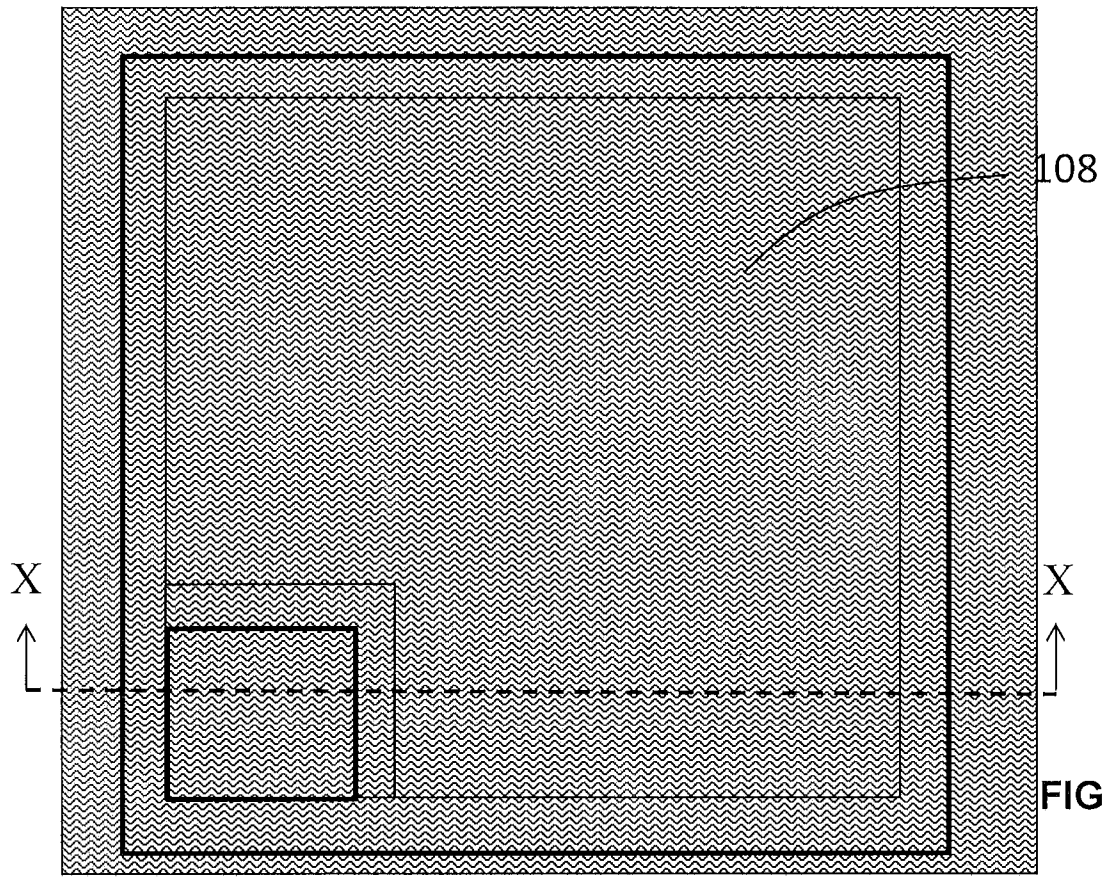


FIG. 3A

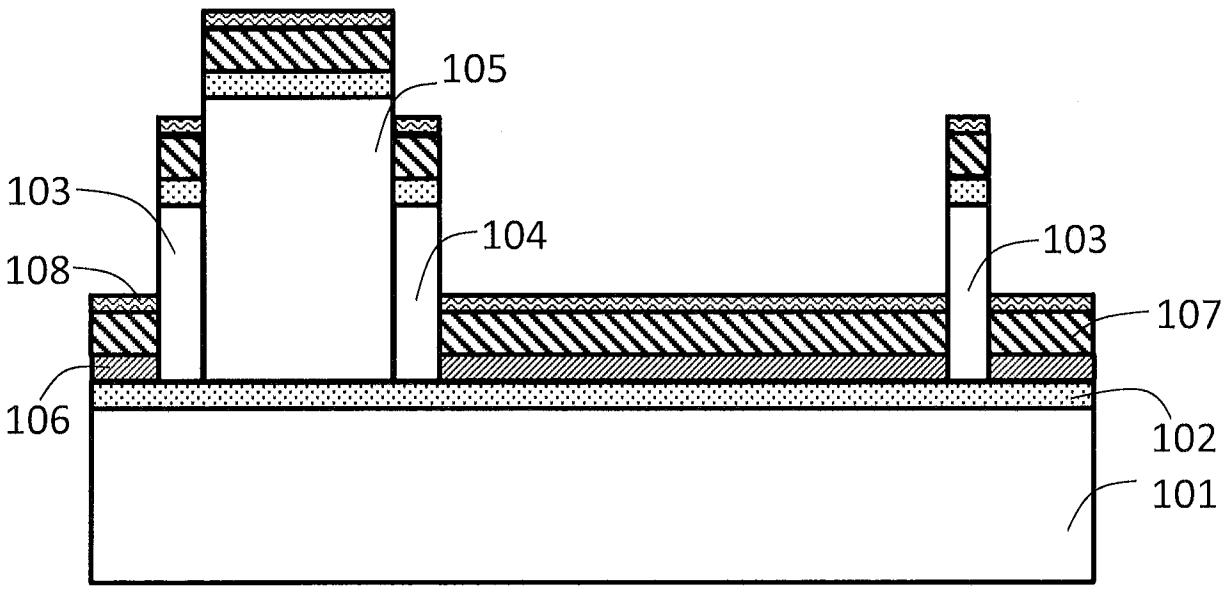


FIG. 3B

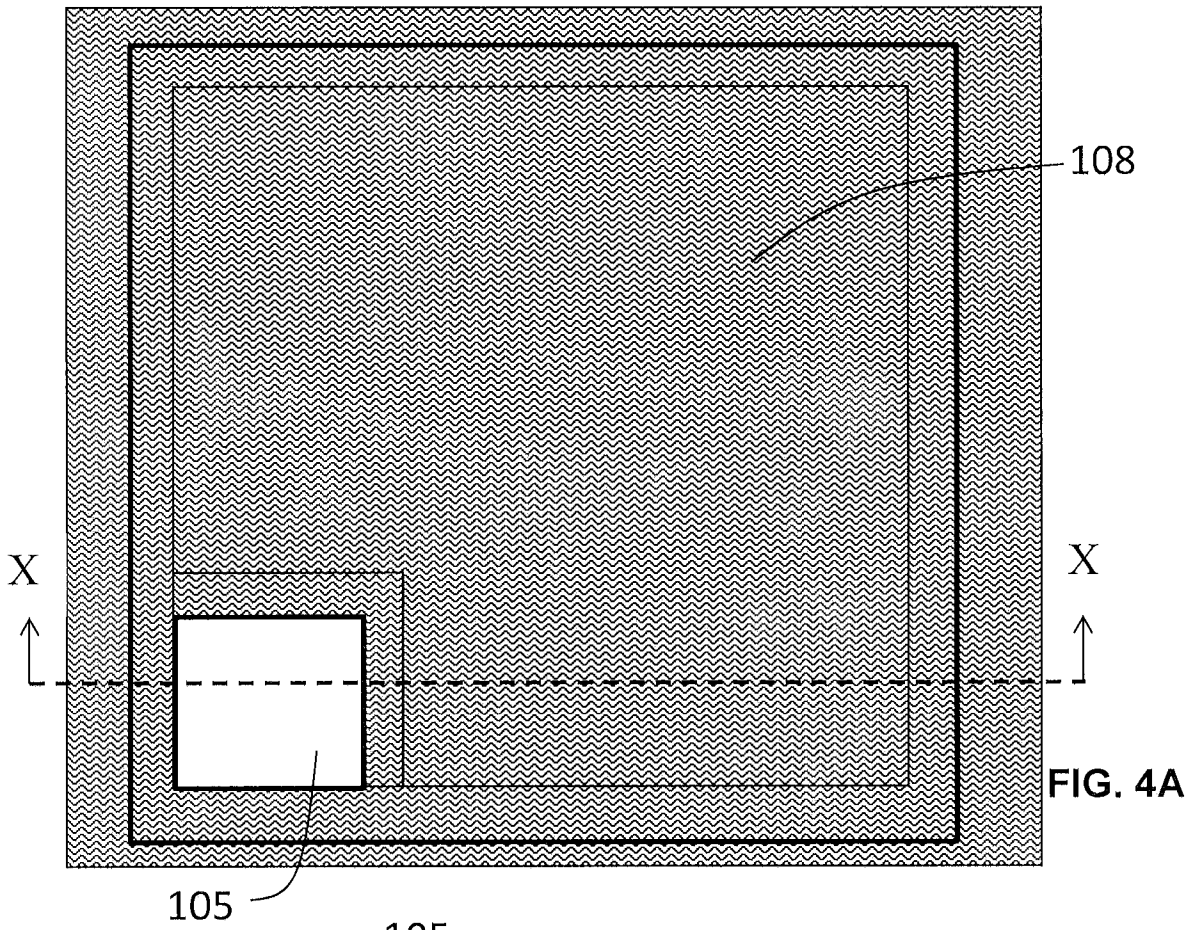


FIG. 4A

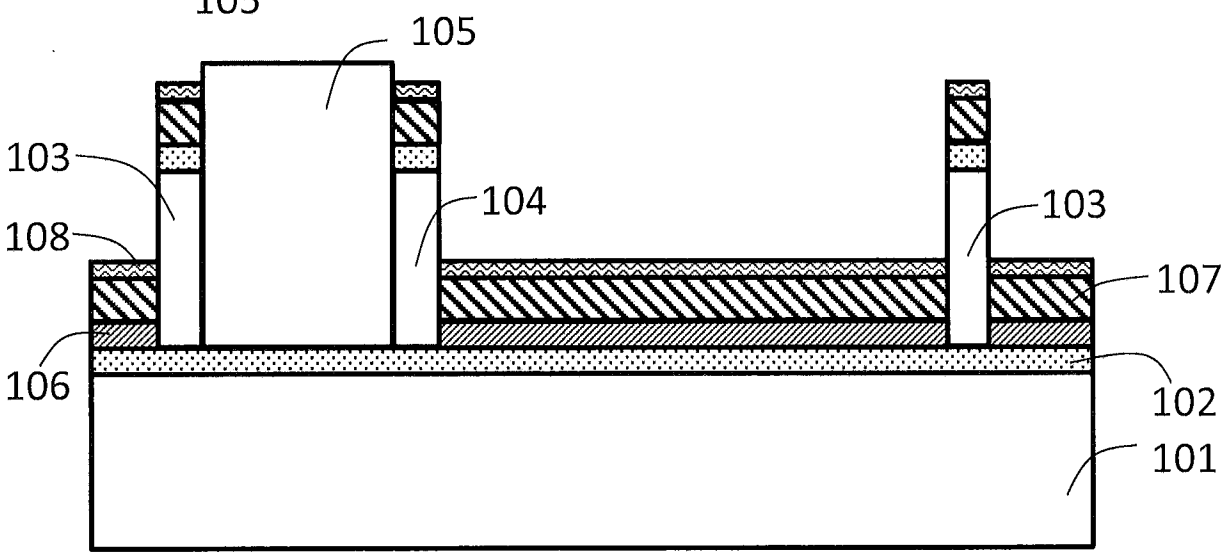


FIG. 4B

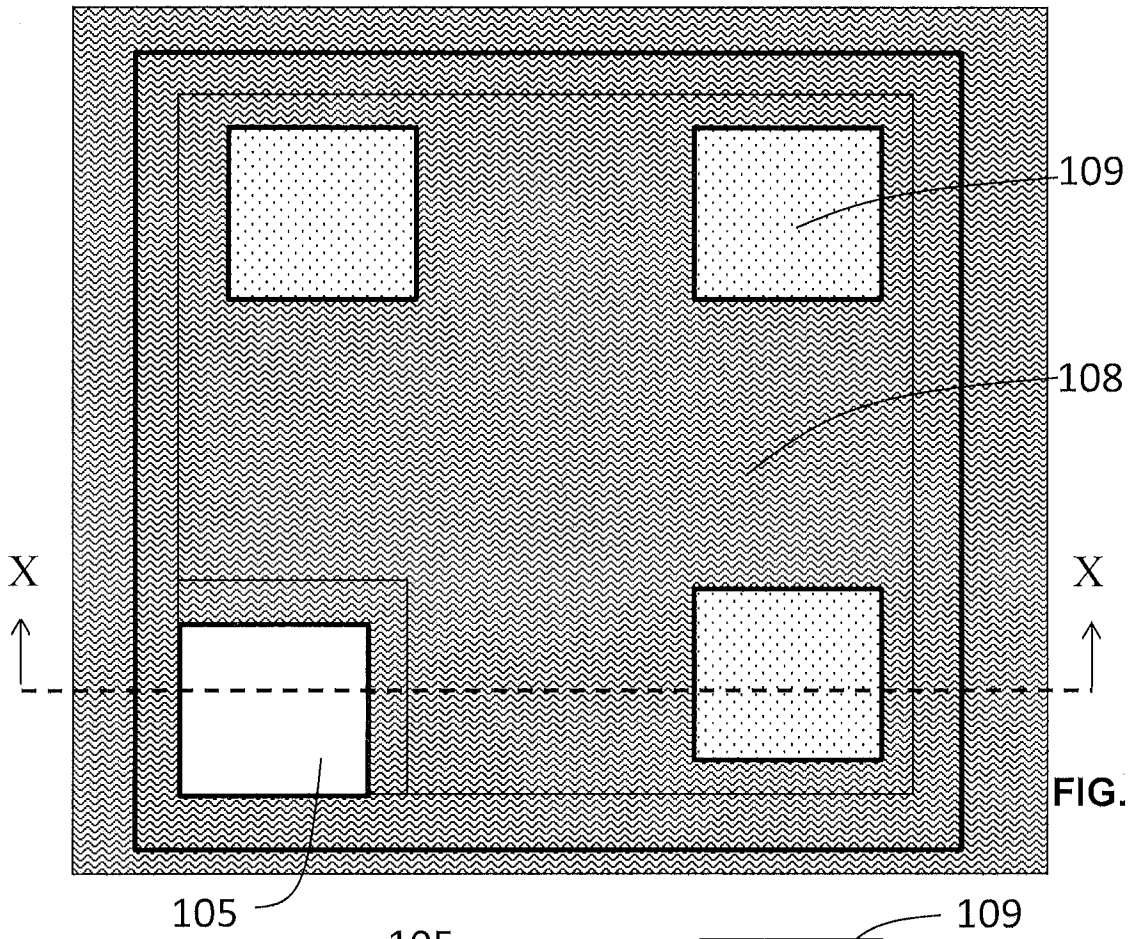


FIG. 5A

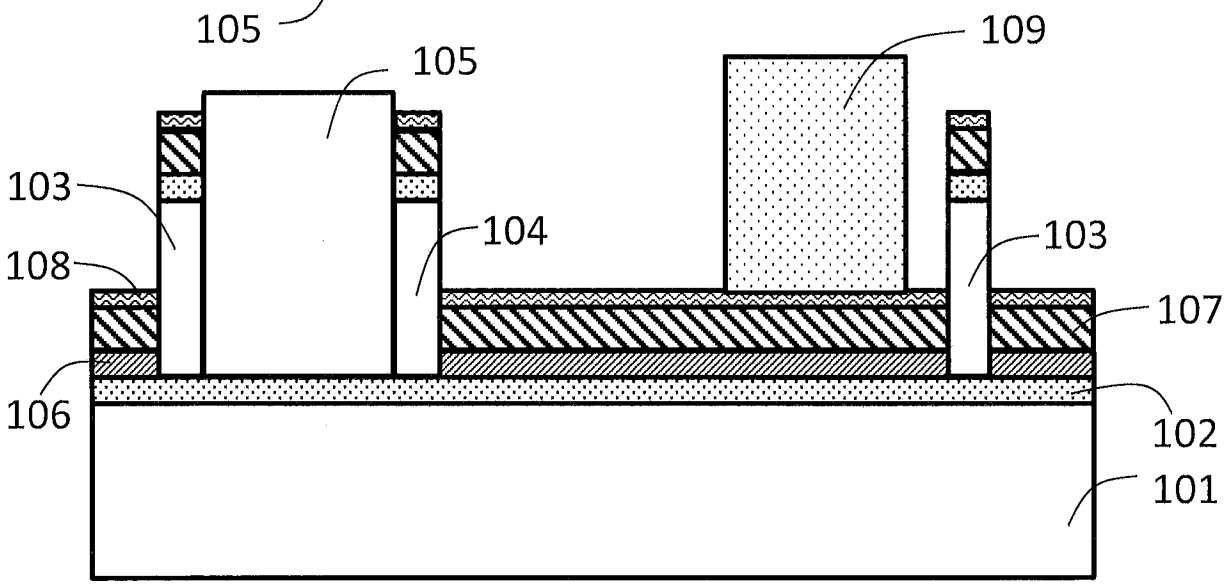


FIG. 5B

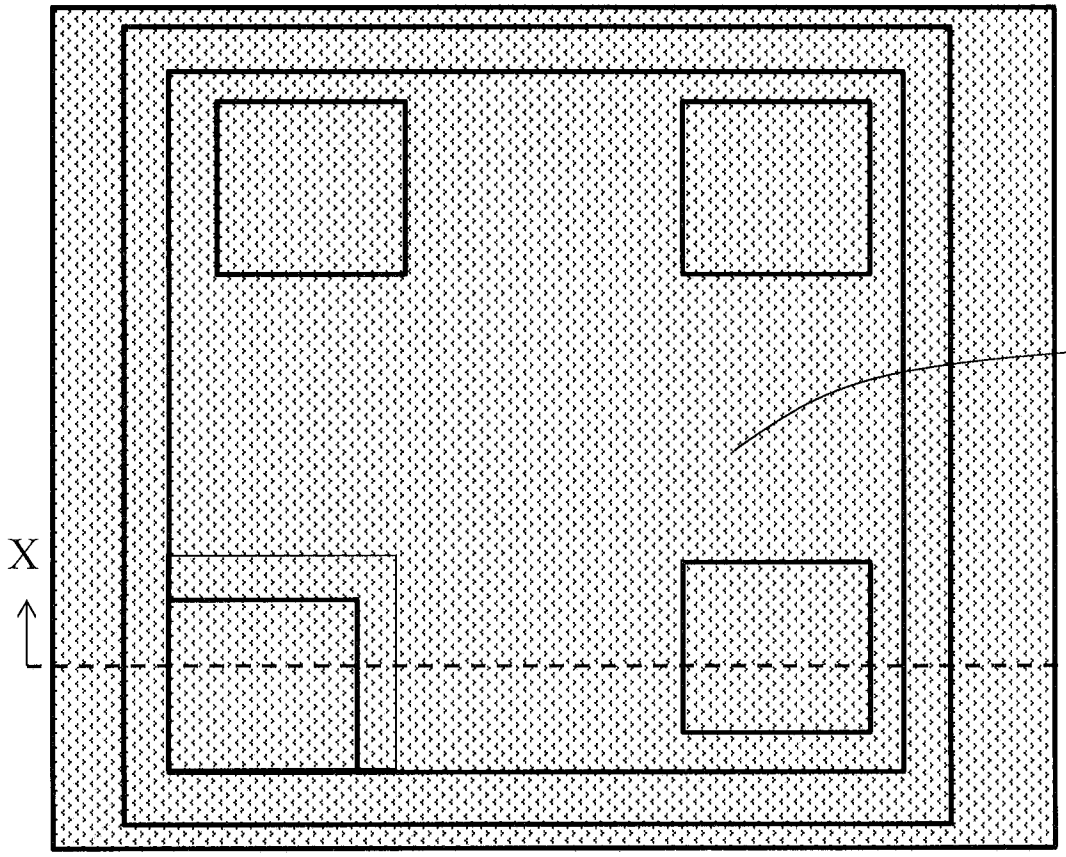


FIG. 6A

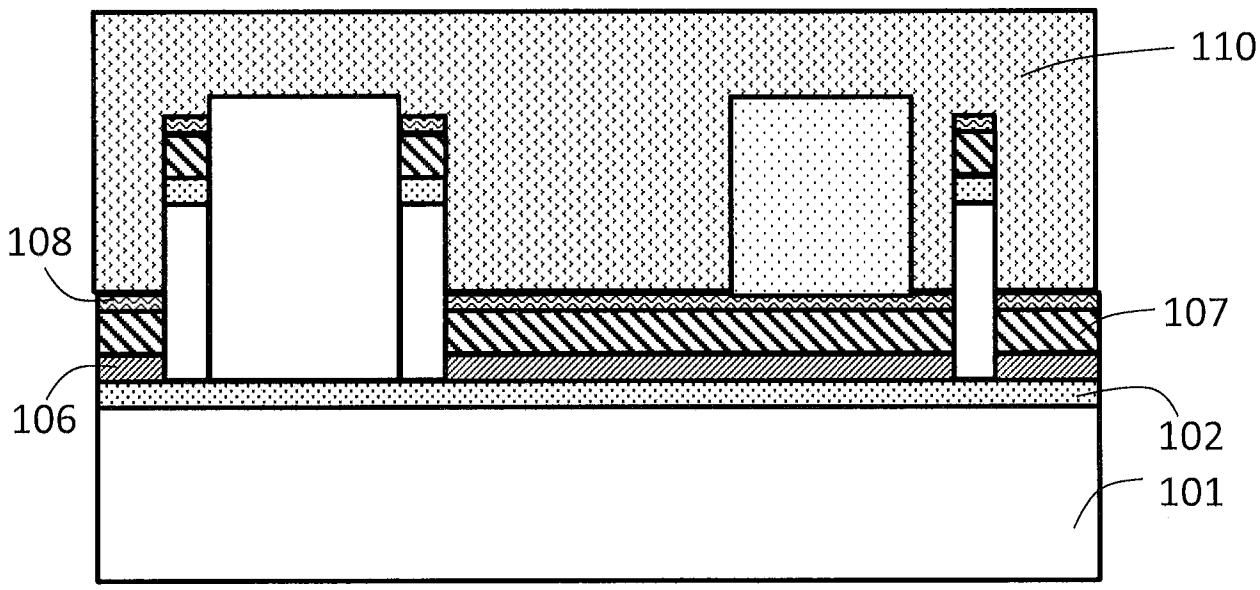


FIG. 6B

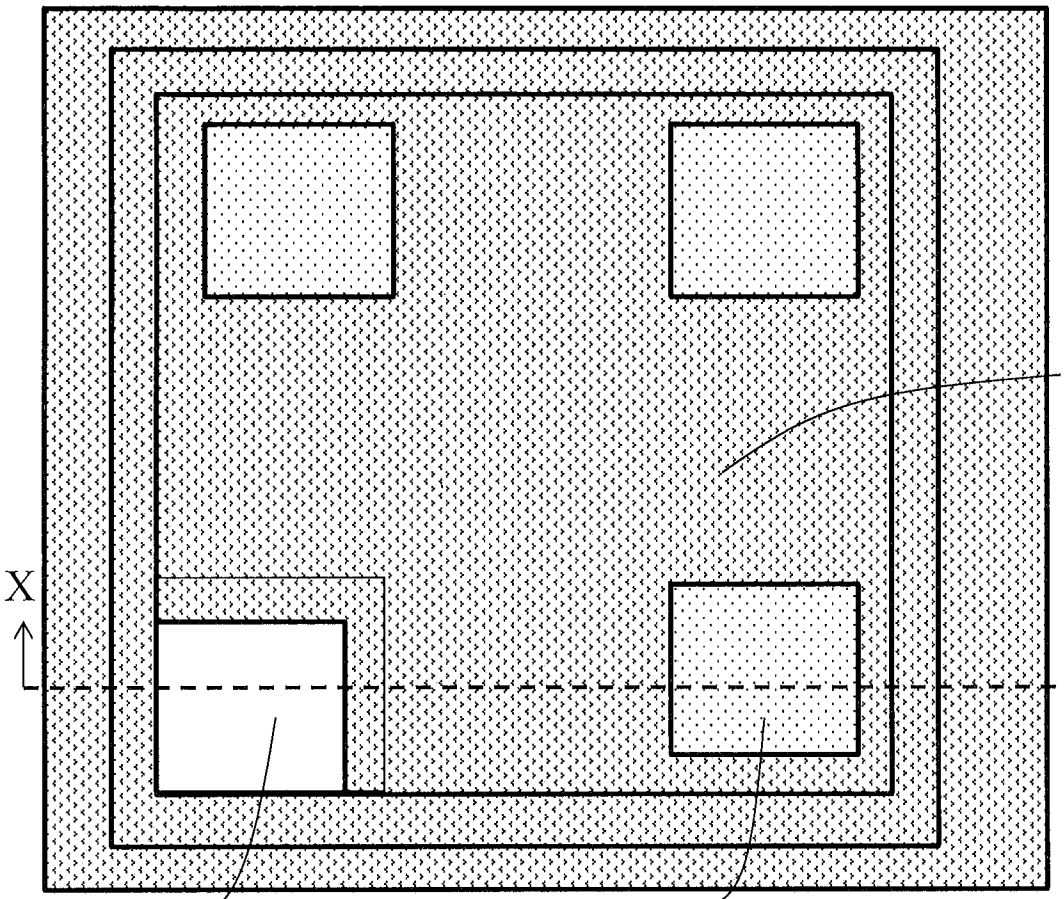


FIG. 7A

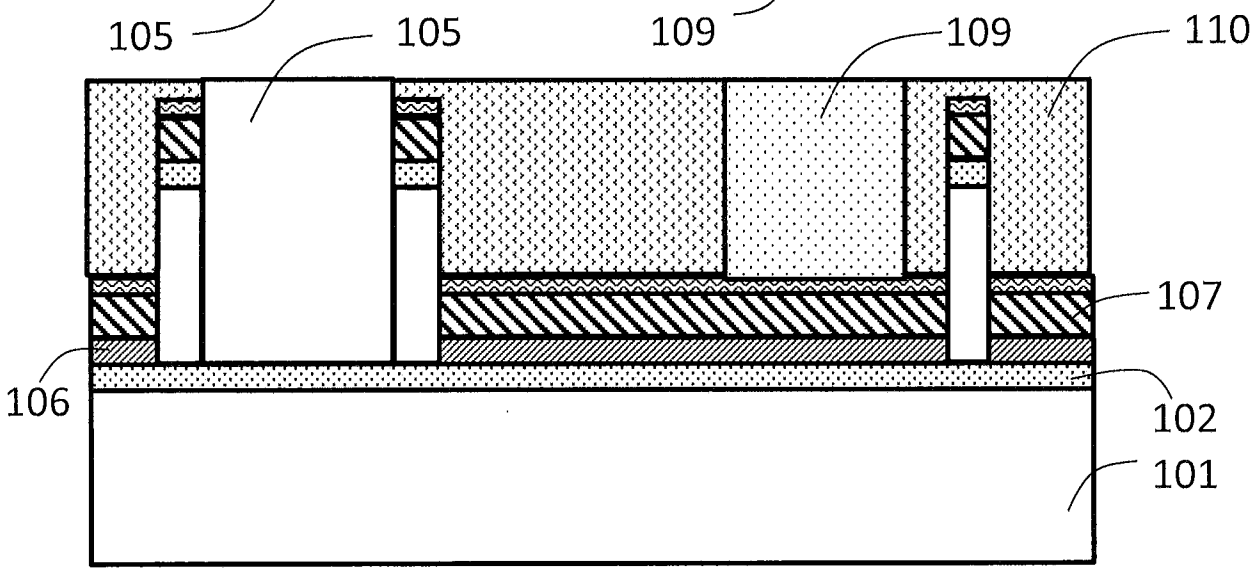


FIG. 7B

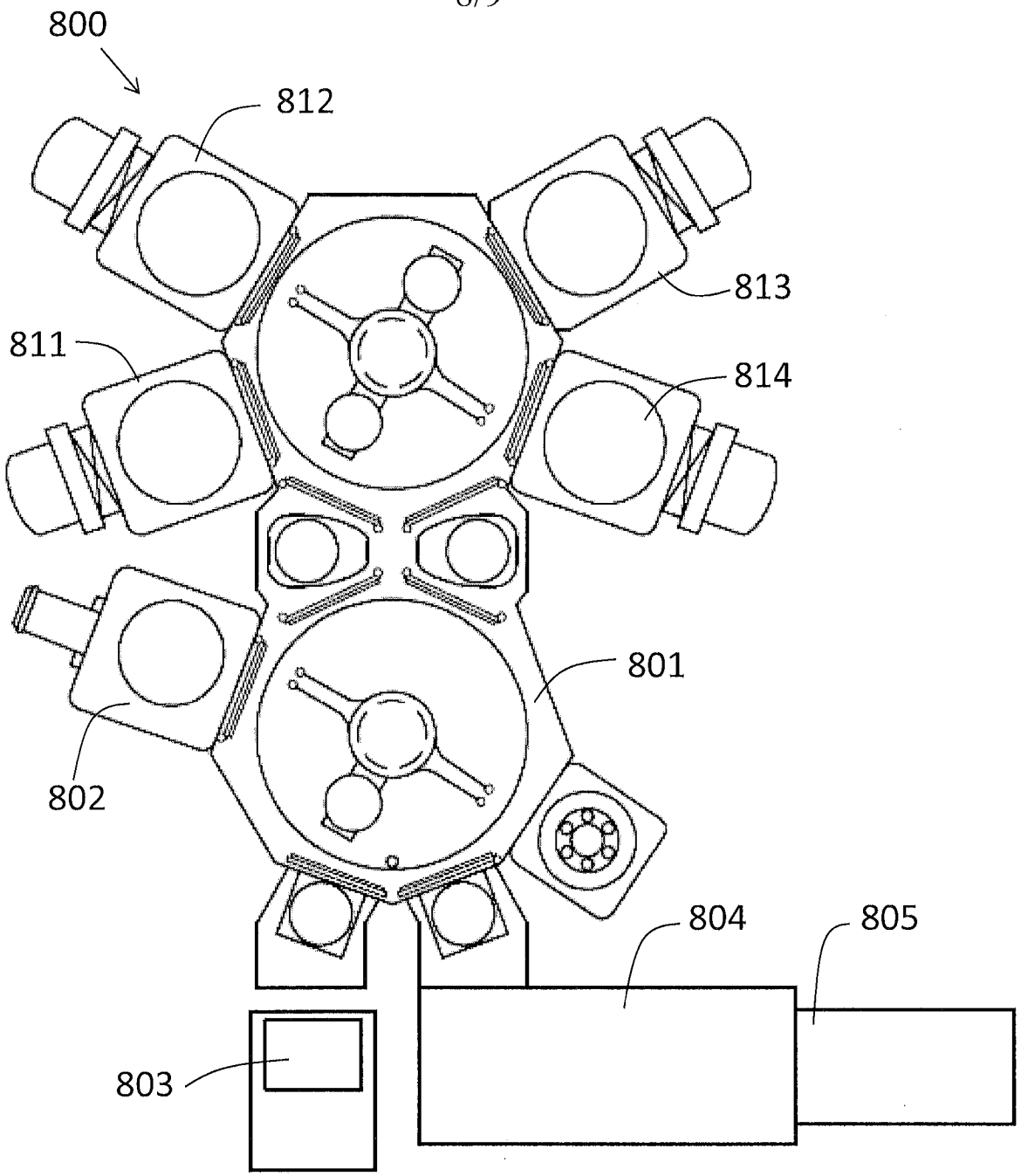


FIG. 8

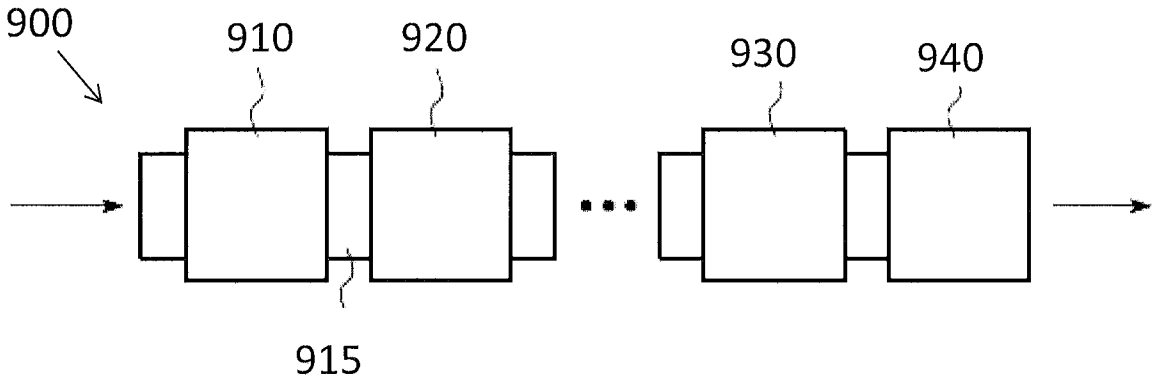


FIG. 9

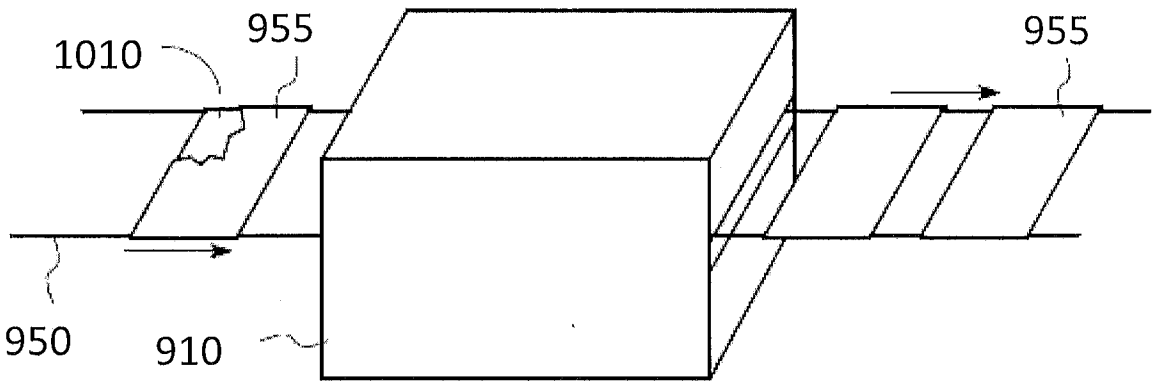


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/029855

A. CLASSIFICATION OF SUBJECT MATTER

H01M 6/40(2006.01)I, H01M 6/18(2006.01)I

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01M 6/40; H01M 10/0525; H05K 1/16; H01M 4/02; H04N 9/09; C25D 13/02; H01M 4/04; H01G 7/00; H01M 10/02; H01M 10/04; H01M 6/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:battery, insulating mesa, current collector, cathode, electrolyte, anode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008-0286651 A1 (NEUDECKER, BERND J. et al.) 20 November 2008 See abstract; paragraphs [0002] and [0053]-[0096]; claims 10 and 13; and figures 10 and 11.	1-15
Y	US 4525766 A (PETERSEN, KURT E.) 25 June 1985 See abstract; columns 1-6; and figures 1 and 4.	1-15
A	US 2011-0287296 A1 (SABI, YUICHI et al.) 24 November 2011 See abstract; paragraphs [0018]-[0027]; claims 10-12; and figure 2.	1-15
A	US 2014-0308576 A1 (I-TEN) 16 October 2014 See abstract; paragraphs [0037]-[0053]; claim 23; and figure 2.	1-15
A	US 2014-0076622 A1 (NEUDECKER, BERND J. et al.) 20 March 2014 See abstract; paragraphs [0014]-[0028]; claim 1; and figure 2.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 August 2016 (09.08.2016)	**09 August 2016 (09.08.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/029855

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