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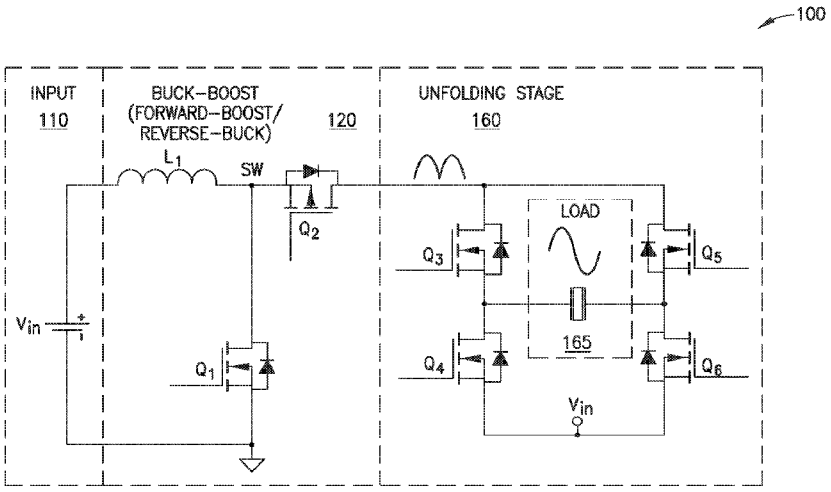


FIG. 1

(57) Abstract: A driver for a circuit with a capacitive load, is disclosed, including a power converter to receive an input voltage and generate a clean folded waveform as an output. An unfolding stage referenced to the input voltage is configured to receive the clean folded waveform from the power converter and unfold the folded waveform into a full waveform. The driver includes a controller to control the driver. The converter may operate bi-directionally.

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Driver for a High Voltage Capacitive Actuator

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application serial number 62/233,631, filed September 28, 2015, entitled "COMPACT, LOW-POWER, AND NOISELESS ACTUATOR DRIVER," and U.S. Provisional Patent Application serial number 62/266,318, filed December 11, 2015, entitled "Piezoelectric Driver," both of which are incorporated by reference herein in their entireties.

FIELD OF THE INVENTION

The present invention relates to the control circuitry (driver) for high voltage capacitive actuators, for example, electrostatic, electro-mechanical polymer (EMP), electro-active polymer (EAP), and piezoelectric actuators.

BACKGROUND OF THE INVENTION

Active cooling systems, such as fans, face multiple challenges when implemented in ultrathin devices, such as tablet or laptop computers. General Electric (GE) has developed a cooling device using two piezoelectric membranes, called a Dual Piezoelectric Cooling Jet (DCJ). The piezoelectric membranes are electrically activated, causing them to expand and contract, forming a cavity that spills air at a high velocity, for example, like a bellows. However, the DCJ is an energy intensive device, and a DCJ driver may be large and expensive. Further, the DCJ membranes operate like a speaker/transducer, so that any oscillations within the human hearing band (approximately 200 Hz to 20 KHz), for example, due to noise or distortion in the driver signal, may be audibly detected.

FIG. 19 shows a prior art topology for a single-phase voltage source inverter for renewable energy sources. The circuit includes an input stage, a buck-boost stage, and an unfolding stage. It was implemented in discrete parts due to the high power to process. This circuit is based on a typical PI controller or Energy controller and very low fixed frequency switching. This typically leads to very high distortion level (> 5%), low power efficiency at low power output and very limited boost voltage ratio ≈ 3.5 (Vout/Vin). Therefore, there is a need in the industry to address one or more of the abovementioned shortcomings.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide a driver for a high voltage capacitive actuator. Briefly described, the present invention is directed to a driver for a circuit with a capacitive load, including a power converter to receive an input voltage and generate a clean folded waveform as an output. An unfolding stage referenced to the input voltage is configured to receive the clean folded waveform from the power converter and unfold the folded waveform into a full waveform. The driver includes a controller to control the driver. The converter may operate bi-directionally.

Other systems, methods and features of the present invention will be or become apparent to one having ordinary skill in the art upon examining the following drawings and detailed description. It is intended that all such additional systems, methods, and features be included in this description, be within the scope of the present invention and protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings

illustrate embodiments of the invention and, together with the description, serve to explain the principals of the invention.

FIG. 1 is a schematic diagram depicting an exemplary first embodiment driver topology.

FIG. 2A is a circuit diagram for a 2-switch buck-boost driver first alternative to the buck-boost driver of FIG. 1.

FIG. 2B is a circuit diagram for a 2-switch tapped inductor buck-boost driver second alternative to the buck-boost driver of FIG. 1.

FIG. 2C is a circuit diagram for a 2-switch flyback buck-boost driver third alternative to the buck-boost driver of FIG. 1.

FIG. 2D is a circuit diagram for a 2-switch flyback buck-boost low side secondary switch fourth alternative to the buck-boost driver of FIG. 1.

FIG. 3A is a circuit diagram illustrating an output configuration with a full-bridge connected to a capacitive load.

FIG. 3B is a circuit diagram illustrating an output configuration in which a full-bridge with discrete voltage reference choices is connected to a capacitive load.

FIG. 3C is a circuit diagram illustrating an output configuration in which a full bridge with an analog variable reference is connected to a capacitive load.

FIG. 3D is a circuit diagram illustrating an output configuration with load connected to a discrete variable reference.

FIG. 3E is a circuit diagram illustrating an output configuration with a load connected to variable analog reference.

FIG. 4 is a circuit diagram illustrating a prior art pseudo-resonant operation of a power converter.

FIG. 5 is a circuit diagram illustrating a more recent prior art pseudo-resonant operation of a power converter using similar principals to the circuit of FIG. 4.

FIG. 6A illustrates a first alternative embodiment of the unidirectional power input.

FIG. 6B illustrates a second alternative embodiment of the unidirectional power input where losses in the input are lowered by using an active switch.

FIG. 6C illustrates a third alternative embodiment of the unidirectional power input where, more generally, any power converter can be used.

FIG. 6D illustrates a first alternative embodiment of the converter with a bi-directional converter for the input.

FIG. 7 shows two voltage plots illustrating the effect of supplying a bi-directional converter with a unidirectional power input.

FIG. 8 is a schematic diagram of an exemplary floating low voltage supply.

FIG. 9 is a circuit diagram of a driver circuit embodiment having a common high-side gate driver vs a new driver.

FIG. 10A is a circuit diagram of a standard current DAC converter.

FIG. 10B is a circuit diagram of an enhanced current DAC for rapid settling of the current output node.

FIG. 11 is a plot showing the effect of decreasing the voltage difference between the DAC output and alternated path.

FIG. 12 is a circuit diagram of an exemplary single sensor bi-directional current sensing circuit with the DAC from FIG. 10B.

FIG. 13 is a schematic diagram illustrating an example of a controller for the present invention.

FIGS. 14A is a schematic block diagram of an exemplary embodiment for a driver controller.

FIG. 14B is a schematic diagram of an exemplary control configuration.

FIG. 15 is a plot of the output of the exemplary driver for a measured 101.8Vpp, 150Hz waveform in a 150nF capacitive load and a plot of its spectrum having a 0.38% THD+N in a 1MHz bandwidth .

FIG. 16 is a plot demonstrating how a pseudo-resonant synchronous buck operation saves up to 8.9% power vs regular buck operation for a 100 Vpp output in a 150 nF capacitor from a 5 V input.

FIG. 17 is a schematic diagram of a real-time adjustment of the current target to achieve precise turn-on/turn-off behavior.

FIG. 18A is a plot diagram of waveforms of the converter of FIG. 1 in boost mode.

FIG. 18B is a plot diagram of waveforms of the converter of FIG. 1 in regular buck mode.

FIG. 19 is a schematic diagram depicting a prior art driver topology.

DETAILED DESCRIPTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

In contrast to the prior art driver shown in FIG. 19, embodiments of the driver under the present invention may boost a voltage ratio in excess of 10 and may achieve a distortion level lower than 1% while being very efficient at a low power output. Implementing the topology using discrete parts for a piezoelectric driver is not an option due to size and cost constraints, but

a highly integrated topology is not straightforward as most CMOS processes cannot accommodate efficient bi-directional operation of the converter due to process limitations.

While the topology used in the present embodiments has similarities to the circuit of FIG. 19, the implementation of the topology in a single integrated circuit achieving significantly lower distortion and high power efficiency while used to drive capacitive load such as piezoelectric actuators is an important step forward to enable a variety of new applications such a high definition haptic feedback in mobile devices, and piezo cooling fans, among others.

Exemplary embodiments of a capacitive driver, for example, a driver for a dual piezoelectric cooling jet (DCJ), include a power converter configured to receive an input voltage v_{in} as input and generate a clean folded sine waveform as an output, an unfolding stage referenced to v_{in}, configured to receive the clean folded sine waveform from the converter and unfold the folded sine waveform into a sinusoidal waveform, and a controller configured to control the driver. The converter may be configured for bi-directional operation.

FIG. 1 shows an exemplary first embodiment 100 of a topology for a single-phase voltage source. The first embodiment 100 may be described as a pseudo-dc-link bi-directional driver with a single inductor L_1, that provides a total harmonic distortion (THD) lower than 0.5% and brings the power close to the effective power used by the load. Exemplary results from a prototype produced a total power of 64.04 mW and a THD+N of 0.38% for a 100 Vpp 150 Hz sinusoid in a 150 nF load from a 3.6 V power supply.

The circuit of the first embodiment 100 includes an input stage 110, a forward-boost/reverse-buck stage 120, and an unfolding stage 160. The circuit of the first embodiment 100 may be implemented in discrete parts due to the high power to process. The input stage may include a voltage source V_{in}, such as a battery. The input stage is described in more detail below

(see FIGS. 7A-7D). The buck-boost stage 120 is a forward-boost/reverse-buck converter that generates a clean folded sine waveform. The buck-boost stage 120 includes an inductor L_1 connected to V_{in}, a first low side switch Q1 connected between L_1 and ground, and a second switch Q2 connected between L_1 and the unfolding stage 160. The gate of the transistor in the first switch Q1 and the second switch may be connected to a gate driver (not shown).

While the first embodiment is described being used for sine waveforms, persons having ordinary skill in the art will appreciate the embodiments described herein may operate upon arbitrary and complex waveforms, for example, square, triangular, AM modulated, FM modulated, and are not limited to operating upon sine waveforms.

The inductor L_1, for example, with a DCJ, may be a 100 μH inductor. The inductor L_1 value may be selected in order to (1) achieve a target distortion (lower inductance increases switching frequency and decreases distortion/THD+N), and/or (2) minimize the switching frequency. In general, a lower switching frequency corresponds to lower power consumption.

The switches Q1 and Q2 may be of the same type, which may be the most practical choice for an integrated circuit (IC) implementation, although embodiments with mixed switches may be used. The switches Q1 and Q2 may be, for example, GaN, PMOS, MEMS switches, among other possible switches.

The unfolding stage 160 is referenced to V_{in} instead of GND. The unfolding stage includes a load 165, for example, a capacitor or a piezoelectric cooling jet, and switches Q3, Q4, Q5, and Q6. Therefore, to obtain 0 V differential, the output and input voltages are equal. Increasing the output voltage across the load 165 above the input voltage V_{in} creates the signal amplitude. Polarity of the output waveform may be selected by the configuration of the

unfolding stage 160. Consequently, using a 2-switch boost converter topology of the buck-boost stage 120 as power stage is sufficient since the input voltage only needs to be stepped up.

Bi-directional operation of the buck-boost stage 120 allows energy efficient control of the capacitive load 165. A full-bridge configuration is referenced to the input voltage (V_{in}) of the input stage 110 instead of ground, and unfolds the signal into a sinusoidal waveform across the load 165 of the unfolding stage 160 .

The maximum output voltage may have a value of $V_{in} + V_p$, where V_p is the differential output signal amplitude. That voltage overhead V_{in} has limited effect on system efficiency. The current passing through the load returns to V_{in}, not to GND. Thus, no direct power dissipation is linked to the voltage overhead. Nevertheless, there may be a small penalty due to the slightly lower efficiency of the converter 100 at a higher conversion ratio.

Given that the power processed by the converter 100 of the first embodiment is on the order of 100 mW with output voltage beyond 50 V, both DC and switching losses are important. Operating the converter 100 in borderline conduction mode (BCM) provides a good trade-off to minimize both. In this mode, the current flowing through the inductor L_1 returns back to zero at the end of a switching cycle and then starts to ramp up immediately for the next cycle. Compared to continuous conduction mode (CCM), BCM provides the opportunity for zero voltage. switching (ZVS) thereby reducing switching losses ($\propto fCV^2$) where f is the switching frequency, C is the parasitic capacitance at the switching node and V is the voltage difference between the minimum and maximum voltage value at the switching node. Compared to discontinuous conduction mode (DCM), the first embodiment 100 offers lower root mean square (RMS)

current thereby reducing DC losses ($\propto I_{rms}^2 R$), where I_{rms} is the root-mean-squared current and the resistance in the current path.

The following describes BCM and its limitations in converters with high conversion ratio as per the first embodiment 100. In this case, the conversion ratio goes up to 14.9 for a 50 Vac output from a 3.6 V input. In FIG. 18A a typical waveform of the converter 100 operating in boost mode is presented. First, Q1 turns on and the inductor L_1 current ramps up linearly. When Q1 turns off the voltage at the switching node increases to the output voltage value. Here, the body diode of Q2 turns on and charges the output. When the inductor L_1 current reaches 0, the diode turns off and the switching node voltage V_{SW} starts to oscillate. In the first embodiment 100, since the boost converter voltage gain is most of the time larger than 2, V_{SW} decreases to a little bit less than 0 and turns on the body diode of Q1. Thereupon, Q1 turns on again under zero voltage switching condition (ZVS), thus reducing the switching losses associated to the parasitic capacitance at the switching node.

FIG. 18B shows a similar case for the buck mode. Switch Q2 turns on and V_{SW} equals the output voltage while the inductor L_1 current magnitude increases. When Q2 turns off, V_{SW} goes to GND and Q1 body diode turns on. In this case, the diode voltage drop creates non-negligible DC losses due to low V_{in}. When the inductor current reaches 0, the LC tank starts an oscillation. In this case the L is L1 and C is the sum of all parasitic capacitance at the node switch.V_{SW} reaches a maximum at about 2 V_{in} at which point Q2 turns on for the next cycle. The considerable difference between the output voltage and V_{in} limits the power saving of that switching mechanism in buck mode.

When the buck-boost stage 120 is performing a buck operation, it is referred to herein as the buck converter 120. Operating the buck converter 120 as a pseudo resonant synchronous

buck converter improves its general efficiency by virtually eliminating switching losses due to the SW node capacitance and reducing DC losses due to diode voltage drop. In this mode, the two switches are used in the buck mode. When Q2 turns off, Q1 turns on in ZVS condition. Instead of going through the diode, the inductor L_1 current goes through Q1 which reduces DC losses. Then Q1 stays on until the inductor accumulates enough energy to charge V_{SW} to V_{out}. When Q1 turns off, V_{SW} rings to V_{out} and Q2 is turned on under ZVS condition thus reducing switching losses.

Alternative circuit blocks shown in FIGS. 2A-2D and described below may boost a voltage ratio between the output and input voltage in excess of 10:1 and may achieve a distortion level lower than 1% while being very efficient at a low power output. Implementing the topology as a discrete part for a piezoelectric driver may involve practical challenges due to size and cost constraints, but integrating the topology may not be straightforward as most CMOS processes do not accommodate efficient bi-directional operation of the converter due to process limitations.

While the topology used in the alternative embodiments of FIGS. 2A-2D have similarities to the circuit of FIG. 1, the topology may be implemented in a single integrated circuit (generally excepting inductor L) with significantly lower distortion and high power efficiency for driving a capacitive load such as a piezoelectric actuator. This is an important step forward to enable a variety of new applications.

The alternative_embodiments of FIGS. 2A-2D use a two-switch power converter cell as a bi-directional driver to control a capacitive load with low distortion analog waveforms. To achieve the desired performance level, the 2-switch power converter is designed to ensure that the switching frequency is high enough to allow the output waveform to reach the low-distortion level targeted. The frequency required can be estimated by:

$$Resolution = \log_2 \frac{f_{sw}}{2*f_{sig}} \quad \text{(Eq. 1)}$$

where f_{sw} is the converter switching frequency and f_{sig} is the frequency of the output signal. By standard analog theory, the resolution can be linked to an ideal distortion level.

FIGS. 2A-2D depict four examples of alternative embodiments of two-switch power converters that may be used to directly generate the output waveform to control a capacitive load. FIG. 2A is a circuit diagram depicting a driver topology for a 2-switch buck-boost converter 221. The 2-switch buck-boost converter 221 does not require a transformer or coupled inductor and may be used directly to drive a unipolar signal (always above 0) on the load. FIG. 2B is a circuit diagram depicting a driver topology for a 2-switch tapped inductor buck-boost converter 222. FIG. 2C is a circuit diagram depicting a driver topology for a 2-switch flyback buck-boost converter 223. FIG. 2D is a circuit diagram depicting a driver topology for a 2-switch flyback buck-boost low side secondary switch converter 223. Fig. 2B, 2C and 2D use the same principle as FIG. 2A. They may be preferable to 2A when the output voltage is higher as they may achieve lower power. The choice of the implementation depends upon the exact requirements for the application (e.g. size, power, fabrication process). The alternative converters 221-224 demonstrate that a capacitive load requiring low distortion analog waveform may be driven directly from a 2-switch bi-directional converter. The exact topology chosen may be application specific. The converter 221 may use synchronous switching, regular switching, or a combination of both to achieve the best performance for the application.

FIGS. 3A-3E present different configurations 301-305 of the unfolding stage 160 (FIG. 1), or output stage, that may be used for different driver embodiments to interface with the capacitive load 365. A standard full-bridge configuration 301 is presented in FIG. 3A, which is similar to the unfolding stage 160 (FIG. 1). The configuration 301 includes a load 365, for

example, a capacitor or an actuator, and switches Q3, Q4, Q5, and Q6. This configuration enables doubling the effective output voltage signal on the load 365, that translates for an actuator as approximately 2 times more displacement. The full-bridge may be a reference to the input voltage to be used with a power converter such as a 2-switch buck-boost (FIG 2A). FIG. 3B shows a full-bridge output 302 with discrete voltage reference choice. FIG. 3C shows a full-bridge output stage 303 with analog variable reference V_{ref}. FIG. 3D shows an output stage 304 with the load 365 connected to a discrete variable reference, whereas FIG. 3E shows an output stage 305 with the load 365 connected to a variable analog reference V_{ref}.

If the first stage is a 2-switch flyback configuration 223 (FIG. 2C), 224 (FIG. 2D), the full bridge may be referenced to GND, as shown by the converter 303 of FIG. 3B. In other cases, a full bridge converter 304 with discrete variable reference (FIG. 3C), enables higher power delivery efficiency. Note that while depicted with two alternative reference points (GND and V_{in} on FIG. 3B), the illustrated concepts may be expanded to an arbitrary number of discrete reference points. In a very low distortion application, a full bridge with variable analog reference may reduce distortion and improve converter stage efficiency. If a unipolar output is desired, the same approach may be used with the same advantages as shown in FIGS. 3D and 3E. For the converter output stage 303 shown in FIG. 3C and the output stage 305 shown in FIG 3E, the triangle symbol represents an amplifier to which one may feed a variable input V_{ref} and control that side of the load 365.

Combining the circuits of FIGS. 3B and 3C or FIGS. 3D and 3E provides for smoothing out the transition between the particular reference voltages while enabling higher power efficiency because the variable analog reference, which is less efficient than a simple switch, may be active only during the transition. Such combinations may provide the lower distortion

advantage of the analog reference while retaining most of the power advantage of the discrete reference approach.

Under the above described embodiments, the folded waveform is depicted as a "half" waveform (sine wave) and that is unfolded into a full waveform by an unfolding output stage 160. However, in some scenarios a better approach is directly applying the circuit of FIG. 2A with no output stage from FIGS. 3A-3E, where the driver generates the full waveform. Therefore, while there may be scenarios where the folded waveform may be a half waveform, the embodiments are not intended to be limited to generating a folded (half) waveform.

FIG. 4 shows a pseudo-resonant operation of a power converter 400 that was first proposed in 1991 to reduce switching losses in high frequency converters. The design is based on knowledge of the fixed input and output condition and the inclusion of a resonant network composed of an inductor and capacitor.

FIG. 5 shows an implementation of a circuit 500 using similar principals to the circuit of FIG. 4. Here again, the implementation includes passive components to achieve the benefit. High voltage capacitors C1 and C2 are included in the circuit thus increasing cost and size of the solution. Moreover, this implementation is a DC/DC converter so the input/output voltage relationship is static, thus simplifying the problem.

Compared with previous circuits, for example, as shown by FIG. 19, the first embodiment 100 (FIG. 1) may operate in pseudo-resonant mode without adding any dedicated reactive (inductive (L) or capacitive (C)) components. This provides the benefit of pseudo-resonant operation without use of additional components. The pseudo-resonant operation constantly monitors the output voltage. The output voltage is used to compute the current required in a first low-side switch Q1 pulse to achieve pseudo-resonant charging of the switching

node up to the output voltage. Moreover, because the output/input relationship is constantly changing, the controller dynamically adapts the current required in Q1 at each switching cycle to the present operating conditions. Since at some point, the converter needs to process levels of power that are below its capability, the pseudo-resonant implementation recognizes discontinuous conduction mode (DCM) and turns off Q1 in zero current switching (ZCS) mode to finish the synchronous switching cycle, without losing extra energy in the circuit. When the converter is in DCM and a new pulse is required to transfer energy, the circuit resumes first by turning on Q1 to generate a pseudo-resonant pulse and avoid high switching losses from hard switching a second switch Q2.

Although bi-directional operation of a power converter is used in many applications, single die bi-directional converters are not practical in standard CMOS technology due to parasitic transistors formed when current is flowing in the reverse direction. To solve that issue, the first embodiment driver 100 may be implemented using a Silicon on Insulator (SOI) technology. This enables the driver to have all its switches Q1-Q6 implemented on a single die which reduces size and cost of the solution.

A bi-directional converter transfers power in two directions: input to output, and output to input. When the bi-directional converter is used to drive a capacitive load, it can be assumed that the net flow of energy over a waveform period (where output starts and finishes at the same voltage level) may be from the input to the output due to the law of energy conservation. Losses in the system make it inevitable that more energy enters the system than exits the system. Also, in power converters, the general case is that the closer the voltage conversion ratio is to unity, the higher the conversion efficiency may be due to lower losses.

Providing a unidirectional power input to a bi-directional converter causes the following to happen. First, power is drawn from the input source when the power converter is in forward mode (input to output). Second, energy recovered accumulates on the input energy storage device, for instance a capacitor, when in reverse mode (output to input).

Energy accumulation on a capacitor causes input voltage to increase, thus lowering the voltage conversion ratio and leading to higher overall power efficiency. This is illustrated by voltage plots in FIG. 7. V_{P1} (top graph) is the differential voltage across a load, V_{in} (bottom graph) is the input voltage of the system, and $V_{in}1$ is the voltage at the input of the bi-directional converter. In phase 0, $V_{in}1$ sits at the same value as V_{in} when the converter operates in forward mode for the first time. In phase 1, the converter changes to reverse mode. The energy recovered accumulates on the bi-directional converter input energy storage device. Consequently, V_{in} increases. When the converter changes back to the forward mode in phase 2, it starts by consuming the energy accumulated on C1 (no current flows from V_{in} in this phase). When $V_{in}1$ reaches V_{in}, the converter starts to use energy from V_{in} again (Phase 3). Phases 1, 2, and 3 repeat themselves as long as the converter operates. Power savings are realized in two ways. First, during phases 2 and 3 the voltage conversion ratio is reduced yielding higher efficiency. Second, the RMS current (I_{rms}) flowing to/from V_{in} is reduced thus DC losses ($\propto I_{rms}^2 R$) where R is the parasitic resistance of the current path between V_{in} and V_{in1}.

The exact voltage increase can be adjusted by first calculating the maximum energy that may be recovered from the load and then sizing the input capacitor (C1) appropriately to achieve the desired voltage increase.

FIGS. 7A-7D illustrate four alternative embodiments of the unidirectional power input. The simplest implementation is a diode D1 as shown in FIG. 6A, having a power source, the

diode D1, a capacitor C1, a bi-directional power converter 705, and a load 765. FIG. 6B presents an implementation where losses in the input may be lowered by using an active switch 721 in place of the diode D1. If the switch 721 has the ability to allow current in both directions, then the reverse conduction capability may be used to also recover the energy stored in the capacitor C1 when the converter prepares to shut down. FIG. 6C shows that, more generally, any power converter, for example, a unidirectional power converter 735, may be used. The potential advantage of including a unidirectional power converter 735 is that it can increase the base value of $V_{in}1$ above V_{in}. That voltage increase enables the main power converter to operate with a lower voltage conversion ratio, thus leading to a better overall efficiency. Charge pumps and inductor based converters are examples of possible power input stages. The optimal implementation depends on the application. Similar to FIG. 6B, FIG. 6D presents the use of a bi-directional converter 745 for the input. While the driver of FIG. 6D has bi-directional capability, its reverse power transfer capability may only be used when the main converter is about to shut down to recover the energy available on the capacitor C1. The reverse power capability can also be used in case of an overvoltage situation is detected on the capacitor C1 to prevent circuit failure.

In a typical step-up converter, the output device for example switch Q2 (FIG.1) is preferably a discrete part or on a different die to avoid triggering parasitic transistors in standard CMOS processes. Triggering of these parasitic devices significantly reduces the amount of energy transferred from the input to the output because a significant amount of the energy is connected to the substrate through these parasitic paths. Presently, integrating a single forward diode in the converter is unconventional and a highlighted feature in data sheets.

In the topology of FIG. 1, there may be up to five problematic devices, in particular Q2, which acts as the output diode in any boost converter arrangement, but also Q3-Q6 when the converter transfers energy from the output to the input. To solve this issue, the first embodiment may employ a Silicon on Insulator CMOS technology. That technology removes the parasitic devices, thus enabling the full integration or nearly full integration of the driver.

The use of a full-bridge (Q3, Q4, Q5, Q6) for a low-cost highly integrated IC may be a problem as the four switches are not referenced to GND which increases the area, size and power required to control them. In response, SOI technology capabilities may be leveraged. FIG. 4 shows a low-voltage supply that sits on top of the V_{in} voltage level. By using a charge pump, an output voltage of twice the input voltage may be produced. However, twice the input voltage puts excessive voltage stress on the transistor. To solve the problem, a full-bridge driver is referenced to V_{in} instead of gnd. Consequently, the voltage across the full-bridge driver devices becomes V_{in}, the normal operating voltage.

The circuit 800 of FIG. 8 only solves the problem to drive Q4 and Q6 which are referenced to Vin. For Q3 and Q5 a different circuit may be used. A common implementation 900 is shown in FIG. 9 driving Q3. Here, driving Q3 uses a very large capacitor, for example, 10s nF C1 to store enough energy to be able to supply the driver controlling Q3 while the source voltage of Q3 is high. Once the source voltage of Q3 goes low again, the capacitor C1 can be recharged in preparation for the next cycle. That approach may not work for a highly integrated solution as C1 may not be integrated on chip due to its high capacitance. Also, that approach needs the designer to guarantee a certain refresh rate of C1 to be able to ensure that the driver works properly. That means a high voltage cannot be held for long.

The circuit 900 of FIG. 9 addresses these problems. When node 2 is low (= V_{in}), Q5 gate may be activated by charging C2 through D3. D3 is connected to the gate of Q4. This charging path is not essential, but enables Q5 to turn on faster. Then when node 2 starts to go higher, charges on C2 may be refreshed to counteract the current associated to the parasitic capacitance of Q5 and leakage paths. To do so, the combination of D1, D2 and C3 acts as a charge pump keeping the gate of Q5 approximately Vin V higher than its source. To turn off Q5, switch Q7 is turned on. All the components depicted here may be very small because very little charge needs to be replaced on C2. For example, capacitors are in the pF range and the diodes are very small since very little power is needed. Also, this arrangement makes it possible to process arbitrary waveforms without imposing any refresh rate constraint for the user. This full-bridge driver, makes possible the integration of a full-bridge on die with very little driver area overhead.

Typically, current digital to analog converters (DAC) have an alternate current path connected to the supply voltage , as per the circuit 1010 of FIG. 10A. However, when the DAC value changes, the parasitic capacitance of each bit line takes longer to settle due to the large variation in voltage between node 1 and node 2. To improve that, both current paths are connected through a pair of cascode devices biased at the appropriate voltage Vbias, as shown by the circuit 1020 of FIG 10B. This reduces the time between a change of DAC value and the time the output of the DAC settles to the new value. FIG. 11 shows simulated results. The Vcasc = 0.45 result is when the alternate current path is connected to a voltage source at a voltage level similar to the output.

FIG. 11 represents the effect of decreasing the voltage difference between the DAC output and alternated path. When difference is smaller transient voltage is smaller and settling is faster. Under the present embodiments this enables the circuit to use a smaller blanking time for

current detection. As used herein, "blanking time" refers to the finite amount of time before the reference settles to the desired value when a change in the current value is detected. During the blanking time, the sensor output may be deactivated to avoid false triggering. On a higher level, this enables more accurate current detection and lower output distortion of the final waveform.

In general, current control may be achieved through a series resistor with an inductor, a parallel RC circuit or senseFet in parallel to each switch. In such a driver, high precision current sensing is desirable to operate in a synchronous mode, as switches should be turned off at absolute zero current (as opposed to peak current detection that may be automatically corrected by the controller). Use of a parallel RC circuit is not an option because the circuit operates in DCM. The senseFet approach may work for the low side switch (Q1). However, implementing a highly accurate senseFet for the switch Q2 is difficult due to the large voltage swings of Q2. Also, to avoid having to create a high side ZVS detection circuit for Q2 ZVS, a series resistance provides good current sensing ability even when both switches are off. That enables detecting the ideal point to turn on Q2 without an additional circuit.

The current sense circuit used in the present embodiments preferably detects up to 3 different events per switching cycle to enable high efficiency of the converter. Regrouping all those events in a single sensor provides for higher sensor power for higher performance, since it replaces three sensors.

Due to wide varying conditions in the converter, the relatively fixed latency of the current sensing circuit means that different offset between the desired switching point and real switching point may occur, which is significant because if the synchronous rectifier turns off at -30 mA instead of 0 mA, the efficiency may be much lower. Accordingly, the controller may calculate a

different offset for the current sensing circuit according to the instantaneous conditions, allowing the switch to activate at the correct time.

The combination of the enhanced current DAC previously described with a bi-directional sense scheme allows the reuse of the same DAC and comparator to sense current in both directions. It also enables a one bit increase in the effective DAC resolution at very low area costs. For example, if the DAC is a nine bit DAC, this configuration allows sensing of current from -511 to 511 mA, instead of a range from 0 to 511 in conventional connections. An embodiment of such a circuit is shown in FIG. 12. The sensed target current flows through S1. Depending on S1 configuration, the value of the current is interpreted as a positive or negative value by the circuit. Q1, Q2, and Q3 form the enhanced current DAC described below. The two current sources I1 and I2 are matched (same current) and bias the two inputs of the comparator at the same voltage if the DAC current is 0 and current sensed is also 0. R2 and R3 are matched resistors providing a DC offset to allow bi-directional sensing and also ease the comparator operation. When current flows through R1, the voltage at the inputs of the comparator changes according to I*R1. Changing the DAC value changes the current required in R1 so that the two inputs of the comparator may return to the same voltage level. Then the comparator fires to indicate that the desired current threshold has been reached.

While transistors are used in the current implementation for power switches, MEMS switches could be used in the future to lower the power path resistance and ease the control of high-side switches. An example of MEMS switches is manufactured by General Electric (2015).

Low distortion is an important performance criteria for piezoelectric actuator drivers. While the power stage design and resolution of the feedback path constrain the distortion level, the control algorithm ensures that the complete solution achieves a superior scenario instead of a

higher distortion level. While a fixed PI controller would be adequate because of the wide varying operating conditions, the controller parameters would need to be set to the most conservative setting to ensure stability in all cases. However, this does not adequately reduce distortion. Leveraging the flexibility of a digital controller, the controller designed for drivers under the current embodiment adapts its proportional and integral gain to the instantaneous operating conditions (output/input voltage, frequency), resulting in up to 20 dB improvement of the distortion.

Automatic offset adjustment of the current DAC enables accurate Zero Current Switching at all times. Because the power converter state varies considerably, a fixed latency through the controller does not always produce the same results in terms of switching time accuracy. In one case, trying to turn-off a switch at 0 mA might turn it off at – 2mA while in another set of condition, it can result to a turn-off at – 30 mA. That uncertainty creates problems for the controller both in terms of power loss and also quality of the output (distortion). To solve the problem, the controller automatically corrects the target current to an "artificial current target." When the current sensor triggers at that artificial value, the controller turns on/off the intended switch. Because the correction function (f(converter state)) knows the system, the switch that triggered at the "artificial current target" beneficially turns on/off at the intended target current value. Importantly, this enables the ability to turn on the High Side switch (Q2) at the right time to achieve zero voltage switching, leading to lower power, but perhaps more importantly, lower distortion.

A controller 1300 for controlling the driver, for example, a digital controller, may be a computer, an example of which is shown in the schematic diagram of FIG. 13. The controller 1300 contains a processor 1302, a storage device 1304, a memory 1306 having software 1308

stored therein that defines the abovementioned functionality, input and output (I/O) devices 1310 (or peripherals), and a local bus, or local interface 1312 allowing for communication within the controller. The local interface 1312 can be, for example but not limited to, one or more buses or other wired or wireless connections, as is known in the art. The local interface 1312 may have additional elements, which are omitted for simplicity, such as controllers, buffers (caches), drivers, repeaters, and receivers, to enable communications. Further, the local interface 1312 may include address, control, and/or data connections to enable appropriate communications among the aforementioned components.

The processor 1302 is a hardware device for executing software, particularly that stored in the memory 1306. The processor 1302 can be any custom made or commercially available single core or multi-core processor, a central processing unit (CPU), an auxiliary processor among several processors associated with the present controller 1300, a semiconductor based microprocessor (in the form of a microchip or chip set), a macroprocessor, or generally any device for executing software instructions.

The memory 1306 can include any one or combination of volatile memory elements (*e.g.*, random access memory (RAM, such as DRAM, SRAM, SDRAM, *etc.*)) and nonvolatile memory elements (*e.g.*, ROM, hard drive, tape, CDROM, *etc.*). Moreover, the memory 1306 may incorporate electronic, magnetic, optical, and/or other types of storage media. Note that the memory 1306 can have a distributed architecture, where various components are situated remotely from one another, but can be accessed by the processor 1302.

The software 1308 defines functionality performed by the controller 1300, in accordance with the present invention. The software 1308 in the memory 1306 may include one or more separate programs, each of which contains an ordered listing of executable instructions for

implementing logical functions of the controller 1300, as described below. The memory 1306 may contain an operating system (O/S) 1320. The operating system essentially controls the execution of programs within the controller 1300 and provides scheduling, input-output control, file and data management, memory management, and communication control and related services.

The I/O devices 1310 may include input devices, for example but not limited to, a keyboard, mouse, scanner, microphone, *etc.* Furthermore, the I/O devices 1310 may also include output devices, for example but not limited to, a printer, display, *etc.* Finally, the I/O devices 1310 may further include devices that communicate via both inputs and outputs, for instance but not limited to, a modulator/demodulator (modem; for accessing another device, system, or network), a radio frequency (RF) or other transceiver, a telephonic interface, a bridge, a router, or other device.

When the controller is in operation, the processor 1302 is configured to execute the software 1308 stored within the memory 1306, to communicate data to and from the memory 1306, and to generally control operations of the controller pursuant to the software 1308, as explained above.

When the functionality of the controller is in operation, the processor 1302 is configured to execute the software 1308 stored within the memory 1306, to communicate data to and from the memory 1306, and to generally control operations of the controller pursuant to the software 1308. The operating system 1320 is read by the processor 1302, perhaps buffered within the processor 1302, and then executed.

When the controller is implemented in software 1308, it should be noted that instructions for implementing the controller can be stored on any computer-readable medium for use by or in

connection with any computer-related device, system, or method. Such a computer-readable medium may, in some embodiments, correspond to either or both the memory 1306 or the storage device 1304. In the context of this document, a computer-readable medium is an electronic, magnetic, optical, or other physical device or means that can contain or store a computer program for use by or in connection with a computer-related device, system, or method. Instructions for implementing the system can be embodied in any computer-readable medium for use by or in connection with the processor or other such instruction execution system, apparatus, or device. Although the processor 1302 has been mentioned by way of example, such instruction execution system, apparatus, or device may, in some embodiments, be any computer-based system, processor-containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions. In the context of this document, a "computer-readable medium" can be any means that can store, communicate, propagate, or transport the program for use by or in connection with the processor or other such instruction execution system, apparatus, or device.

Such a computer-readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a nonexhaustive list) of the computer-readable medium would include the following: an electrical connection (electronic) having one or more wires, a portable computer diskette (magnetic), a random access memory (RAM) (electronic), a read-only memory (ROM) (electronic), an erasable programmable read-only memory (EPROM, EEPROM, or Flash memory) (electronic), an optical fiber (optical), and a portable compact disc read-only memory (CDROM) (optical). Note that the computer-readable medium could even be paper or another suitable medium upon which the program is printed, as the program can be

electronically captured, via for instance optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in a computer memory.

In an alternative embodiment, where the controller is implemented in hardware, the controller can be implemented with any or a combination of the following technologies, which are each well known in the art: a discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit (ASIC) having appropriate combinational logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), etc.

As used within this disclosure, a proportional–integral–derivative controller (PID controller) describes a control loop feedback mechanism (controller). A PID controller continuously calculates an error as the difference between a desired setpoint and a measured process variable. The controller attempts to minimize the error over time by adjustment of a control variable, such as the position of an actuator, to a new value determined by a weighted sum. The proportional response may be adjusted by multiplying the error by a constant proportional gain (Kp).

FIGS. 14A and 14B are two block diagrams of exemplary embodiments 1410, 1420 of control drivers, providing compact, low-power, low-noise piezoelectric cooling. In these embodiment the controllers 1410, 1420 use information available through different state variables inside the digital controller on the current state of the driver to adapt the proportional gain Kp and an integral gain (Ki) of the controller. As a result, the waveform distortion is reduced. FIG. 14A is more specific. FIG. 14B is more general to illustrate how the scaling of Kp and Ki according to a function of the driver state variables enhances the system performance.

FIGS. 14A and 14B, indicate the converter switching frequency (fsw), the voltage reference to track (Vref), the proportional gain (Kp), the integral gain (Ki), the converter transfer function (H(z)), an external disturbance (D), feedback gain (Gain), and output voltage of the converter (Vout). In the simplest embodiment, Kp may be scaled linearly with the output voltage ($Kp' \propto Vout \times Kp$) and Ki may be scaled linearly with the switching frequency (fsw) ($Ki' \propto fsw \times Ki$). D represents any disturbance that could exist in a practical implementation. H(z) represents the transfer function of the system in a discrete-time representation. z^{-1} is an operator associated with the z-transform commonly used in controllers using discrete-time representation. In the exemplary embodiment, fsw is in the range between 150 kHz and 1 MHz.

FIGS. 15 and 16 illustrate results using the prototype of FIG. 11. FIG 15 presents a 150 Hz, 101.8 Vpp sinusoid in a 150 nF capacitive load generated with the prototype from a 3.6 V supply. Even without a magnetic output filter, the prototype achieves a THD+N of 0.38% in a 1 MHz bandwidth. The spectrum shows the switching noise of the converter in the hundreds of kHz range does not significantly degrade the waveform. At that operating point, the prototype consumes 64.04 mW, 40.00 mW from the power path and 24.04 mW from the controller excluding the FPGA. This result is 7.81 to 13.85 times lower than prior single-inductor solutions providing high-voltage low-distortion outputs. The pseudo-resonant synchronous buck mode achieves up to 8.9% reduction in power compared to regular buck mode as seen in FIG. 16.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. For example, the exemplary drivers may be used other types of piezoelectric actuators than a DCJ, for example, a haptic feedback actuator, or a micro robotics actuator. More generally, the exemplary drivers may be advantageous when used with any capacitive load that

requires a high voltage/low distortion waveform, such as an electrostatic actuator like a micro-mirror, an electro-mechanical polymer, an electro-active polymer, or another type of MEMS device.

In addition to the benefits of the embodiments described above, another important benefit is to make the circuit compatible with a wide range of energy sources. For example, if connecting a bi-directional power converter to a certain type of battery as input energy source, with previous converters the battery might not be able to sink current (e.g. non-rechargeable batteries) or need to sink current in a very controlled way to avoid potential failures (e.g. Li-Ion). The unidirectional power addresses this problem, for example, during system integration.

In summary, embodiments of the driver under the present invention may include one or more of the following features:

1. A capacitive load drive circuit having a two-switch bi-directional power converter generating a low distortion analog waveform (without an output low-pass filter). Any circuit configuration of FIGS. 2A, 2B, 2C, and 2D is a viable circuit that may be interchanged depending on the specific capacitive load. circuit configuration of FIGS. 2A, 2B, 2C, and 2D may be operated in synchronous or normal switching mode. Forward and reverse operation may use different modes. For instance, forward operation may use normal switching and reverse operation may use synchronous switching.

2. The output stage configurations from any of FIGS. 3A, 3B, 3C, 3D, and 3E may be appended to any circuit configuration of FIGS. 2A, 2B, 2C, and 2D to enable higher output peak-to-peak voltage. Also note that FIG. 3A can be modified by referencing to GND instead of V_{in}.

3. For the output stage 303 shown in FIG. 3C and the output stage 305 shown in FIG 3E, the triangle symbol represents an amplifier to which one may feed a variable input V_{ref} and control that side of the load 365.

4. Other output stage combinations (not shown) are also possible. For example, mixing FIG. 3B and 3C or mixing FIG. 3D and 3E provides for a very clean transition between the different voltage references (low distortion) while only having to pay the power cost of the amplifier during the transitions.

5. A method to reduce the converter switching losses and waveform distortion may be combined with any of the circuits above, providing for the generation of a variable pre-drive pulse to achieve zero voltage and zero-current switching of the high side switch under all operating conditions (pseudo-resonant operation).

6. A method to provide a unidirectional power input to increase power efficiency may be combined with one or more of the circuits described above, as described above.

7. The variable pre-drive pulse of 5 (above) may be computed by a digital controller.

8. The method of 5 may be implemented where the ZVS/ZCS point is detected through a current sensor.

9. The current sensor of 7 may be implemented wherein the current sensor is implemented as in FIG. 12.

10. The DAC enhancement of FIG. 10B may be implemented where the ZVS/ZCS point is detected through a current sensor.

11. The high side floating driver from FIG. 9 may be incorporated in the driver. Note that the minimum realization of that driver uses only D1, D2, C3 and Q7. The extra capacitor C2

provides increased noise tolerance. The diode D3 provides a faster charging path to increase the turn-on speed of Q5.

12. The control algorithm of FIG. 14B may be incorporated to further lower the output distortion

13. The real-time current adjustment of FIG. 17 may be incorporated.

14. The realization of the circuit may be monolithic for all switches (although some passive elements like the inductor may be discrete parts) and systems in packages (SiP) where for instance the controller and power circuit are on two different die, but the two dies may be included together in a single package. The circuit may also be implemented as a fully discrete realization or any compromise between full integration and full discrete implementation.

15. Part of or all power transistors may be implemented as a MEMS switch in some implementations.

These circuits may preferably drive a capacitive load, for example, (but not limited to) piezoelectric actuators, electroactive polymer actuators, or electrostatic actuators. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

CLAIMS

What is claimed is:

1. A driver for a circuit with a capacitive load, comprising:

a power converter to receive an input voltage v_{in} as input and generate a clean folded waveform as an output;

an unfolding stage referenced to v_{in}, to receive the clean folded waveform from the power converter and unfold the folded waveform into a full waveform; and

a controller to control the driver,

wherein the converter operates bi-directionally.

2. The driver of claim 1, wherein the capacitive load comprises a piezoelectric actuator.

3. The driver of claim 1, wherein the piezoelectric actuator comprises a dual piezoelectric cooling jet (DCJ).

4. The driver of claim 1, wherein the power converter further comprises a forward boost/reverse buck converter.

5. The driver of claim 4, wherein the power converter further comprises a 2-switch power stage.

6. The driver of claim 5, wherein the power converter operates in a borderline conduction mode (BCM).

7. The driver of claim 4, wherein the converter operates as a pseudo resonant synchronous buck converter.

8. The driver of claim 1, wherein the controller further comprises an adaptive PI controller configured to dynamically adjust a proportional gain and an integral gain according to a power converter state.

9. The driver of claim 1, further comprising a two-switch bi-directional power converter to generate an analog output control waveform directly without an output low-pass filter.

10. The load drive circuit of claim 9 wherein the power converter further comprises a full-bridge configuration.

11. The load drive circuit of claim 10 wherein the full-bridge is referenced to ground.

12. The load drive circuit of claim 10 wherein the full-bridge is referenced to the input voltage.

13. The load drive circuit of claim 9 wherein the power converter further comprises a variable reference for the capacitive load.

14. The load drive circuit of claim 10 wherein the full-bridge comprises a variable reference full-bridge.

15. The circuit of claim 9 further comprising a plurality of power switches integrated in a single package with the controller.

16. The circuit of claim 9 further comprising a plurality of power switches integrated on a single die with the controller.

17. The circuit of claim 9 wherein the capacitive load comprises a piezoelectric actuator.

18. The circuit of claim 9 wherein the capacitive load comprises an electrostatic actuator.

19. The circuit of claim 15, wherein the plurality of power switches comprises at least one high side switch and at least one low side switch, and the at least one high-side switch is controlled with a charge pump comprising three switches and a capacitor to directly control the gate of the high side switch.

20. The circuit of claim 19 further comprising a capacitor disposed between a gate and a source of the at least one high side switch.

21. The circuit of claim 1, wherein the input further comprises a digital to analog converter (DAC) comprising:

a first output line connected to a first cascaded device comprising a first gate; and

a complementary second output line connected to a second cascoded device comprising a second gate,

wherein the first gate and the second gate are configured to have the same voltage.

22. A method for reducing switching losses and waveform distortion in a driver for a circuit with a capacitive load, comprising a power converter to receive an input voltage v_{in} as input and generate a clean folded waveform as an output, an unfolding stage referenced to v_{in}, to receive the clean folded waveform from the converter and unfold the folded waveform into a full waveform, and a controller to control the driver, wherein the converter operates bi-directionally, the method comprising the step of:

generating a variable pre-drive pulse to achieve zero voltage and zero-current switching of a high side switch of the unfolding stage under all operating conditions.

23. The method of claim 22, further comprising the step of computing the variable pre-drive pulse with a digital controller.

24. The method of claim 23, further comprising the step of detecting a zero voltage switching condition point and or a zero voltage switching condition point through a current sensor.

25. The method of claim 24, wherein the current sensor is a sense resistor in series with the power converter inductor.

26. A method to reduce the blanking time after a switching event for a converter comprising a digital to analog converter (DAC) comprising the steps of:

connecting a first DAC output line to a first cascaded device comprising a first gate; and

connecting a complementary DAC second output line to a second cascaded device comprising a second gate; and

configuring the first gate and the second gate to have the same voltage.

27. A method for reducing waveform distortion for a controller circuit with a capacitive load, comprising the steps of;

receiving an input parameter of the controller circuit;

identifying a reference voltage (Vref) of the controller circuit; and

adapting a proportional gain (Kp) and an integral gain (Ki) of the controller circuit according to a converter transfer function (H(z)).

28. The method of claim 27 wherein the controller is based on a proportional-integral (PI) controller wherein the proportional and integral parameters are adjusted dynamically.

29. The method of claim 27 wherein the controller is based on a proportional–integral–derivative (PID) controller wherein the proportional, integral and differential gain are adjusted dynamically.

30. The method of claim 27 wherein the input parameters comprise a desired output voltage and the current switching frequency of the controller circuit.

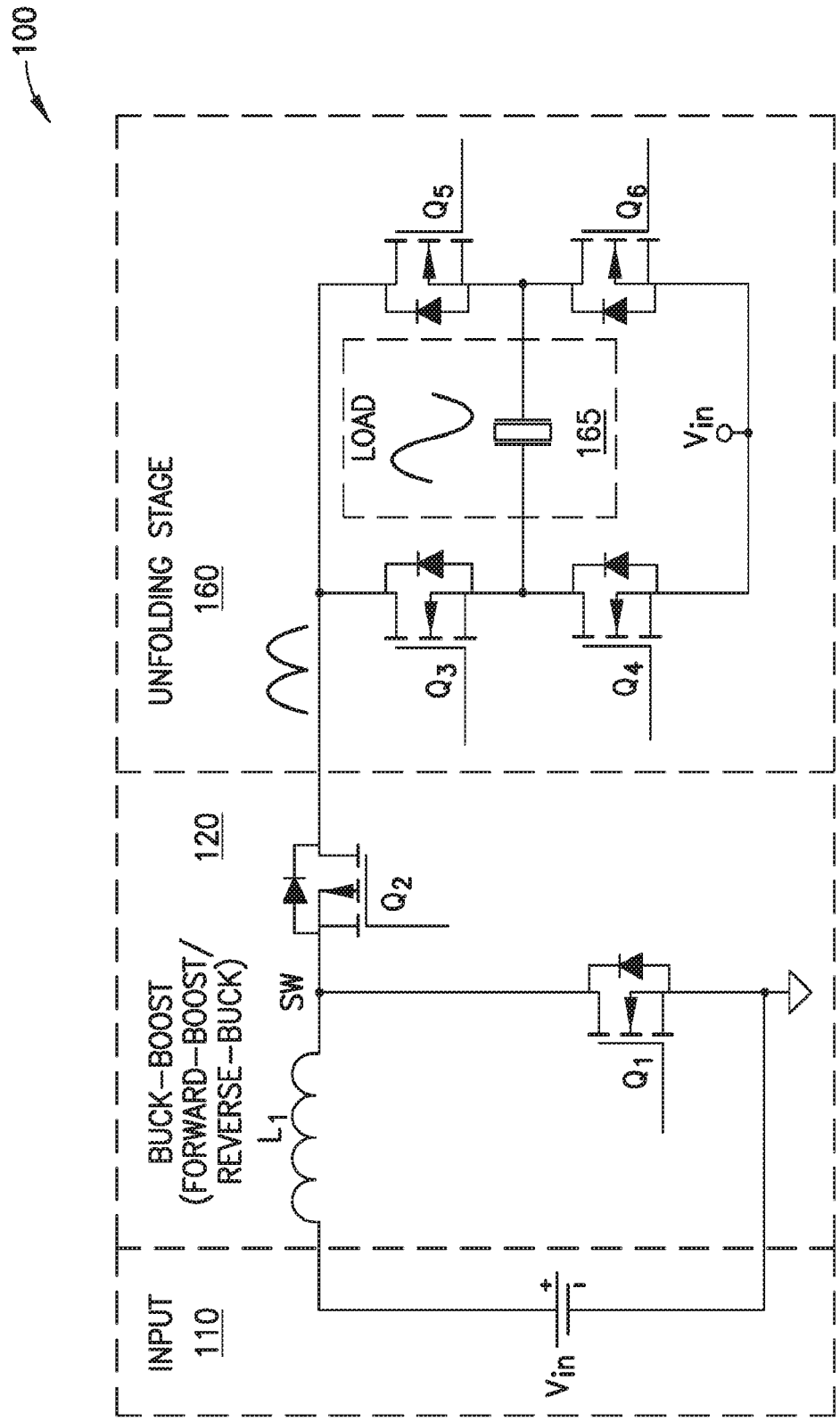

100
INPUT
110
BUCK–BOOST
(FORWARD–BOOST/
REVERSE–BUCK)
120
UNFOLDING STAGE
160
LOAD
165
V_{in}
L_1
SW
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6

FIG. 1

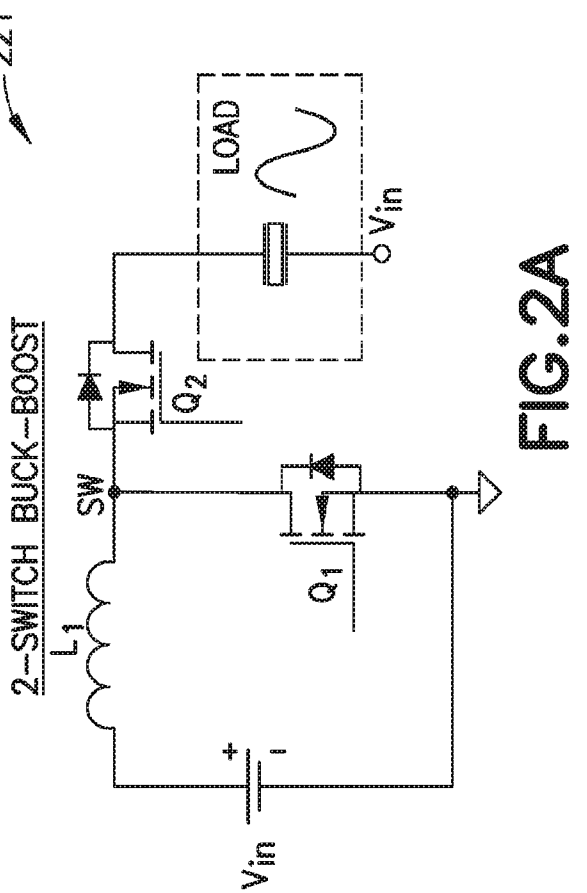


FIG.2A

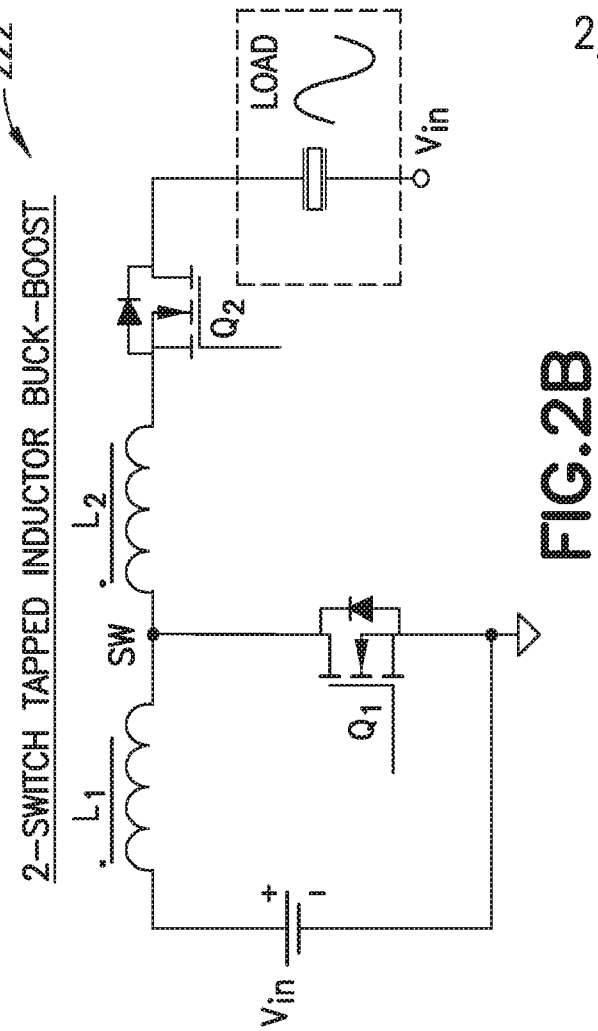


FIG.2B

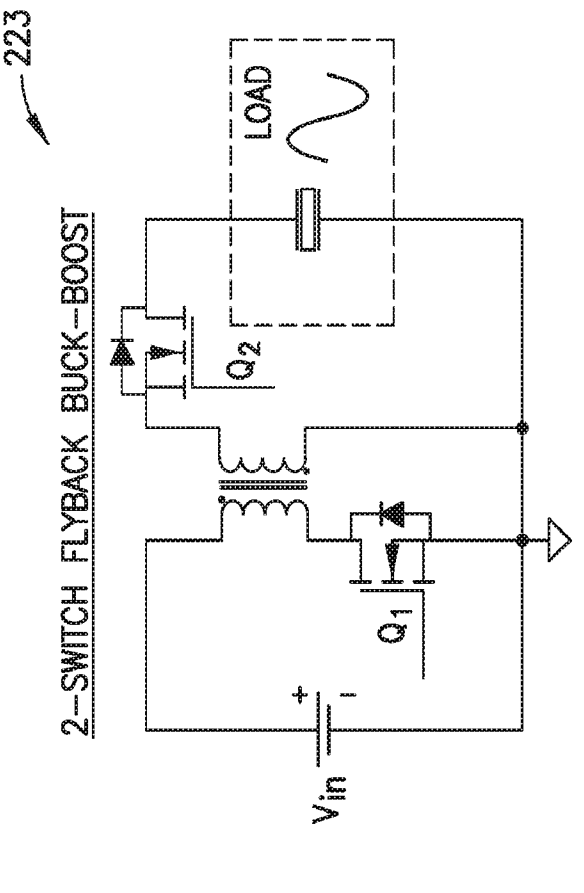


FIG.2C

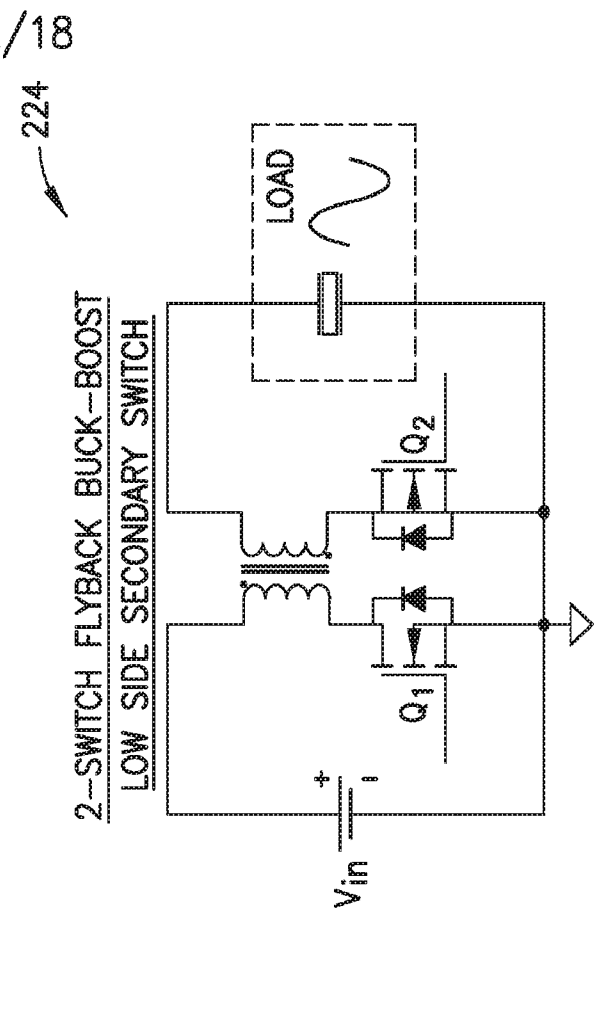


FIG.2D

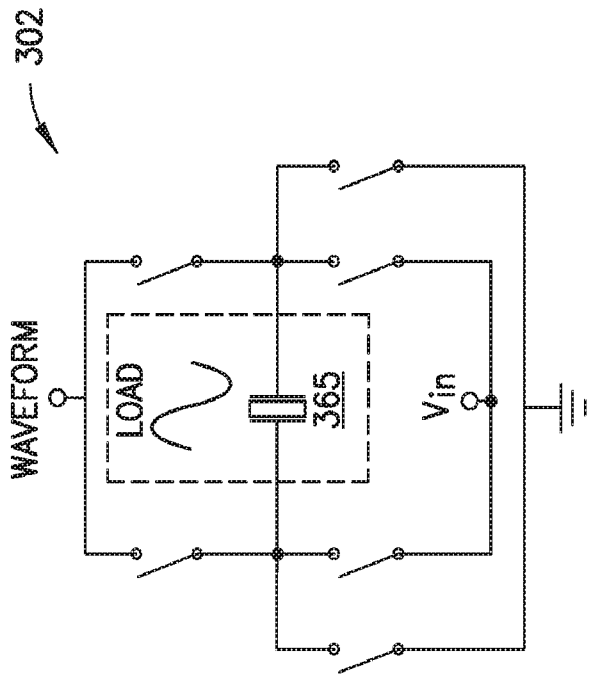


FIG.3B

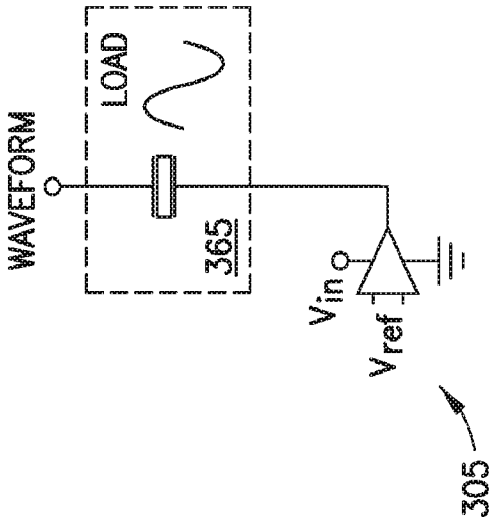


FIG.3E

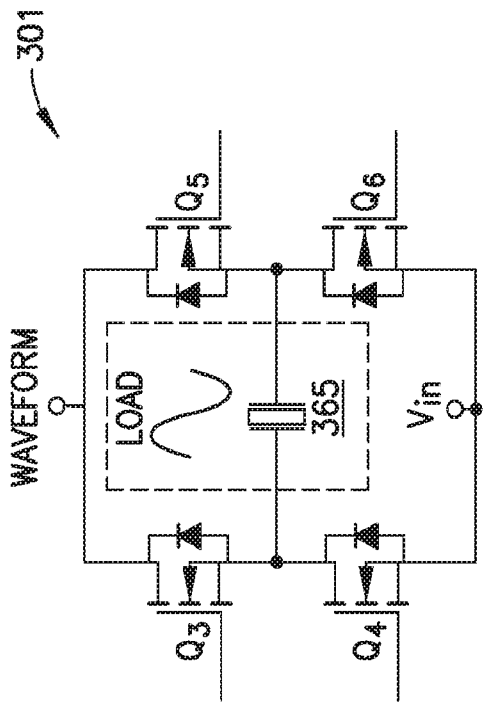


FIG.3A

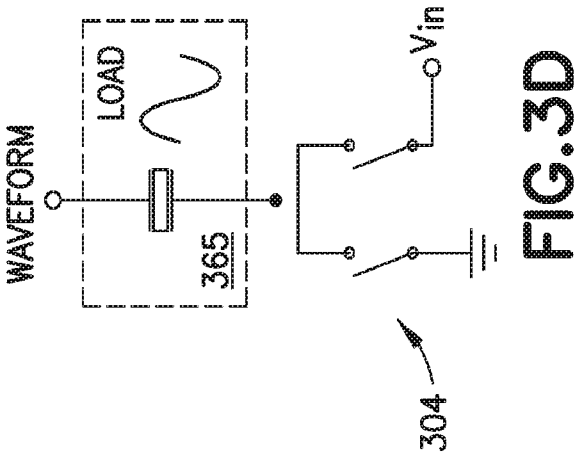


FIG.3D

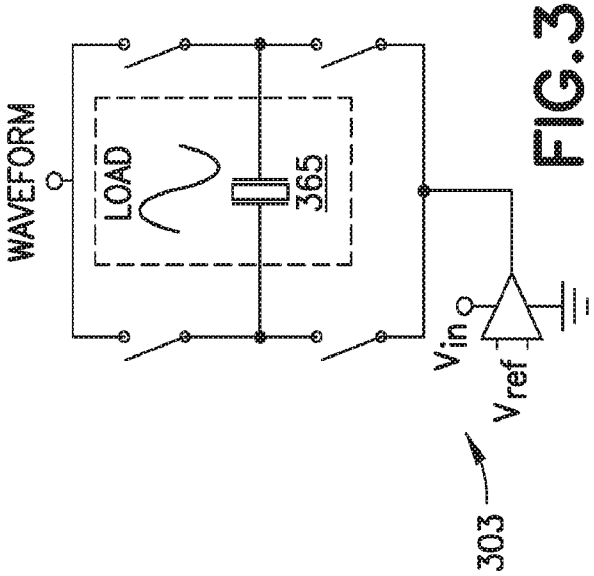


FIG.3C

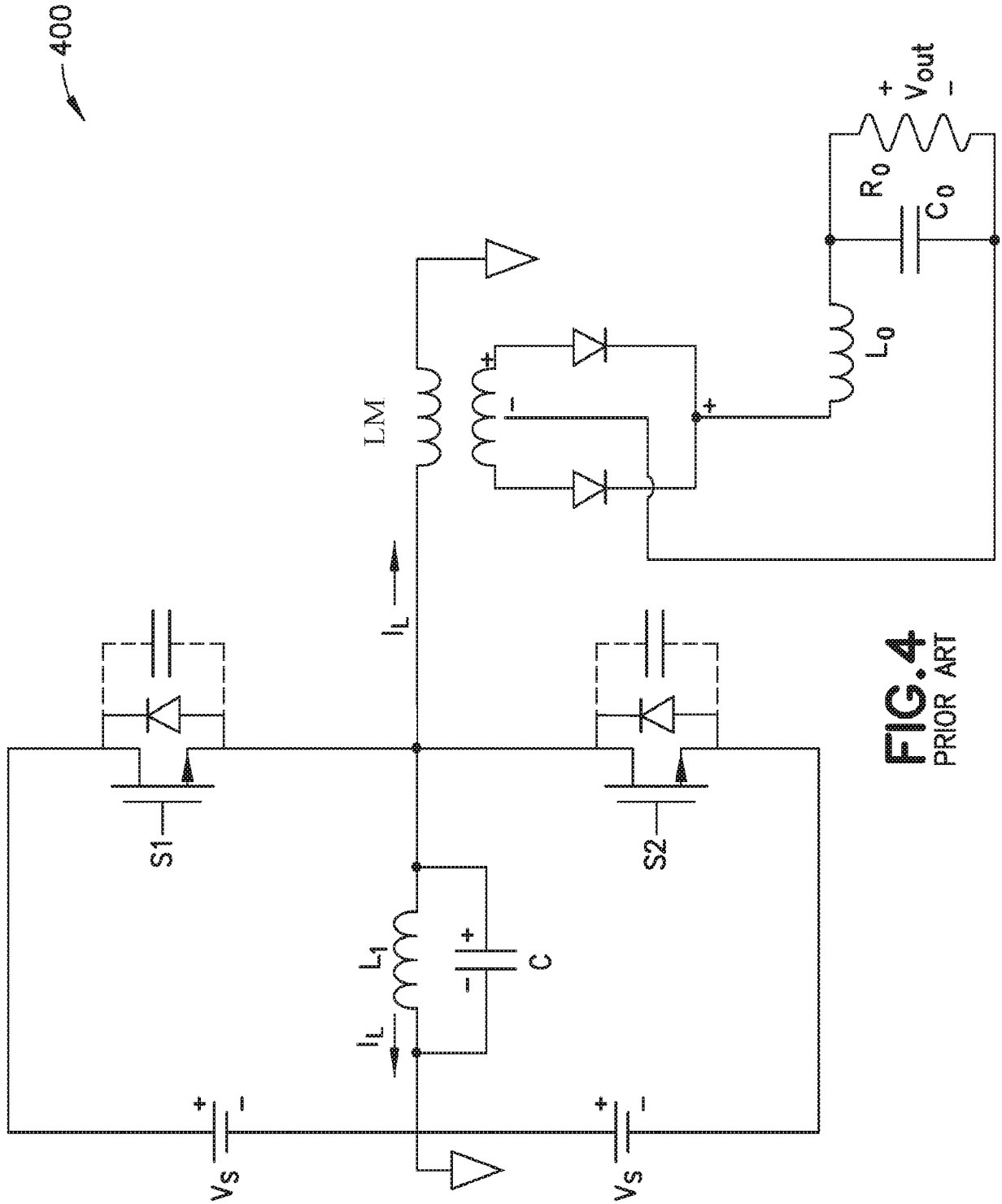


FIG.4
PRIOR ART

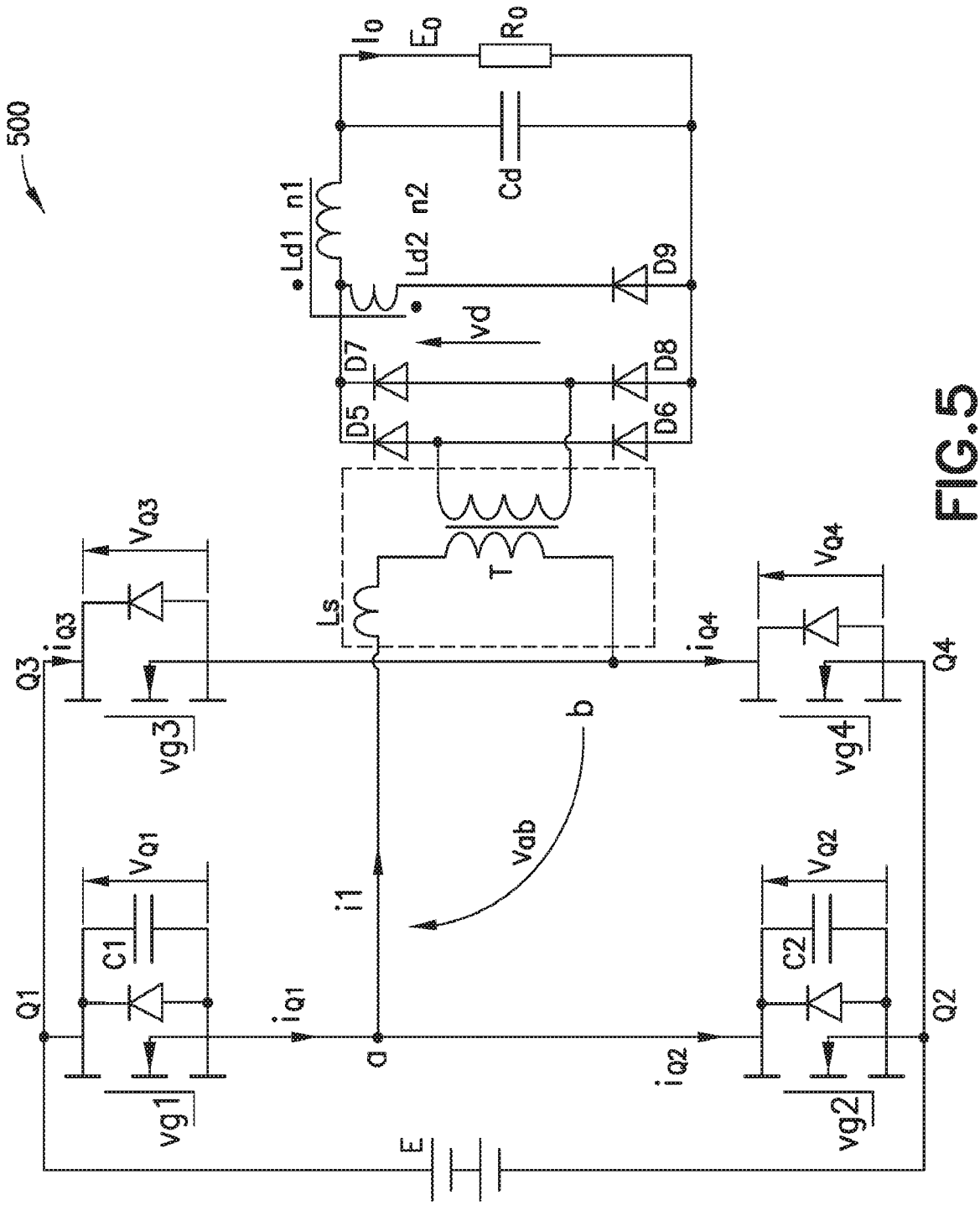


FIG.5
PRIOR ART

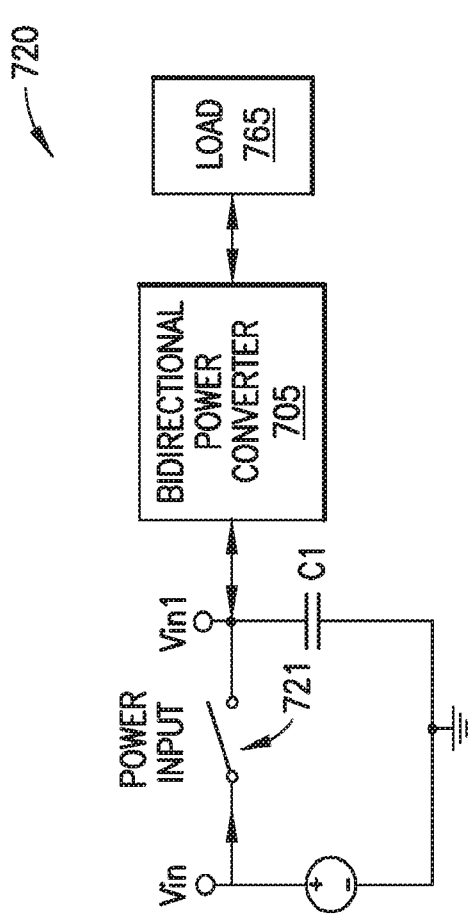


FIG.6B

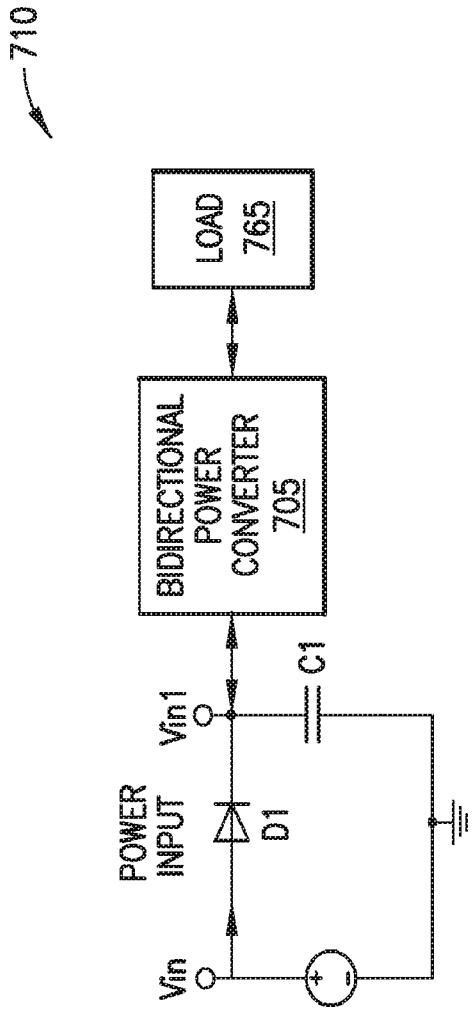


FIG.6A

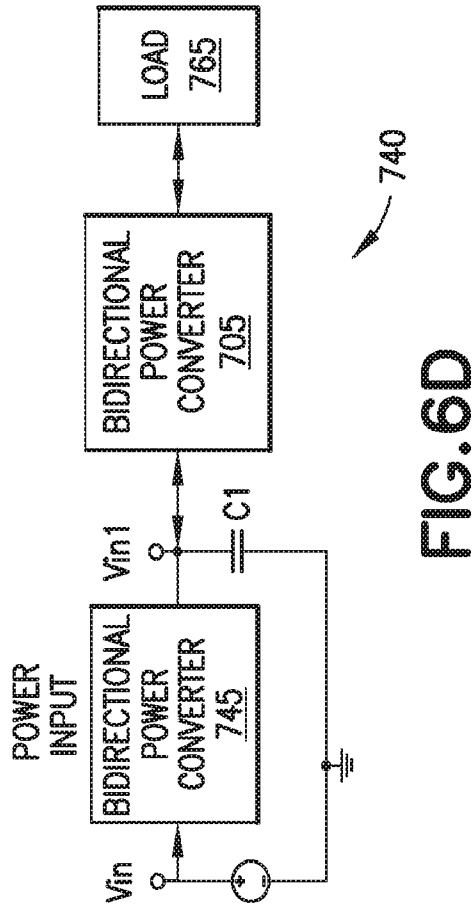


FIG.6D

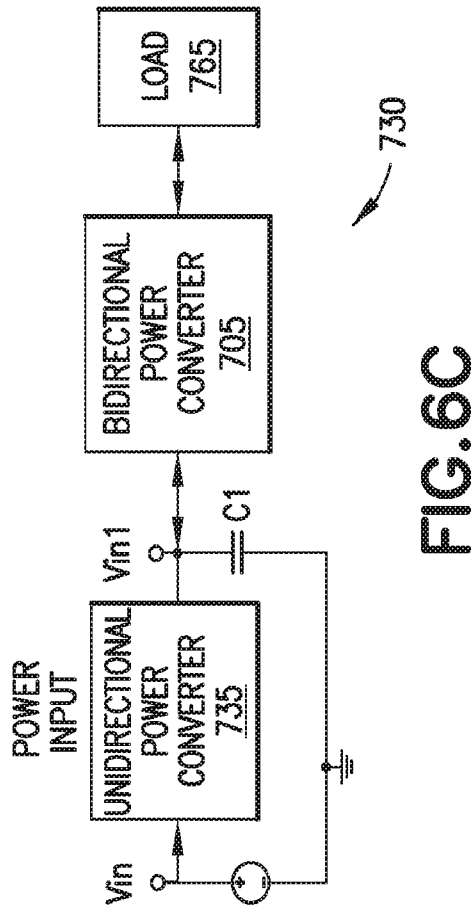


FIG.6C

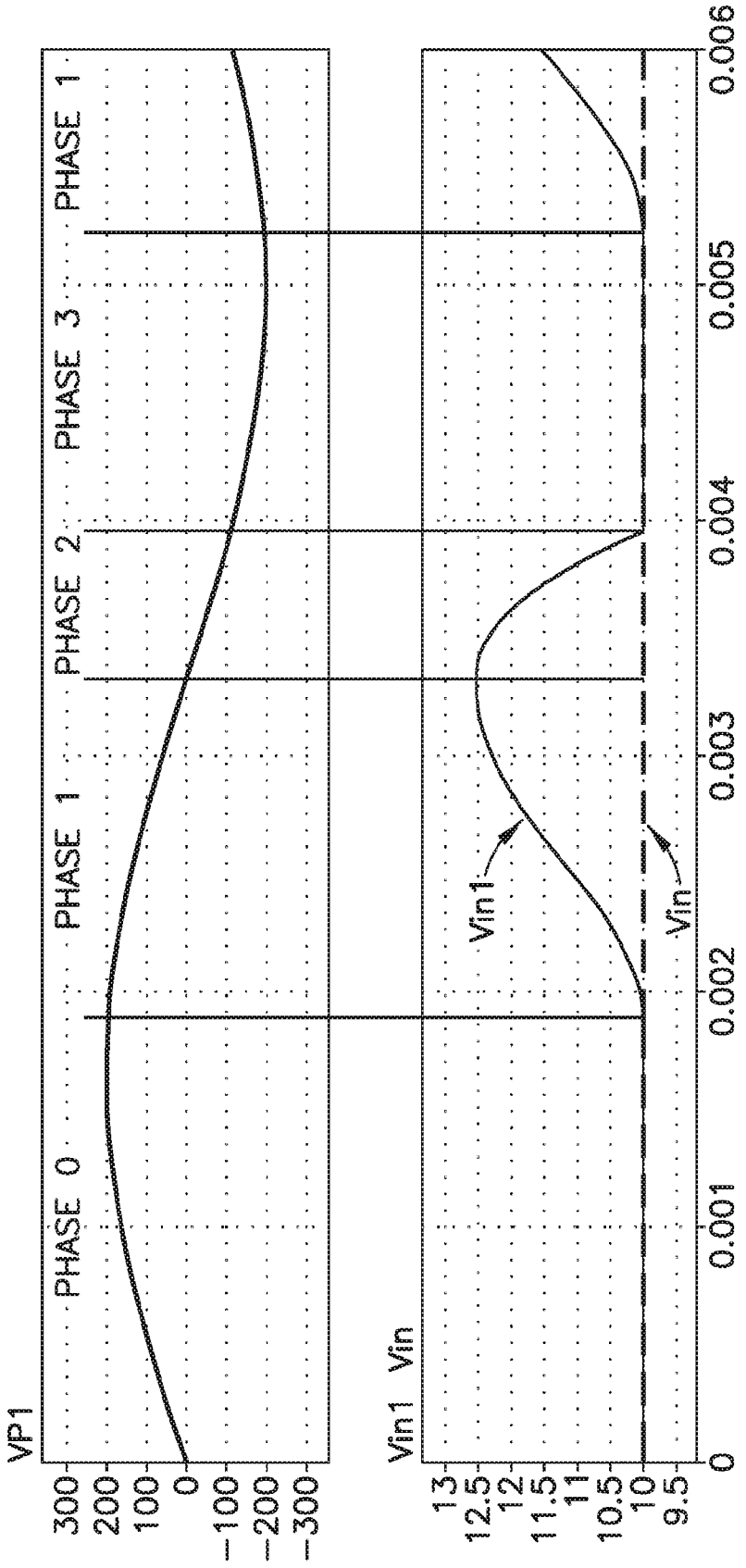

VP1
300
200
100
0
−100
−200
−300
PHASE 0
PHASE 1
PHASE 2
PHASE 3
PHASE 1
Vin1 Vin
13
12.5
12
11.5
11
10.5
10
9.5
Vin1
Vin
0
0.001
0.002
0.003
0.004
0.005
0.006
TIME (s)

FIG.7

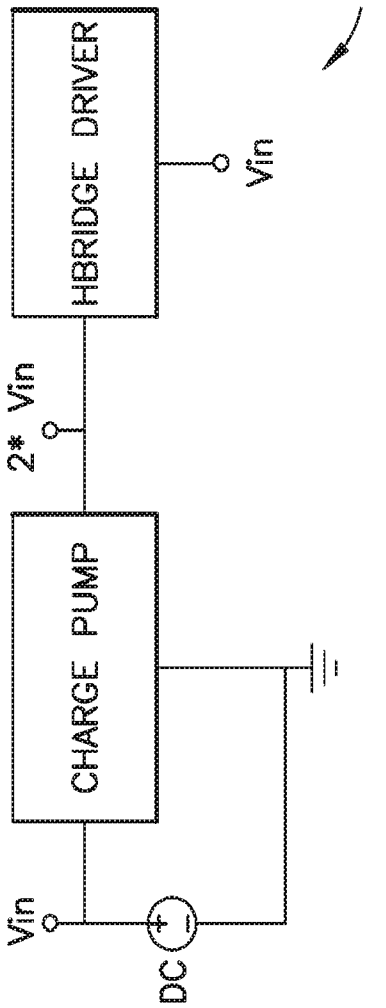


FIG.8

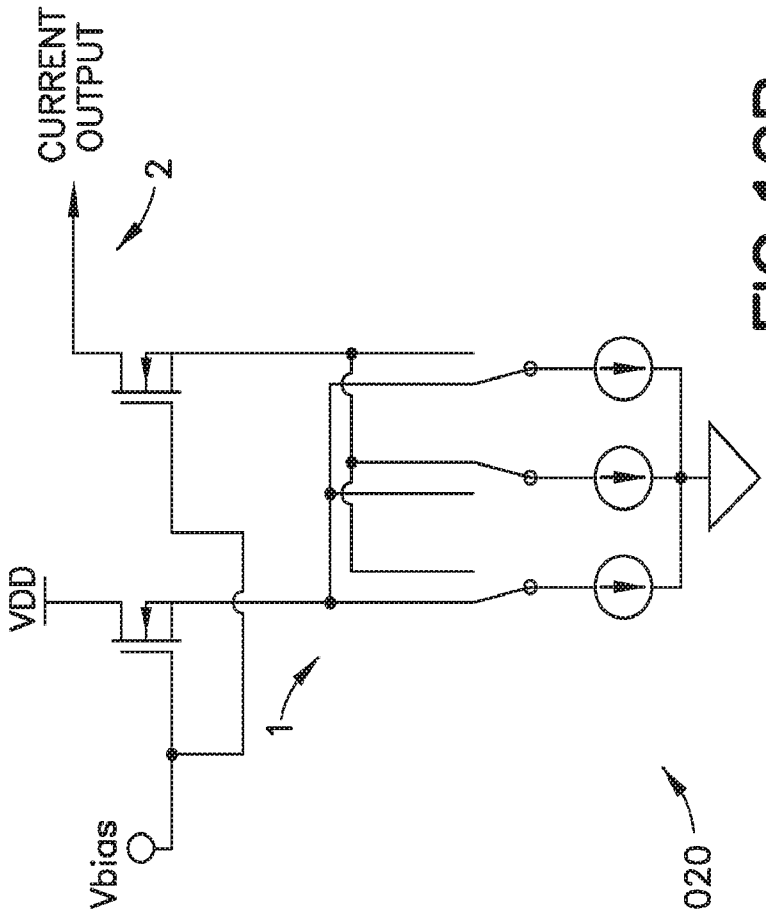


FIG.10B

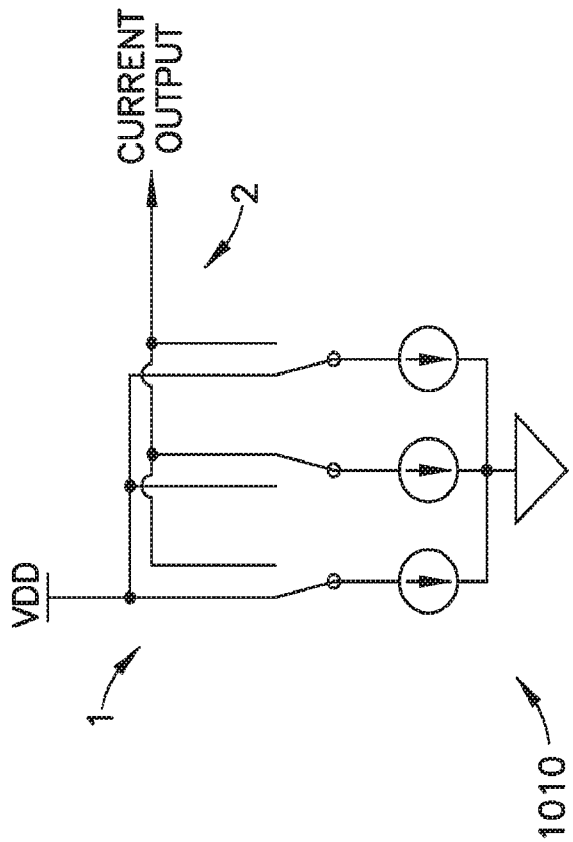


FIG.10A

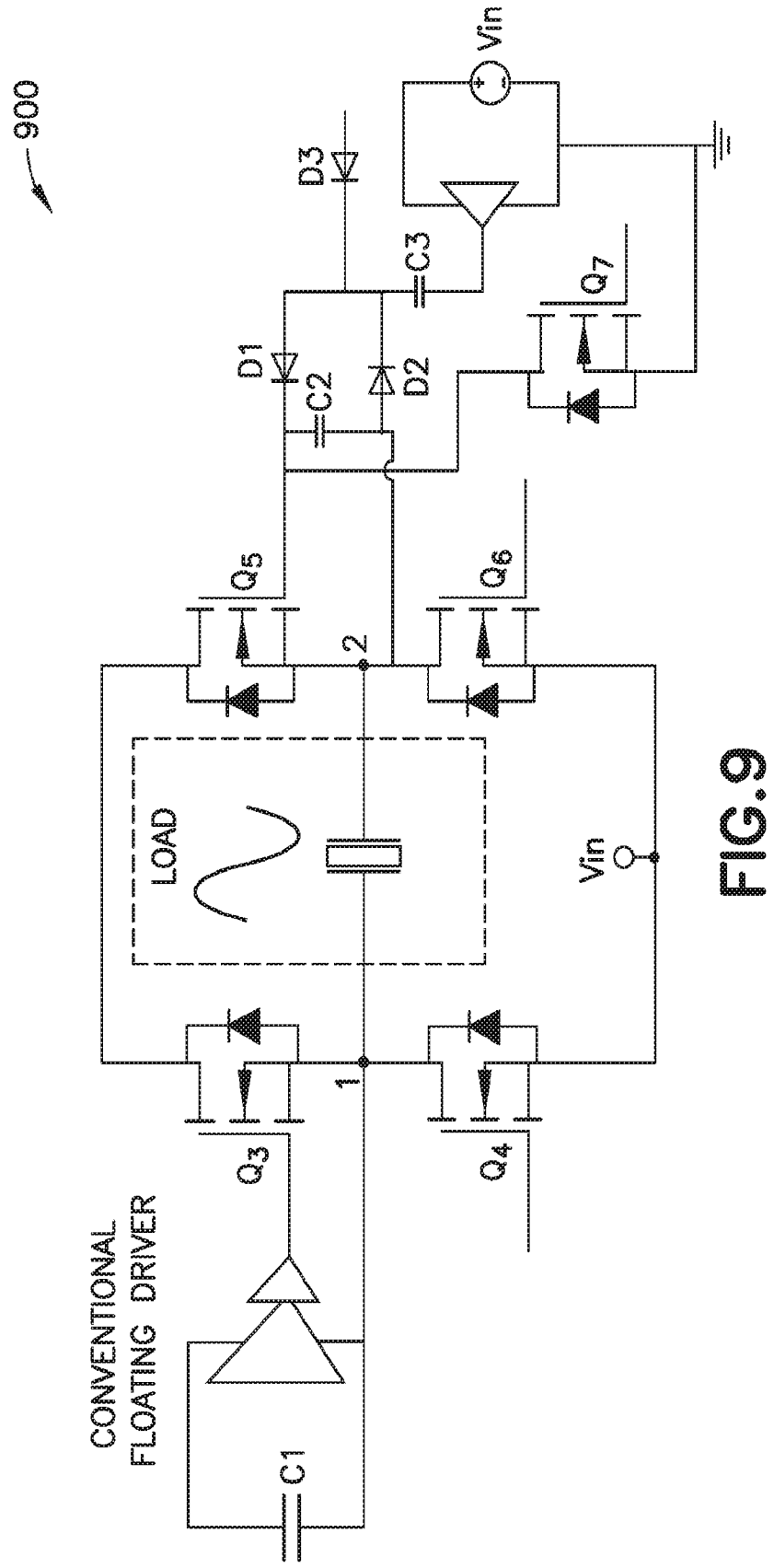

900
Vin
D3
C3
Q7
D1
C2
D2
Q5
Q6
2
LOAD
Vin
1
Q3
Q4
CONVENTIONAL
FLOATING DRIVER
C1

FIG.9

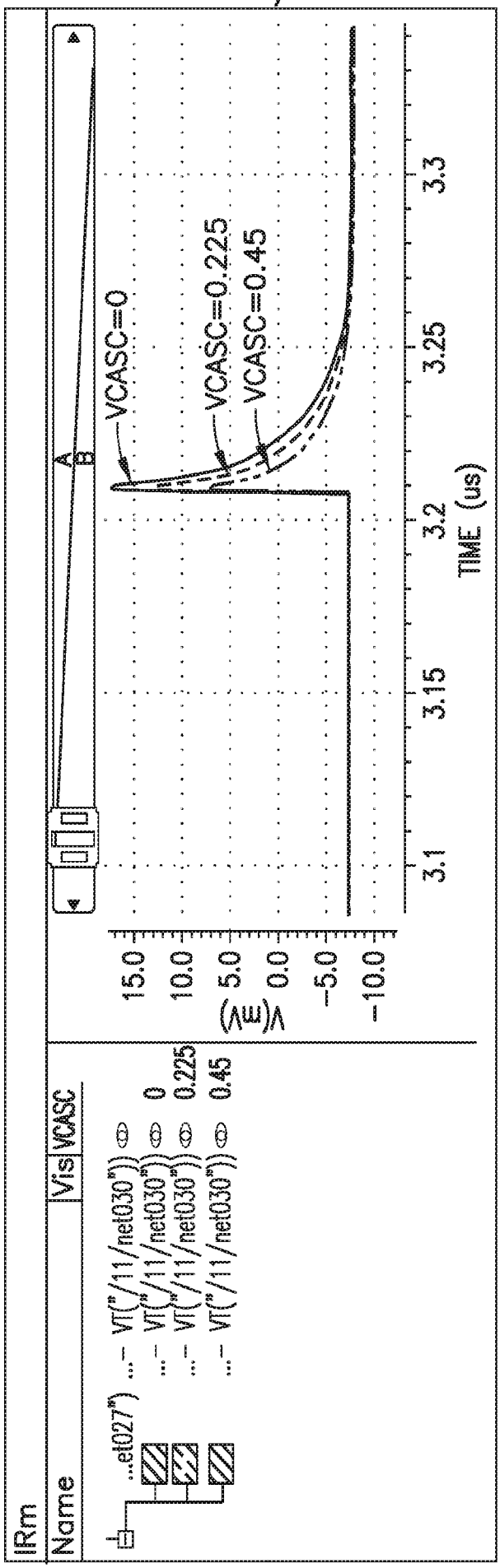

IRm
Name
Vis
VCASC
...et027")
... – VT("/11/net030") 0
... – VT("/11/net030") 0.225
... – VT("/11/net030") 0.45
A
B
VCASC=0
VCASC=0.225
VCASC=0.45
15.0
10.0
5.0
0.0
−5.0
−10.0
V(Ξ)
3.1
3.15
3.2
3.25
3.3
TIME (us)

FIG.11

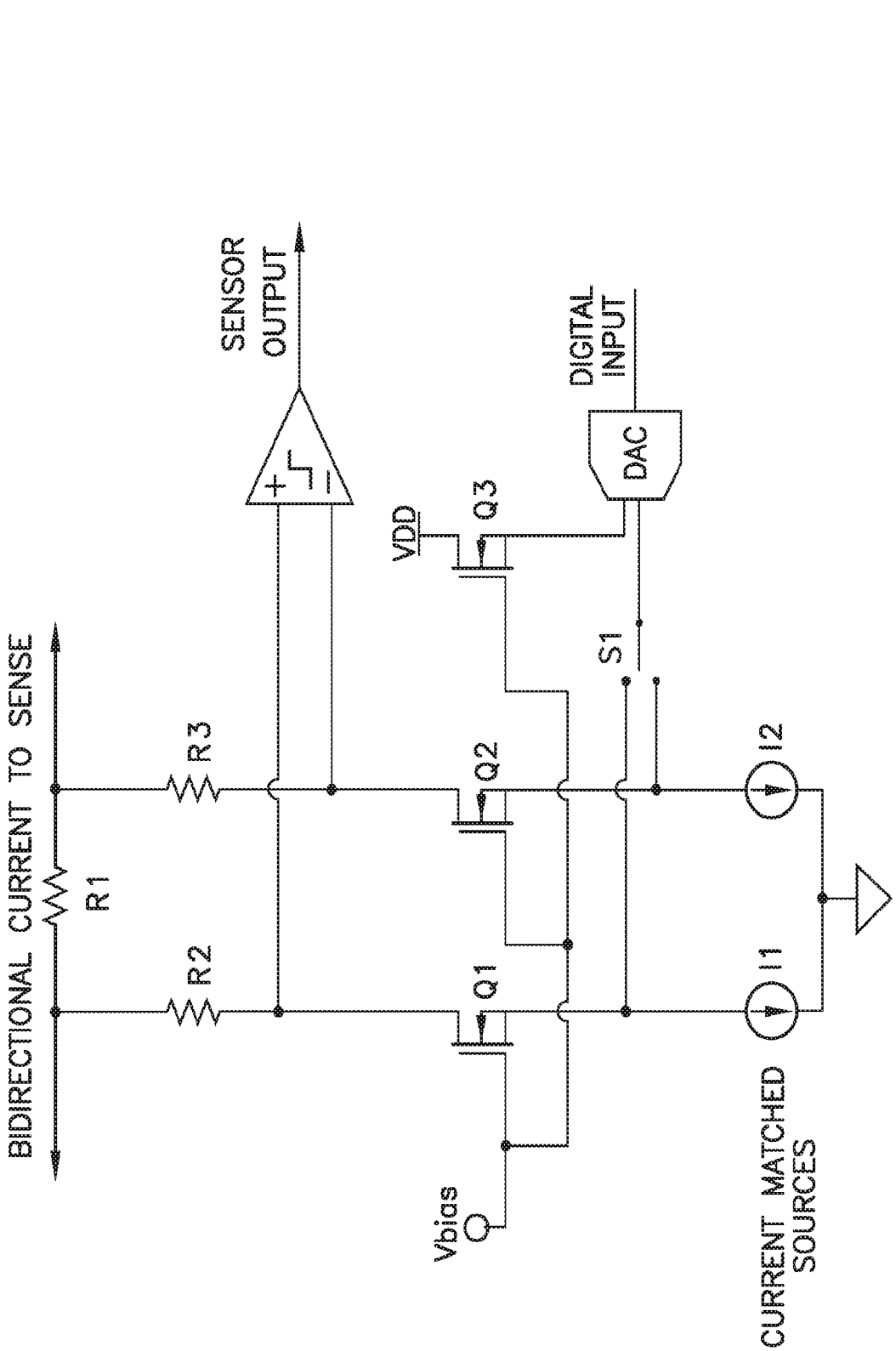

1200
SENSOR OUTPUT
DIGITAL INPUT
DAC
VDD
Q3
S1
BIDIRECTIONAL CURRENT TO SENSE
R3
R1
R2
Q2
Q1
I2
I1
Vbias
CURRENT MATCHED SOURCES

FIG.12

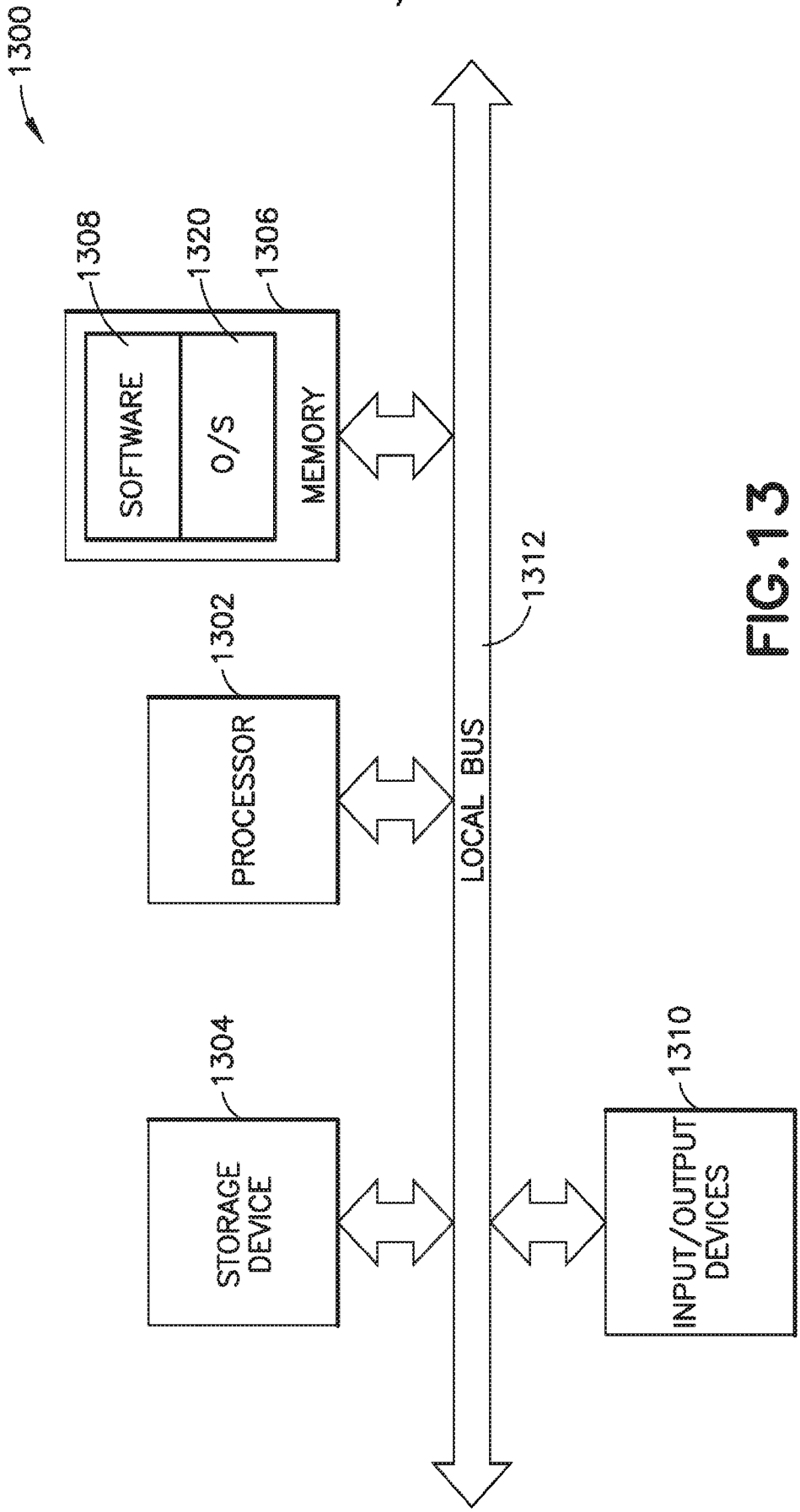

1300
1308
1320
1306
SOFTWARE
O/S
MEMORY
1312
1302
PROCESSOR
LOCAL BUS
1304
STORAGE DEVICE
1310
INPUT/OUTPUT DEVICES

FIG. 13

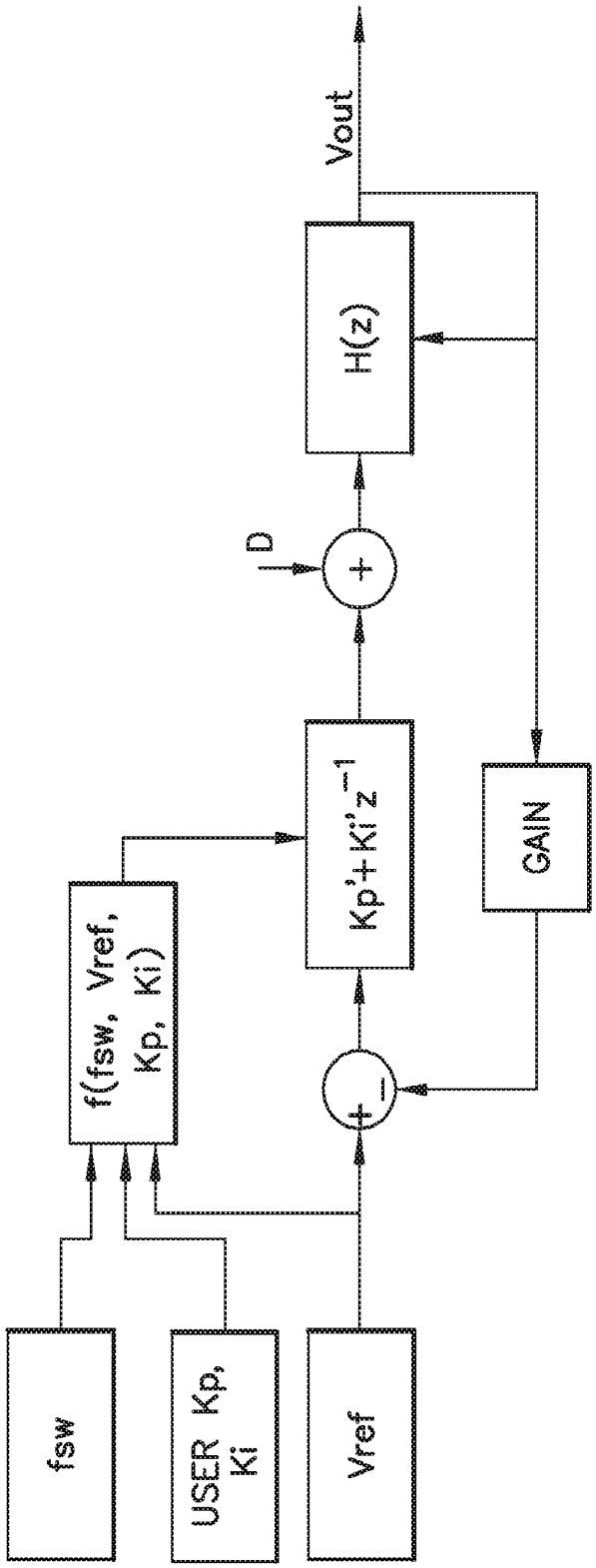


FIG. 14A

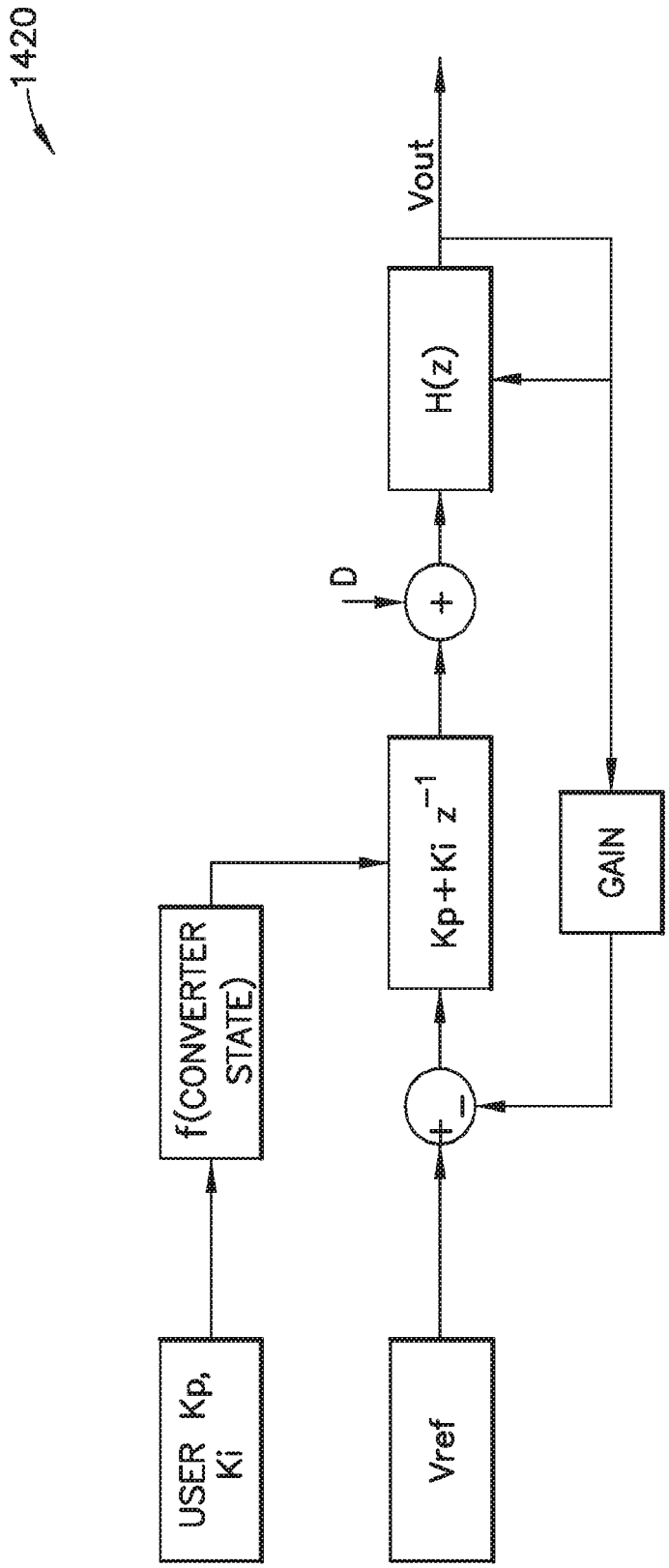


FIG.14B

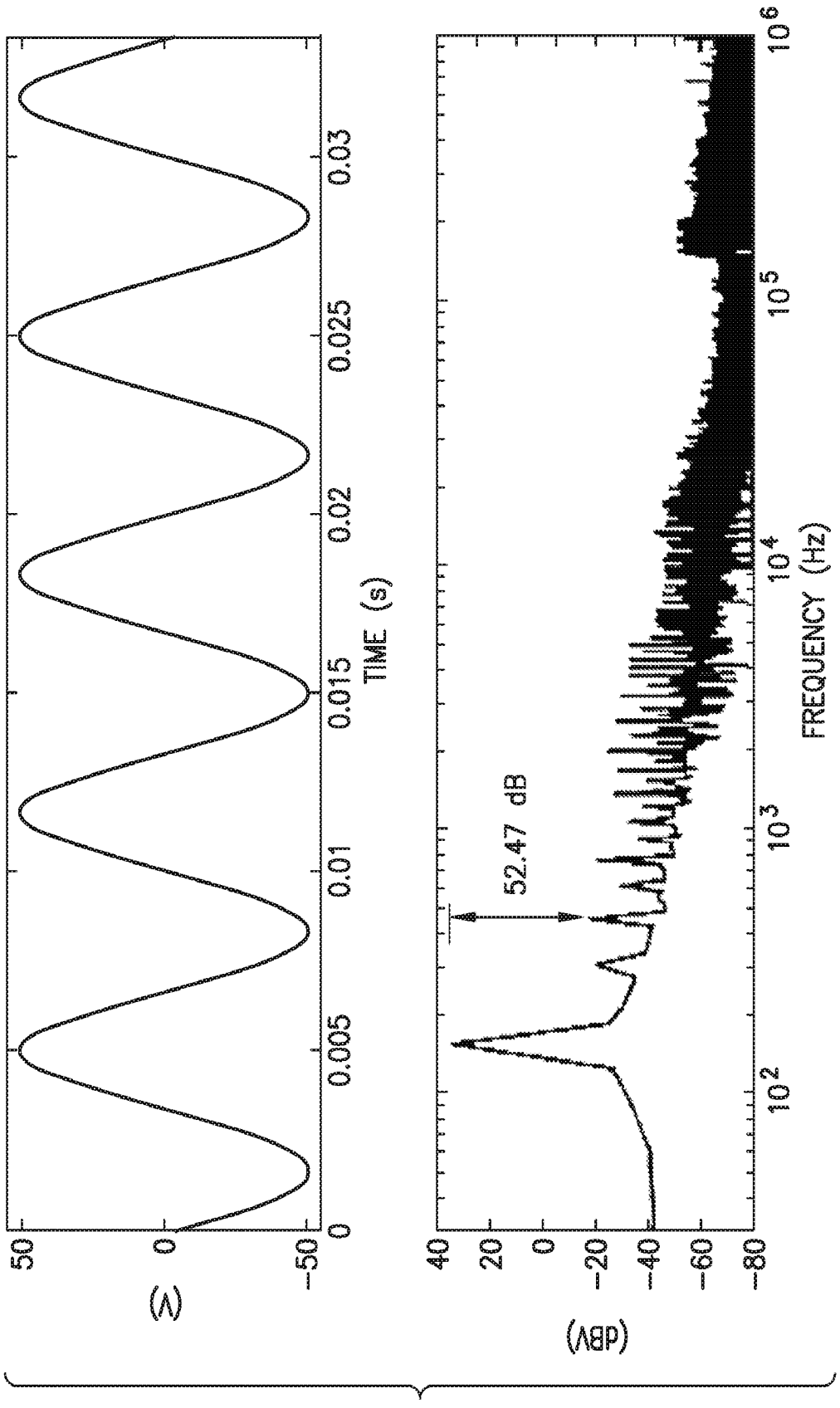

50
0
−50
(V)
0
0.005
0.01
0.015
0.02
0.025
0.03
TIME (s)
40
20
0
−20
−40
−60
−80
(dBV)
52.47 dB
10^2
10^3
10^4
10^5
10^6
FREQUENCY (Hz)

FIG.15

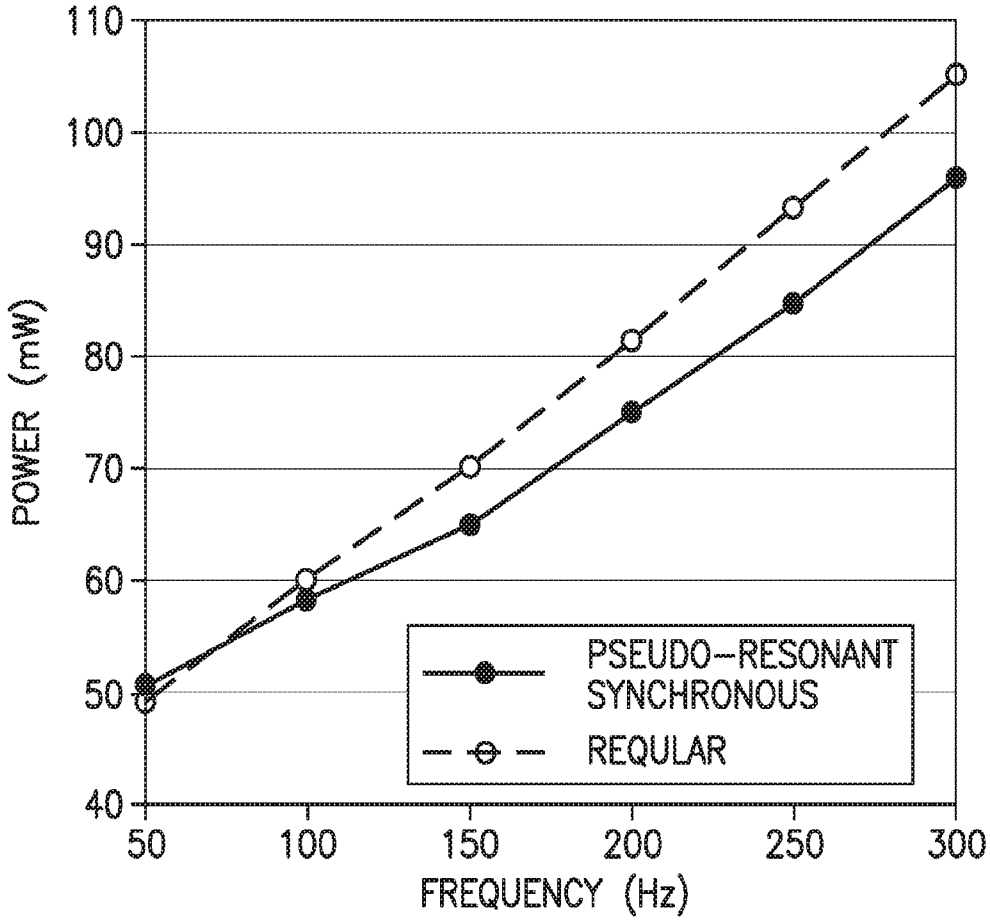

110
100
90
80
70
60
50
40
POWER (mW)
50
100
150
200
250
300
FREQUENCY (Hz)
PSEUDO-RESONANT SYNCHRONOUS
REQULAR

FIG.16

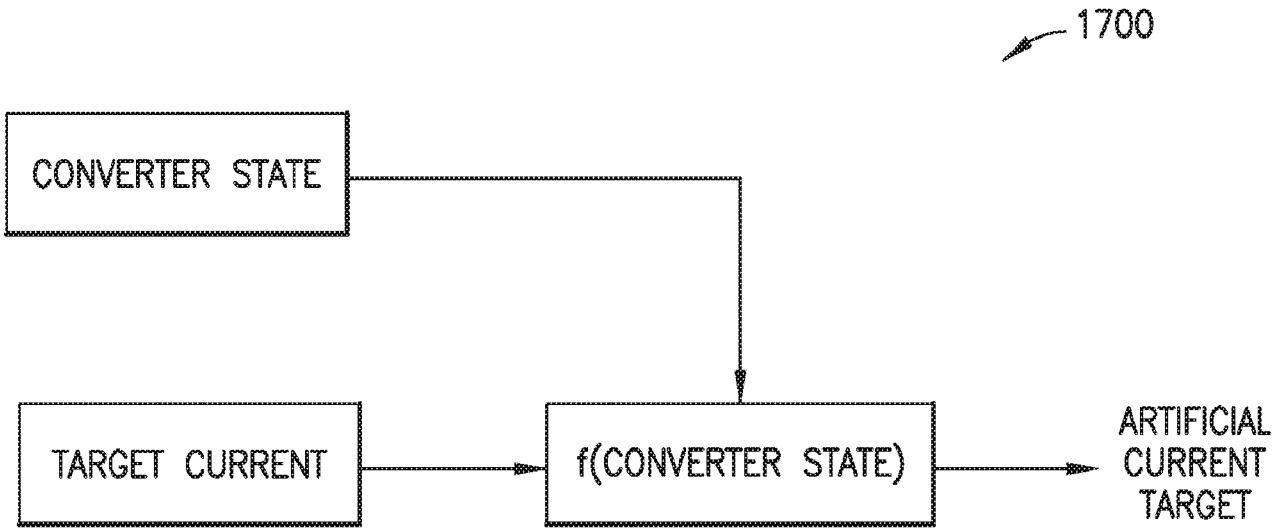

1700
CONVERTER STATE
TARGET CURRENT
f(CONVERTER STATE)
ARTIFICIAL CURRENT TARGET

FIG.17

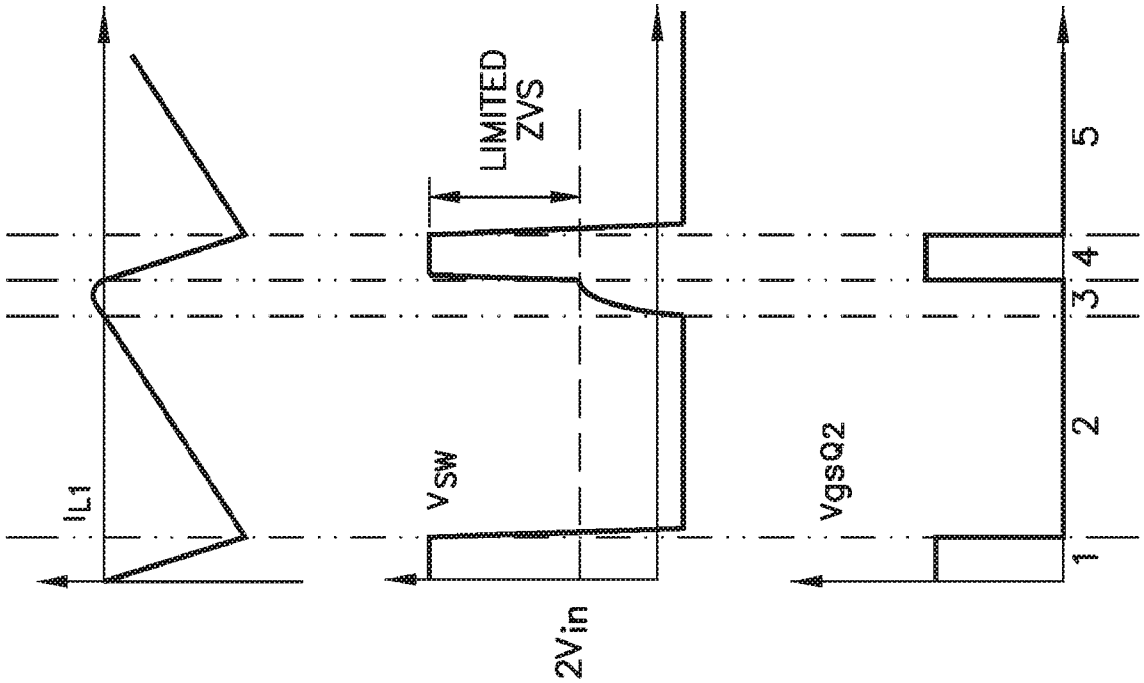


FIG. 18B

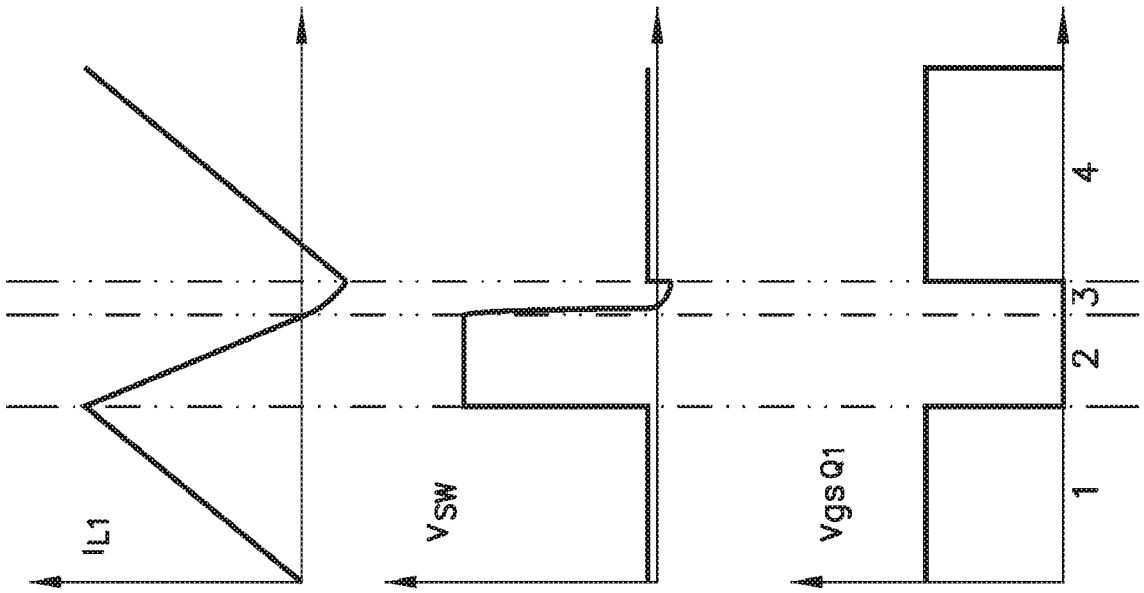


FIG. 18A

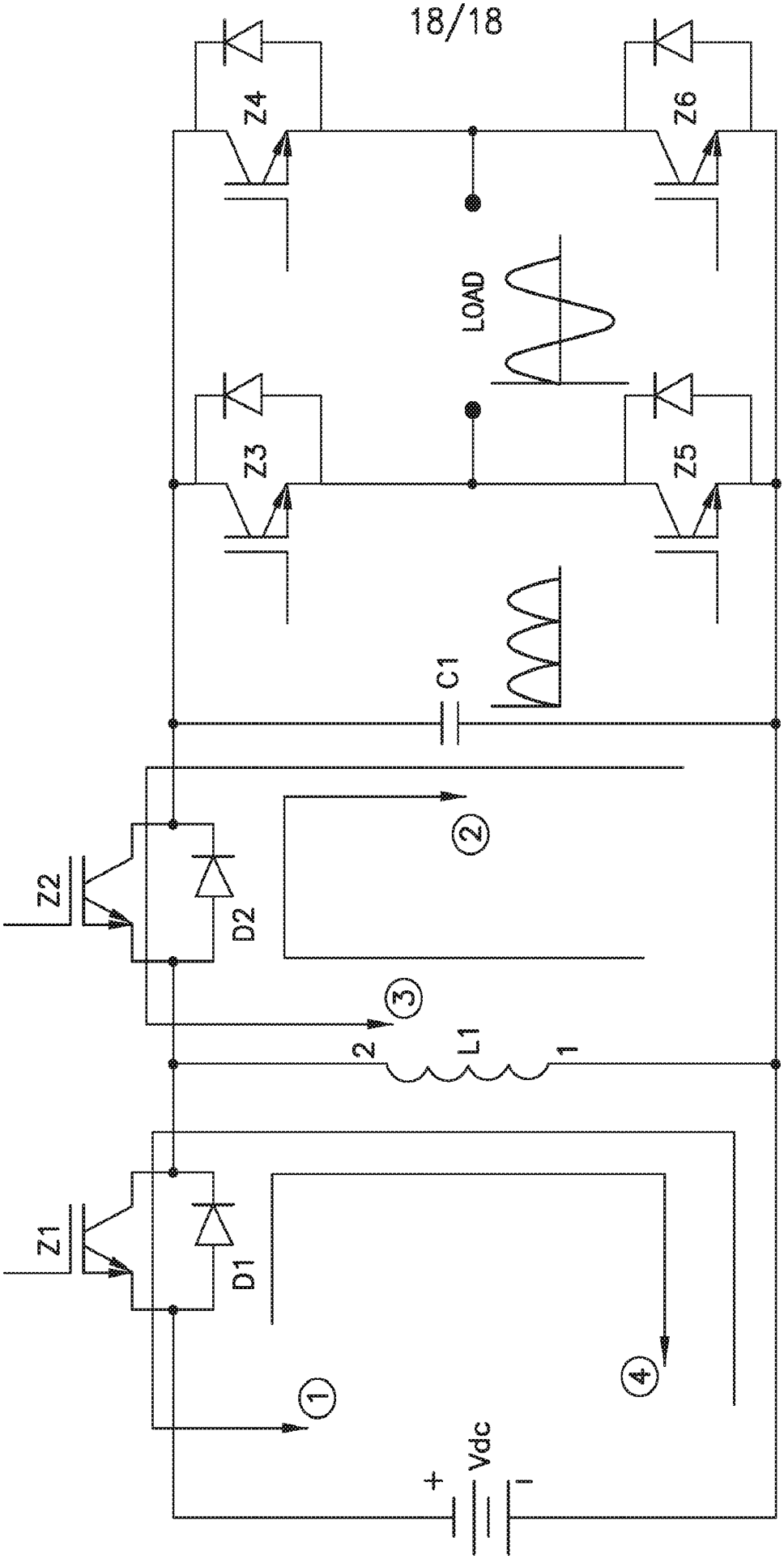


FIG. 19
PRIOR ART

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/053915

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See supplemental page

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-25

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/053915

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H02M 3/335; H02M 3/00; H02M 5/40 (2017.01)
CPC - H02M 3/3376; H02M 3/337; H02M 3/33507 (2017.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC - H02M 3/00; H02M 3/335; H02M 5/40
CPC - H02M 3/337; H02M 3/33507; H02M 3/3376

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC- 363/17, 21.03, 21.04, 21.1, 21.13, 34, 89 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patents, Google Scholar
Search terms used: converter, driver, input voltage, piezoelectric, unfolding, waveform, digital to analog converter, gate, amplifiers, cascaded, switch, zero voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014/0009981 A1 (CHARLES KNILL et al) 09 January 2014 (09.01.2014) entire document	1-25
Y	US 5,969,484 A (SANTI et al) 19 October 1999 (19.10.1999) entire document	1-25
Y	US 2015/0041104 A1 (GE AVIATION SYSTEMS, LLC.,) 12 February 2015 (12.02.2015) entire document	2, 3, 17
Y	US 2012/0268969 A1 (CUK) 25 October 2012 (25.10.2012) entire document	5, 6, 9-20
Y	US 2011/0261599 A1 (DUERBAUM et al) 27 October 2011 (27.10.2011) entire document	6
Y	US 2009/0251925 A1 (USUI et al) 08 October 2009 (08.10.2009) entire document	7
Y	US 2012/0019217 A1 (JENNI) 26 January 2012 (26.01.2012) entire document	8
Y	US 2015/0015072 A1 (INFINEON TECHNOLOGIES) 15 January 2015 (15.01.2015) entire document	10-12, 14
Y	US 2005/0104473 A1 (YOSHIDA) 19 May 2005 (19.05.2005) entire document	18
Y	US 6,781,422 B1 (YANG) 24 August 2004 (24.08.2004) entire document	19, 20
Y	US 2014/0166856 A1 (SONY CORPORATION) 19 June 2014 (19.06.2014) entire document	21
Y	US 2012/0063184 A1 (MAZUMDER) 15 March 2012 (15.03.2012) entire document	22-25

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 2017	21 FEB 2017
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/053915

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2015/028652 A1 (KONINKLIJKE PHILIPS N.V.) 05 March 2015 (05.03.2015) entire document	24, 25
A	US 2012/0081933 A1 (GARRITY) 05 April 2012 (05.04.2012) entire document	1-25
A	US 2010/0052963 A1 (SOUDE et al) 04 March 2010 (04.03.2010) entire document	1-25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/053915

Continued from Box No. III Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.
Group I, claims 1-25, drawn to a driver and method for a circuit with a capacitative load.
Group II, claim 26, drawn to method to reduce the blanking time after a switching event for a converter comprising a digital to analog converter (DAC).
Group III, claims 27-30, drawn to a method for reducing waveform distortion for a controller circuit with a capacitive load.

The inventions listed as Groups I, II and III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: receive an input voltage Vin as input and generate a clean folded waveform as an output; an unfolding stage referenced to Vin, to receive the clean folded waveform from the power converter and unfold the folded waveform into a full waveform, wherein the converter operates bi-directionally as claimed therein is not present in the invention of Groups II and III. The special technical feature of the Group II invention: connecting a first DAC output line to a first cascaded device comprising a first gate; and connecting a complementary DAC second output line to a second cascaded device comprising a second gate; and configuring the first gate and the second gate to have the same voltage as claimed therein is not present in the invention of Groups I or III. The special technical feature of the Group III invention: receiving an input parameter of the controller circuit; identifying a reference voltage (Vref) of the controller circuit; and adapting a proportional gain (Kp) and an integral gain (Ki) of the controller circuit according to a converter transfer function (H(z)) as claimed therein is not present in the invention of Groups I or II.

Groups I, II and III lack unity of invention because even though the inventions of these groups require the technical feature of a digital to analog (DAC) or power converter having a capacitative load, where an input voltage is received by the converter, this technical feature is not a special technical feature as it does not make a contribution over the prior art. Specifically, US 2010/0052963 A1 (SOUDE et al) 04 March 2010 (04.03.2010) teaches a digital to analog (DAC) or power converter having a capacitative load, where an input voltage is received by the converter (DAC 100 that receives digital input D having N bits ([0010]; a capacitive load CL can be coupled to the resistive network at the output of the PRA-DAC 100, [0011]; fig 1).

Since none of the special technical features of the Group I, II or III inventions are found in more than one of the inventions, unity of invention is lacking.