United States Patent

[11] 3,602,138

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[54] **HAMMER DRIVER TIMING FROM A PRINT BUFFER RING**

5 Claims, 3 Drawing Figs.

[52] U.S. Cl. 101/93
[51] Int. Cl. B41j 9/00, B41j 1/20, G06f 7/00
[50] Field of Search ..... 101/93 C; 340/172.5

[56] References Cited

UNITED STATES PATENTS

2,993,437	7/1961	Demer et al.	101/93 C
3,066,601	12/1962	Eden	101/93 C
3,289,576	12/1966	Bloom et al.	101/93 C
3,303,775	2/1967	Giannuzzi	101/93 C
3,303,776	2/1967	Rausch	101/93 C
3,312,174	4/1967	Cunningham	101/93 C
3,343,131	9/1967	Bloom et al.	340/172.5

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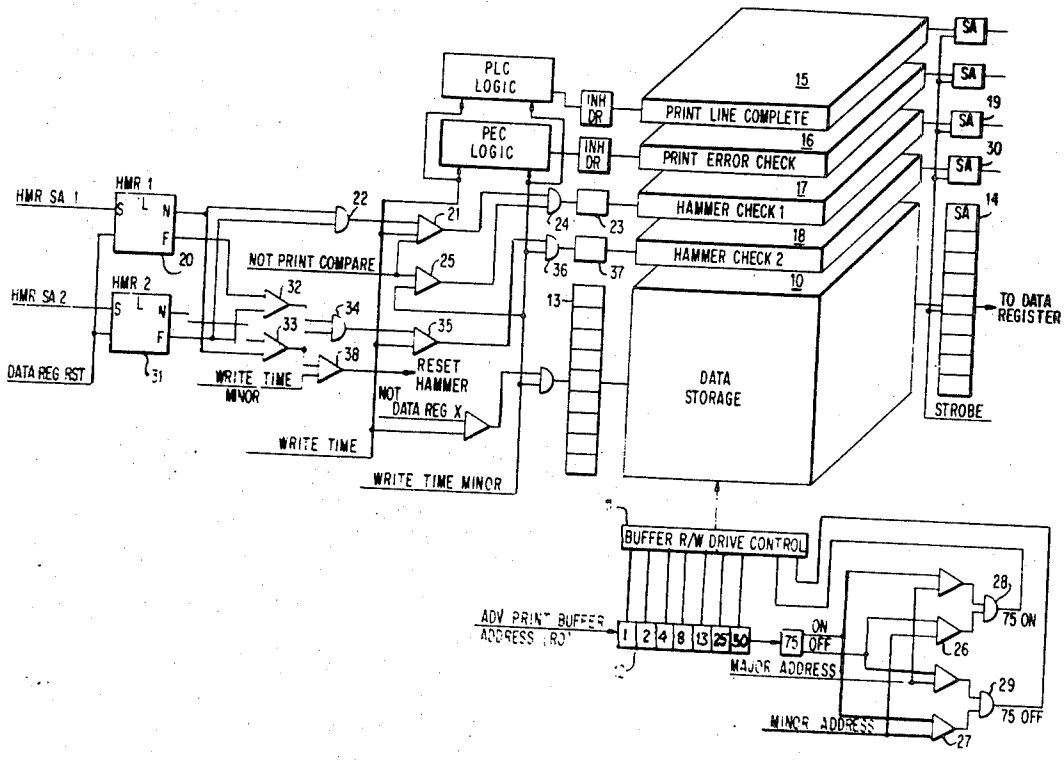
ABSTRACT: There is disclosed timing logic which is useful in high speed chain printer apparatus. The function of the logic is to time the print hammers accurately to any pulse duration that is needed regardless of the print scan timing. In the version specifically described, the logic times the hammer pulse to 2.5 print scans by modifying the hammer address by one-half of a print scan.



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SHEET 1 OF 2

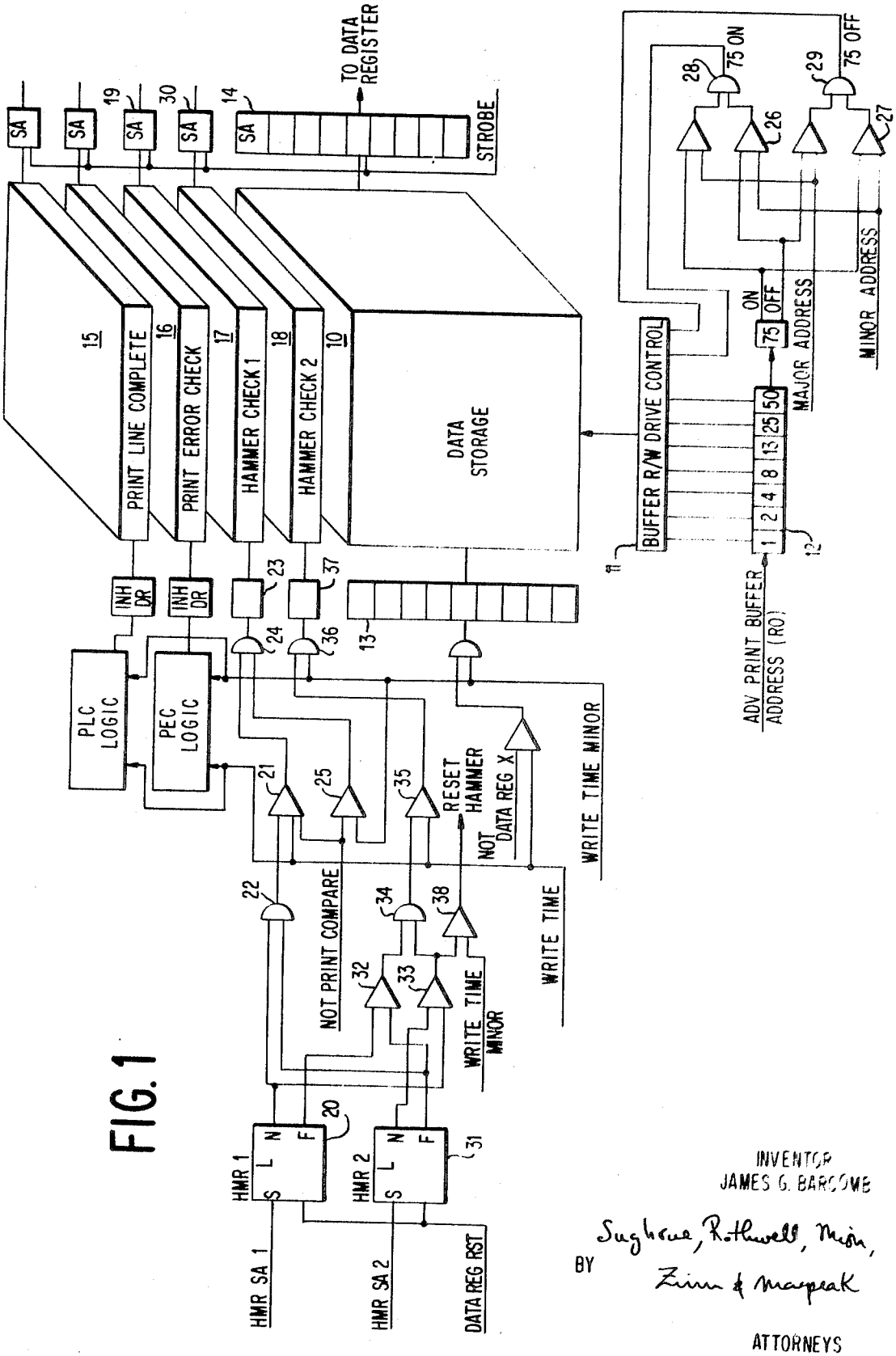

FIG. 1

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ATTORNEYS

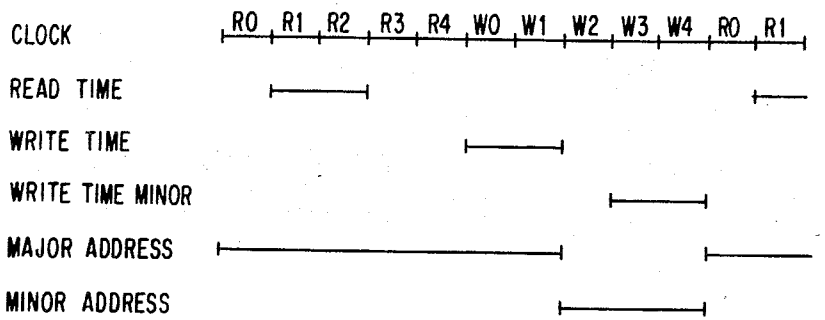
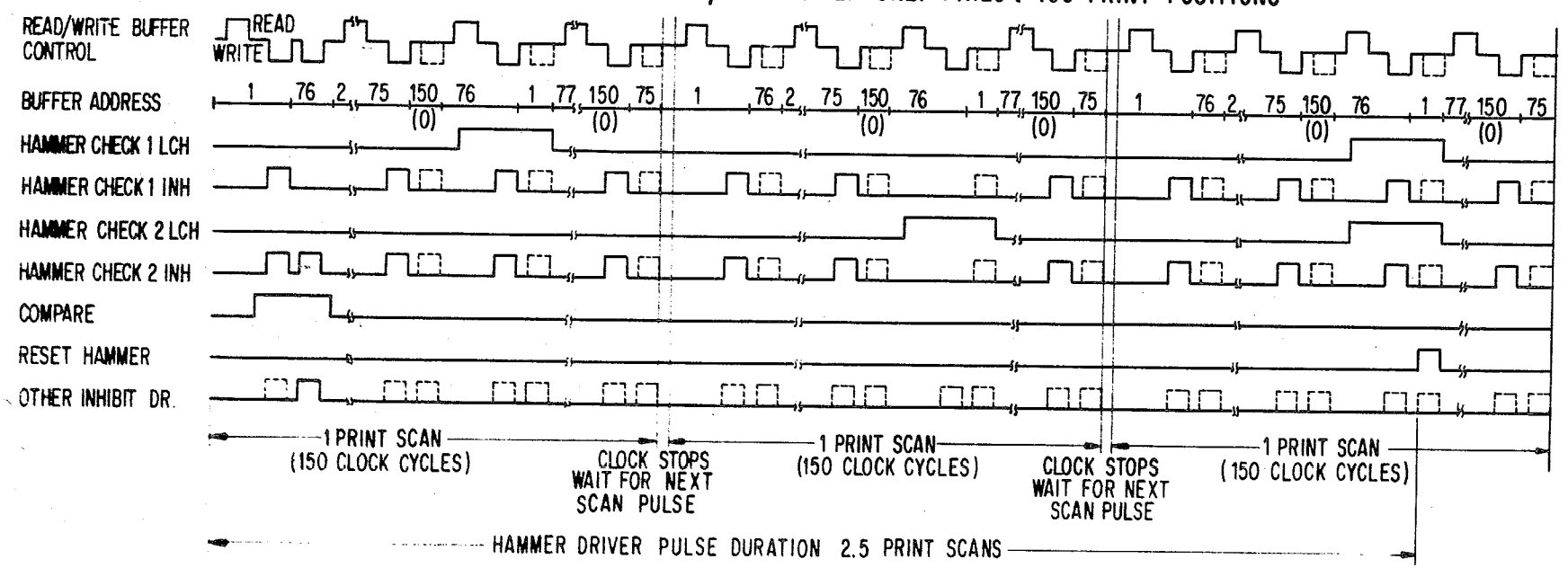


FIG. 2

FIG. 3

EXAMPLE OF SEQUENCE FOR HMR TIMING, #1 HAMMER ONLY FIRES . 150 PRINT POSITIONS



HAMMER DRIVER TIMING FROM A PRINT BUFFER RING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to high speed printer apparatus, and more particularly to hammer driver timing using the print line buffer address ring. While not necessarily limited thereto, the invention has particular utility in a chain printer apparatus of the type shown in U.S. Pat. No. 2,993,437 of F. M. Demer et al., issued July 25, 1961; U.S. Pat. No. 3,066,601 of H. E. Eden, issued Dec. 4, 1962; and U.S. Pat. No. 3,289,576 of E. M. Bloom et al., issued Dec. 6, 1966.

2. Description of the Prior Art

In general, the chain printer apparatus as described in the above patents comprises a print mechanism and controls designed to print data a line at a time on a record medium. The print mechanism comprises a constantly moving type chain, a plurality of hammers arranged in a row parallel to a straight portion of the path of travel of the type and means for guiding and feeding a record medium between the hammer array and type chain. The type chain comprises plural type elements attached to a flexible belt or the like. Each type element bears one or more type characters, and the elements are arranged on the belt so that one or more character sequences in a continuous loop is formed. The print hammers are arranged in a linear array so that one hammer is located at each print position in a line. Since the type chain is moving constantly, the characters coming into alignment with various hammers are constantly changing. The process whereby the characters move into alignment is referred to as scanning.

Printing occurs by selective operation of various hammers in the array in timed relation with the arrival of desired characters at predetermined print positions. The printer control for accomplishing this preferably comprises a magnetic core storage device, means for identifying the characters in the sequence in which they appear on the type chain, means for selecting hammers as the characters register therewith, means for timing the various control and print functions, and means for initiating and terminating the printer operation, paper feeding and data storage transfers. The core storage device, which may be part of the data processing system or may be a separate buffer storage for receiving data from the central processor, stores one line of data at a time. Within the core storage device, an individual core storage position is provided for each hammer position, and there are as many storage positions as there are hammers. When a line of data is stored in the storage device, an instruction is received to print. Data is then read from the storage one character at a time by an address readout means. In the preferred form, the readout means scans the core storage positions in the same sequence in which the characters are alignable with the hammer positions. During the course of a print scan, every position of data storage is scanned once. The process is repeated as many times as there are different characters in the type set.

Simultaneously, with the storage readout operation, the type identifying means, which is a character code generator such as binary counters or the like, is generating a sequence of signals which identify those characters which are registering with the print hammer during the print scan. The data signals read out of the various storage positions are compared with the character signals generated by the character generator for the corresponding print positions. When the comparison circuit detects an identity in signals from the character generator and the data storage, an equal compare signal is produced and used for sending a hammer operate signal through the hammer selection means to the addressed hammer. The timing for the scanning of storage and the stepping of the type identifying counters is provided by a pulse generator, driven in synchronism with the type chain, and a cyclically operable electronic clock. The pulse generator is designed to generate a timing pulse at the beginning of each print scan. The timing pulse initiates clock operation whereupon a series of pulses is generated by the clock each clock cycle to stop the type tracking counters, advance the storage readout and hammer selection means, and fire hammers in the event of an equal compare signal. In the preferred form, the clock is designed to repeatedly generate a sequence of pulses whereby address, compare, hammer firing functions occur in sequence along with various checking functions as described in the above Eden patent.

SUMMARY OF THE INVENTION

Generally stated, an object of this invention is to provide magnetic core storage devices for checking the operation of printing apparatus and timing the operation of the print hammers.

More specifically, it is an object of this invention to provide timing logic operable with the magnetic core storage of a high speed chain printer apparatus for accurately timing the print hammers to any duration that is needed regardless of the print scan timing.

The above as well as other advantages and objects are achieved in accordance with the practice of the present invention by providing timing logic which cooperates with two or more core planes associated with the magnetic core storage device of the printing apparatus. In one version described in more detail hereinafter, the on duration of the print hammers is timed for 2.5 print scans during the regular cycle by modifying the hammer address by one-half of a print scan. Assuming a total of 150 print positions, this is accomplished by modifying the address when a compare is obtained for print position 1 to address 1+75 and by changing the condition of the 75 trigger and writing a bit into position 76 of hammer number 1 core plane. At 76 time, HMR plane 1 and HMR plane 2 are checked for a RESET condition (1, 1) which does not yet exist. The scan continues, and at this address 76 the contents of the HMR planes are modified again to read out the 1 in HMR 1 plane and write a 1 into HMR 2 plane at buffer address 76. At the same time a check is made for a RESET condition, which does not yet exist. On the second scan, at address 76 the contents of the HMR planes are again modified by reading out the number 2 plane and writing a 1 in both the number 1 and number 2 planes. Upon arrival at position 76 of the third scan, a 1 exists in both number 1 and number 2 planes, and a RESET condition signal exists, permitting the firing of a reset for hammer number 1 on minor cycle (hammer address 1). This is 2.5 scans from the time hammer 1 was fired. Thus, the two core planes are used as a binary counter to count the desired number of print scans.

BRIEF DESCRIPTION OF THE DRAWINGS

The specific nature of the invention, as well as other objects, aspects, uses and advantages thereof, will clearly appear from the following description and from the accompanying drawings, in which:

FIG. 1 is a logic block diagram of the printer control which incorporates the hammer driver timing logic according to the invention;

FIG. 2 is a timing diagram showing the sequence of clock pulses and cycles employed by the logic of FIG. 1;

FIG. 3 is an exemplary pulse timing diagram illustrating the sequence for hammer driver timing for a pulse duration of 2.5 print scans.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference is made to the above patents of Demer et al., Eden and Bloom et al., for a detailed description of chain type printer mechanisms. For printing, the action of this type of printer mechanism is basically as follows: With the type chain moving at a constant linear velocity, the type characters serially scan the print hammers. During the course of printing a line of data, the print hammers are selectively operated in timed relation with the arrival of characters desired to be

printed. The printer control system for selectively operating the print hammers comprises a multiposition data storage device such as a multiplane magnetic core storage matrix **10** having as many positions of storage as there are print hammers. The information to be printed in the different positions of a line of data is stored in multiple bit form with each bit stored in a magnetic core arranged in a particular position of the various core planes of matrix **10**. For example, matrix **10** would have seven core planes for each bit of a 7-bit binary code, and each plane comprises plural cores arranged in a row and column configuration. A specific core plane arrangement might comprise 150 cores arranged in 15 rows of 10 cores each to accommodate a corresponding number of hammers.

The information to be printed is written into different positions of matrix **10** from a data input channel. The writing of information in the various storage locations of matrix **10** is performed in a well-known manner by the read/write drive control **11** which selectively energizes write windings of different cores in matrix **10** that are addressed by the buffer address ring counter **12**. The stepping of the address ring **12** is under control of the RO timing pulse (see FIG. **2**) of an electronic clock and oscillator, details of which may be had by referring to the above-mentioned patents. The writing operation is completed when the write drivers are operated in response to a WI clock signal in combination with a readin signal. Inhibit latches **13**, which are energized or set on readin by clock pulse RO and selectively reset in response to data input, have output lines connected to selectively controlled inhibit windings of the cores in the multiple planes of matrix **10** in opposition to the write lines. As is well known in the art, these inhibit lines which are energized will oppose switching of write windings energized by control **11**. Addressed cores having nonenergized inhibit lines are switched from a 0 to a 1 state by the energizing of write windings through control **11**.

Readout of information from the various storage positions of matrix **10** for printing is also effected in a manner well known in the art. The different core positions that are addressed by control **11** under the control of address ring **12** are energized by read drivers in response to an RI clock signal and a Print Scan signal. Outputs upon readout from the sense windings of the cores are fed through sense amplifiers **14** via a feedback connection (not shown) to inhibit latches **13**. The readout is also fed to a compare circuit (also not shown). At clock time WI, the information in latches **13** is rewritten into the same position of storage by read/write drive control **11**. During the readout, the print hammers are addressed in the same manner and sequence as matrix **10** is scanned.

Associated with the data storage matrix **10** **15–18** a plurality of additional core planes **15, 16, 17**, and **18**. These core planes have row and column arrangements corresponding with the arrangement of core planes of matrix **10**. Briefly, the additional core planes comprise print line complete (PLC) plane **15**, print error check (PEC) plane **16**, hammer number **1** check plane **17**, and hammer number 2 check plane **18**. The cores of planes **15–18** are addressed simultaneously with the corresponding positions of storage matrix **10**. For that purpose, the cores of planes **15–18** are wound in a manner known in the art so that core addressing of matrix **10** produces concurrent addressing of corresponding cores in planes **15–18**. The function of the core planes **15–18** is to record various functions occurring in the control system and printer apparatus for checking purposes and for determining when print operation is to be terminated. A detailed description of these basic functions may be had by reference to the Eden and Bloom et al. patents.

The present invention uses core planes **17** and **18** as a binary counter to accurately time the print hammers to any pulse duration. This is accomplished with address modification logic which, in one embodiment of the invention, provides a hammer timing pulse duration of 2.5 print scans.

The clock cycle is shown in FIG. **2** of the drawings, and in the specific embodiment to be described, comprises 10 sections. These include five read RO to R4 and five write WO to W4 sections. The clock can be arbitrarily divided into "major" and "minor " cycles. In the present embodiment, the first seven sections of the clock cycle comprise the major cycle, and the last three comprise the minor cycle. During the major cycle, the buffer and hammer addresses are the same as that of the address ring, while during the minor cycle, the buffer and hammer addresses are different from the address counter by a factor of 75. On this minor cycle, a write operation (write time minor) can take place in the buffer's complement address (±75). This modification of the buffer and hammer addresses on the minor cycle is the principal feature of the present invention. It is this feature which allows the timing to be changes to fit any requirement.

For purposes of illustration, it will be assumed that only hammer number 1 is fired. Now referring to FIGS. **1** and **3**, it will also be assumed that a print scan has just begun and the address counter **12** is at address 1 and after the buffer read. The data read out of matrix **10** is compared with the type character in front of that hammer and a "compare" takes place. Print compare is sampled at clock time R4 and fires hammer number 1 since the buffer and hammer addresses are both 1. Core plane **17** functions in a similar manner as the equal check plane described in the Eden patent. Initially, all the cores in plane **17** are set to 0. Thus, during the read cycle, the readout of the core in plane **17** corresponding to address 1 results in a 0 output from sense amplifier (SA) **19**. The output of sense amplifier **19** is connected to latch **20**. Since a 0 was read out, latch **20** remains in its reset condition and latch **31** which is in reset state supplies a 1 to one input of AND gate **21** by way of OR gate **22**. Normally during the write time of the clock cycle, AND gate **21** provides a 1 output to inhibit driver latch (INH DR) **23** by way of OR gate **24**. However, AND gates **25** and **21** supply a 0 to inhibit driver **23** since a print compare has been generated at write time minor when the buffer address has been modified to 76. As a result, latch **23** remains off thereby permitting a 1 to be written in the core of plane **17** which would ordinarily correspond to address 76. In this manner, plane **17** records a bit each time a memory compare equal signal occurs.

The basic difference between this invention and the Eden patent is that in the present invention an address modification takes place on the latter portion of each clock cycle (minor cycle). This occurs at clock time W2 when the buffer and hammer address is changed to 76 by inverting the output of the 75 stage of the address ring counter **12**. AND gates **26** and **27** sample the outputs of the 75 stage during the minor address cycle of the clock. The outputs of AND gates **26** and **27** are connected by way or OR gates **28** and **29** to address position 76 in buffer read/write drive control **11**. At W3W4 time, minor write current is turned on to the buffer. All inhibit drivers except driver **23** are turned on also. This prevents any additional bits from being entered to all planes except plane **17** which writes a 1 in address position 76.

The scan continues until the address counter **12** reaches 76. When the read current is activated in address 76 of core planes **17** and **18**, sense amplifiers **19** and **30** read out a 1 and a 0, respectively. The 1 from sense amplifier **19** sets latch **20**, but latch **31** remains in its reset condition. At write time, a 1 is gated by AND gate **21** to inhibit driver **23** resulting in a 0 being "written" at address 76 of core plane **17**. Meanwhile, AND gates **32** and **33** and OR gate **34**, which form a compare circuit for latches **20** and **31**, provide a 0 output to AND gate **35**. The output of AND gate **35** is connected by way of OR gate **36** to inhibit driver **37** which remains turned off. This permits a 1 to be written at address position 76 in core plane **18**. At this point, one-half of a print scan has taken pace.

The scan continues to address counter position 150 and then stops and waits for another scan timing pulse to come from the printer. When this pulse occurs, another scan is started. When address counter **12** again reaches position 76 for the second time, the sense amplifiers **19** and **30** read out a 0 and 1, respectively. Latch **20**, therefore, remains reset, and latch **31** is set. As a result, inhibit drivers **23** and **37** are both

turned off, and 1 's are written into position 76 of both core planes 17 and 18. At this point in time, 1.5 print scans have taken place since the firing of hammer number 1.

The scan continues to 150 as before, and when another scan pulse is obtained from the printer, another scan is started. When the address counter 12 reaches 76 once more, sense amplifiers 19 and 30 read out a 1 and 1, respectively. This combination indicates that 2.5 scans have taken place since hammer number 1 has been fired, and hammer number 1 should now be turned off. Inhibit drivers 23 and 37 then write a 0 and 0, respectively, back into core planes 17 and 18 at address position 76 during the write time. On this clock cycle, however, when the minor address of 1 appears during time W2W3W4, the reset will be given to hammer number 1 by AND gate 38. In this manner, hammer number 1 will have been timed for 2.5 print scans.

The operation of any other hammer is essentially the same as that described above. The two core planes 17 and 18 thus serve the dual purposes of timing the hammers and checking the hammers.

If more or less time is required to time the hammers, the number of hammer planes can be increased or decreased accordingly i.e., to tie from four to seven print scans, three hammer planes would be needed.

The circuit described in this application is for 2½ scans. In this scheme the address ring is tailored for the one-half scan count of 75. This produces "complement" addresses, i.e. hammer number 1 is timed in position 76 of the hammer check planes, and hammer 76 is times in position 1. Likewise hammer number 2 is timed in position 77 and hammer number 77 in position 2. Also, 0 (150 is timed in position 75 and 75 is timed in position 0 (150).

For other fractional scans other "complement rings" would come about, i.e. to time to 2¼scans an address ring having the last two stages of values 38 and 76 could be used. Under these conditions hammer 1 would be timed in position 39, hammer 39 timed in position 77, hammer 77 timed in position 115, and hammer115 timed in position 1. For other fractional scans other arrangements of the ring or other means for changing the hammer and buffer addresses on the "minor cycle" can be made.

It will be apparent from the foregoing that the embodiment shown is only exemplary and that various modifications can be made in construction and arrangement within the scope of the invention as defined in the appended claims.

What is claimed is:

1. In a printer having a plurality of pring hammers with firing means and a chain bearing a plurality of characters movable past said hammers, core storage means for storing data to be printed in each of a plurality of positions corresponding to said hammers, means for determining the character at a particular hammer position means for comparing the character in core storage for the particular hammer position and generating a print compare signal, the improvement of hammer timing logic comprising:

a. a plurality of additional core planes having row and column arrangements corresponding with the arrangement in the core storage and addressed simultaneously therewith,

b. address modification means responsive to said print compare signal for changing the address of the currently addressed hammer and recording an indication of said print compare signal in the first of said plurality of additional core planes,

c. means responsive to the readout from said plurality of additional core planes for advancing the data stored therein in a binary progression during each print scan, and

d. means responsive to a predetermined count read out from said plurality of additional core planes for generating a reset pulse to the print hammer.

2. The hammer timing logic as recited in claim 1 wherein said plurality of additional core planes comprise two core planes and said reset pulse generating means is responsive to a binary count of 1, 1 for generating said reset pulse.

3. The hammer timing logic as recited in claim 2 wherein said address modification means modifies the hammer address by one-half of a print scan.

4. The hammer timing logic of claim 1 wherein each print scan consists of a plurality of clock cycles, each clock cycle consisting of a sequence of pulses defining a plurality of read and write subcycles, a first group of said subcycles being termed a MAJOR cycle and a second group of said subcycles being termed a MINOR cycle, said MINOR cycle occurring at the latter portion of each of said clock cycles and comprising a plurality of write subcycles, said address modification means including:

a. address counter means for selectively designating an address corresponding to a location in said core planes,

b. read/write control means responsive to said clock subcycles for addressing a location in said core planes designated by said counter means during a MAJOR cycle, and

c. logic means responsive to the MINOR cycle for altering the location addressed by said read/write control means during the MINOR cycle.

whereby two locations in said core planes are addressed during each clock cycle, said two locations being subjected successively to a write operation without an intervening read operation.

5. The hammer timing logic as recited in claim 1 wherein said address modifications means includes means for providing two successive write cycles for changing the address of the currently addressed hammer without an intervening read cycle.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,602,138 Dated August 31, 1971

Inventor(s) JAMES G. BARCOMB

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 1, line 53 - "readout" should be "read-out" (twice)
line 59 - "readout" should be "read-out"

Col. 2, line 3 - "readout" should be "read-out"

Col. 3, line 26 - "readin" should be "read-in"
line 27 - "readin" should be "read-in"
line 36 - "readout" should be "read-out"
line 41 - "readout" should be "read-out"
line 44 - "readout" should be "read-out"
line 48 - "readout" should be "read-out"
line 49 - delete "15-18" and substitute "are"

Col. 4,
line 26 - "readout" should be "read-out"
line 31 - Comma (,) should be inserted after "normally"

Col. 5, line 23 - "tie" should be "time"
line 29 - "times" should be "timed"
line 32 - "(150" should be "(150)"

Col. 6, line 13 - "readout" should be "read-out"

Signed and sealed this 11th day of April 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

FORM PO-1050 (10-69)

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