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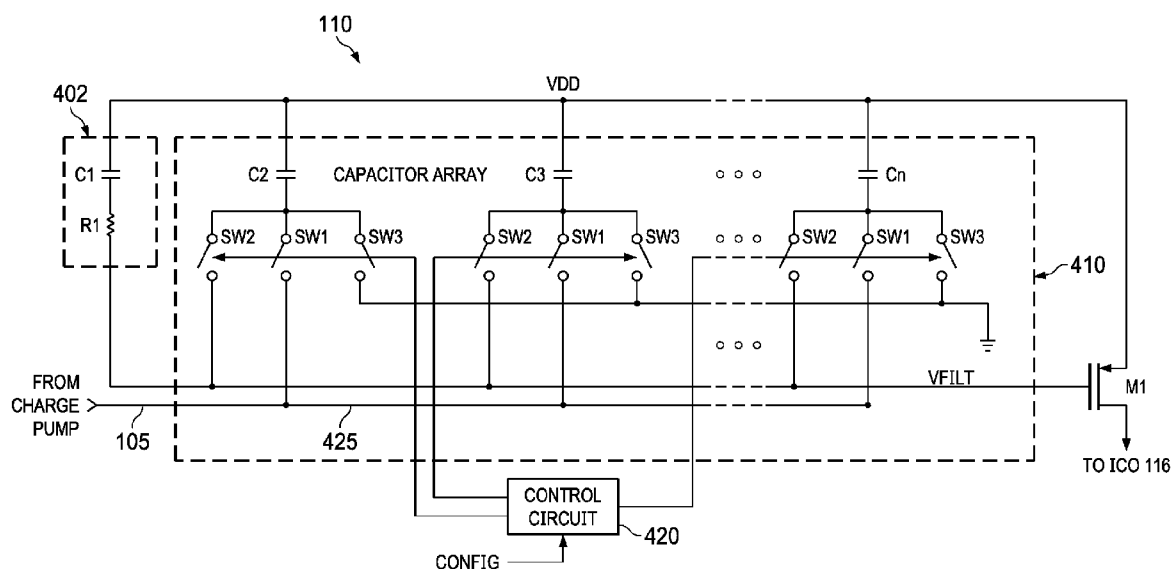


FIG. 4

(57) **Abstract:** A circuit includes a first filter (402), a plurality of binary -weighted capacitors (C1, C2, Cn), and a current source device (M1). The circuit also includes a first plurality of switches (SW3). Each of the first plurality of switches (SW3) is connected to a separate capacitor of the plurality of binary- weighted capacitors (C1, C2, Cn). The first plurality of switches (SW3) are connected together, and the first plurality of switches (C1, C2, Cn) are not connected to the first filter. A second plurality of switches (SW2) is also included, and each of the second plurality of switches (SW2) is connected to a separate capacitor of the plurality of binary-weighted capacitors (C1, C2, Cn) and to the first filter (402) and to a control input of the current source device (M1). The first plurality of switches (SW3) is not connected to the control input.



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LOOP FILTER FOR A PHASE-LOCKED LOOP

BACKGROUND

[0001] Many phase-locked loops (PLLs) include a loop filter that filters a signal produced by a charge pump or other type of circuit. The output of the loop filter can be used to control, for example, a current source device which provides current to a current controlled oscillator.

SUMMARY

[0002] In one example, a circuit includes a first filter, a plurality of binary-weighted capacitors, and a current source device. The circuit also includes a first plurality of switches. Each of the first plurality of switches is connected to a separate capacitor of the plurality of binary-weighted capacitors. The first plurality of switches are connected together, and the first plurality of switches are not connected to the first filter. A second plurality of switches is also included, and each of the second plurality of switches is connected to a separate capacitor of the plurality of binary-weighted capacitors and to the first filter and to a control input of the current source device. The first plurality of switches are not connected to the control input. The circuit can be used as part of a phase-locked loop.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] For a detailed description of various examples, reference will now be made to the accompanying drawings in which:

[0004] FIG. 1 illustrates an analog phase-locked loop in an example.

[0005] FIG. 2 illustrates waveforms of various signals of the described analog phase-locked loop.

[0006] FIG. 3 shows a charge pump circuit usable in the analog phase-locked loop in an example.

[0007] FIG. 4 shows an example of a loop filter usable in the analog phase-locked loop.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] An analog PLL (APLL) is described. The described APLL includes, among other components, a charge pump, a loop filter, and a current controlled oscillator. In some examples, the output of the loop filter is used to control a current source device that provides current to the

current controlled oscillator. In practice, parasitic capacitance is present on the control input to the current source device. The parasitic capacitance can cause noise on the power supply to impact the loop filter's signal to the current source device and thus the current to the current controlled oscillator. The loop filter described herein has architecture that addresses this problem.

[0009] FIG. 1 shows an example of APLL 100. The example APLL 100 includes a phase and frequency detector 102, a charge pump 104, a loop filter 110, a current controlled oscillator (ICO) 116 and a frequency divider 118. The output signal from the ICO 116 is an output clock (OUTCLK) 117. A reference clock (REFCLK) 101 is provided to an input of the phase and frequency detector 102. In some examples, the phase and frequency detector 102 generates an error signal 103 based on the frequency and/or phase difference (error) between REFCLK 101 and OUTCLK 117. In the example of FIG. 1, the frequency of OUTCLK 117 is greater than the frequency of REFCLK 101. The frequency divider 118 divides down the frequency of OUTCLK 117 to produce a feedback clock (FBCLK) 119 that is approximately of the same frequency as REFCLK 101. Reference herein to the FBCLK 119 includes the output signal from a frequency divider (e.g., frequency divider 118) as well as to the output clock from ICO 116 in the implementation in which the frequency of OUTCLK 117 is of the same frequency as REFCLK 101.

[0010] The APLL 100 adjusts the frequency and phase of OUTCLK 117 so as to match the phase of REFCLK 101. FIG. 2 shows an example of REFCLK 101 and FBCLK 119 where the rising and falling edges of FBCLK 119 are phase aligned to the edges of REFCLK 101. FBCLK 119 is said to be "locked" on to REFCLK 101. Accordingly, OUTCLK 117 also is phase aligned to REFCLK in the locked state, although the frequency of OUTCLK 117 may be the same or greater than that of REFCLK 101.

[0011] In some examples, the error signal 103 comprises a series of UP pulses as well as a series of DOWN pulses. FIG. 2 also shows an example of UP pulses and DOWN pulses. Responsive to the edges of FBCLK 119 lagging the corresponding edges of REFCLK 101, the phase and frequency detector 102 generates the width W1 of the UP pulses to be wider than the width W2 of the DOWN pulses. Conversely, responsive to the edges of FBCLK 119 leading the corresponding edges of REFCLK 101, the phase and frequency detector 102 generates the width W1 of the UP pulses to be narrower than the width W2 of the DOWN pulses.

[0012] FIG. 3 provides an example of charge pump 104. In this example, the charge pump 104

includes a current source device I1 coupled to a current device I2 through a selectable switch SWA. Switch SWB selectively couples I2 to ground. The DOWN pulses 302 of the error signal 103 control the on and off state of SWA and the UP pulses 312 control the on and off state of SWB. When SWA is closed by an active DOWN pulse 302, current flows through SWA and to the loop filter 110. When SWB is closed by an active UP pulse 302, current flows from the loop filter 110 through SWB to ground. Charge pump signal 105 thus includes a series of positive and negative current pulses based on the UP and DOWN pulses of the error signal 103.

[0013] FIG. 4 shows an example of the loop filter 110. The illustrated loop filter 110 includes a first filter 402, a capacitor array 410, a control circuit 420, and a current source device M1. The first filter 402 in this example includes a capacitor C1 (also referred to as a filter capacitor) connected in series to a resistor R1. Capacitor C1 connects to supply voltage node (VDD) and resistor R1 connects to a control input of M1. In this example M1 is a p-type metal oxide semiconductor field effect transistor (PFET) and, as such resistor R1 connects to the gate of M1. In other implementations, M1 may be implemented as an n-type metal oxide semiconductor field effect transistor (NFET), as a p-type or n-type bipolar junction transistor, or as another type of transistor. The signal line between R1 and the control input to M1 is labeled as VFILT and represents the filtered output voltage from the loop filter 110, which is used to control the operating state of M1 and thus current magnitude to the ICO 116.

[0014] The capacitor array 410 includes a plurality of capacitors C2, C3,..., Cn. In some examples, the capacitor array 410 is implemented as a binary-weighted capacitor array which allows the PLL to operate over a wide range of input reference frequencies, although the capacitors need not be binary weighted in other implementations. As such, the capacitors C2, C3,..., Cn have different capacitance values that are binary weighted. For example, the weightings of the capacitance values of the capacitors C2, C3,..., Cn may be 16C, 8C, 4C, etc. Capacitor C2 may be 16C and capacitor C3 may be 8C meaning that capacitor C2's capacitance value is double that of capacitor C3. In some implementations, capacitor C1 also is implemented as a configurable capacitor array (similar to capacitor array 410) to facilitate operability over a wide frequency range.

[0015] The loop filter 110 of FIG. 4 includes a plurality of first switches SW1, a plurality of second switches SW2, and a plurality of third switches SW3. Each capacitor C2, C3,... Cn connects to a set of first, second and third switches SW1-SW3 as shown. Each of first switches

SW1 connects to each of the other second switches SW1 as well to the charge pump 104. Current from the charge pump 104 flows through switches SW1 to their respective capacitors C2, C3,..., Cn and current from the capacitors C2, C3, ... Cn flows through the respective switch SW1 and to the charge pump 104. Each of the second switches SW2 connects to each of the other second switches SW2 and to the loop filter 402 (e.g., to the resistor R1) and to the control input of M1. Each of the third switches SW3 connects to each of the other third switches SW3 and either to a ground node as shown or another fixed voltage node to reduce their leakage current.

[0016] Node 425 connects to the charge pump 104 and first switches SW1, but not to the first filter 402 or the control input of M1. Instead, the control input of M1 is connected to second switches SW2 and the first filter 402. As such, the charge pump 104 is not connected to M1.

[0017] In some examples, first switches SW1 are binary-weighted like their corresponding capacitors C2, C3,..., Cn. The ratio of channel width (W) to channel length (L) of each switch SW1 is binary weighted. For example, SW1 connected to C2 has a W/L ratio (e.g., $16 \cdot W/L$) that is twice that of C3 (e.g., $8 \cdot W/L$), and so on. The W/L ratios of switches S2 and S3 need not be binary weighted and can be smaller than switches SW1. The W/L ratios of switches SW2 can all be the same and the W/L ratios of switches SW2 also can all be the same, albeit different than (or the same as) for switches SW2.

[0018] In practice, the switches create a parasitic capacitance to ground which injects supply noise into the ISO 116. Referring to FIG. 4, in the absence of any parasitic capacitance to ground, any noise on the voltage supply will also be directly coupled to the gate of M1 through the capacitors C2, C3,..., Cn. Thus, the supply noise seen at the gate of M1 would be zero. However, if there is a parasitic capacitance to ground from either VFILT or the gate of M1, there will be a potential division between C2, C3,..., Cn and the parasitic capacitance resulting in a non-zero supply noise component on the gate-to-source voltage of M1. The size of the parasitic capacitance is directly proportional to the sizes of the switches.

[0019] An advantage of the described examples is that the size (W/L) of the switches can be small, for the following reasons. A direct consequence of reducing the W/L of a metal oxide semiconductor (MOS) switch is that its resistance increases. The described architecture has the advantage that a higher switch resistance can be tolerated. To explain this advantage, consider the three sets of switches in FIG. 4 separately. The switches SW1 connect C2, C3,..., Cn to the charge pump 104 which generally has a high output resistance. Thus, the resistance of the switches SW1

can be relatively large without any significant effect on performance. The switches SW2 connect C2, C3,..., Cn to the filter 402 which contains a resistor R1 whose value is relatively large. As such, the resistance of SW2 can be relatively large. The switches SW3 are used to connect C2, C3,..., Cn to a dummy node when they are not used. Thus, the resistance of SW3 is for all practical purposes inconsequential and SW3 can be made arbitrarily small. By making switches SW3 relatively small, the parasitic capacitance at the gate of M1 can be reduced. The injection of supply noise into the gate-to-source voltage of M1 is reduced which in turn minimizes the effect of supply noise on the oscillator frequency. The control circuit 420 may be implemented as a controller, a finite state machine or other type of hardware device that can assert control signals to control the on and off state of the switches SW1-SW3. The control circuit 420 receives configuration (CONFIG) which specifies which of the binary weighted capacitors C2, C3,..., Cn are to be included in operation of the loop filter 110. The configuration information may be stored in a register within the control circuit 420. Various combinations of capacitors C2, C3,..., Cn can be activated by the control circuit 420 based on the configuration information. For a given capacitor C2, C3,..., Cn to be activated, the control circuit 420 asserts control signals so as to turn on (close) the corresponding SW1 and SW2 switches for those particular capacitors and to turn off (opens) switch SW3 for those same capacitors. For all other capacitors not to be activated as part of the loop filter's operation, the control circuit 420 asserts control signals so as to turn off the corresponding SW1 and SW2 switches and turn on switch SW3 for those capacitors.

[0020] The current from M1 flows to the ICO 116, which produces OUTCLK 117 with a frequency that is a function of the current from M1. The frequency and phase of OUTCLK 117 is repeatedly adjusted so as to maintain frequency and phase lock between FBCLK 119 and REFCLK 101.

[0021] In this description, the term “couple” or “couples” means either an indirect or direct wired or wireless connection. Thus, if a first device couples to a second device, that connection may be through a direct connection or through an indirect connection via other devices and connections. The recitation “based on” means “based at least in part on.” Therefore, if X is based on Y, X may be a function of Y and any number of other factors.

[0022] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit, comprising:

a charge pump to receive voltage pulses indicative of a phase error between a reference clock and a feedback clock and to generate current pulses based on the voltage pulses;

a loop filter coupled to the charge pump, the loop filter to filter the current pulses and to generate a signal to control a current source device, and the loop filter including a first filter coupled to a binary-weighted capacitor array, the binary-weighted capacitor array comprises a plurality of capacitors;

a current controlled oscillator coupled to the current source device, the current controlled oscillator to generate an output clock at a frequency based on current from the current source device;

a plurality of first switches connected to each other and to the charge pump, and each capacitor connects to a separate one of the first switches; and

a plurality of second switches connected to each other and to the first filter, and each capacitor connects to a separate one of the second switches.

2. The circuit of claim 1, further comprising a plurality of third switches, and each capacitor of the binary-weighted capacitor array connects to a separate one of the third switches.

3. The circuit of claim 2, further comprising a control circuit to generate control signals to control the on/off state of the first, second, and third switches associated with each capacitor of the binary-weighted capacitor array, wherein for each capacitor, the control circuit is to control the third switch to be off while the first and second switches are on and to control the third switch to be on while the first and second switches are off.

4. The circuit of claim 1, wherein:

each capacitor of the binary-weighted capacitor array has a capacitance value that is binary-weighted with respect to each of the other binary-weighted capacitors; and

each of the first switches has a width and a length, and a ratio of the width to length associated with each of the first switches is binary-weighted with respect to the ratio of width to length each of the other first switches.

5. The circuit of claim 4, wherein the ratio of width to length of each of the second switches is approximately equal to the ratio of width to length of each of the other second switches.

6. The circuit of claim 1, wherein the first filter includes a resistor connected to a first filter capacitor, the resistor connects to the second switches, and the first filter capacitor connects to each of the capacitors of the binary-weighted capacitor array.
7. A circuit, comprising:
a first filter;
a plurality of binary-weighted capacitors;
a current source device;
a first plurality of switches, each of the first plurality of switches connected to a separate capacitor of the plurality of binary-weighted capacitors, the first plurality of switches are connected together, and the first plurality of switches are not connected to the first filter; and
a second plurality of switches, each of the second plurality of switches connected to a separate capacitor of the plurality of binary-weighted capacitors and to the first filter and to a control input of the current source device;
wherein the first plurality of switches are not connected to the control input.
8. The circuit of claim 7, further comprising a charge pump connected to each of the first plurality of switches but not connected to the first filter nor the control input of the current source device.
9. The circuit of claim 7, further comprising a plurality of third switches, and each capacitor of the binary-weighted capacitor array connects to a separate one of the third switches.
10. The circuit of claim 9, wherein each of the plurality of third switches connects to a fixed voltage node.
11. The circuit of claim 9, further comprising a control circuit to generate control signals to control the on/off state of the first, second, and third switches associated with each capacitor of the binary-weighted capacitor array, wherein for each capacitor, the control circuit is to control the third switch to be off while the first and second switches are on and to control the third switch to be on while the first and second switches are off.
12. The circuit of claim 7, wherein each of the first switches has a width and a length, and a ratio of the width to length associated with each of the first switches is binary weighted with respect to the ratio of width to length each of the other first switches.
13. The circuit of claim 12, wherein the ratio of width to length of each of the second switches is approximately equal to the ratio of width to length of each of the other second switches.

14. The circuit of claim 7, wherein the first filter includes a resistor connected to a first filter capacitor, the resistor connects to the second switches, and the first filter capacitor connects to each of the capacitors of the binary-weighted capacitor array.

15. A circuit, comprising:

a loop filter to filter current pulses and to generate a signal to control a current source device, and the loop filter including a first filter coupled to a capacitor array, the capacitor array comprises a plurality of capacitors;

a current controlled oscillator coupled to the current source device, the current controlled oscillator to generate an output clock at a frequency based on current from the current source device;

a plurality of first switches connected to each other and to the charge pump, and each capacitor connects to a separate one of the first switches;

a plurality of second switches connected to each other and to the first filter, and each capacitor connects to a separate one of the second switches; and

a plurality of third switches, and each capacitor connects to a separate one of the third switches.

16. The circuit of claim 15, wherein the capacitor array comprises a binary-weighted capacitor array.

17. The circuit of claim 15, further comprising a control circuit to generate control signals to control the on/off state of the first, second, and third switches associated with each capacitor of the capacitor array, wherein for each capacitor, the control circuit is to control the third switch to be off while the first and second switches are on and to control the third switch to be on while the first and second switches are off.

18. The circuit of claim 15, wherein each of the plurality of third switches connects to a fixed voltage node.

19. The circuit of claim 15, further comprising a charge pump connected to each of the first switches, but not connected to the first filter.

20. The circuit of claim 15, wherein each of the second switches is connected to a control input of the current source device, but none of the first nor third switches is connected to the control input.

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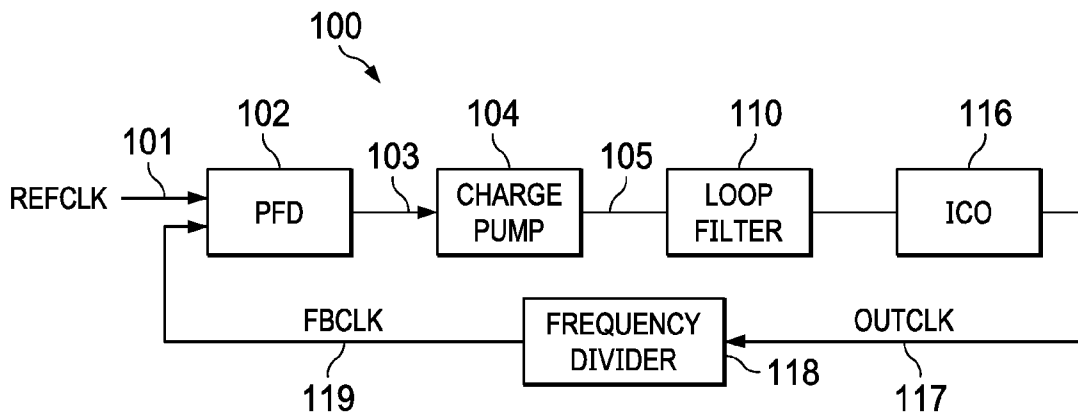


FIG. 1

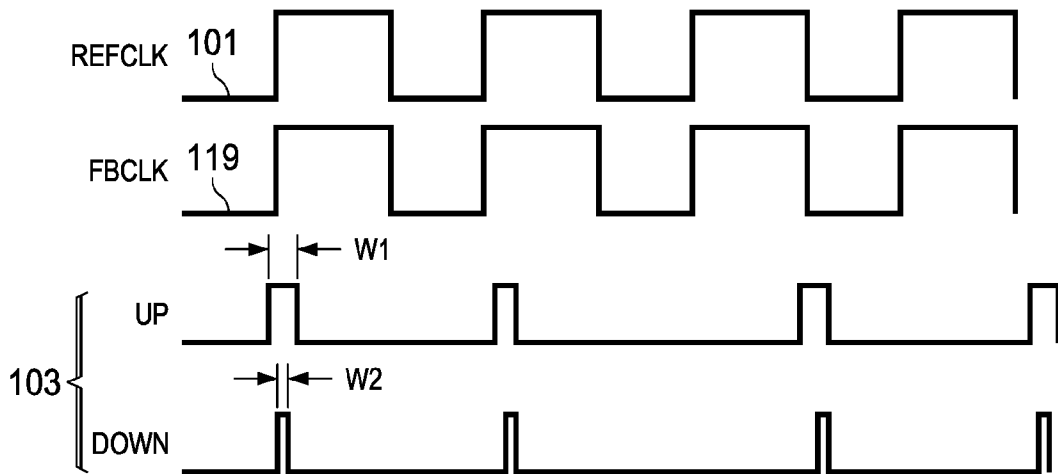


FIG. 2

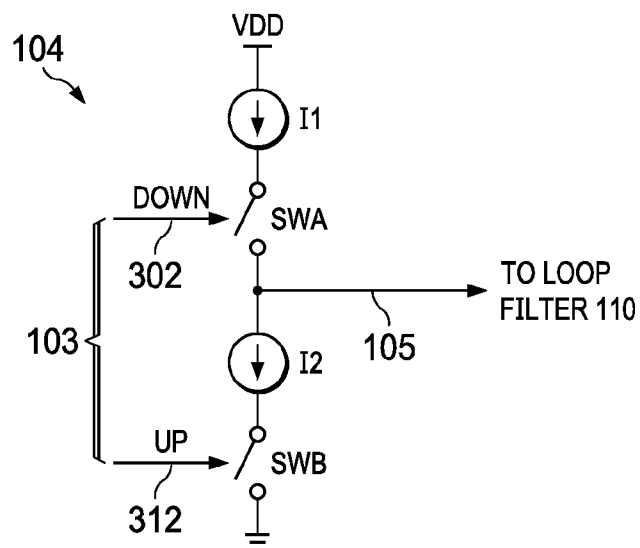


FIG. 3

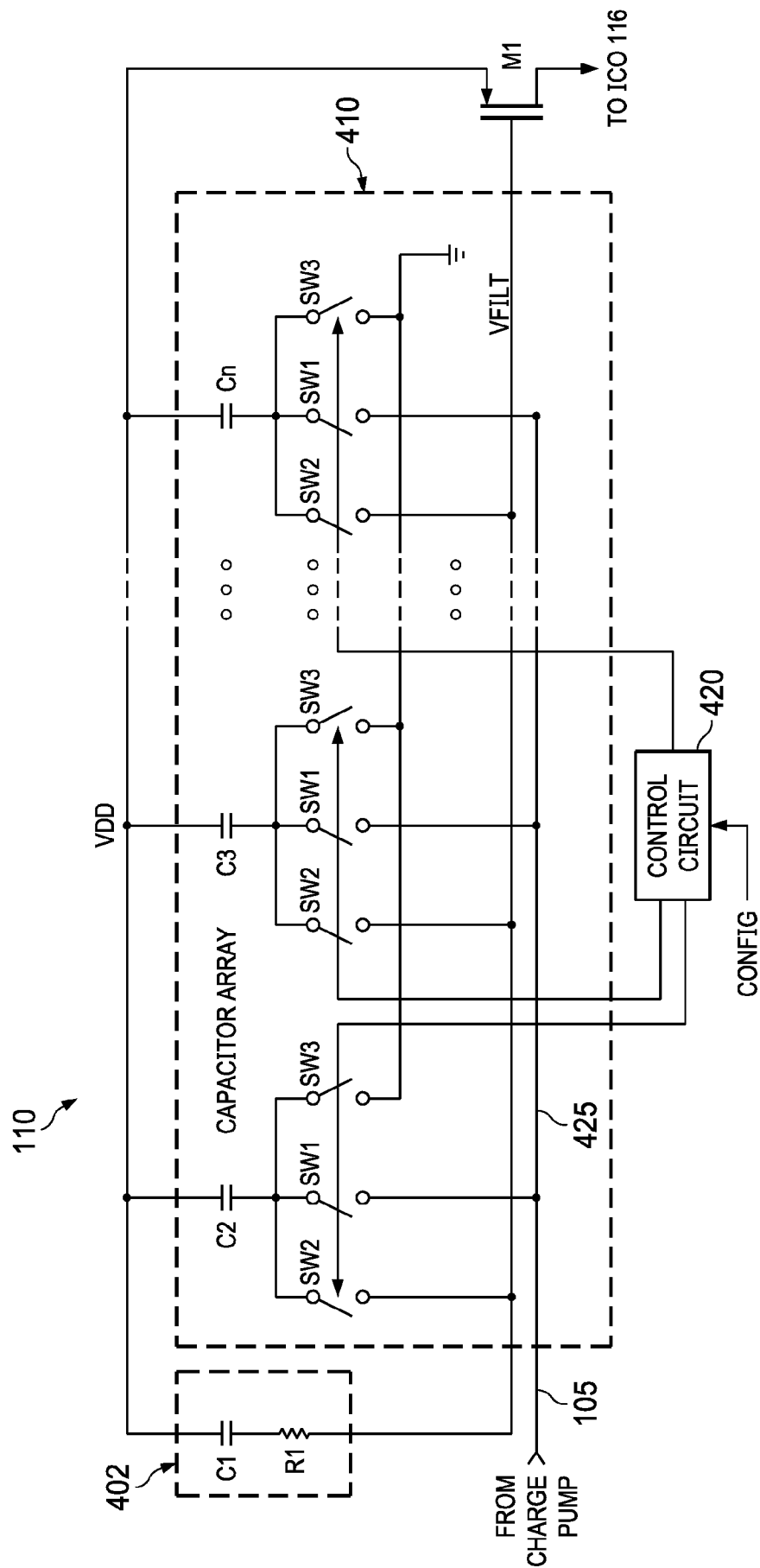


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

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A. CLASSIFICATION OF SUBJECT MATTER

H03L 7/06(2006.01)
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Espacenet, PatSearch, PAJ, WIPO, USPTO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 108377148 A (SHENZHEN XUNDA MICROELECTRONICS TECH CO LTD) 07.08.2018	1-20
A	US 2012/0133405 A1 (FREESCALE SEMICONDUCTOR INC) 31.05.2012	1-20
A	US 8432204 B1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD) 30.04.2013	1-20



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