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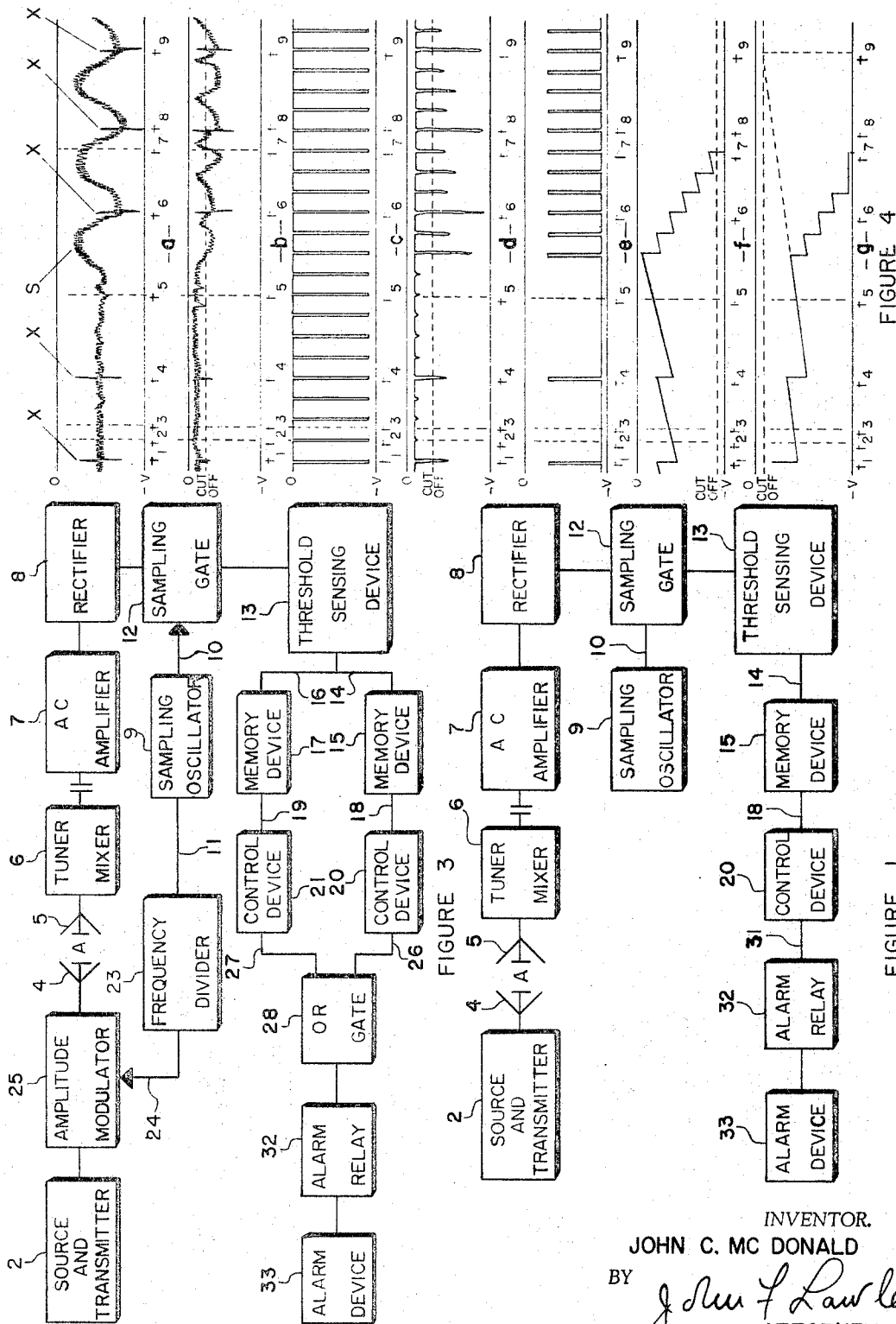
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3,331,065

SIGNAL PROCESSING CIRCUIT FOR INTRUSION ALARM SYSTEM

Filed May 31, 1962

2 Sheets-Sheet 1



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2 Sheets-Sheet 2

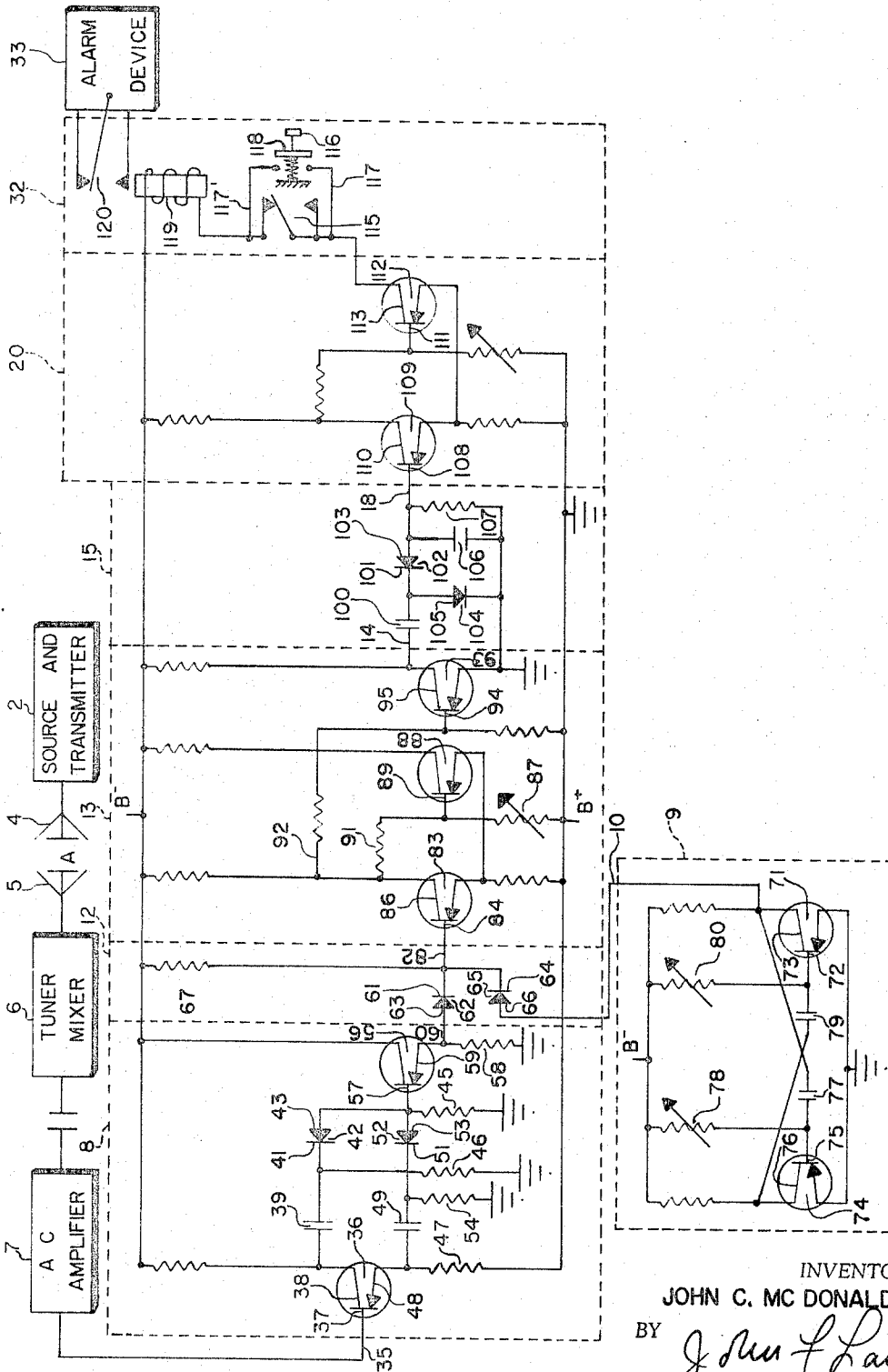


FIGURE 2

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3,331,065

SIGNAL PROCESSING CIRCUIT FOR INTRUSION ALARM SYSTEM

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This invention relates to intrusion detection apparatus for detecting the presence of an intruder in a designated secure area by processing an alarm signal that is proportional to movement in the designated area, and more particularly to an electronic circuit which differentiates between intruder generated alarm signals and spurious signals generated by change in environmental conditions or transient fluctuations in the system.

A variety of intrusion alarm systems for protecting areas against intrusion have been suggested in the past. Some of these systems employ the principle of photoelectricity, capacitance, sonic or ultrasonic energy transmission, radio frequency energy transmission, and seismic indication. It is possible to minimize defeatability of such intrusion alarm systems by increasing their sensitivity, but this results in a high false alarm rate which seriously detracts from the utility and reliability of the system.

False alarms may occur as a result of changes in environmental conditions such as temperature, wind, rain, snow, noise, moving trees, birds or other small animals, or as a result of internally generated noise or line voltage transients.

This invention provides a technique for minimizing the false alarm rate by means of a circuit which discriminates between signals generated by the movement of an intruder and spurious signals.

A principal object of this invention is the provision of a signal processing circuit which distinguishes between signals generated by intruder movement and spurious signals without detracting from the inherent sensitivity of the basic intrusion alarm system.

Another object is the provision of a signal processing circuit which is capable of detecting intrusions with maximum system sensitivity and minimum false alarm rate.

Still another object is the provision of a signal processing circuit which detects an intruder moving at minimum velocity and alarms the system, but which does not activate as a result of spurious environmental signals or internally generated transients.

A further object is the provision of a signal processing circuit which automatically verifies itself and actuates an alarm if the circuit is not functioning properly.

The intrusion detection system employs a high frequency source connected to an antenna which transmits radio frequency energy across an area to be protected, called the secured area, to a second antenna connected to a receiver. Movement of an object in the secured area causes a shift in the frequency of at least a part of the transmitted signal according to the Doppler principle. The received signal is mixed with the transmitted signal to produce a very low frequency output signal, the frequency of which is proportional to the position of the intruder and the rate at which the intruder moves. The beat signal, the amplitude and frequency of which are proportional to movement in the secured area, appears at the output of the mixer. This output of the intrusion detection equipment is fed to the signal processing circuit disclosed herein which discriminates between spurious and intruder generated signals by periodically sampling the rectified output of the intrusion detection equipment.

This periodic sampling technique is based upon recognition of the fact that intruder generated signals are periodic in nature and have an amplitude that is proportional to the

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intruder's size and distance from the transmitting and receiving antennas. In contrast, the voltage characteristic of spurious signals is random in nature and may have a large amplitude for a short time interval.

If the output voltage of the rectifier is greater than a pre-set level during a sampling interval, an event is recorded in a memory device. If this output voltage is above the pre-set level during succeeding sampling intervals, additional events are stored in the memory device. If, during a pre-determined time interval, the number of events stored in the memory device exceeds a threshold value an alarm is generated. This occurs when there is coincidence between a succession of intruder-type periodic signals and the sampling interval. The likelihood of coincidence between the sampling interval and random signals of sufficient magnitude to cause an event to be stored in the memory device is low, and the probability of a succession of large random signals occurring in coincidence with particular sampling intervals is even less likely. Therefore, discrimination against such signals is provided. The memory device continually resets itself in order to eliminate the possibility of spurious signals building up the number of events in memory and alarming the system.

A modified version of the above system incorporates an automatic self-verification feature which provides continual monitoring of system operation and actuates an alarm if the system is not functioning properly. The transmitter is periodically modulated, in time coincidence with the aforementioned sampling interval, to produce a simulated alarm signal. The received signal is amplified, rectified, and applied to parallel memory devices, a unit charge being placed in the memory of each device. One memory device is identical to that described above and resets itself at such a rate that during normal and/or ideal operation the charge induced on the device due to the simulated intruder signal will be completely dissipated before the occurrence of the next simulated intruder signal. The other memory device, however, resets itself at a much slower rate such that during normal and/or ideal operation (no noise or transient signals), its stored energy level is maintained greater than some minimum value by the periodic simulated alarm signals, that is, the charge induced on the device due to a simulated intruder signal is not entirely dissipated between the occurrence of simulated intruder signals. If the charge on the memory device falls below a preset level, due to system malfunction, a control device is actuated and an alarm is generated. Thus, an alarm is generated when an intrusion of the secured area is attempted or the system malfunctions.

Other objects of the invention will become apparent from the following description of a preferred embodiment thereof, reference being made to the accompanying drawings in which:

FIGURE 1 is a block diagram of an intrusion detection system embodying the invention;

FIGURE 2 is a combined block and detailed circuit diagram of the system of FIGURE 1;

FIGURE 3 is a block diagram of a modified intrusion detection system which includes an automatic self-verification circuit; and

FIGURE 4 is a select group of waveshapes of the system of FIGURE 2 in which:

a is the amplified beat signal from AC amplifier 7,

b is the output of rectifier 8 taken from emitter 59 of emitter follower 56,

c is the output of sampling oscillator 9 taken from collector 73 of transistor 71,

d is the output of sampling gate 12 taken from cathode 61 of diode 62,

e is the output of threshold sensing device 13 taken from collector 86 of transistor 83,

f is the output of memory device 15 taken across memory capacitor 106, and

g is the output of memory device 17 taken across its memory capacitor.

A particular system utilizing the present invention is the intrusion alarm system shown in FIGURE 1 and consists of a source 2 of continuous wave radio frequency energy, such as an oscillator, connected to transmitting antenna 4. The radio frequency energy is transmitted over the protected area A, is reflected by the objects within the area and is received by receiving antenna 5. A tuner-mixer 6 connected to antenna 5 and having a cavity tuned to the frequency of transmitter 2 mixes reflected and unreflected signals and develops a very low frequency output signal, the amplitude of which is proportional to the intruder's size and position. The low frequency "beat" signal is coupled to and amplified by AC amplifier 7 and rectified by rectifier 8.

The frequency of the received signal is directly proportional to the velocity of the movement of the intruder, the signal being periodic in nature. In contrast, spurious signals are random in nature. In accordance with this invention the periodicity of intruder generated signals is used by incorporating a sampling circuit to periodically check or sample the received signal.

The sampling circuit consists of a multivibrator or sampling oscillator 9 and sampling gate 12, the output of oscillator 9 being fed through line 10 to control the conduction time and sampling rate of gate 12. The output of rectifier 8 is applied to gate 12. When sampling gate 12 is in its conduction state, the output of rectifier 8 is applied directly through the gate to a Schmidt trigger or threshold sensing device 13. When this rectified output is greater than a predetermined level, as occurs when an intruder signal is present, threshold sensing device 13 conducts. The output of threshold sensing device 13 is applied through line 14 to a counter or memory device 15 and causes a unit count to be recorded each time device 13 conducts. The output of memory device 15 is applied through line 18 to a normally conducting amplifier or control device 20. Control device 20 conducts through line 31 and alarm relay 32 to energize the relay and hold alarm device 33 in its de-activated or non-alarm state. If the count exceeds a preset level during a predetermined time interval, control device 20 is cut off, alarm relay 32 is de-energized and alarm device 33 is activated to energize a lamp, ring a bell, or otherwise indicate an alarm.

Particular reference being made to FIGURE 2, rectifier 8 comprises a phase splitting input transistor 36 that is operating class A and whose base 37 is directly connected to the output AC amplifier 7. An output of transistor 36 is taken from the collector 38 and is capacitively coupled through capacitor 39 to rectifier diode 42. The anode 43 of diode 42 is connected through line 44 and load resistor 45 to ground. Diode load resistor 46 is connected between cathode 41 of diode 42 and ground. A second output of transistor 36, developed across emitter resistor 47, is taken from emitter 48 and capacitively coupled through capacitor 49 to rectifier diode 52. Anode 53 of this diode is connected through line 44 to the anode 43 of diode 42 and through load resistor 45 to ground. Diode load resistor 54 is connected between cathode 51 of diode 52 and ground. Diodes 42 and 52 comprise a full-wave rectifier, the output of which is taken across load resistor 45. Anodes 43 and 53 of diodes 42 and 52, respectively, are directly connected to the base 57 of emitter follower 56, the output of which is taken across emitter resistor 58 and applied through line 60 to anode 63 of diode 62 of sampling gate 12.

Sampling gate 12 essentially consists of diode gates 62 and 65. Cathodes 61 and 64 of diodes 62 and 65, respectively, are connected through line 82 to base 84 of transistor 83 of threshold sensing device 13 and through resistor 67 to the negative supply potential. Anode 66 of

diode 65 is connected through line 10 to the output of sampling oscillator 9.

Oscillator 9 is essentially a collector-coupled transistor multivibrator consisting of transistors 71 and 74. Base 75 of transistor 74 is connected through potentiometer 78, which controls the repetition rate of oscillator 9, to the negative supply potential and through coupling capacitor 77 to collector 73 of transistor 71. Similarly, base 72 is connected through potentiometer 80, which controls the duration of the sampling interval of sampling gate 12, to the negative supply potential and through coupling capacitor 79 to collector 76 of transistor 74.

The output of sampling gate 12 is applied through line 82 to base 84 of normally non-conducting transistor 83 of threshold sensing device 13 which preferably consists of a modified Schmidt trigger circuit similar to that shown on page 164 of Pulse and Digital Circuits by Millman and Taub, published by McGraw-Hill, 1956. Potentiometer 87, connected between the positive supply potential and base 89 of transistor 88 and through resistor 91 to collector 86 of transistor 83, controls the threshold potential of the Schmidt trigger. The output of the Schmidt trigger is taken from collector 86 of transistor 83 and applied through line 92 to base 94 of normally conducting transistor 93.

The input to memory device 15 is taken from collector 95 of transistor 93 through line 14 and coupling capacitor 100 which is connected to normally non-conducting diode 102. Anode 103 of diode 102 is connected through memory capacitor 106, in parallel with by-pass resistor 107, to ground. Diode 104, normally non-conducting, is connected between cathode 101 of diode 102 and ground. The output of memory device 15 is taken across memory capacitor 106 through line 18 and applied to the base 108 of transistor 109 of control device 20.

Control device 20 preferably comprises a Schmidt trigger similar to the one employed in threshold sensing device 13. Collector 110 of transistor 109 is connected to base 111 of transistor 112. The output of control device 20 is taken from collector 113 of transistor 112 which conducts through normally closed contacts 115 to energize relay coil 119 and maintain alarm device 33 in its non-alarm state.

Relay contacts 115 may be short circuited to energize relay coil 119 and/or reset the system by actuating button 116 which connects lines 117 and 117' through bar 118. Relay coil 119 is energized and relay contacts 115 make connection. Alarm relay 32 is maintained in its energized state as long as transistor 112 conducts.

The signals shown in the waveforms of FIGURE 4a through g , to be explained more fully in the operational description of the circuits of FIGURES 2 and 3, are: identified by the letters X in FIGURE 4a at time t_1 , t_4 , t_6 , t_8 , and t_9 , simulated intruder signals generated by frequency divider 23 and amplitude modulator 25; in FIGURE 4a at time t_2 , random noise of insufficient magnitude to cause a count to be recorded by memory device 15 or 17; in FIGURES 4f and g at time t_3 , illustrating the slope of the reset of memory devices 15 and 17; in FIGURE 4g at time t_5 , illustrating the operation of memory device 17 when a simulated intruder signal is missing; in FIGURE 4b at time t_7 , illustrating the point at which memory device 15 is caused to conduct; and, in FIGURE 4g at time t_9 , illustrating the point at which memory device 17 would conduct if consecutive simulated intruder signals were missing.

The operation of the circuit of FIGURE 2 will now be described. The intruder generated "beat" frequency output signal of tuner-mixer 6 is amplified by AC amplifier 7 and is shown at S in FIGURE 4a. The amplified signal is applied through line 35 to base 37 of phase splitting transistor 36. The voltages at collector 38 and emitter 48 are approximately equal in magnitude and opposite in polarity. When transistor 36 conducts more heavily due to a less positive potential on its base 37, the potential

on collector 38 becomes less negative and the potential on emitter 48 becomes less positive. Coupling capacitors 39 and 49 remove the DC components from the voltages at the collector 38 and emitter 48, respectively, of transistor 36. The voltages developed across resistors 46 and 54 are approximately equal in magnitude and 180 degrees out of phase. The voltage across resistor 45 is the more negative of the voltage across resistor 46 or resistor 54. If the voltage at cathode 51 of diode 52 is more negative than the voltage at cathode 41 of diode 42, diode 52 conducts, diode 42 is reverse biased and cut off, and the voltage across resistor 45 is then equal to the voltage across resistor 54. Conversely, if the voltage at cathode 41 of diode 42 is more negative than the voltage at cathode 51 of diode 52, diode 42 conducts, diode 52 is reverse biased and cut off, and the voltage across resistor 45 is equal to the voltage across resistor 46.

The output of emitter follower 56 is a negative going wave, as shown in FIGURE 4b, derived by rectifying, in full wave rectifier 8, the input signal to phase splitting transistor 36, shown in FIGURE 4a, but clamped to approximately zero volt. The cutoff potential noted in FIGURE 4b denotes the negative bias potential that must be exceeded, more negative than, to cause a unit charge to be recorded in memory device 15.

It can be shown that the Doppler frequency shift caused by intruder movement within the protected area is proportional to the frequency of the transmitted signal, the velocity of the introducer, the position of the intruder relative to the transmitter and receiver, and the direction in which the intruder is moving. One method of detecting an intruder in a secured area is to mix the received signal with the transmitted signal and apply the beat signal to a bandpass filter having a flat response and sharp cutoff characteristics. The upper frequency cutoff of the filter controls the boundary of the protected area. Thus, the beat signal frequency produced by an intruder outside this boundary exceeds the upper frequency cutoff while beat frequencies generated by intruders within the boundary are within the pass band of the filter. The upper frequency cutoff of the filter, and thus the location of the boundary of the secured area may be varied by changing the size of filter components, such as the capacitive element.

In accordance with this invention, the boundary of the protected area may be expanded or contracted without necessitating the physical changing of circuit components. This is accomplished by utilizing a signal sampling technique for processing the beat frequency output of the mixer and changing the sampling rate.

Continuous monitoring of the received signal is equivalent to 100 percent sampling of the received signal and an intrusion of the protected area will always be detected when the intruder is a predetermined distance from the signal source. The boundary of the protected area is determined by adjusting the threshold level of the system and the received signal must exceed that level to trigger the system. All systems and environments contain noise of various frequencies, and according to probability theory this noise level will eventually exceed the threshold level necessary to trigger the system. Thus from time to time the system would give false alarms. On the other hand, if the received signal is monitored at a very low sampling rate the probability of a noise signal or an intruder generated signal exceeding the threshold level necessary to trigger the system is very low. Under these conditions the system will have a very low false alarm rate and a very low probability of intrusion detection.

In accordance with the Doppler principle, the frequency of the beat signal decreases and the magnitude of the beat signal increases as the reflecting object, the intruder, moves toward the protected area. By adjusting the system to have a particular threshold level and sampling rate, the intruder will be detected when the amplitude of the intruder signal is greater than the preset threshold level for

a number of successive sampling intervals. This causes a number of unit charges to be impressed on a memory device until a second threshold level is exceeded and the system is alarmed. It has been determined empirically that the frequency of the beat signal must be approximately equal to the sampling rate before an intruder will be detected.

As the frequency of the beat signal decreases (as when the intruder moves closer to the signal source) the probability that the magnitude of the beat signal will exceed the threshold level during a succession of sampling intervals is increased (one-half cycle of the beat signal may be greater than the threshold level during more than one sampling interval). Conversely, as the frequency of the beat signal increases (when the intruder moves away from the signal source) the probability that the magnitude of the beat signal will exceed the threshold level during a succession of sampling intervals is decreased. Thus, the output of the sampling circuit is proportional to the position of the intruder and to the frequency of the beat signal.

It follows from the foregoing explanation that the maximum beat frequency to which the sampling circuit is responsive is controlled by increasing or decreasing the sampling rate, that is, the boundary of the protected area may be increased by increasing the sampling rate and may be decreased by decreasing the sampling rate. Specifically, increasing or decreasing the size of the protected area is accomplished by adjusting a rate potentiometer in the sampling oscillator circuit, and more specifically potentiometer 78 of sampling oscillator 9.

In sampling oscillator 9, transistor 71 conducts between sampling intervals and capacitor 77 and potentiometer 78 control the repetition rate of the oscillator, i.e., the conduction time of transistor 71. When transistor 71 is conducting the potential on collector 73 is approximately zero volts as shown in FIGURE 4c, time t_3 . During the sampling interval transistor 74 conducts and capacitor 79 and potentiometer 80 control the sampling interval, i.e., the length of time transistor 71 is cut off. When transistor 71 is cut off the potential on collector 73 falls to approximately the negative supply potential as shown in FIGURE 4c, time t_2 .

The output of sampling oscillator 9 is taken from collector 73 of transistor 71 and applied through line 10 to anode 66 of diode 65, diodes 62 and 65 essentially comprising sampling gate 12. When transistor 71 conducts (between sampling intervals) the potential on collector 73 of transistor 71 and anode 66 of diode 65 become less negative and forward bias the diode causing it to conduct through resistor 67 and drive the potential on base 84 of transistor 83 to approximately ground potential, clamping this transistor in its cutoff state. Under these conditions the gate circuit 12 blocks transmission of any signals from rectifier 8.

When transistor 71 of oscillator 9 is cut off the potential on collector 73 approaches the negative supply potential and reverse biases and cuts off diode 65. The potential on cathode 61 of gate diode 62 then follows the potential on emitter 59 of emitter follower 56, see FIGURE 4b, and diode 62 conducts. If during the sampling interval a negative pulse of sufficient magnitude appears at cathode 61 of diode 62, a negative pulse the magnitude of which is more negative than the cutoff potential indicated in FIGURE 4d, normally non-conducting transistor 83 is forward biased and saturates. Transistor 83 and transistor 88 form a regenerative loop which causes a discrete change in voltage at collector 86 of transistor 83. When transistor 83 saturates, the potential at collector 86 becomes less negative, maintaining transistor 83 in its conducting state until the sampling interval is terminated or the potential on emitter 59 of emitter follower 56 becomes less negative than the cutoff potential of transistor 83 and its base 84 is again reverse biased. If the sampling interval is short compared with the time necessary for the

potential on emitter 59 of emitter follower 56 to reach the cutoff potential of transistor 84 a constant output is obtained from collector 86 of transistor 83 during the rectified signal whose width is determined by the sampling interval. The output of emitter follower 56 is applied to the base 84 of transistor 83 only during the sampling interval.

The output of transistor 83, taken from collector 86, is a positive going pulse, as shown in FIGURE 4e, time t_1 , and is applied through line 92 to reverse bias and cut off normally conducting transistor 93. When this occurs the potential on collector 95 goes negative, forward biases and causes diode 102 to conduct, and reverse biases non-conducting diode 104. Memory capacitor 106 is charged through diode 102 and coupling capacitor 100, accumulating a charge of predetermined magnitude during the sampling interval. When the sampling interval is terminated transistor 93 is again forward biased and saturates. The potential on collector 95 becomes less negative causing diode 102 to be reverse biased and cut off and by-pass diode 104 to conduct momentarily to discharge coupling capacitor 100. After capacitor 100 is discharged diode 104 is again reverse biased and ceases to conduct. The charge on memory capacitor 106 leaks off through by-pass resistor 107 at a predetermined rate between sampling intervals as shown in FIGURE 4f, time t_3 , in order to eliminate the possibility of spurious signals building up the number of events in memory and alarming the system. Capacitor 106 does not completely discharge between sampling intervals. Memory capacitor 106 builds up a charge, as shown between time t_5 and t_7 , in FIGURE 4f, if during succeeding sampling intervals the output of emitter follower 56 is of sufficient magnitude to trigger threshold sensing device 13.

Control device 20 is preferably a Schmidt trigger in which transistor 109 is normally non-conducting and transistor 112 is conducting. Transistor 112 conducts through and energizes alarm relay 32 which holds alarm device 33 in its de-activated state.

The output of memory device 15 is developed across capacitor 106 and is applied through line 18 to base 108 of transistor 109. This input has no effect on the operation of control device 20 or transistor 112 until the potential across capacitor 106 becomes sufficiently negative to forward bias base 108 and cause transistor 109 to conduct. This condition is indicated at time t_7 in FIGURE 4f. When transistor 109 of control device 20 is caused to conduct the potential on collector 110 becomes less negative, reverse biases base 111 and cuts off transistor 112. The current necessary to keep relay 32 energized is terminated and alarm device 33 is activated to indicate an attempted intrusion of the protected area.

A modification of the present invention incorporating an automatic self-verification circuit, to provide a fail-safe feature, is shown in FIGURE 3. The fail-safe circuitry consists generally of frequency divider 23, amplitude modulator 25, memory device 17, control device 21, and OR gate 28. OR gate 28 is a conventional OR gate modified to change its conduction state in response to a positive or negative input signal. In other respects the circuit is similar to that of FIGURE 1 and like reference characters indicate like parts on the drawings.

Briefly, the output of sampling oscillator 9 is fed simultaneously through line 10 to sampling gate 12 and through line 11 to frequency divider 23 which produces an output that is a submultiple of the input from oscillator 9. The frequency divider 23 may be the type described in Waveforms, volume 19, MIT Rad Lab Series, chapter 16, "Pulse-Recurrence-Frequency Division," McGraw-Hill, 1949. Frequency divider 23 is synchronized with sampling oscillator 9 and, at a predetermined rate, triggers amplitude modulator 25 which generates a simulated intruder signal in time coincidence with the triggering of sampling gate 12, as indicated by the letters X in FIGURE 4a. This signal is transmitted across the protected area, re-

ceived by antenna 5, mixed, amplified, rectified, and applied to and triggers threshold sensing device 13 causing a unit charge, which simulates an event, to be transmitted through parallel lines 14 and 16 for storage by memory devices 15 and 17, respectively. If the stored charge on memory device 15 becomes more negative than a predetermined value, FIGURE 4f, time t_7 , indicating the presence of an intruder in the protected area, control device 20 is triggered and changes its operating state. The output of control device 20 on line 26 reverse biases and cuts off OR gate 28 so that alarm relay 32 is de-energized and alarm device 33 is activated as described in relation to the circuit of FIGURE 2.

Memory device 17 is adjusted so that the simulated intruder signals generated by amplitude modulator 25 build up the count on the device, due to the time constant of the device, and, during normal operation, maintains the count on the device at a potential more negative than some minimum cutoff potential as shown in FIGURE 4g. If for any reason the system should fail, i.e., power failure, component failure, loss of synchronization, the simulated intruder signals from amplitude modulator 25 either disappear or fall out of synchronism with the sampling interval, and the charge stored on memory device 17 decreases to the cutoff potential on control device 21, as indicated by the broken line in FIGURE 4g, time t_9 , and causes the device to conduct. The output of control device 21 on line 27 reverse biases and cuts off OR gate 28 causing relay 32 to de-energize and activate alarm device 33. Thus, the system alarms when an intrusion of the secured area is attempted or the system fails.

More specifically, the embodiment of the invention shown in FIGURE 3 operates as described in the operational analysis of the circuit of FIGURE 2 through the output of threshold sensing device 13 taken from collector 95 of transistor 93, except that sampling oscillator 9 triggers frequency divider 23 through line 11 at the start of each sampling interval. Frequency divider 23 produces an output which is a submultiple of the input from oscillator 9, for example, one output pulse for four sampling intervals, that triggers amplitude modulator 25. Amplitude modulator 25 generates a simulated intruder signal indicated by the letters X in FIGURE 4a, time t_1 , t_4 , t_6 , t_8 , t_9 , in time coincidence with the sampling interval, and that signal is transmitted across the protected area, is received, and is processed through threshold sensing device 13 as described in the operational analysis of the circuit of FIGURE 2. This causes an event or unit charge to be stored in the memory capacitor of memory devices 15 and 17.

Memory device 15 operates as described in the operational analysis of the circuit of FIGURE 2; the time constant of the device being adjusted such that a unit charge on the device is completely dissipated during a time interval that is less than the time interval between simulated intruder signals, for example, less than the time between t_1 and t_4 of FIGURE 4f. Thus, the length of the time constant may be adjusted such that the system is not alarmed as a result of the count induced on the memory devices due to intermittent noise signals. If intruder signals are received during succeeding sampling intervals the charge or count on the memory capacitor builds up a sufficiently negative value to forward bias control device 20, see FIGURE 4f, at time t_7 . Control device 20 conducts and reverse biases and cuts off OR gate 28, so that relay 32 is de-energized and alarm device 33 is activated to indicate an intrusion of the protected area.

The circuits of memory devices 15 and 17 are identical except that the latter has a larger time constant than device 15 such that a unit charge on the memory capacitor in device 17 is not entirely dissipated during the time interval between simulated intruder signals. The difference between the decay time of devices 15 and 17 is illustrated at times t_1 to t_4 in FIGURES 4f and g, respectively.

During normal system operation a count is recorded in

memory devices 15 and 17 in response to the periodic simulated intruder signals of amplitude modulator 25, as shown in FIGURES 4f and g, time t_1 , t_4 , t_6 , t_8 , t_9 . When intruder or noise generated signals are absent during succeeding sampling intervals the count or charge on memory device 17 falls off more slowly than the charge on memory device 15 as illustrated by the different slopes of the waveform in FIGURES 4f and g at time t_3 . When this occurs, a residual charge is retained on the memory capacitor of device 17 at the time the next simulated intruder signal is generated while the unit charge on device 15 is entirely dissipated prior to the occurrence of the next simulated intruder signal. Thus, when simulated intruder signals are present the charge on memory device 15 will not build up to generate a false alarm indicating an intrusion of the secured area; however, a resultant or net negative charge is built up on memory device 17 and maintained as long as the system functions properly.

If for any reason the system should malfunction or fail the simulated intruder signals will either be out of synchronism with the simulated intruder signals or missing entirely. In either case memory device 17 is not "pumped-up" as in normal operation and the resultant charge on the device leaks-off and becomes less negative. The waveform of FIGURE 4g at time t_5 and the broken line extending to the cutoff potential at time t_9 illustrate the response of memory device 17 when a simulated intruder signal is not carried by the circuits. When the charge falls to a predetermined less negative value, FIGURE 4g, time t_9 , control device 21 is triggered and switches its mode of operation causing OR gate 28 to be reverse biased and cut off.

The circuit of control device 21 is the reciprocal of the circuit of control device 20, for example, a Schmidt trigger utilizing NPN transistors rather than PNP transistors. In other words, device 21 responds to or is triggered by an input that is a minimum negative potential whereas device 20 is triggered by an input that is a maximum negative potential. This distinction is more clearly illustrated by noting the cutoff potentials shown in FIGURE 4g and f, respectively.

When either control device 20 or 21 switches from its normal operating state, OR gate 28 is reverse biased and cut off, causing alarm relay 32 to de-energize and activate alarm device 33. Thus, the system produces an alarm when an intrusion of the secured area is attempted or the system itself fails.

What is claimed is:

1. An intrusion detection system adapted to respond to signals produced by movement of an intruder in a protected area and to discriminate against spurious random signals, comprising

gating means having first and second inputs and having first and second operating states, means for applying intruder and spurious signals to said first input, said gating means in said first operating state blocking said input signals and in said second operating state passing said input signals,

a sampling oscillator connected to the second input of said gating means and adapted successively to switch said gating means between said first and second operating states at the frequency of said oscillator, means for selectively changing the frequency of said oscillator,

signal storage means connected to the output of said gating means comprising a resistor-capacitor network having a predetermined discharge rate, said network being charged by each signal passed by said gating means that exceeds a predetermined level, and

means responsive to the charge on said network in excess of a predetermined magnitude for indicating that condition.

2. Intrusion alarm apparatus for detecting moving objects comprising

a source of electromagnetic wave energy,

means for radiating said energy,

antenna means for receiving reflected energy from a moving object and for receiving unreflected energy directly from said transmitting means,

receiver means connected to said antenna means comprising

means for mixing said reflected energy with said unreflected energy to derive an intermediate frequency beat signal,

means for rectifying said beat signal,

sampling circuit means connected to said rectifying means for sampling the rectified beat signal at a predetermined rate to produce an output,

means for monitoring the output of said sampling circuit and producing an output when the sampling circuit output exceeds a predetermined value, and

an alarm apparatus responsive to the output of said monitoring means for indicating movement of an object.

3. Intrusion alarm apparatus for detecting moving objects comprising

a source of electromagnetic wave energy,

means for radiating said energy,

antenna means for receiving reflected energy from a moving object and for receiving unreflected energy directly from said transmitting means,

receiving and signal processing means connected to said antenna means comprising

means for mixing said reflected energy with said unreflected energy to derive an intermediate frequency beat signal,

amplifier means to amplify said beat signal,

rectifying means connected to said amplifier means to rectify said beat signal,

gating means having a first input and a second input and having first and second operating states for respectively blocking and passing signals applied to the first input, said first input being connected to the output of said rectifying means,

a sampling oscillator connected to said second input for successively switching said gating means automatically between said first and second operating states,

memory means adapted to receive the output of said gating means for adding successively sampled rectified beat signals,

level sensor circuit means connected to the output of said memory means and producing an alarm signal when the output of the memory means exceeds a predetermined level, and

alarm apparatus responsive to said alarm signal for indicating the presence of a moving object.

4. Apparatus according to claim 3 in which said memory means automatically resets in the absence of an output from said gating means.

5. Apparatus according to claim 4 in which said memory means comprises a resistance and capacitor network.

6. Apparatus according to claim 5 in which said resistance-capacitor network has a time constant that is related to the period of the sampling oscillator such that a predetermined number of successively sampled signals must be applied to said network to produce an output capable of generating an alarm signal.

7. Intrusion alarm apparatus for detecting moving objects comprising

a source of electromagnetic wave energy,

means for radiating said energy,

antenna means for receiving reflected energy from a moving object and for receiving unreflected energy directly from said transmitting means,

receiving and signal processing means connected to said antenna means comprising

means for mixing said reflected energy with said

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unreflected energy to derive an intermediate frequency beat signal,
 amplifier means to amplify said beat signal,
 rectifying means connected to said amplifier means to rectify said beat signal,
 gating means having a first input and a second input and having first and second operating states for respectively blocking and passing signals applied to the first input, said first input being connected to the output of said rectifying means,
 a sampling oscillator connected to said second input for successively switching said gating means automatically between said first and second operating states,
 first level sensor circuit means connected to the output of said gating means for monitoring the output of said rectifying means to produce a unit output if the magnitude of said rectified beat signal is greater than a preset level when said gating means is in the second operating state,
 memory means connected to said first level sensor circuit means and comprising a resistance-capacitor network adapted to receive a unit charge in response to a unit output of said first level sensor circuit means, said network having a time constant adjusted so that the network continually resets itself at a predetermined rate during operation,
 second level sensor circuit means responsive to the magnitude of the stored charge in said network for producing an alarm signal when said charge exceeds a preset level, and
 alarm apparatus responsive to said alarm signal for indicating the presence of a moving object.
 8. Intrusion alarm apparatus for detecting moving objects in a protected area comprising
 a source of electromagnetic waves,
 means for modulating said waves at a predetermined rate to simulate reflected energy from a moving object,
 means for radiating said modulated waves,
 means for receiving modulated waves and reflected waves from a moving object and unreflected waves directly from said radiating means, comprising
 means for mixing said reflected and directly transmitted waves to derive an intermediate frequency beat signal,
 means to rectify said beat signal,
 means for periodically sampling the rectified beat signal at a rate functional of said modulation rate to produce an output,
 level sensor means connected to the output of said sampling means and producing an output when said beat signal exceeds a predetermined level,
 first memory means responsive to the output of said level sensor means for producing an output in the absence of a beat signal derived from said modulation means,
 second memory means responsive to the output of said level sensor means for producing an output when beat signals are derived from waves reflected from a moving object, and
 alarm means responsive to the outputs of either first or second memory means for indicating the presence of a moving object in the protected area or a system malfunction.
 9. Intrusion alarm apparatus for detecting moving objects comprising
 a source of electromagnetic wave energy,
 amplitude modulation means having first input connected to the output of said source and having a second input and being adapted to amplitude modulate

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the output of said energy source in response to a signal applied to said second input,
 means for transmitting said energy,
 means for receiving the modulated energy and reflected energy from a moving object and unreflected energy directly from said transmitting means, comprising
 means for mixing said reflected and directly transmitted waves to derive an intermediate frequency beat signal,
 means connected to said mixing means to rectify said beat signal,
 gating means having first and second inputs and having first and second operating states, the first input of said gating means being connected to the output of said rectifying means,
 sampling oscillator means having first and second outputs, said first oscillator output being connected to the second input of said gating means successively to switch said gating means between said first and second operating states,
 a frequency divider connected to the second output of the sampling oscillator to produce an output that is a sub-multiple of the output of the sampling oscillator, the output of said frequency divider means being connected to said second input of the amplitude modulation means,
 recognition and memory means connected to said gating means to monitor and add the rectified beat signals when the gating means is in said second operating state,
 level sensor circuit means connected to the output of said recognition and memory means for producing an alarm signal to indicate an intrusion of said protected area when the output of said memory means exceeds a predetermined level and to indicate a system malfunction when the output of said memory means is less than a predetermined level, and
 alarm apparatus responsive to said alarm signal for indicating the presence of a moving object in said protected area or a system malfunction.
 10. Intrusion alarm apparatus for detecting moving objects comprising
 a source of electromagnetic wave energy,
 amplitude modulation means having first input connected to the output of said source and having a second input and being adapted to amplitude modulate the output of said energy source in response to a signal applied to said second input,
 means for transmitting said energy,
 means for receiving the modulated energy and reflected energy from a moving object and unreflected energy directly from said transmitting means, comprising
 means for mixing said reflected and directly transmitted waves to derive an intermediate frequency beat signal,
 means connected to said mixing means to rectify said beat signal,
 gating means having first and second inputs and having first and second operating states, the first input of said gating means being connected to the output of said rectifying means,
 sampling oscillator means having first and second outputs, said first oscillator output being connected to the second input of said gating means successively to switch said gating means between said first and second operating states,
 a frequency divider connected to the second output of the sampling oscillator to produce an output that is a sub-multiple of the output of the sampling oscillator, the output of said frequency divider means being connected to said second input of the amplitude modulation means,
 first level sensor circuit means responsive to the

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output of said rectifying means when said gating means is in said second operating state to produce an output if the magnitude of the rectified beat signal is greater than a preset level,

first memory means connected to said first level sensor circuit means and responsive to its output for storing unit charges, 5

second memory means connected to said first level sensor circuit means and responsive to its output for storing unit charges, 10

second level sensor circuit means responsive to the magnitude of the charge on said first memory means to produce an alarm signal indicating an intrusion of the protected area when said charge exceeds a preset level, 15

third level sensor circuit means responsive to the magnitude of the charge on said second memory means to produce an alarm signal indicating a system malfunction when said charge is less than a preset level, and 20

alarm apparatus responsive to said alarm signals for indicating the presence of a moving object in the protected area or a system malfunction.

11. Apparatus according to claim 10 in which said first and second memory means each comprise a resistance-capacitance network, the time constant of the second memory means being greater than the time constant of the first memory means. 25

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12. An intrusion detection system adapted to respond to signals produced by movement of an intruder in a protected area and to discriminate against spurious random signals, comprising

gating means,

means for applying to the input of said gating means intruder and spurious signals, said gating means having a first operating state for blocking said input signals and having a second operating state for passing said input signals as an output,

means for switching said gating means from said first state to said second state and back to said first state at discrete equally spaced time intervals,

signal storage means responsive to a plurality of successive signals passed by said gating means to produce an output, and

means responsive to the storage means output in excess of a predetermined magnitude for indicating that condition.

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